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(54) Title: DIGITALLY CONTROLLED SWITCHED CURRENT SOURCE ACTIVE GATE DRIVER FOR SILICON CARBIDE MOSFET WITH LINE CURRENT SENSING

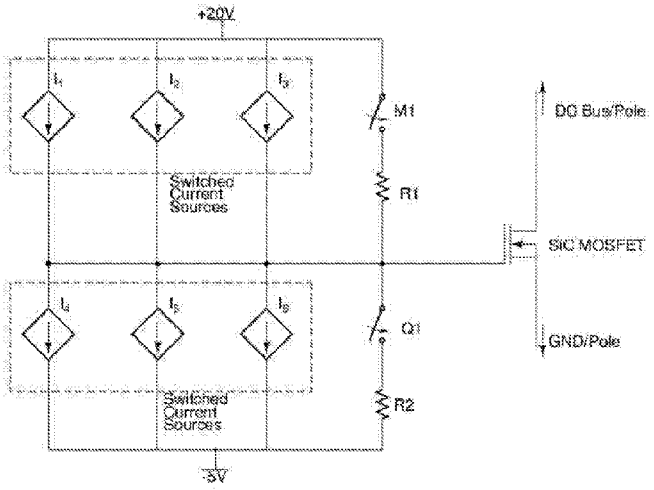


FIGURE 1

(57) Abstract: The present invention relates to SiC MOSFET which has fast switching times of nearly 20ns to 50ns. To control the voltage and current overshoot of the SiC MOSFET during the switching transient an active gate driver is required. The invention presented describes an active gate driver for SiC MOSFET used in power converter topology. The proposed four step active gate driving method uses a digitally controlled switched current source to control the gate current of the SiC MOSFET. The control signals are generated by means of onboard digital control logic which can be implemented in either in a FPGA or CPLD. The voltage and the current of the device are measured to control the overshoot and ringing in the device voltage and current. The proposed gate driver has novel current sensing mechanism based on kelvin voltage measurement. The measured load current can be used for control and

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protection of the device from faults. Since the switching time of the SiC MOSFET is very less it is difficult to control the voltage and current overshoot in the same switching instant hence, a low speed control loop is also proposed in the invention. The low speed control loop takes its control decision based on the previous switching cycle information. The low speed control loop essentially decides the time intervals of the switching steps of the gate driver.

DESCRIPTION

TITLE OF THE INVENTION

DIGITALLY CONTROLLED SWITCHED CURRENT SOURCE ACTIVE GATE DRIVER FOR SILICON CARBIDE MOSFET WITH LINE CURRENT SENSING

FIELD OF THE INVENTION

The present invention relates to digitally controlled switched current source active gate driver is applicable for silicon carbide MOSFETs used in switched power converter applications with fixed DC Bus voltage.

BACKGROUND OF THE INVENTION

SiC MOSFET are fast switching devices, typical switching speeds are in the range of 20ns to 50ns, nearly times faster than state of the art IGBTs of similar rating. The potential of SiC MOSFET cannot be completely captured due to the parasitic leakage inductance of the converter being significant. Designing a converter layout with very low parasitic inductance is practically not feasible. Thus, there is a need for an Active Gate Driving mechanism which controls the SiC MOSFET so that the parasitic inductance and capacitance do not hamper the switching performance of the SiC MOSFET and thus we can have good switching performance along with tolerable parasitic inductance and capacitance.

In this invention the gate current of SiC MOSFET is digitally controlled using the device voltage and device current information. Due to fast switching nature of the SiC MOSFET a low speed control technique is also proposed which controls the time interval of the switching steps. A novel current sensing technique using the kelvin inductor is adopted which helps in control and protection.

SUMMARY OF THE INVENTION

The present invention relate to an active gate driver which can precisely control the rate of rise and fall of the device current and voltage without compromising on the switching speed of the SiC MOSFET.

In one embodiment, the proposed Active Gate Driver implements a digital control making the control implementation simpler and control signals more robust to noise and

interference. A low frequency control loop is used for control methodology which can effectively limit the current and voltage overshoot within desired limits.

In other embodiment, the invention presents an active gate driver for SiC MOSFET used in power converter topology. The hardware topology of the proposed active gate driver consist of two sections the Turn-on section (I_1, I_2, I_3 and M_1) and the Turn-off section (I_4, I_5, I_6 and Q_1).

The proposed four step active gate driving method uses a digitally controlled switched current source to control the gate current of the SiC MOSFET. The control signals are generated by means of onboard digital control logic which can be implemented in either in a FPGA or CPLD. The voltage and the current of the device are measured to control the overshoot and ringing in the device voltage and current. The proposed gate driver has novel current sensing mechanism based on kelvin voltage measurement. The measured load current can be used for control and protection of the device from faults. Since the switching time of the SiC MOSFET is very less it is difficult to control the voltage and current overshoot in the same switching instant hence, a low speed control loop is also proposed in the invention. The low speed control loop takes its control decision based on the previous switching cycle information. The low speed control loop essentially decides the time intervals of the switching steps of the gate driver.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows Topology of the Active Gate Driver.

Figure 2 indicates the turn-on steps of the proposed Active Gate Driver**.**

Figure 3 indicates the turn-off steps of the proposed Active Gate Driver.

Figure 4 shows the Line current sensing mechanism.

Figure 5 shows the control Flow chart.

Referring to the drawings, the embodiments of the present invention are further described. The figures are not necessarily drawn to scale, and in some instances the drawings have been exaggerated or simplified for illustrative purposes only. One of ordinary skill in the art may appreciate the many possible applications and variations of the present invention based on the following examples of possible embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The following description is presented to enable any person skilled in the art to make and use the embodiments, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present disclosure. Thus, the present invention is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

The description of the Active Gate Driver can be divided into 3 sections. Section I describes the Hardware topology of the disclosed Active Gate Driver. Section II describes the control methodology followed to obtain the desired performance. Section III describes the line current sensing and measurement for protection and control followed by low frequency control loop.

Section I

Hardware Topology of the Proposed Active Gate Driver:

Fig. 1 depicts the topology for the active gate driver. It consists of two sections the Turn-on section (I_1, I_2,I_3 and M_1) and the Turn-off section (I_4, I_5,I_6 and Q_1).

Turn-On section

I_1, I_2 and I_3 are switched current sources which current into the gate of the SiC MOSFET, thus controlling the rate of charging of the gate-source capacitor (C_{gs}) of the SiC MOSFET. The current sources are controlled through logic which can be implemented through discrete gates, CPLD or FPGA. The current sources can be realized using current mirrors or appropriately biased transistors. M_1 is a switch which essentially connects the resistors R1 to the gate of the SiC MOSFET.

Turn-Off section

Similar to the turn-on section the turn-off section consists of I_4, I_5 and I6 are switched current sources which control the discharge of the gate-source capacitor (C_{gs}). Q_1 is a switch which connects resistor R_2 to the gate of the SiC. For reliable turn-off the gate should be brought to -5V. The current sources and the switch can be controlled through logic implemented as discrete gates, or in CPLD or FPGA.

Section II

Control Methodology

From the previous section it can be seen that there are three controlled steps in each of the turn on section and turn-off section. In order to achieve the optimum performance the correct sequence of these stages in imperative.

Turn-on

1. Step 1 for turn-on is the switched current source I_1. I_1 is switched on gate capacitor (C_{gs}) of SiC is charges with a constant current. Step 1 essentially reduces the delay time by charging the gate capacitor (C_{gs}) as quickly as possible upto the threshold voltage by charging the gate capacitor with a larger current. Once the gate voltage exceeds threshold voltage ($V_{gs}>V_{th}$) channel current (I_{ch}) is established. This marks the end of the first step.
2. Step 2 for the turn-on process is the switched current source I_2 as shown in Fig.1. The current source I_2 is turned on after the preceding current source I_1 in step 1 has turned off. The current source charges the gate to source capacitor (C_{gs}) with a constant current. The rate of rise of drain current (i_d) of the SiC MOSFET is given by the equation :-

$$\frac{di_d}{dt} = \frac{g_m i_g}{C_{iss}}$$

i_d = drain current of the SiC MOSFET.

g_m= forward transconductance of the SiC MOSFET.

C_{iss} = Input capacitance of the SiC MOSFET (Ciss = Cgs + Cgd).

i_g= Gate current of SiC MOSFET.

Thus, by maintaining ig constant we can have a complete control over the di_d/dt of the MOSFET in the current rise region (Saturation region of MOSFET).

Step 2 ends at the instant when the drain current i_d is equal to the load current I_L. At the end of 2nd step the current source I_2 is turned off.

3. Step 3 of the turn-on process is the switched current source I_3 as shown in Fig.1. The current source I_3 is turned on when the drain current id is equal to I_L (Stage 2 is turned off). 3rd step of the turn-on section controls the current overshoot and oscillations in the drain current and the rate of voltage (V_{ds}) fall (dV_{ds}/dt) of the SiC MOSFET. The current overshoot of the SiC MOSFET is proportional to the gate current i_g. The steady state

voltage fall (dV_{ds}/dt) is also proportional to the gate current i_g. It is given by the following equation:-

$$\frac{dV_{ds}}{dt} = \frac{i_g}{C_{gd}}$$

Thus, by appropriately controlling the magnitude of gate current the overshoot and ringing in the drain current of the SiC MOSFET can be arrested.

4. The transistor M_1 is turned on after the current overshoot is arrested. Basically, M_1 and resistor R_1 clamp the gate-source voltage (V_{gs}) to 20V.

Fig.2 illustrates the sequence of stages with respect to the drain current (id) and gate–source voltage (V_{gs}). It can be seen from the figure that during stage 2 of the turn-on process the rate of rise of drain current di_d/dt remains constant.

Turn-off

1. Step 4 for turn-off is a switched current source I_4 as illustrated in Fig.1. Step 4 essentially reduces the delay time by discharging the gate capacitor (C_{gs}) as quickly as possible. Step 4 ends as soon as the Drain-Source voltage (V_{ds}) of SiC MOSFET starts rising.
2. Step5 for turn-off is the switched current source I_5 shown in Fig.1. The switched current source I_5 is turned on after Step 4. The switched current source I_3 controls the drain-source voltage (V_{ds}) rise, (dV_{ds}/dt) of SiC MOSFET. Step 5 ends as the Drain Source voltage (Vds) reaches the DC bus voltage V_{DC}.
3. Step 6 of the turn-off process is a switched current source I_6. Step 6 controls the drain-source voltage (V_{ds}) overshoot and V_{ds} ringing. The 6th step is turned on after the 5th step. The voltage rise, (dV_{ds}/dt) during turn-off is proportional to the gate current i_g.
4. Similar to the turn-on process the transistor Q_1 is turned on after the switching transient is completed to connect the gate of the SiC MOSFET to -5V. Q_1 and R_2 clamp the gate-source voltage to -5V.

Section III

Line current sensing and Low frequency control of the Active Gate Driver

i. Line current sensing

The proposed Active Gate Driver implements a novel method to measure the line current of the inverter using the kelvin inductance. The line current information on the AGD enables better control for switching stages and eliminates the need of external current sensors. Line current measurement within the AGD itself reduces the time for detection of overcurrent fault than conventional methods that require external current sensors. This in turn improves the overall overcurrent fault response time.

Fig.4 depicts the block diagram for line current measurement. The voltage across kelvin inductor L_k is L_K. d_{id}/dt this is integrated to obtain the drain current. However, when drain current is equal to load current the voltage L_K. d_{id}/dt is very small as d_{id}/dt s corresponding to the low frequency load current. To integrate this voltage an active integrator is used. The output of integrator is given to a sample and hold circuit which samples the output atleast once every switching cycle of SiC MOSFET. The output of sample and hold circuit is a voltage which is proportional to the line current. This voltage can be optionally given to an ADC for further processing.

ii. Low frequency Control of Active Gate Driver

The typical switching (turn-on/turn-off) time of the SiC MOSFET is in the range of 50-60 ns. The typical delay in measurement of voltage (V_{ds}) and current (i_d) is 5-10 ns. Thus, it is very difficult to accurately control the switching instants of the driving stages (Section I) in such a small interval of time.

Alternatively, a low frequency control can be implemented which will correctly set the sequence of the stages not in the current switching cycle but over a few cycles. The operation of the low frequency control can be illustrated as follows.

Consider the turn-on switching instant. The Active Gate Driver starts operation with fixed time intervals for the four stages. During the turn-on process the rise of drain current (i_d) is controlled by stages 1 and 2. After the drain current (i_d) crosses the load current (I_L), an overshoot is observed in the drain current due to reverse recovery effect of the top diode. The magnitude of overshoot is proportional to the gate current (i_g) of the SiC MOSFET.

The overshoot and subsequent ringing can be controlled within an allowable tolerance by timing the Stage 3 of the turn-on section (Section I) appropriately. Under the assumption that the load current does not vary rapidly the current overshoot remains more or less constant over a period of few cycles. The low frequency control essentially adjusts the switching time instant of 3rd stage of turn-on section in the proceeding switching cycles. Since, it is a low frequency control it will take atleast one entire switching cycle to limit the current overshoot in the allowable tolerance range.

The drain current (i_d) is measured and compared with the measured line current (Section III. i) and the overshoot is calculated. The switching instant of 3rd stage of turn-on section is adjusted for the next switching cycle and then the overshoot is observed in the following cycle. If the overshoot is in the tolerable limits the timing instants of the stages are fixed. If the overshoot is not within the tolerable limits the process continues until it converges. The control algorithm can be summarized using the flowchart Fig.5.

It may be appreciated by those skilled in the art that the drawings, examples and detailed description herein are to be regarded in an illustrative rather than a restrictive manner.

We Claim:

1. An active gate driver for silicon carbide MOSFETs for digitally controlling the switched current using the device voltage and device current information, wherein the active gate driver involves;-

   turn-on section (I_1, I_2, I_3 and M_1) and the turn-off section (I_4, I_5,I_6 and Q_1) for controlling the rate of charging and discharging of the gate-source capacitor (C_{gs}) of the SiC MOSFET respectively;

   the rate of rise and fall of drain current (i_d) of the SiC MOSFET is controlled by turn-on and turn-off process;

   a method for sensing and measuring the line current for protection and followed by low frequency control.

2. The active gate driver as claimed in claim 1, wherein the turn-on process controls the rate of charging of the gate-source capacitor (C_{gs}) of the SiC MOSFET.
3. The active gate driver as claimed in claim 1, wherein the turn-off process controls the rate of discharging of the gate-source capacitor (C_{gs}) of the SiC MOSFET.
4. The active gate driver as claimed in claim 1, wherein the current sources are controlled through logic via discrete gates includes CPLD and FPGA.
5. The active gate driver as claimed in claim 1, wherein the rate of rise of drain current (i_d) of the SiC MOSFET is controlled by maintaining gate current (i_g) at constant.
6. The active gate driver as claimed in claim 1, wherein controlling the magnitude of gate current the overshoot and ringing in the drain current of the SiC MOSFET is arrested.
7. The active gate driver as claimed in claim 1, wherein the turn-on section controls the current overshoot and oscillations in the drain current and the rate of voltage (V_{ds}) fall of the SiC MOSFET.
8. The active gate driver as claimed in claim 6, wherein the current overshoot of the SiC MOSFET is proportional to the gate current (i_g).
9. The active gate driver as claimed in claim 1, wherein the line current of the inverter is measured using the kelvin inductance.
10. The active gate driver as claimed in claim 8, wherein the line current information on the active gate driver enables better control for switching stages and eliminates the need of external current sensors.

11. The active gate driver as claimed in claim 1, wherein the low frequency control is implemented to correctly set the sequence of the stages in switching cycles.
12. The active gate driver as claimed in claim 1, wherein the low frequency control take atleast one entire switching cycle to limit the current overshoot in the allowable tolerance range.

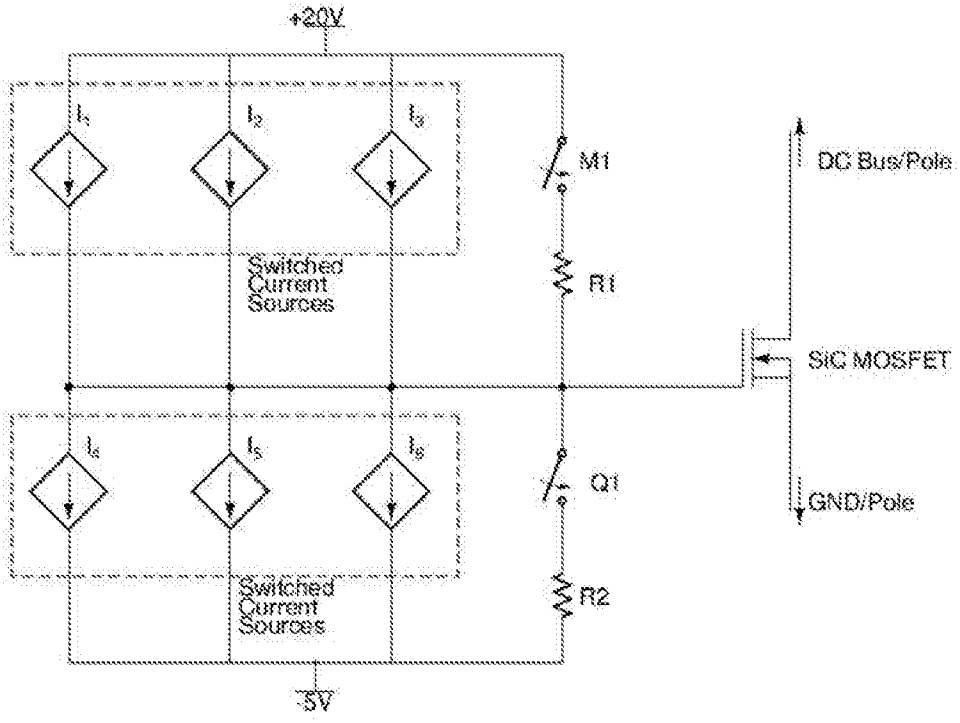

+20V
I1
I2
I3
M1
DC Bus/Pole
Switched Current Sources
R1
SiC MOSFET
I4
I5
I6
Q1
GND/Pole
Switched Current Sources
R2
-5V

FIGURE 1

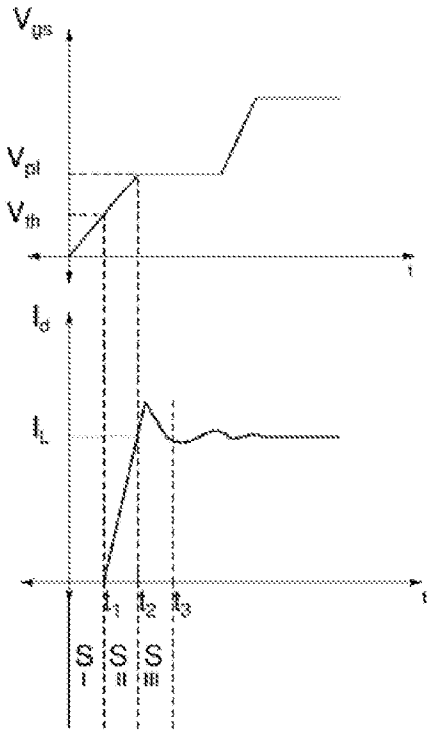


FIGURE 2

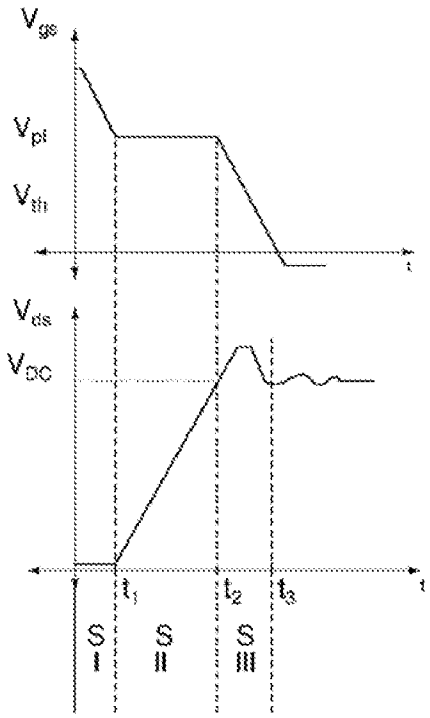


FIGURE 3

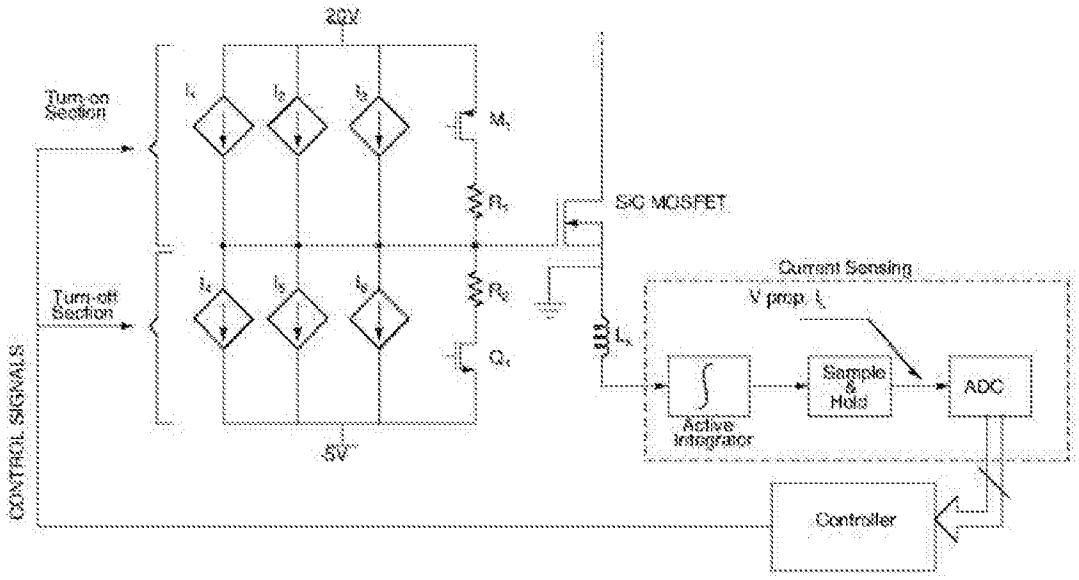

22V
Turn-on Section
Turn-off Section
CONTROL SIGNALS
SiC MOSFET
Current Sensing
V prop. I_L
Sample & Hold
ADC
Active Integrator
Controller
5V

FIGURE 4

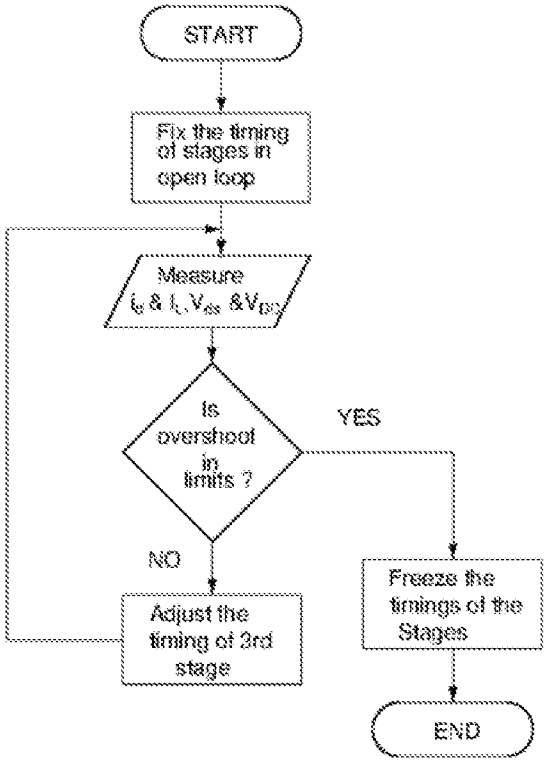

START
Fix the timing of stages in open loop
Measure
Is overshoot in limits ?
YES
NO
Adjust the timing of 3rd stage
Freeze the timings of the Stages
END

FIGURE 5

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
H01L29/772,H03K17/00 Version=2018.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: TotalPatent One, IPO Internal Database
Keywords: MOSFET, Active Gate Driver, Inductor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US20130181750A1 (ABB RESEARCH LTD.), 18 JULY 2013 (18-07-2013), Whole document	1-12
A	GB2532215A (MASCHINENFABRIK REINHAUSEN GMBH), 18 MAY 2016 (18-05-2016), Whole document	1-12
PA	IN201641042631A (INDIAN INSTITUTE OF TECHNOLOGY MADRAS), 15 JUNE 2018 (15-06-2018), Whole document	1-12

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12-09-2018	12-09-2018

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IN2018/050354

Citation	Pub.Date	Family	Pub.Date
US 20130181750 A1	18-07-2013	US 8710876 B2	29-04-2014
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