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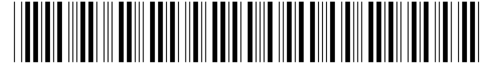

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(54) Process or forming MOS-gated devices having self-aligned trenches

(57) A process for forming an MOS-gated device having sell-aligned trenches, a screen oxide layer is formed on an upper layer of a semiconductor substrate, and a nitride layer is formed on the screen oxide layer. Using a well mask, the nitride layer is patterned and etched to define a well region in the upper layer, and ions of a first conduction type are diffused into the masked upper layer to form the well region. Ions of a second, opposite conduction type are implanted into the well region of the masked upper layer to form a source region extending to a selected depth that defines a source-well junction. The well mask is removed, exposing the portion of the nitride layer previously underlying the mask. An oxide insulating layer providing a hard mask is formed overlying the well and source regions in the upper layer. The remaining portions of the nitride layer and the screen oxide layer underlying it, which had been protected by the well mask, are removed, exposing the portion of the substrate not masked by the oxide insulating layer.

The portion of the substrate thus exposed is etched to form a gate trench extending through the substrate to a selected depth beneath the well region. Sidewalls and a floor of an insulator are formed in the gate trench, which is filled with a semiconductor. The semiconductor in the trench is planarized to be substantially coplanar with the upper surface of the oxide insulating layer. An interlevel dielectric layer is formed on the planarized gate trench semiconductor and the upper surface of the oxide insulating layer.

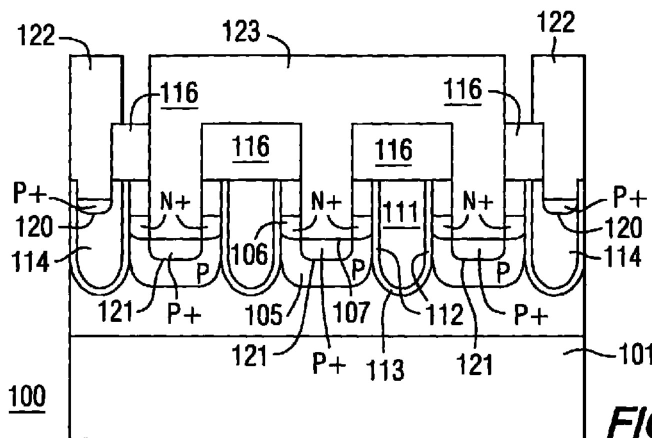

FIG. 1-9

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Description

[0001] The present invention relates to semiconductor devices and, more particularly, to process for forming MOS-gated devices having sell-aligned trenches.

[0002] An MOS transistor that includes a trench gate structure offers important advantages over a planar transistor for high current, low voltage switching applications. In the latter configuration, constriction occurs at high current flows, an effect that places substantial constraints on the design of a transistor intended for operation under such conditions.

[0003] A trench gate of a DMOS device typically includes a trench extending from the source to the drain and having sidewalls and a floor that are each lined with a layer of thermally grown silicon dioxide. The lined trench is filled with doped polysilicon. The structure of the trench gate allows less constricted current flow and, consequently, provides lower values of specific on-resistance. Furthermore, the trench gate makes possible a decreased cell pitch in an MOS channel extending along the vertical sidewalls of the trench from the bottom of the source across the body of the transistor to the drain below. Channel density is thereby increased, which reduces the contribution of the channel to on-resistance. The structure and performance of trench DMOS transistors are disclosed in Bulucea and Rossen, "Trench DMOS Transistor Technology for High-Current (100 A Range) Switching," in Solid-State Electronics, 1991, Vol. 34, No. 5, pp 493-507. In addition to their utility in DMOS devices, trench gates are also advantageously employed in insulated gate bipolar transistors (IGBTs), MOS-controlled thyristors (MCTs), and other MOS-gated devices.

[0004] Self-aligned trenches in an MOS device allow the distance between source and trench gate contacts to be substantially reduced, enabling a beneficial increase in packing density for VLSI fabrication. The specification of U.S. Patent No. 5,393,704 discloses a method of forming in and on a substrate a self-aligned trench contact for a device region that includes gate electrodes on the semiconductor substrate, source/drain regions within the substrate, and spacers on the gate electrode sidewalls. The sidewall spacers are used as a mask to provide an opening to the substrate where the trench contact is to be formed.

[0005] The specification of U.S. Patent No. 5,716,886 discloses a method of fabricating a high-voltage MOS device in which a silicon nitride layer is used as a mask to form trench type source/drain regions in a substrate. The trench source/drain regions contain two conductive layers; portions of the same two conductive layers are included in a gate on the substrate surface.

[0006] The specification of U.S. Patent No. 5,665,619 discloses a method of fabricating a DMOS transistor having self-aligned contact trenches that are etched through a masked oxide/nitride/oxide (ONO) sandwich on a silicon substrate. Gate polysilicon is deposited in the trenches and planarized with the nitride layer. The planarized polysilicon is covered with oxide; doping and four additional photolithographic masking steps are employed to form N+ source regions adjacent to the trenches and a P+ body ohmic content region between the source regions.

[0007] There is a continuing need for facilitating the fabrication of MOS-gated devices by a simplified process requiring fewer masking steps than are currently used.

[0008] The present invention includes a process for forming an MOS-gated device having self-aligned trenches, said process comprising:

(a) forming a screen oxide layer on an upper layer of a semiconductor substrate;
(b) forming a nitride layer on said screen layer;
(c) using a well mask, patterning and etching said nitride layer, thereby defining a well region in the masked upper layer of the substrate;
(d) implanting and diffusing ions of a first conduction type into the masked upper layer, to form a well region in said upper layer; characterized by
(e) implanting and diffusing ions of a second, opposite conduction type into the well region of the masked upper layer under conditions effective to form a source region extending to a selected depth in said upper layer, said selected depth defining a source-well junction;
(f) removing the well mask, so as to expose the portion of the nitride layer previously underlying said mask;
(g) forming an oxide insulating layer substantially overlying said well and source regions, said insulating layer forming a hard mask over a portion of the upper layer;
(h) etching said portion of the nitride layer and screen oxide layer underlying said nitride layer portion, to expose the portion of the upper layer not masked by the oxide insulating layer;
(i) etching said portion of the upper layer not masked by the oxide insulating layer, to form a gate trench extending into the upper layer to a selected depth below the well region;
(j) forming sidewalls and a floor comprising an insulator in said trench;
(k) filling the gate trench with a semiconductor, and planarizing the semiconductor in said trench to a surface substantially coplanar with an upper surface of the oxide insulating layer;
(l) forming an interlevel dielectric layer on the planarized trench semiconductor and the upper surface of the oxide insulating layer;
(m) forming a contact window mask on the interlevel dielectric layer and etching said interlevel dielectric layer and said oxide insulating layer, to form contact openings to the gate trench semiconductor

and the source region;

(n) through said contact openings, simultaneously etching the gate trench semiconductor and the source region, said source region being etched to a depth substantially corresponding to the depth of said source-well junction;

(o) implanting ions of said first conduction type through said contact openings into the gate trench semiconductor and the source region;

(p) removing said contact window mask and depositing metal on said interlevel dielectric layer and in said contact openings; and

(q) patterning said metal to form discrete source and gate connectors.

[0009] The invention also includes a process for forming a sell-aligned gate trench in a vertical MOS device, said process comprising:

(a) forming a first mask on an upper surface of a semiconductor substrate to define potential well-source regions in said substrate;

(b) implanting well dopants and source dopants into said potential well-source regions, thereby forming, respectively, well regions and source regions in said substrate;

(c) growing an oxide mask over said well regions and said source regions;

(d) removing the first mask; and

(e) using the oxide mask, etching gate trenches between said source regions, said trenches extending into the substrate to a selected depth below said well regions.

[0010] Conveniently, the present invention is directed to a process for forming an MOS-gated device having self-aligned trenches. A screen oxide layer is formed on an upper layer of a semiconductor substrate, and a nitride layer is formed on the screen oxide layer. Using a well mask, the nitride layer is patterned and etched to define a well region in the upper layer, and ions of a first conduction type are diffused into the masked upper layer to form the well region.

[0011] Ions of a second, opposite conduction type are implanted into the well region of the masked upper layer to form a source region extending to a selected depth that defines a source-well junction. The well mask is removed, exposing the portion of the nitride layer previously underlying the mask. An oxide insulating layer providing a hard mask is formed overlying the well and source regions in the upper layer. The remaining portions of the nitride layer and the screen oxide layer underlying it, which had been protected by the well mask, are removed, thereby exposing the portion of the substrate not masked by the oxide insulating layer.

[0012] The portion of the substrate thus exposed is etched to form a gate trench extending through the substrate to a selected depth beneath the well region. Sidewalls and a floor of an insulator are formed in the gate trench, which is filled with a semiconductor. The semiconductor in the trench is planarized to be substantially coplanar with the upper surface of the oxide insulating layer. An interlevel dielectric layer is formed on the planarized gate trench semiconductor and the upper surface of the oxide insulating layer. Following formation of a contact window mask on the interlevel dielectric layer, it and the underlying oxide insulating layer are etched to form contact openings to gate semiconductor and the source region.

[0013] The gate semiconductor and the source region are simultaneously etched through the contact openings, the source region being etched to a depth substantially corresponding to the depth of the source-well junction. Ions of the first conduction type are implanted through the contact openings into the gate semiconductor and the source region. The contact window mask is removed, and metal is deposited on the interlevel dielectric layer and in the contact openings, then patterned to form discrete source and gate connectors.

[0014] The invention will now be described, by way of example, with reference to the accompanying drawings in which:

FIGS. 1-1 through 1-9 schematically depict the process for forming an MOS-gated device.

[0015] The simplified process for fabricating an MOS-gated device is schematically depicted in FIGS. 1-1 through 1-9. As shown in FIG. 1-1, a semiconductor substrate 101 has an upper layer 102, on which is formed a thin screen oxide layer 103. A nitride layer 104 is deposited on layer 103 and patterned by a photoresist well mask WM. Semiconductor substrate 101 preferably comprises monocrystalline silicon, upper layer 102 comprises epitaxially grown silicon, and screen layer 103 comprises silicon dioxide. The deposition of nitride layer 104 can be carried out by chemical vapor deposition (CVD) or low pressure chemical vapor deposition (LPCVD).

[0016] As shown in FIG. 1-2, well regions 105 are formed by implantation and diffusion by ions of a first conduction type, following which source regions 106 are formed by implantation and diffusion of ions of a second, opposite conduction type to a selected depth that defines a source-well junction 107. Following formation of well regions 105 and source regions 106, well mask WM is stripped from screen layer 103.

[0017] In FIG. 1-2, the first conduction type is represented as P, producing P-well regions 105, and the second conduction type is N, resulting in N+ source regions 106. It is understood that these conduction types can each be reversed to the opposite type. Boron is a preferred P dopant; arsenic and phosphorus are useful N dopants.

[0018] As depicted in FIG. 1-3, an oxide insulating

layer 108, silicon dioxide, is formed over source regions 106 and well regions 105. A small amount of oxide insulating layer 108, which has a thickness of at least about 1200 angstroms, is etched to form surface 109; this etching step ensures that any oxide formed on nitride layer 104 is concurrently removed. Nitride layer 104 is then removed by selective etching, leaving the structure depicted in FIG. 1-4.

[0019] Oxide insulating layer 108, which has substantially vertical sidewalls 110, provides a hard mask for the etching of trenches 111, which extend substantially to a selected depth 112 below that of well regions 105, as shown in FIG. 1-5. Insulating sidewalls 112 and floor 113, preferably comprising silicon dioxide, are formed in trenches 111, as depicted in FIG. 1-6. Trenches 111 are filled with a semiconductor 114, comprising polysilicon. The semiconductor 114 is planarized by etching or mechanical processing to provide a surface 115 that is substantially coplanar with surface 109 of oxide insulating layer 108.

[0020] As shown in FIG. 1-7, an interlevel dielectric layer 116 is deposited on surfaces 109 and 115 and patterned and etched using a contact window mask (not shown) to provide trench contact openings 117 and source contact openings 118. The interlevel dielectric layer 116 can be formed from, for example borophosphosilicate glass (BPSG). Silicon dimple etching using the patterned interlevel dielectric layer 116 as a hard mask is employed to extend trench contact openings 117 to depth 119 and source contact openings 118 through source regions 106 substantially to source-well junctions 107. Implantation and diffusion of ions of the first conduction type through contact openings 117 and 118 produces P+ regions 120 in gate semiconductor 114 and P+ emitter regions 121 adjacent to source regions 106.

[0021] Following removal of the contact window mask (not shown), a metal such as aluminum is deposited and patterned, as shown in FIG. 1-9, to provide gate connectors 122 and source/ emitter connectors 123, thereby completing the fabrication of device 100 in accordance with the present invention.

[0022] The process which utilizes oxide insulating layer 108 and interlevel dielectric layer 116 as hard masks and requires only three photolithographic masks (well, contact window, and metal), is significantly simpler and more convenient than typical known device fabrication processes.

[0023] In a process for forming an MOS-gated device having self-aligned trenches, a screen oxide layer is formed on an upper layer of a semiconductor substrate, and a nitride layer is formed on the screen oxide layer. Using a well mask, the nitride layer is patterned and etched to define a well region in the upper layer, and ions of a first conduction type are diffused into the masked upper layer to form the well region. Ions of a second, opposite conduction type are implanted into the well region of the masked upper layer to form a source region extending to a selected depth that defines a source-well junction. The well mask is removed, exposing the portion of the nitride layer previously underlying the mask. An oxide insulating layer providing a hard mask is formed overlying the well and source regions in the upper layer. The remaining portions of the nitride layer and the screen oxide layer underlying it, which had been protected by the well mask, are removed, thereby exposing the portion of the substrate not masked by the oxide insulating layer.

[0024] The portion of the substrate thus exposed is etched to form a gate trench extending through the substrate to a selected depth beneath the well region. Sidewalls and a floor of an insulator are formed in the gate trench, which is filled with a semiconductor. The semiconductor in the trench is planarized to be substantially coplanar with the upper surface of the oxide insulating layer. An interlevel dielectric layer is formed on the planarized gate trench semiconductor and the upper surface of the oxide insulating layer.

Claims

1. A process for forming an MOS-gated device having self-aligned trenches, said process comprising:

(a) forming a screen oxide layer on an upper layer of a semiconductor substrate;
(b) forming a nitride layer on said screen layer;
(c) using a well mask, patterning and etching said nitride layer, thereby defining a well region in the masked upper layer of the substrate;
(d) implanting and diffusing ions of a first conduction type into the masked upper layer, to form a well region in said upper layer; characterized by
(e) implanting and diffusing ions of a second, opposite conduction type into the well region of the masked upper layer under conditions effective to form a source region extending to a selected depth in said upper layer, said selected depth defining a source-well junction;
(f) removing the well mask, so as to expose the portion of the nitride layer previously underlying said mask;
(g) forming an oxide insulating layer substantially overlying said well and source regions, said insulating layer forming a hard mask over a portion of the upper layer;
(h) etching said portion of the nitride layer and screen oxide layer underlying said nitride layer portion, to expose the portion of the upper layer not masked by the oxide insulating layer;
(i) etching said portion of the upper layer not masked by the oxide insulating layer, to form a gate trench extending into the upper layer to a selected depth below the well region;
(j) forming sidewalls and a floor comprising an

insulator in said trench;

(k) filling the gate trench with a semiconductor, and planarizing the semiconductor in said trench to a surface substantially coplanar with an upper surface of the oxide insulating layer;

(l) forming an interlevel dielectric layer on the planarized trench semiconductor and the upper surface of the oxide insulating layer;

(m) forming a contact window mask on the interlevel dielectric layer and etching said interlevel dielectric layer and said oxide insulating layer, to form contact openings to the gate trench semiconductor and the source region;

(n) through said contact openings, simultaneously etching the gate trench semiconductor and the source region, said source region being etched to a depth substantially corresponding to the depth of said source-well junction;

(o) implanting ions of said first conduction type through said contact openings into the gate trench semiconductor and the source region;

(p) removing said contact window mask and depositing metal on said interlevel dielectric layer and in said contact openings; and

(q) patterning said metal to form discrete source and gate connectors.

2. A process as claimed in claim 1 characterized by

(g') etching a small portion of the oxide insulating layer, to define an upper surface of said layer and removing any oxide present on said portion of the nitride layer;

3. A process as claimed in claim 1 characterized by said substrate comprises monocrystalline silicon and aid upper layer comprises epitaxially grown silicon, and in which said screen oxide layer, said oxide insulating layer, and said trench sidewalls and floor each comprise silicon dioxide.

4. A process as claimed in claim 4 characterized by said oxide insulating layer has a thickness of at least about 1200 angstroms.

5. A process as claimed in claim 1 characterized by said semiconductor in said gate trench comprises polysilicon, said first conduction type is P and said second conduction type is N, or said first conduction type is N and said second conduction type is P.

6. A process as claimed in claim 1 wherein said implanting and diffusing ions of a first conduction type comprises implanting and diffusing boron ions, and said implanting and diffusing ions of a second conduction type comprises implanting arsenic ions or phosphorus ions.

7. A process as claimed in claim 1 characterized by said interlevel dielectric layer comprises borophosphosilicate glass, and said metal comprises aluminum.

8. A process for forming a self-aligned gate trench in a vertical MOS device, said process comprising:

(a) forming a first mask on an upper surface of a semiconductor substrate to define potential well- source regions in said substrate;

(b) implanting well dopants and source dopants into said potential well-source regions, thereby forming, respectively, well regions and source regions in said substrate;

(c) growing an oxide mask over said well regions and said source regions;

(d) removing the first mask; and

(e) using the oxide mask, etching gate trenches between said source regions, said trenches extending into the substrate to a selected depth below said well regions.

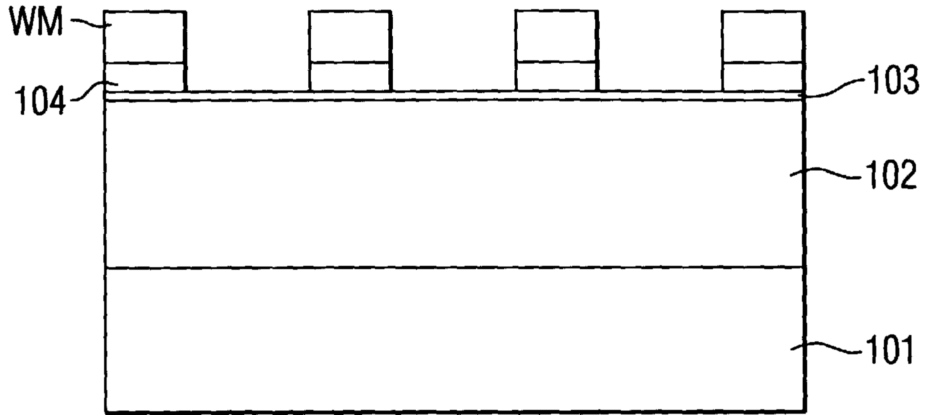

FIG. 1-1

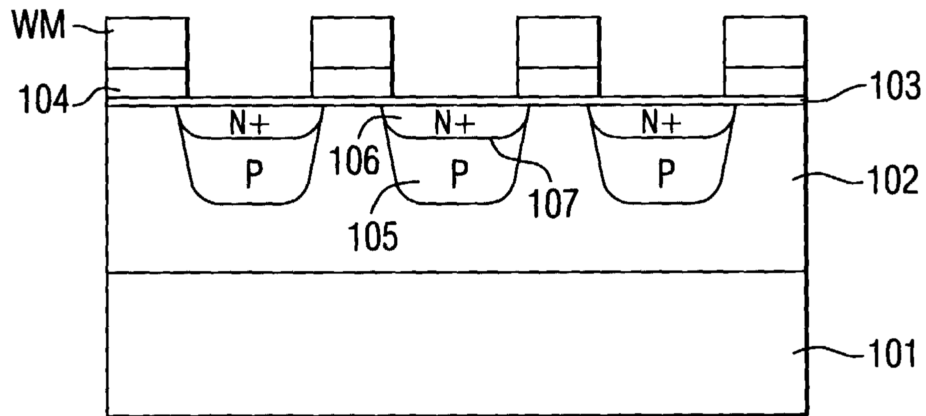

FIG. 1-2

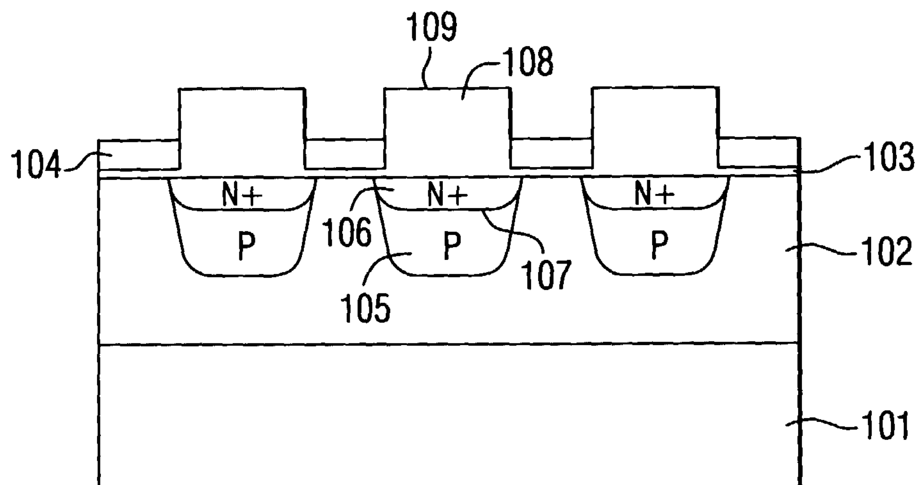

FIG. 1-3

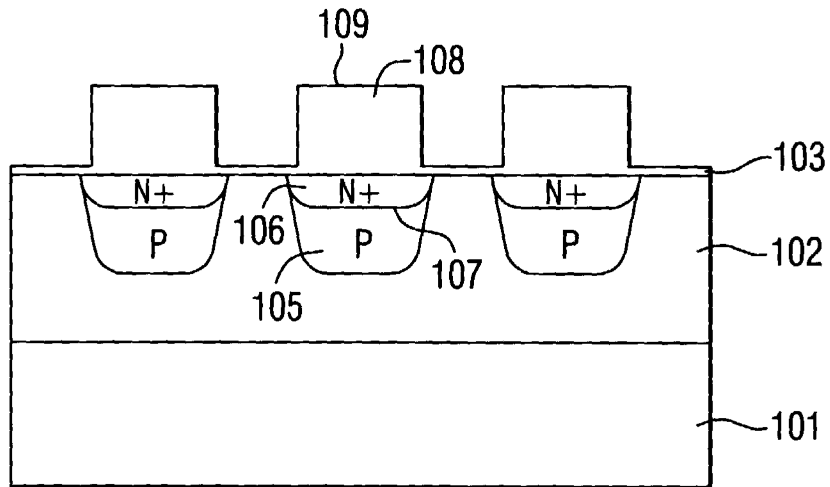

FIG. 1-4

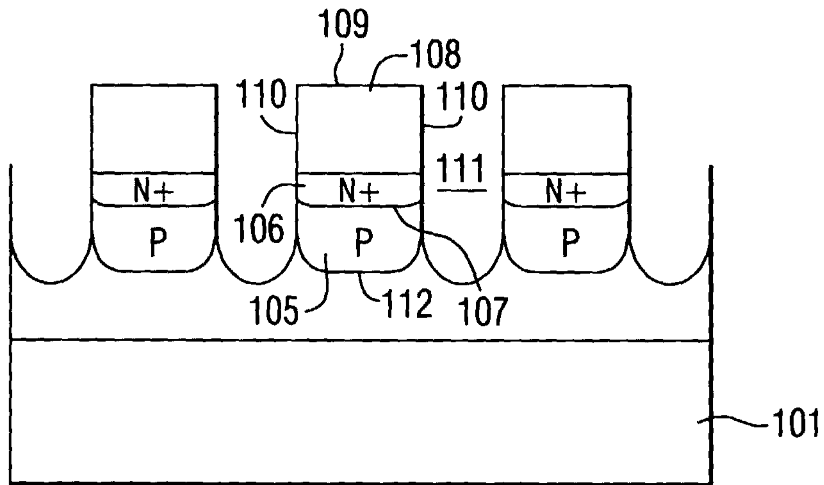

FIG. 1-5

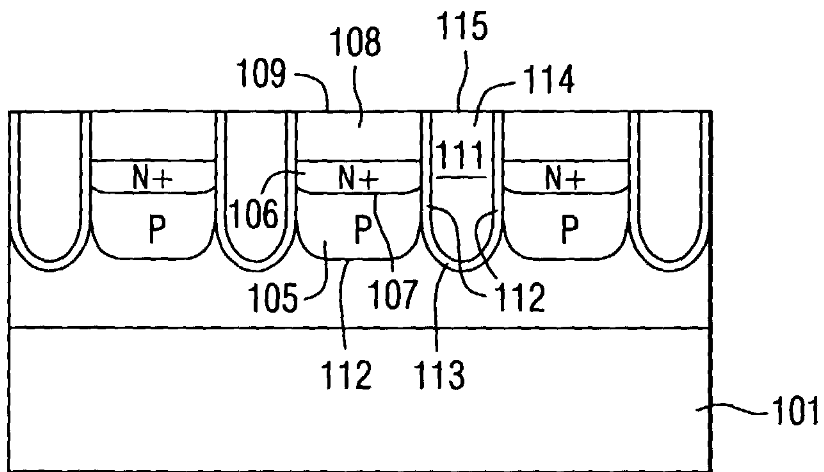

FIG. 1-6

FIG. 1-7

FIG. 1-8

FIG. 1-9