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(54) Title: TEMPERATURE COMPENSATION CIRCUITS

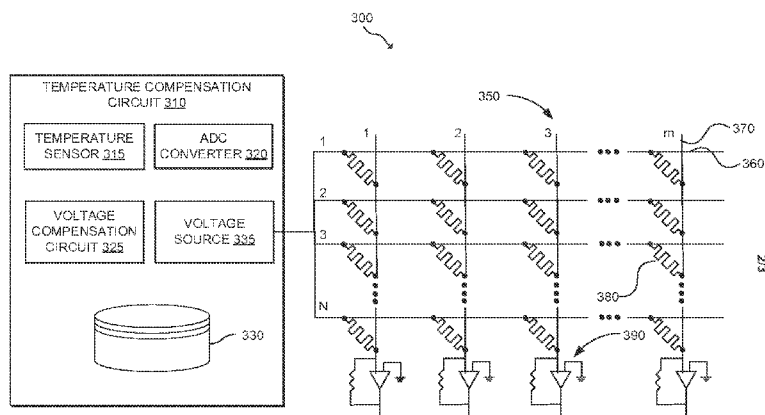


FIG. 3

(57) Abstract: A temperature compensation circuit may comprise a temperature sensor to sense a temperature signal of a memristor crossbar array, a signal converter to convert the temperature signal to an electrical control signal, and a voltage compensation circuit to determine a compensation voltage based on the electrical control signal and pre-calibrated temperature data of the memristor crossbar array.

TEMPERATURE COMPENSATION CIRCUITS

BACKGROUND

[0001] Memristors are devices that can be programmed to different resistive states by applying a programming energy, such as a voltage. Large crossbar arrays of memory devices can be used in a variety of applications, including random access memory, non-volatile solid state memory, programmable logic, signal processing control systems, pattern recognition, and other applications. The electrical properties of memristors may be affected by the temperature of the memristors or its surrounding circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The following detailed description references the drawings, wherein:

[0003] FIG. 1 is a block diagram of an example temperature compensation circuit;

[0004] FIG. 2 is a diagram of an example crossbar array;

[0005] FIG. 3 is a diagram of an example crossbar array with a temperature compensation circuit; and

[0006] FIG. 4 is a flowchart of an example method for applying a compensated voltage.

DETAILED DESCRIPTION

[0007] Memristors are devices that may be used as components in a wide range of electronic circuits, such as memories, switches, radio frequency circuits, and logic circuits and systems. A memristor crossbar array can be used to perform vector-matrix or dot product computations. For example, an input voltage signal from each row of the crossbar is weighted by the conductance of the resistive devices in each column and accumulated as the current output from each column. Ideally, if wire resistances can be ignored, the current vector, I , flowing out of the crossbar array will be approximately $I^T = V^T G$, where V is the input voltage vector and G is the conductance matrix, including contributions from each

memristor in the crossbar array. The need for fast and efficient vector-matrix processing techniques arises in many computing applications. For example, vector-matrix operations are utilized in data-compression, digital data processing, neural networks, encryption, and optimization, to name a few.

[0008] The use of memristors at each junction or cross-point of the crossbar array enables programming the resistance (or conductance) at each such junction corresponding to the values of G , leading to use of the crossbar array as a dot product engine (DPE). Accuracy is important in the design and application of dot product engines. However, many memristors exhibit electrical properties that are temperature-dependent. For example, the resistance of a memristor may depend on the temperature of the memristor. Because temperature fluctuations are common in circuit operations, using a memristor crossbar array as a DPE may present challenges in ensuring accurate calculations. For example, stabilizing the temperature of crossbar arrays may be practically difficult.

[0009] Examples disclosed herein provide for temperature compensation circuits to account for temperature fluctuations in a memristor crossbar array. In example implementations, temperature compensation circuits may include a temperature sensor to sense a temperature of the memristor crossbar array. Example temperature compensation circuits may have a signal converter to convert the temperature to an electrical control signal. The electrical control signal may direct a voltage compensation circuit to determine a compensation voltage based on pre-calibrated temperature data of the memristor crossbar array. In this manner, examples herein provide for temperature compensation of a memristor crossbar array. By accounting for temperature effects, memristor crossbar arrays can be used as accurate dot product engines.

[0010] Referring now to the drawings, FIG. 1 is a block diagram of an example temperature compensation circuit 100. Temperature compensation circuit 100 may determine a compensation voltage that may be applied to a memristor crossbar array in order to neutralize or account for temperature effects on the resistance of the memristors of the array. Temperature compensation circuit 100 may have a temperature sensor 110, a signal converter which is illustrated in FIG. 1 as an analog-to-digital (ADC) converter 120, a voltage compensation circuit 130, and a storage 140.

[0011] Temperature sensor 110 may sense a temperature of a memristor crossbar array. Temperature sensor 110 may be a device, circuit, or component that is capable of sensing the temperature of an object. Specifically, temperature sensor 110 may sense the temperature of the memristor crossbar array to detect the temperature effect on the memristors. Examples for temperature sensor 110 may include thermistors, diode sensors, temperature coefficient sensors, and bandgap circuit sensors. Other examples include mechanical sensors such as thermometers and bimetal sensors. In some examples, temperature sensor 110 may include memristors.

[0012] A memristor crossbar array may be a configuration of sets of parallel crossing lines with memristors and/or other components coupled between intersections of lines. For example, a memristor array may have a first plurality of parallel lines referred to as row lines intersecting another plurality of parallel lines referred to as column lines, where memristors serve as cross-points of the lines. Each memristor of a memristor array may be coupled between a unique combination of a row line and a column line. In other words, no memristors share both a row line and a column line. As used herein, components may be coupled by forming an electrical connection between the components. For example, memristors may be coupled to lines by forming a direct, surface contact or by other forms of physical connection. Additional discussion of memristors and crossbar arrays are provided herein in relation to FIG. 2.

[0013] ADC converter 120 may be a device that converts a continuous physical quantity to a digital number that represents the quantity. Specifically, ADC converter 120 may convert the temperature sensed by the temperature sensor 110 to a digital control signal. For example, ADC converter 120 may take a continuous-time and continuous-amplitude analog temperature signal and convert it to a sequence of digital values that represent a discrete-time and discrete-amplitude digital signal. The digital control signal may communicate the temperature sensed by temperature sensor 110 to voltage compensation circuit 130. It should be noted that while 120 illustrates an ADC converter, other types of signal converters may be used according to the teachings herein.

[0014] Voltage compensation circuit 130 may determine a compensation voltage based on the digital control signal provided by ADC converter 120 and pre-calibrated temperature

data of the memristor crossbar array, which may be stored in and accessed from storage 140. The digital control signal may tell voltage compensation circuit 130 the temperature of the memristors in the array. The pre-calibrated temperature data can be accessed and compared to determine the amplitude of the compensation voltage.

[0015] In some implementations, the pre-calibrated temperature data of the memristor crossbar array may include temperature-dependent resistance of the memristors. As described previously, the resistance of the memristors may change depending on the temperature of the memristors. This data may be stored in storage 140 and accessed by voltage compensation circuit 130 in determining the compensation voltage. For example, voltage compensation circuit 130 may determine the compensation voltage by matching the temperature of the memristor crossbar array with the pre-calibrated data.

[0016] Storage 140 may store the pre-calibrated temperature data of the memristor crossbar array. Storage 140 may be any electronic, magnetic, optical, or other physical storage device. Thus, storage 140 may be for example, a Random Access Memory (RAM), an Electrically Erasable Programmable Read-Only Memory (EEPROM), a storage device, an optical disc, and the like. Storage 140 may be a non-transitory storage medium, where the term "non-transitory" does not encompass transitory propagating signals. Storage 140 may be located in temperature compensation circuit 100, in another device in communication with temperature compensation circuit 100, or it may be, for example, cloud-hosted storage.

[0017] FIG. 2 is a diagram of an example memristor crossbar array 200, such as an example crossbar array operable connected to temperature compensation circuit 100. Memristor array 200 may be a configuration of parallel and perpendicular lines with memristors and other components coupled between lines at cross-points. Memristor array 200 may include a plurality of row lines 210, a plurality of column lines 220, and a plurality of memristors 230. Each memristor may be coupled between a unique combination of one row line and one column line. In other words, no memristors share both a row line and a column line. Memristor array 200 may be used in a variety of applications, including as a dot product engine as described herein.

[0018] Row lines 210 may be electrodes that carry current through memristor array 200. In some examples, row lines 210 may be in parallel to each other, generally with equal spacing. Row lines 210 may sometimes be referred to as bit lines. Depending on orientation, row lines 210 may alternatively be referred to as word lines. Similarly, column lines 220 may be electrodes that run nonparallel to row lines 210. Column lines 220 may be referred to as word lines in some conventions. In other orientations, column lines 220 may refer to bit lines. Row lines 210 and column lines 220 may be made of conducting materials, such as platinum (Pt), tantalum (Ta), hafnium (Hf), zirconium (Zr), aluminum (Al), cobalt (Co), nickel (Ni), iron (Fe), niobium (Nb), molybdenum (Mo), tungsten (W), copper (Cu), titanium (Ti), tantalum nitrides (TaN_x), titanium nitrides (TiN_x), WN_2 , NbN , MoN , TiSi_2 , TiSi , Ti_5Si_3 , TaSi_2 , WSi_2 , NbSi_2 , V_3Si , electrically doped Si polycrystalline, electrically doped Ge polycrystalline, and combinations thereof. Row lines 210 and column lines 220 may serve as electrodes that deliver voltage and current to the memristors 230.

[0019] Memristors 230 may be coupled between row lines 210 and column lines 220. In some implementations, a memristor 230 may have a resistance that changes with an applied voltage or current. Furthermore, memristor 230 may “memorize” its last resistance. In this manner, each memristor 230 may be set to at least two states. Furthermore in some examples, other components may be coupled with memristors 230. For example, each memristor may be coupled in series with a transistor and/or a selector.

[0020] In some examples, the resistance of the memristors 230 may be dependent on its temperature. For example, the resistance of a memristor 230 may decrease with increasing temperature. Accordingly, the current through each memristor 230 may depend on its temperature in addition to an applied voltage.

[0021] In some examples, a memristor may be nitride-based, meaning that at least a portion of the memristor is formed from a nitride-containing composition. A memristor may also be oxide-based, meaning that at least a portion of the memristor is formed from an oxide-containing material. Furthermore, a memristor may be oxy-nitride based, meaning that at least a portion of the memristor is formed from an oxide-containing material and that at least a portion of the memristor is formed from a nitride-containing material. Example materials of memristors may include tantalum oxide, hafnium oxide, titanium oxide,

yttrium oxide, niobium oxide, zirconium oxide, or other like oxides, or non-transition metal oxides, such as aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, silicon nitride, and oxynitrides such as silicon oxynitride. In addition, other functioning memristors may be employed in the practice of the teachings herein.

[0022] Memristors 230 may exhibit nonlinear or linear current-voltage behavior. Nonlinear may describe a function that grows differently than a linear function. For example, this may mean that current flowing through memristor 230 increases faster than linear growth with relation to applied voltage. Linear materials may follow Ohm's law, where the current through them is proportional to the voltage. On the other hand, the current flowing through a nonlinear material may disproportionately increase as the voltage is increased. In some implementations, such as a typical DPE application, the memristors 230 may be linear.

[0023] FIG. 3 is a diagram of an example memory circuit 300 with a crossbar array 350 and a temperature compensation circuit 310. Temperature compensation circuit 310 may be analogous to temperature compensation circuit 100 of FIG. 1, and crossbar array 350 may be analogous to crossbar array 200 of FIG. 2. System 300 may be utilized as a dot product engine. In some examples, system 300 may be a part of a larger system, such as a computing device. For example, system 300 may be components on a computing chip. In some examples, memory circuit 300 may be used as a memristive dot product engine.

[0024] Temperature compensation circuit 310 may include a temperature sensor 315 analogous to temperature sensor 110, an ADC converter 320 analogous to ADC converter 120, voltage compensation circuit 325 analogous to voltage compensation circuit 130, and storage 330 analogous to storage 140. Temperature sensor 110 may sense a temperature of crossbar array 350. ADC converter 320 may convert the temperature to a digital control signal. Voltage compensation circuit 325 may determine a compensation voltage based on the digital control signal and on temperature-dependent resistance of memory elements 380 of crossbar array 350. The temperature-dependent resistance of memory elements 380 may be stored in and accessed from storage 330.

[0025] Additionally, temperature compensation circuit 310 may include at least one voltage source 335 to apply the compensation voltage to crossbar array 350. The compensation voltage may compensate for a difference in resistance of the memory cells as a result of the temperature of the crossbar array 350. Voltage source 335 may be coupled to the crossbar array 350 so that all of the memory cells 380 may be accessed by the compensation voltage. For example, voltage source 335 may be coupled to all of the plurality of row lines 360 or all of the plurality of column lines 370 or both. As shown in FIG. 3, voltage source 335 is connected to the row lines 360 of crossbar array 350.

[0026] In some examples, temperature compensation circuit 310 may include one voltage source 335 that provides the compensation voltage to all of the lines or multiple lines of crossbar array 350. Alternatively, temperature compensation circuit 310 may include multiple voltage sources 335. For example, each line may be connected to a different voltage source 335.

[0027] In some implementations, temperature sensor 315 may sense the temperature of individual memory cells 380 or groups of memory cells. In such cases, the compensation voltage to be applied by each voltage source 335 may be different due to different memory cells having different temperatures, which may result in the memory cells exhibiting different resistances.

[0028] In some examples, the compensation voltage is added to an input voltage which is applied during the DPE operation in order to obtain a compensated voltage. The compensated voltage may cause an amount of current to pass through memristors 380 that may be equivalent to the current that would pass through the memristor when the input voltage is applied while the memristor is at a neutral temperature. The neutral temperature may be the temperature at which the resistance of the memristor is calibrated.

[0029] Crossbar array 350 may include a plurality of row lines 360, a plurality of column lines 370, a plurality of memory cells 380, and a plurality of sensing circuits 390. Crossbar array 350 may be connected to temperature compensation circuit 310, which may provide a compensation voltage that may compensate for temperature effects on the crossbar array.

[0030] As illustrated in FIG. 3, voltages may be applied to row lines 360, which causes a current to be driven through memory cells 380. In some examples, sensing circuits 390 may convert an electrical current, such as that passing through the memory cells, in a column line 370 to a voltage. In an example of the principles described herein, the sensing circuits 390 include an operational amplifier and a resistor, which can be arranged to represent a virtual ground for read operations.

[0031] Although not illustrated in FIG. 3, crossbar array 350 may also include other peripheral circuitry. For example, crossbar array 350 may include drivers connected to the row lines 360. An address decoder can be used to select a row line 360 and activate a driver corresponding to the selected row line 360. The driver for a selected row line 360 can drive a corresponding row line 360 with different voltages corresponding to a vector-matrix multiplication or the process of setting resistance values within the memory cells 380 of the crossbar array 350. In some examples, the drivers may be the voltage sources 335 of the temperature compensation circuit 310. Similar driver and decoder circuitry may be included for the column lines 370.

[0032] Control circuitry may also be used to control application of voltages at the inputs and reading of voltages at the outputs of the crossbar array 350. Digital to analog circuitry and analog to digital circuitry may be used in some examples in the control circuitry. The peripheral circuitry above described can be fabricated using semiconductor processing techniques in the same integrated structure or semiconductor die as crossbar array 350.

[0033] As described in further detail below, there are two main operations that occur during operation of a dot-product engine. The first operation is to program memristors in a crossbar array so as to map the mathematic values in an $N \times M$ matrix to the array. In one example, only one memristor is programmed at a time during the programming operation. The second operation is the dot-product or matrix multiplication operation. In this operation, input voltages are applied and output voltages obtained, corresponding to the result of multiplying an $N \times M$ matrix by an $N \times 1$ vector. Generally, the input voltages are below the threshold of programming voltages of the memristors so the resistance values of the memristors in the array are not changed during the matrix multiplication operation.

[0034] In one example of dot-product engine operation according to the principles described herein, vector and matrix multiplications may be executed through memory circuit 300 by applying a set of voltages simultaneously along the row lines 360 of the NxM crossbar array 350 and collecting the currents through the column lines 370 and measuring the output voltage. On each column, every input voltage is weighted by a corresponding memristance ($1/G_{ij}$) and the weighted summation is reflected at the output voltage. Using Ohm's law, the relation between the input voltages and output voltages can be represented by a vector matrix multiplication of the form: $\{VO\}^T = - \{VI\}^T [G] RS$, where G_{ij} is an NxM matrix determined by the conductance (inverse of resistance) of the crossbar array 350, RS is the resistance value of the sense amplifiers and T denotes the transpose of the column vectors VO and VI. The negative sign follows from use of a negative feedback operational amplifier in the sense amplifiers. From the foregoing, it follows that the dot-product engine can be utilized for vector processing and, more specifically, for multiplying a first vector of values $\{b_i\}^T$ by a matrix of values $[a_{ij}]$ to obtain a second vector of values $\{c_j\}^T$, where $i=1,N$ and $j=1,M$. The vector operation can be set forth in more detail as follows.

$$a_{11}b_1 + a_{21}b_2 + \dots + a_{N1}b_N = c_1$$

...

$$a_{1M}b_1 + a_{2M}b_2 + \dots + a_{NM}b_N = c_M.$$

[0035] The vector processing or multiplication using the principles described herein generally starts by mapping a matrix of values $[a_{ij}]$ onto the crossbar array 350 or, stated otherwise, programming — e.g., writing — conductance values G_{ij} into the crossbar junctions of array 350. In one example, each of the conductance values G_{ij} is set by sequentially imposing a voltage drop over each of the crossbar junctions. For example, the conductance value $G_{2,3}$ may be set by applying a voltage equal to V_{Row2} at the 2nd row line 360 of the crossbar array 350 and a voltage equal to V_{Col3} at the 3rd column line of the array. In one example, the voltage input, V_{Row2} , will be applied to the 2nd row line adjacent the $j=1$ column electrode. The voltage input, V_{Col3} , will be applied to the 3rd column line adjacent

either the $i=1$ or $i=N$ location. When applying a voltage at a column line, the sensing circuit 390 for that line may be switched out and a voltage driver switched in. The voltage difference $V_{Row2} - V_{Col3}$ will generally determine the resulting conductance value $G_{2,3}$ based on the characteristics of the memory cell 380 located at the intersection. When following this approach, the unselected column lines and row lines may be addressed according to one of several schemes, including, for example, floating all unselected columns and rows or grounding all unselected columns and rows. Other schemes involve grounding columns or grounding partial columns. Grounding all unselected columns and rows is beneficial in that the scheme helps to isolate the unselected columns and rows to minimize the sneak path currents to the selected output column. Following programming, operation of the dot-product engine proceeds by applying the vector of input voltages and reading the vector of output voltages.

[0036] In accordance with an example of the principles disclosed herein, the memory cells 380 used for the dot product engine may have a linear current-voltage relation. For example memory cell 380 may have a linear memristor. Linear current-voltage relations permit higher accuracy in the vector multiplication process. However, crossbar arrays 350 having linear memristors are prone to having large sneak path currents during programming of the array, particularly when the size of the crossbar array 350 is larger than a certain size, for instance, 32×32 . In such cases, the current running through a selected memory cell 380 may not be sufficient to program the memory cell because most of the current runs through the sneak paths.

[0037] Alternatively, a memory cell 380 may be programmed at an inaccurate value because of the sneak paths. To alleviate the sneak path currents in such instances, and especially when larger arrays are desired, an access device, such as a non-linear selector or transistor (e.g., a normally ON depletion mode transistor) may be incorporated within or utilized in the memory cell 380 to minimize the sneak path currents in the array. More specifically, memory cell 380 should be broadly interpreted to include memristive devices including, for example, a memristor, a memristor and selector, or a memristor and transistor.

[0038] FIG. 4 depicts an example method 400 for applying a compensated voltage. Although execution of method 400 is described below with reference to memory circuit 300

of FIG. 3, other suitable components for execution of method 400 should be apparent, including voltage compensation circuit 100 of FIG. 1.

[0039] In an operation 410, temperature sensor 315 may sense a temperature of memory crossbar array 350. In some implementations, temperature sensor 315 may sense the temperature of individual memory elements 380 or groups of memory elements. In some examples, the temperature of the memory cell may be communicated to ADC converter 320, which may convert the temperature data to a digital control signal.

[0040] In an operation 420, voltage compensation circuit 325 may receive a temperature-dependent resistance of memory elements 380 of crossbar array 350. Temperature-dependent resistance of the memory elements may be pre-calibrated and may be stored in storage 330 to be accessed.

[0041] In an operation 430, voltage compensation circuit 325 may determine a compensation voltage based on the temperature of crossbar array 350 and on the temperature-dependent resistance of memory elements 380. For example, voltage compensation circuit 325 may receive the digital control signal from ADC converter. The digital control signal may communicate the temperature levels of crossbar array 350 and/or the individual memory elements 380. Voltage compensation circuit 325 may match digital control signal with the pre-calibrated resistance data to determine the compensation voltage.

[0042] In an operation 440, voltage source 335 may apply a compensated voltage, which includes the compensation voltage and an input voltage. The input voltage may be a default voltage that produces a certain amount of current through a memory element 380 at a neutral or calibration temperature. Therefore, the compensated voltage provides the input voltage adjusted by the compensation voltage in order to account for temperature differences in the crossbar array 350.

[0043] The foregoing describes a number of examples for voltage compensation circuits. It should be understood that the voltage compensation circuits and applications described herein may include additional components or steps and that some of the components or steps described herein may be removed or modified without departing from the scope of the voltage compensation circuits. It should also be understood that the

components depicted in the figures are not drawn to scale, and thus, the components may have different relative sizes with respect to each other than as shown in the figures.

[0044] It should be noted that, as used in this application and the appended claims, the singular forms “a,” “an,” and “the” include plural elements unless the context clearly dictates otherwise.

CLAIMS

What is claimed is:

1. A temperature compensation circuit, comprising:
a temperature sensor to sense a temperature signal of a memristor crossbar array;
a signal converter to convert the temperature signal to an electrical control signal;
and
a voltage compensation circuit to determine a compensation voltage based on the electrical control signal and pre-calibrated temperature data of the memristor crossbar array.
2. The temperature compensation circuit of claim 1, further comprising a voltage source to apply the compensation voltage to the memristor crossbar array.
3. The temperature compensation circuit of claim 1, wherein the pre-calibrated temperature data comprises a temperature-dependent resistance of the memristors.
4. The temperature compensation circuit of claim 3, wherein the compensation voltage is to compensate for a difference in resistance of the memristors as a result of the temperature of the memristor crossbar array.
5. The temperature compensation circuit of claim 1, wherein the memristor crossbar array comprises:
a plurality of row lines;
a plurality of column lines;
a plurality of memristors coupled between a unique combination of one row line and one column line.
6. The temperature compensation circuit of claim 5, wherein each of the memristors exhibits linear current-voltage behavior.

7. The temperature compensation circuit of claim 5, wherein the signal converter is an analog-to-digital converter.
8. The temperature compensation circuit of claim 1, wherein the temperature sensor comprises any of a diode sensor, a temperature coefficient sensor, a band gap circuit sensor, and a memristor-based sensor.
9. A memory circuit, comprising:
 - a memory crossbar array comprising a plurality of row lines, a plurality of column lines, and a plurality of memory elements, wherein each memory element is coupled between a unique combination of one row line and one column line; and
 - a temperature compensation circuit, comprising:
 - a temperature sensor to sense a temperature signal of the memory crossbar array;
 - a signal converter to convert the temperature to an electrical control signal;
 - a voltage compensation circuit to determine a compensation voltage based on the electrical control signal and on a temperature-dependent resistance of the memory elements, wherein the compensation voltage is to compensate for a difference in resistance of the memory cells as a result of the temperature of the memory crossbar array; and
 - a voltage source to apply the compensation voltage to the memory crossbar array.
10. The memory circuit of claim 9, wherein each of the memory elements exhibits linear current-voltage behavior.
11. The memory circuit of claim 9, further comprising a storage for storing the temperature-dependent resistance data of the memory elements.
12. The memory circuit of claim 9, wherein each of the memory elements comprises a

memristor.

13. A method, comprising:

sensing a temperature of a memory crossbar array, wherein the memory crossbar array comprises a plurality of memory elements;

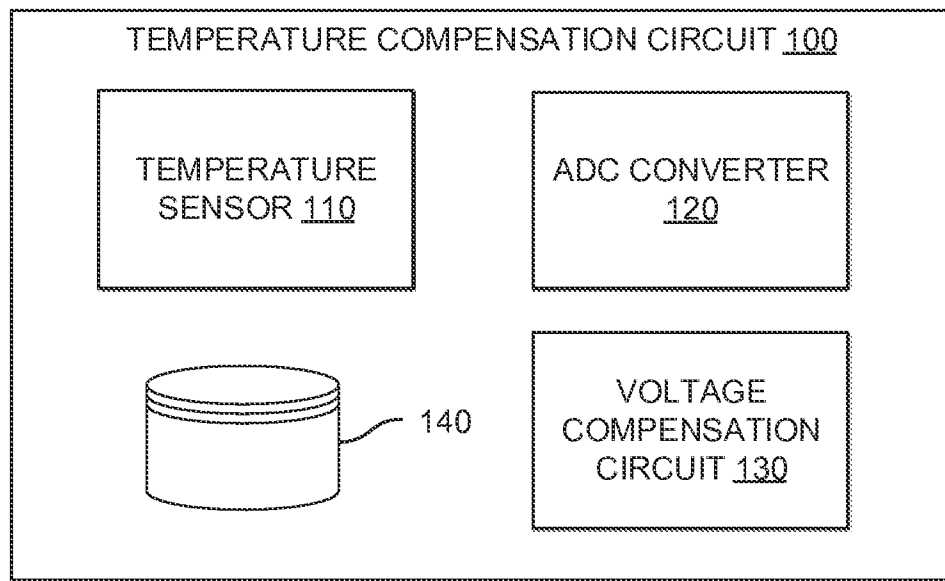
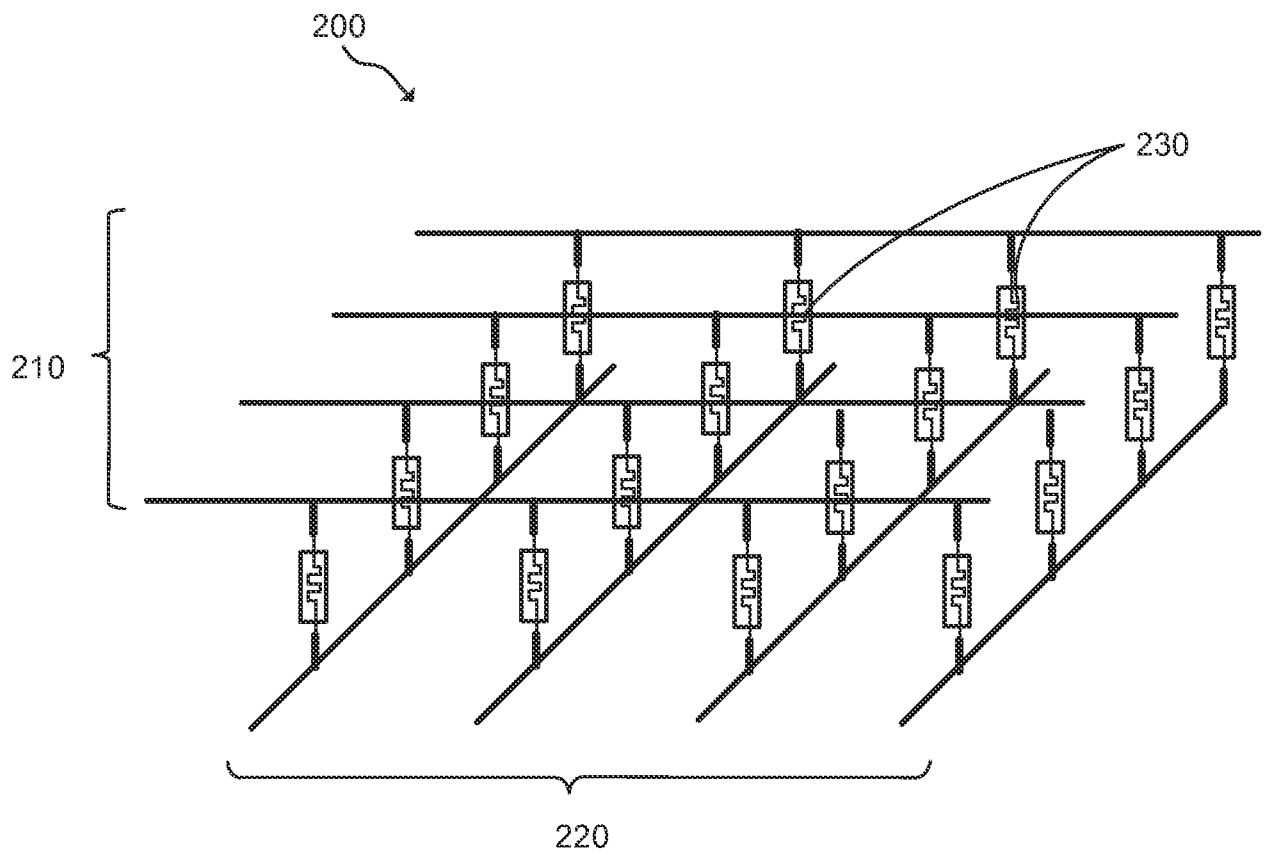
receiving a temperature-dependent resistance of the memory elements;

determining a compensation voltage based on the temperature of the memory crossbar array and on the temperature-dependent resistance of the memory elements; and

applying a compensated voltage, wherein the compensated voltage comprises the compensation voltage and an input voltage.

14. The method of claim 13, wherein applying the compensation voltage is to compensate for a difference in resistance of the memory elements as a result of the temperature of the memory crossbar array.

15. The method of claim 13, wherein the memory crossbar array comprises a plurality of row lines and a plurality of column lines, and wherein each memory element comprises a memristor coupled between a unique combination of one row line and one column line.

**FIG. 1****FIG. 2**

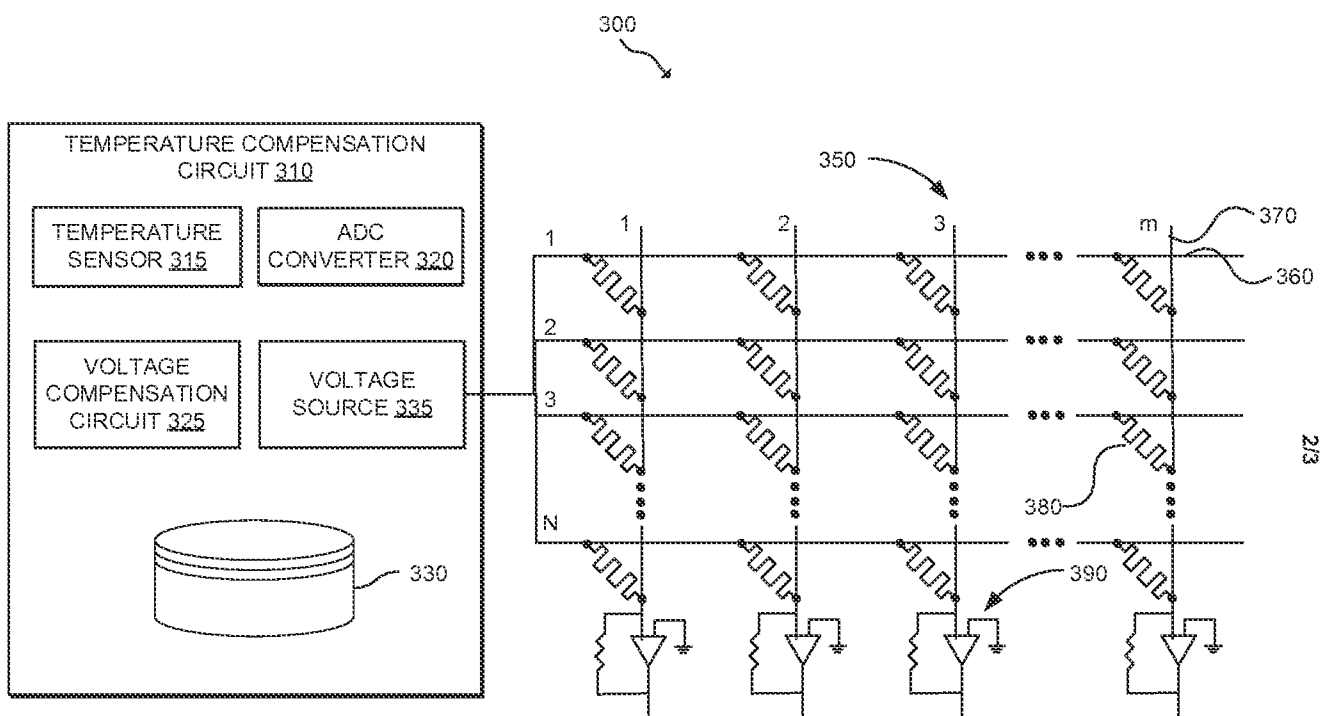
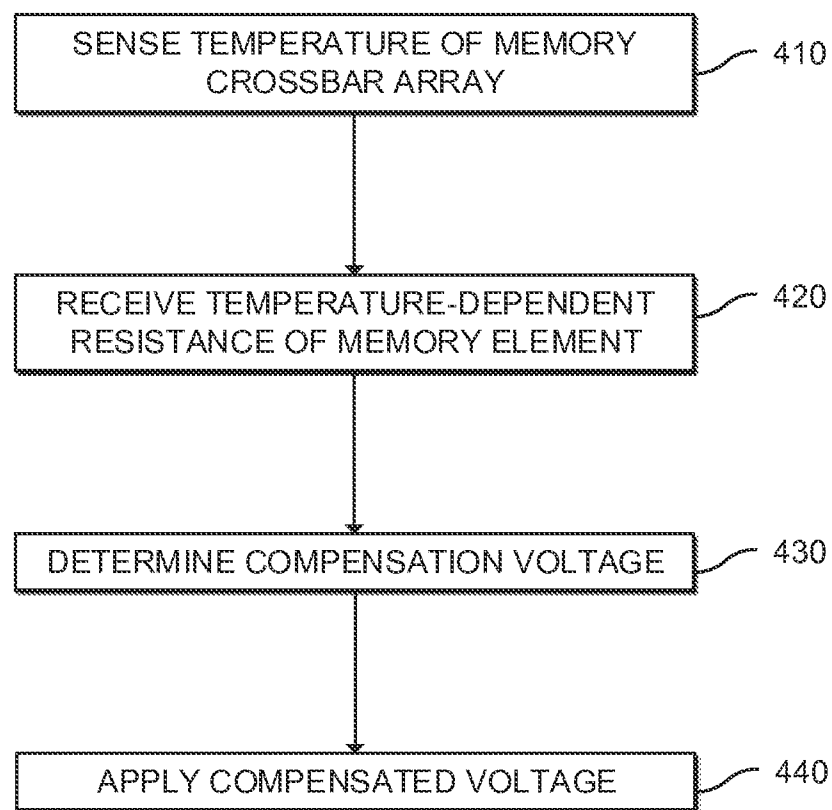


FIG. 3

3/3

400
↓**FIG. 4**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/025450**A. CLASSIFICATION OF SUBJECT MATTER****G11C 11/15(2006.01)i, G11C 7/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/15; H03M 1/34; G06F 12/02; H01L 31/0336; G11C 11/02; H03M 1/12; G11C 7/12; G11C 11/00; G11C 7/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: temperature, compensation, circuit, sensor, converter, pre-calibrated, data, crossbar, array, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0003438 A1 (CORY MERKEL et al.) 03 January 2013 See paragraphs [0013]-[0014], [0025], [0046]-[0048], [0054]; and figures 2, 7.	1-15
A	US 2014-0167999 A1 (CHARLES CULLEN MOORE) 19 June 2014 See paragraphs [0010], [0036]; and figure 3.	1-15
A	US 2005-0127403 A1 (SHENG TENG HSU) 16 June 2005 See paragraphs [0125]-[0128]; and figure 10.	1-15
A	US 2014-0133211 A1 (HAGOP NAZARIAN et al.) 15 May 2014 See paragraphs [0035]-[0041]; and figure 1.	1-15
A	US 2014-0136755 A1 (RODERICK A. HYDE et al.) 15 May 2014 See paragraphs [0133]-[0156]; and figure 14.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0003438 A1	03/01/2013	US 8750065 B2	10/06/2014
US 2014-0167999 A1	19/06/2014	US 8749422 B1	10/06/2014
US 2005-0127403 A1	16/06/2005	DE 602004013391 D1	12/06/2008
		DE 602004013391 T2	10/06/2009
		EP 1460637 A1	22/09/2004
		EP 1460637 B1	30/04/2008
		JP 04187673 B2	26/11/2008
		JP 2004-273110 A	30/09/2004
		KR 10-0601806 B1	19/07/2006
		KR 10-2004-0080357 A	18/09/2004
		TW 200425161 A	16/11/2004
		TW I248088 B	21/01/2006
		US 2004-0179414 A1	16/09/2004
		US 6868025 B2	15/03/2005
		US 6967884 B2	22/11/2005
US 2014-0133211 A1	15/05/2014	CN 103871462 A	18/06/2014
		TW 201432690 A	16/08/2014
		US 8982647 B2	17/03/2015
US 2014-0136755 A1	15/05/2014	None	