## (19) World Intellectual Property Organization

International Bureau





(43) International Publication Date 9 November 2006 (09.11.2006)

(10) International Publication Number **WO 2006/118789** 

- (51) International Patent Classification: H01L 21/318 (2006.01) H01L 21/768 (2006.01) H01L 21/314 (2006.01)
- (21) International Application Number:

PCT/US2006/014676

- (22) International Filing Date: 19 April 2006 (19.04.2006)
- (25) Filing Language: English
- (26) Publication Language: **English**
- (30) Priority Data:

11/119,660

2 May 2005 (02.05.2005) US

- (71) Applicant (for all designated States except US): AD-VANCED MICRO DEVICES, INC. [US/US]; One Amd Place, Mail Stop 68, P.o. Box 3453, Sunnyvale, California 94088-3453 (US).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): CHAN, Darin [US/US]; 1514 31st Avenue, San Francisco, California 94122 (US).
- (74) Agent: DRAKE, Paul; ADVANCED MICRO DEVICES. INC., 5204 East Ben White Boulevard, Mail Stop 562, Austin, Texas 78741 (US).

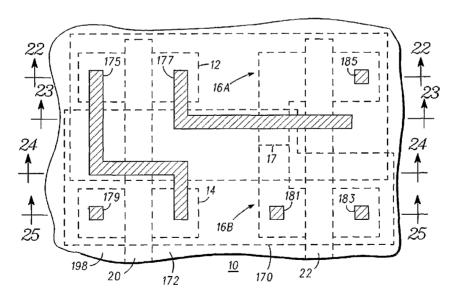
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

#### Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE



(57) Abstract: An integrated circuit (10, 250) having a plurality of active areas (12, 14, 16) separated from each other by a field region (18) and a method for manufacturing the integrated circuit (10, 250). A first polysilicon finger (20) is formed over the first active area (12) and the field region (18) and a second polysilicon finger (22) is formed over the second active area (16) and the field region (18). A first dielectric layer (168) is formed over the first active area (12) and the field region (18) and a second dielectric layer (170) is formed over the second active area (16) and the portion of the first dielectric layer (168) over the field region (18). A first electrical interconnect (175) is formed over and dielectrically isolated from the first polysilicon finger (20) and a second electrical interconnect (177) is formed over and dielectrically isolated from the second active area (16). The second electrical interconnect (177) is electrically coupled to the second polysilicon finger (22).



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# (88) Date of publication of the international search report:

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

#### INTERNATIONAL SEARCH REPORT

International application No PCT/US2006/014676

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L21/318 H01L21/314 H01L21/768 According to International Patent Classification (IPC) or to both national classification and IPC B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal C. DOCUMENTS CONSIDERED TO BE RELEVANT Category\* Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. X US 6 287 951 B1 (LUCAS KEVIN D [US] ET AL) 1 - 511 September 2001 (2001-09-11) column 2, line 65 - column 5, line 33; figures 1-7 X US 2002/081794 A1 (ITO SHINYA [JP]) 1 27 June 2002 (2002-06-27) figures 1A-20 EP 0 252 179 A1 (IBM [US]) Α 2-5 13 January 1988 (1988-01-13) abstract X US 2004/029323 A1 (SHIMIZU AKIHIRO [JP] ET 6 AL) 12 February 2004 (2004-02-12) paragraphs [0095] - [0100]; figure 4 · -/--ΙX Further documents are listed in the continuation of Box C. See patent family annex. Special categories of cited documents 'T' later document published after the international filing date or priority date and not in conflict with the application but dited to understand the principle or theory underlying the "A" document defining the general state of the art which is not considered to be of particular relevance \*E\* earlier document but published on or after the international "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such docu-ments, such combination being obvious to a person skilled in the art. "O" document referring to an oral disclosure, use, exhibition or document published prior to the international filing date but later than the priority date claimed "&" document member of the same patent family Date of the actual completion of the international search Date of mailing of the international search report 25/09/2007 29 August 2007 Name and mailing address of the ISA/ Authorized officer European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 Kenevey, Kester

## INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/014676

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A	US 2004/029378 A1 (KANG DAE-KEUN [KR] ET AL) 12 February 2004 (2004-02-12) paragraph [0027]	6,7							
A	EP 0 893 820 A (TEXAS INSTRUMENTS INC [US]; CONSORZIO EAGLE [IT]) 27 January 1999 (1999-01-27) the whole document	6,7							
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International application No. PCT/US2006/014676

### INTERNATIONAL SEARCH REPORT

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)
This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:
Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:
Claims Nos.:     because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).
Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)
This International Searching Authority found multiple inventions in this international application, as follows:
see additional sheet
As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:  1-7
4. No required additional search fees were timely paid by the applicant. Consequently, this international Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
Remark on Protest  The additional search fees were accompanied by the applicant's protest.  No protest accompanied the payment of additional search fees.

### FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

#### 1. claims: 1-5

A method for manufacturing an integrated circuit, comprising the steps of: providing a semiconductor substrate having at least one active area and at least one field region, the at least one active area having at least one semiconductor device; forming a first dielectric structure over the at least one active area and the at least one field region; forming a second dielectric structure over a portion of the first dielectric structure; removing a portion of the second dielectric structure that is over the at least one active area; and forming at least one interconnect that extends from the at least one semiconductor device over the at least one active area and over the at least one field region.

#### 2. claims: 6-7

A method for manufacturing an integrated circuit, comprising the steps of:

providing a semiconductor substrate having first and second active areas that are electrically isolated from each other by a field region:

forming a first semiconductor device from the first active area and a second semiconductor device from the second active area:

forming a first layer of dielectric material over the first active area and over the field region; and forming a second layer of dielectric material over the second active area and over the portion of the first layer of dielectric material and over the field region, wherein the first layer of dielectric material is substantially absent from areas over the second active area and the second layer of dielectric material is substantially absent from areas over the first active area.

3. claims: 8-10

## FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

An integrated circuit, comprising:

- a semiconductor substrate having an active area and a field region;
- a semiconductor device formed from the active area;
- a strip of polysilicon disposed over a portion of the active area and the field region;
- a first layer of dielectric material disposed over the active area and the field region;
- a second layer of dielectric material disposed over the portion of the first layer of dielectric material that is disposed over the field region: and
- disposed over the field region; and an electrical interconnect structure disposed over the strip of polysilicon, wherein the electrical interconnect structure is dielectrically separated from the strip of polysilicon.

## INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2006/014676

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