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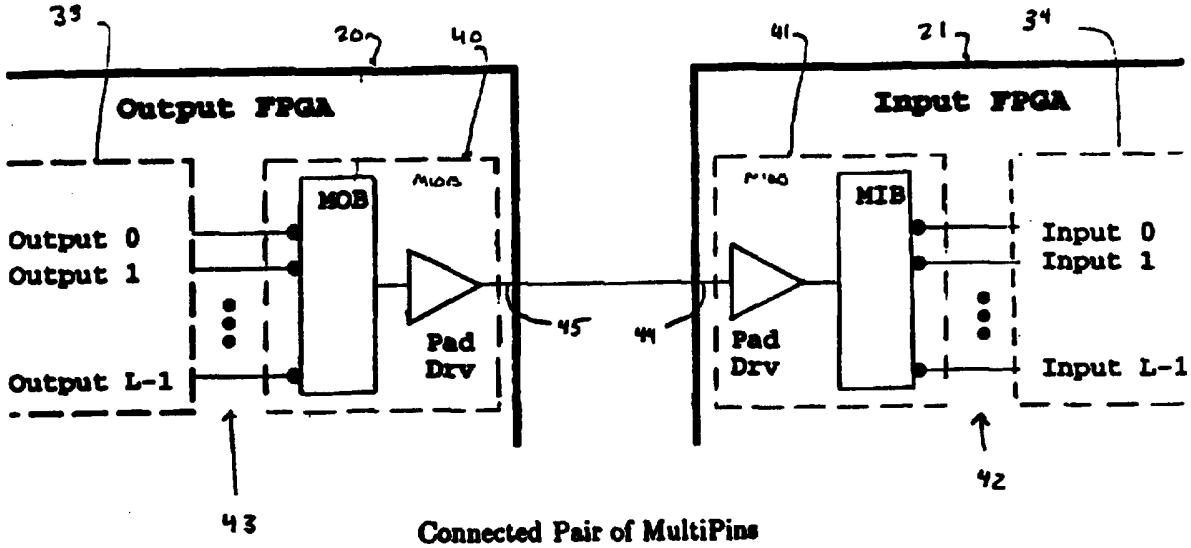

Connected Pair of MultiPins

(57) Abstract

An input/output port design for integrated circuits which improves communications bandwidth. Through multiplexing techniques the design creates virtual input/output pins (40, 41) while utilizing a single physical pin (44, 45). The virtual pins improve the communications bandwidth while minimizing the physical design of the integrated circuit. The invention can be utilized in a variety of integrated circuits, including programmable logic devices and field programmable gate arrays (14).

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Programmable Multiplexing Input/Output Port

Background of the Invention

The present invention relates to multiplexing input/output ports for use on field programmable gate arrays and other devices with programmable hardware. The invention uses time-domain multiplexing, a technique involving the sequential transmission of a collection of values over a single wire or channel.

Field Programmable gate arrays (FPGA) such as those manufactured by Altera (San Jose, CA), ATT (Allentown, PA) or Xilinx (San Jose, CA) are integrated circuits which contain arrays of user configurable logic gates. FPGAs consist of a central core of configurable logic surrounded by programmable input/output ports, see for, for example Trimberger, *Field-Programmable Gate Array Technology*, Kluwer Academic Press, 1994. The logic array and input/output ports are externally customizable, such that an FPGA can function, within the physical limits of the logic array and input/output ports, as an arbitrary logic circuit.

Large digital logic circuits can be implemented using an interconnected collection of FPGAs. The circuit is partitioned such that each FPGA is configured (programmed) to implement a specific portion of the logic circuit. Through the FPGA interconnections, each FPGA is able to communicate with other FPGAs so as to convey logic values (signals) to the rest of the circuit partitions. Thus, working in concert, the interconnected FPGAs are able to implement the entire circuit. Logic emulation is an example application in which large circuits are implemented with a collection of FPGAs.

In order for an implemented circuit to properly function, the partitioning of the

circuit must take into account not only the size of the logic array of each FPGA, but also the number of input/output ports. The size of the logic array limits the computational resources available in a particular FPGA. The finite number of input/output ports limits the communication resources available in a particular FPGA. These finite resources typically limit the efficient utilization of the FPGA.

In a partitioned circuit, each partition contains a certain number of signals requiring communication to other partitions. Prior systems of interconnected FPGAs would assign each of these signals to an individual input/output port. This partitioning scheme results in a partition that is typically input/output port limited. Therefore, utilizing this scheme, the determining factor in the number of FPGAs required to implement a particular circuit is the number of input/output ports available for communication. This results in inefficient utilization of the individual FPGA core logic array.

In addition, the functions performed by a programmed core logic array typically run slower than the potential rate of the input/output ports. Communications bandwidth is wasted as the input/output ports wait for logical values to be computed by the central core. This mismatch between the speed of the core logic array and the input/output ports also represents an inefficient utilization of the FPGA.

Therefore, it is a goal of the present invention to improve communications bandwidth between logic circuits. It is a further goal of the invention to provide a more flexible input/output port for logic circuits. In addition, it is also a goal of the present invention to provide these functions without utilizing a portion of the underlying logic array of the logic circuit.

Summary of the Invention

The present invention discloses an input/output buffer design for FPGAs and other programmable devices. An output buffer of the present invention multiplexes a selection of internal signals onto a single wire. An input buffer of the present invention demultiplexes such signals for utilization within the programmable device.

A multiplexing output buffer comprises a means for selecting a portion of the internal device signals for multiplexing, a multiplexor and a buffer for driving the multiplexed signals onto the device pin. The control logic for the multiplexor may be either internal or external to the programmable device. If the control is internal, it may be created either by the programmable logic array or by dedicated hardware.

A multiplexing input buffer comprises an input buffer for receiving the multiplexed signal from the pin, a demultiplexor and means for driving the demultiplexed signals into the programmable device. The control logic for the demultiplexor may be either internal or external to the programmable device. If the control is internal, it may be created either by the programmable logic array or by dedicated hardware.

A buffer hardware may comprise either an multiplexing input buffer, a multiplexing output buffer or both. In addition, the buffer hardware may also comprise the conventional programmable pin circuit of the underlying programmable device. The device is then programmed to select the proper buffer form.

Brief Description of the Drawings

The invention will be better understood from the following detailed description when read with reference to the following drawings in which:

Figure 1 is a block diagram illustrating a prior art collection of interconnected FPGAs.

Figure 2 is a block diagram of a prior art direct hardwire interconnect for a connected pair of FPGAs.

Figure 3 is a block diagram of a prior art interconnect design utilizing the logic arrays of FPGAs.

Figure 4 is block diagram of a connected MultiPin input buffer and MultiPin output buffer pair of the invention.

Figure 5 is a block diagram of the behavioral model of a connected pair of MultiPins of the invention.

Figure 6 is a schematic diagram of two MultiPin output buffer embodiments.

Figure 7 is a schematic diagram of a MultiPin input buffer.

Figure 8 is a timing diagram showing the relationship between the clock and control signals.

Figure 9 is a schematic diagram of a skew tolerant MultiPin input buffer.

Figure 10 is a schematic diagram of a latch based MultiPin input buffer.

Figure 11 is a timing diagram showing the relationship between the clock and select control signals.

Detailed Description of the Preferred Embodiment

A system comprising a collection of FPGAs implementing a logic circuit design is illustrated in Fig. 1. The FPGA system 12 is an array of interconnected FPGAs 14 with possibly the addition of other elements (i.e. memory) 16. The FPGA system 12 utilizes communications paths 10 for internal FPGA to FPGA

communication.

Prior non-multiplexing versions of FPGA circuit implementations, as illustrated by Fig. 2, partition a circuit such that a portion of the circuit is implemented by individual FPGAs 20 and 21. Each partition contains a certain number of signals 22a, 22b, and 22c requiring communication to other partitions. Each of these communicated signals 22a, 22b, and 22c is thus assigned an individual input/output port 24a, 24b, and 24c. As input/output ports are finite in number, this partitioning scheme typically results in partitions that are input/output port limited, rather than logic array limited. Therefore, the limiting factor in the size of a circuit partition implemented in a particular FPGA is the number of input/output ports available for communication. As a result, the FPGA resources (i.e. logic array) are not fully and efficiently utilized.

One solution to this problem, as illustrate in Fig. 3, is to share an input/output wire 30 amongst a variety of signals. This can be accomplished by multiplexing/demultiplexing the input/output ports 31 and 32 as illustrated in Fig. 3. Implementation of this multiplexing/demultiplexing scheme within existing FPGAs 20 and 21 would require the allocation of a portion of the logic arrays 33 and 34 in the creation of the multiplexors 35 and 36.

The allocation of logic gates within the logic array for the creation of the multiplexors/demultiplexors leaves less of the array available as a computation resource. In addition, this solution uses the same clock as that of the underlying logic array, which limits the communications bandwidth. Therefore, while this solution utilizes fewer input/output ports, it comes with an associated cost.

The present invention discloses various hardware FPGA pin-multiplexing

techniques that tradeoff between speed, space and complexity of use. The invention involves replacing the input/output buffers (ports) on some or all of the FPGA pins with special multiplexing input/output buffers which synchronously transmit multiple bits of data using a clock which is potentially faster that the clock(s) used within the logic in the logic in the reprogrammable FPGA logic array core.

Virtual Pins Abstraction

The virtual pins abstraction of the present invention is a simplified behavioral model for time-domain, multiplexed FPGA pins. In this model, a MultiPin is defined as an FPGA pin which will be multiplexed. L is defined as the level of multiplexing of a MultiPin, the number of bits which are transmitted via this pin during the period of the FPGA core clock.

With reference to Fig. 4, a MultiPin is connected to a multiplexing input/output buffer (MIOB) 40 and 41 rather than a normal FPGA input/output buffer. An MIOB has an interface to the reprogrammable FPGA array 33 and 34 consisting of a collection of L input ports 42 or L output ports 43, where an input or output port is behaviorally similar to an input or output port of a normal input/output buffer. A connection is achieved by connecting an output MultiPin 45 on one FPGA 20 to an input MultiPin 44 of another FPGA 21.

The abstract behavioral model of this interconnection, indicated in Figure 5, is a pair-wise connection of specific output 43 and input 42 ports with flip-flops 50 between the two sets of ports. Note again that this structure with a multiplicity of port pairs is the result of connecting a single pair of MultiPins 40 and 41.

All flip-flops in this construct have the same clock signal. This is the clock used in synchronous logic in the reprogrammable core which connects to the MIOB

ports. Timing constraints necessary for correct virtual pins multiplexing behavior can be represented as setup and hold time constraints on the embedded flip-flops in the abstract behavioral model.

The virtue of this model is that it readily maps into an understandable partitioning constraint, either for human or automated partitioning of a design. Partition boundaries should be at the inputs and outputs of flip-flops, which are then subsumed in the virtual pin multiplexing hardware. Whenever this constraint cannot be met, the inter-FPGA signal must use a normal non-multiplexed pin. Circuit techniques such as those described in the pending United States Patent Application Serial No. 08/042,151, whose teaching are hereby incorporated by reference, can be used to relax this constraint, if desired.

Multiplexing Embodiments

An implementation of the virtual pins multiplexing system contains three hardware structures: a Multiplexing Output Buffer, (MOB); a Multiplexing Input Buffer (MIB); and means for clocking and control signal generation (CTL). A variety of implementations exist for these fundamental hardware structures.

Pin-Multiplexing Embodiment: Level 1

In a Level-1 embodiment of the invention, MIB and MOB multiplexing/demultiplexing buffer structures are implemented directly on FPGAs. The CTL control and clock generation circuitry is implemented externally to the FPGAs. Control signals are distributed to dedicated pins in each FPGA and then internally routed via dedicated low skew paths to the MIB and MOB structures.

In the Level-1 embodiment exhibits behavior which is functionally consistent with the virtual pins abstract model. Since CTL is implemented externally to the FPGAs, it can easily operate at speeds in excess of those of the programmable core FPGA logic.

Fig. 6 illustrates two circuit diagrams for two forms of MOBs. The first MOB 60 is simply an L:1 multiplexor (where L is the number of multiplexed output signal) whose $Log_2(L)$ select lines are globally distributed from a single source to all MOBs. The second MOB circuit 61 is an AND-OR multiplexor 62 with a local finite state machine 63 to produce the required multiplexing control signals. This finite state machine 63 requires a globally distributed MClk and Go signal and produces all the needed control signals for any level of multiplexing. Fig. 6 shows a circuit diagrams for each form of MOB for L = 4.

The MIB is designed to include a bank of registers whose purpose is to cause all multiplexed inputs to become available simultaneously and to remain available for the entire duration of the FPGA core clock Clk. Referring to Fig. 7, a Level-1 MIB 70 consists of a shift-register chain 71 which collects the multiplexed input signals and a bank of registers 72 into which these collected values are transported once per FPGA core clock. Together, the shift-register and flip-flop bank double-buffer the inputs to decouple reading from writing. Notice that the shift-register receives MClk, which is the high speed clock for multiplexed data transmission, whereas the second bank of flip-flops receives, Clk, the FPGA core clock clk.

The control circuitry must produce the clock and control signals used by the MOBs and MIBs: Clk, MClk, Sel<*i*> or Go. Once these signals are produced,

either externally or internally to the FPGA, they are routed to all MIOBs via dedicated low-skew paths.

It is assumed for these embodiments that the basic clock signal Clk, which is the clock of the flip-flops in the abstract model and the clock used by synchronous core logic connected to the MultiPin ports, is always received on a dedicated FPGA input pin and routed to all MIOBs on the FPGA with low skew. It is also assumed that the signals MClk and Go are externally produced. If the MOB using a multiplexor without local control is used, a finite state machine is required to produce the appropriate Sel<*i*> signals, triggered by Go. Several acceptable forms for this FSM, all counters of various sorts, should be evident to one skilled in the art.

The timing diagram in Fig. 8 indicates the minimal set of timing constraints which must be satisfied by Clk, MClk and Go. Within each period of Clk, MClk must have at least L+1 rising edges. The last L consecutive rising edges of MClk are used to drive data over the pin and are referred to as transport edges. One or more additional non-transport edges are also required. It is legitimate for the first non-transport edge in MClk to coincide with the rising edge of Clk, however if this is the case then the edges must be synchronized, (ie. a non-transport edge in MClk cannot precede Clk.) The time from the last transport edge to the rising edge of Clk must be at least the period of MClk.

Go must be asserted prior to the first transport edge and must remain high for all transport edges. It must be deasserted prior to the first non-transport edge and must remain low for all edges.

MClk can have as many non-transport edges as is desired with a minimum

of 1. The reason for allowing multiple transport edges is that outgoing data from the FPGA core must achieve a setup time to the first transport edge. In order to avoid constraining the period of MClk as a result of core FPGA speeds, we allow multiple MClk periods for core FPGA computation, followed by data transmission at 1-bit per MClk edge. (One can achieve the same effect with only one non-transport edge by using an MClk with non-constant period.)

Timing constraints on the period of MClk are that it must include the propagation delay of the output FPGA control circuit, MOB multiplexor, output pad driver, input pad receiver and the setup time of the sampling MIB flip-flop, plus any clock skew between MClk on the two FPGAs.

Note that if fewer than the L-way multiplexing supported by the hardware is needed, the MOB and MIB circuits illustrated above support any number fewer than L by using fewer transport edges and not using the last one or more MultiPin port pairs.

In contrast to methods which utilize core FPGA logic for multiplexing and control, dedicated hardware offers a speed improvement in comparison to reprogrammable logic by decoupling communication bandwidth from core clock speeds. Dedicated hardware avoids the need for a user to design or synthesize multiplexing circuitry. Finally, dedicated hardware frees up reprogrammable logic which can then be utilized for the logic partition.

Pin-Multiplexing Embodiment: Level 2

Level 2 extends Level 1 by incorporating the CTL submodule directly in dedicated hardware on the FPGA. The FPGA CTL circuitry must generate MClk

and Go signals directly from the core clock signal Clk. the Level-2 CTL submodule comprises a phase-locked loop or other type of clock multiplier circuit which produces MClk as some fixed or selectable synchronized multiple of Clk and produces Go setup to a fixed or selectable MClk edge.

If the clock-multiplier is fixed then a prespecified number of transport and non-transport edges of MClk will exist. This will give less flexibility in optimizing the timing of circuits but eliminates complexity in the clock-multiplier circuitry.

Skew-Tolerance

Hold time considerations for the sampling flip-flops in the MIB lead to skew restrictions on the distribution systems for Clk and MClk between the communicating FPGAs. The MClk received by flip-flops on two distinct FPGAs must have skew no greater than the hold time of the sampling flip-flops in the MIB.

A slight variation of the design of MIBs leads to a skew tolerant system, at a cost in communication speed. A schematic of the resulting circuit is provided as Fig. 9. One extra sampling flip-flop has been added to the shift-register and the entire shift-register has been implemented using negative edge triggered flip-flops. With this design, the input signal changes synchronously with rising MClk edges and is sampled on falling edges.

In this design, the period of Mclk in the Level-1 section must now be the interval between a rising and falling edge of MClk. Time between falling and rising edges provides controllable hold time margins in the face of MClk skew between the two FPGAs.

Latch based circuitry

On the input side, the use of edge-triggered master-slave flip-flops rather

than latches increases the per-MultiPin hardware cost by about a factor of 2. Fig. 10 illustrates the latch-based MIB. This approach adds some hardware complexity and cost to the control and control-signal distribution circuitry in exchange for a savings in each MIB. Since an FPGA has many MIBs and only a single CTL module, the cost savings accrued over multiple MIBs can outweigh the added CTL cost.

Referring to Fig. 10, the control signals are all latching strobes. Clk' is a version of Clk with the same rising edge but with a falling edge which precedes the falling edge of L0. L0 .. L3 are negative active latching strobes whose rising edges must be coincident with transition edges 1 through 3 of MClk (where the initial transition edge is numbered 0), plus a non-transition edge coincident with the rising edge of Clk. Fig. 11 illustrates the timing constraints on Clk, MClk, Clk', L0, L1, L2 and L3.

Pipelining

In the embodiments described above, the critical path dictating the period of Clk may involve logic in the programmable core followed by the extended setup-time associated with the traversal of a MultiPin.

One might choose to add a bank of registers clocked by CLK prior to the multiplexor in the MOB. (A functionally equivalent implementation involves a shift-register which can be parallel-loaded on edges in CLK and shifted on edges in MClk, avoiding the need for multiplexing.) With either modification, there is no unregistered path that involves both core FPGA logic and MultiPin transport.

This change impacts the behavioral model, replacing each abstract flip-flop be a pair of flip-flops. Stated differently, it adds an additional stage of pipeline

delay on the communication path.

Bidirectional Pins

The discussion above describes unidirectional, either MOB and MIB MultiPins. A bidirectional structure can be supported with the addition of a tri-state driver and the inclusion of both an MOB and MIB into a single MIOB.

Multiplexed vs. Non-multiplexed Pin Tradeoffs

Multiplexing pins using the present invention can be mixed freely on an FPGA with non-multiplexing pins in any ration that is desired. In addition, the hardware for a non-multiplexed input/output buffer and a MIOB can be merged into a single aggregate structure that can act as either a MultiPin or a normal pin. The mode of operation of this structure is programmatically selectable using the programming mechanism of the core logic array.

It is to be understood that the above description is only of one preferred embodiment of the invention. Numerous other arrangements may be devised by one skilled in the art without departing from the scope of the invention. The invention is thus limited only as defined in the claims.

What is claimed is:

1. A configurable multiplexing output port in an integrated circuit comprising:

at least one signal transmission medium for carrying input signals;

means for selecting a portion of said input signals, said selecting means being operationally associated with said wires so that said signals travelling on said wires arrive at said selecting means;

means for multiplexing said portion, said multiplexing means being operationally associated with said selecting means so that said multiplexing means multiplexes said portion; and

means for transmitting said multiplexed portion, said means being operationally associated with said mutliplexing means and capable of transmitting said multiplexing portion off said integrated circuit.

2. A configurable demultiplexing input port in an integrated circuit comprising:

means for receiving multiplexed input signals;

means for demultiplexing said received multiplexed input signals, said demultiplexing means being operationally associated with said receiving means so that said demultiplexing means demultiplexes said multiplexed input signals into a portion; and

means for configurably communicating said portion, said means for communicating being operationally associated with said demultiplexing means so that said portion is communicated into said integrated circuit.

3. An integrated circuit comprising:

a configurable multiplexing output port, said output port comprising:

wires for carrying input signals;

means for selecting a portion of said input signals, said selecting means being operationally associated with said wires so that said signals travelling on said wires arrive at said selecting means;

means for multiplexing said portion, said multiplexing means being operationally associated with said selecting means so that said multiplexing means multiplexes said portion; and

means for transmitting said multiplexed portion, said means being operationally associated with said mutliplexing means and capable of transmitting said multiplexed portion off said integrated circuit; and

a configurable demultiplexing input port, said input port comprising:

means for receiving multiplexed input signals;

means for demultiplexing said received multiplexed input signals, said demultiplexing means being operationally associated with said receiving means so that said demultiplexing means demultiplexes said multiplexed input signals into a portion; and

means for configurably communicating said portion, said means for communicating being operationally associated with said demultiplexing means so that said portion is communicated

into said integrated circuit.

4. The integrated circuit of claim 3 further comprising:

a pin on said integrated circuit wherein said multiplexing output port and said multiplexing input port are connected to said pin.

5. The integrated circuit of claim 4 further comprising:

means for selecting one of said output port or said input ports

6. The multiplexing output port of claim 1 further comprising:

means for controlling said multiplexing means, said controlling means being operationally associated with said multiplexing means so that said portion is controllably multiplexed.

7. The demultiplexing input port of claim 2 further comprising:

means for controlling said demultiplexing means, said controlling means being operationally associated with said demultiplexing means so that said multiplexed input signals are controllably demultiplexed.

8. The integrated circuit of claim 4 or 5 further comprising:

means for controlling said multiplexing means, said multiplexing controlling means being operationally associated with said multiplexing means so that said portion is controllably multiplexed; and

means for controlling said demultiplexing means, said demultiplexing controlling means being operationally associated with said demultiplexing means so that said multiplexed input signals are controllably demultiplexed.

9. The integrated circuit of claim 6 or 7 wherein said control means is external to said integrated circuit.

10. The integrated circuit of claim 8 wherein said multiplexing control means and said demultiplexing control means are external to said integrated circuit.

11. The multiplexing output port of claim 1 wherein said multiplexing means comprises at least one flip-flop.

12. The multiplexing output port of claim 1 wherein said multiplexing means comprises at least one latch.

13. The demultiplexing input port of claim 2 wherein said demultiplexing means comprises a combinatorial selector.

14. The demultiplexing input port of claim 2 wherein said demultiplexing means comprises a shift register.

15. The integrated circuit of claim 1, 2, or 4 wherein said integrated circuit is a reconfigurable logic device.

16. The integrated circuit of claim 8 wherein said integrated circuit is a reconfigurable logic device and said control means is internal to said integrated circuit.

17. The integrated circuit of claim 1, 2 or 4 wherein said integrated circuit is a FPGA.

18. The integrated circuit of claim 8 wherein said integrated circuit is a FPGA.

19. The integrated circuit of claim 17 wherein said control means is internal to said integrated circuit.

20. The integrated circuit of claim 18 wherein said control means comprises programmable logic.

21. The integrated circuit of claim 1, 2 or 4 wherein said integrated circuit is a gate array.

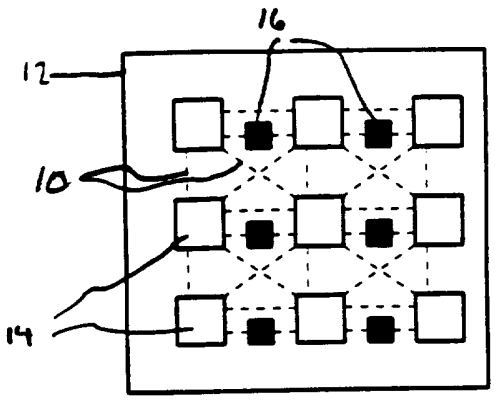


Fig. 1

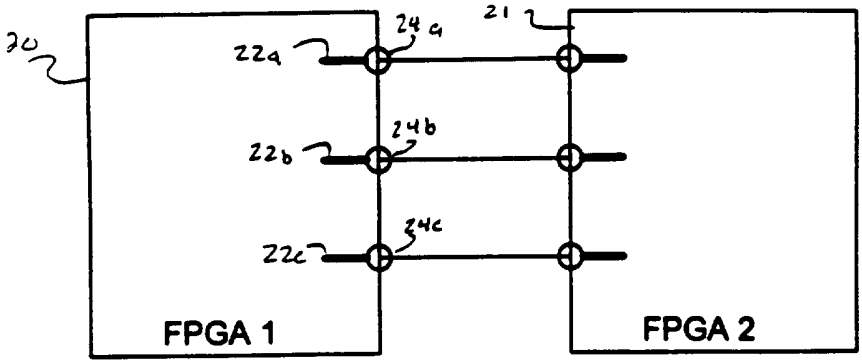


Fig. 2

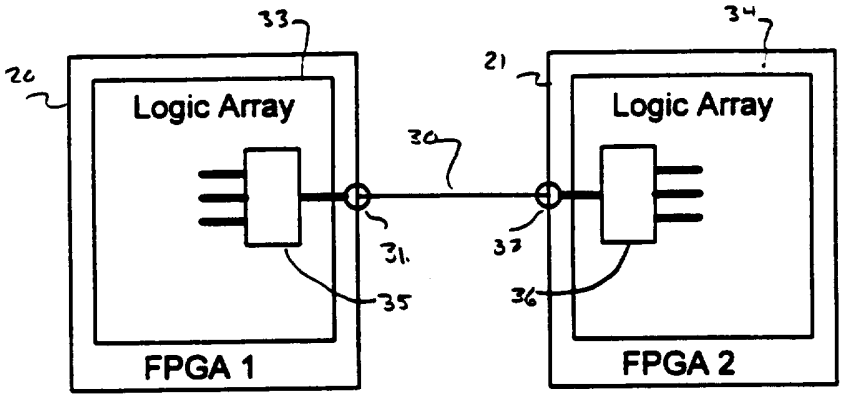


Fig. 3

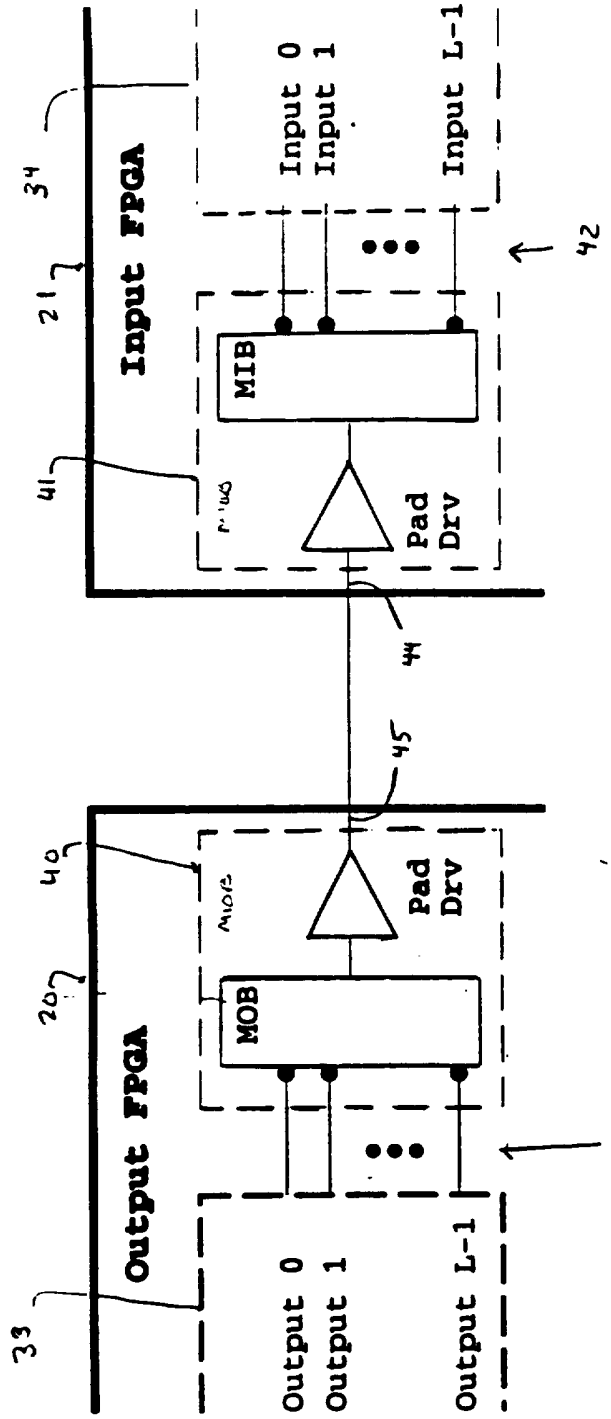


Figure 4: Connected Pair of MultiPins

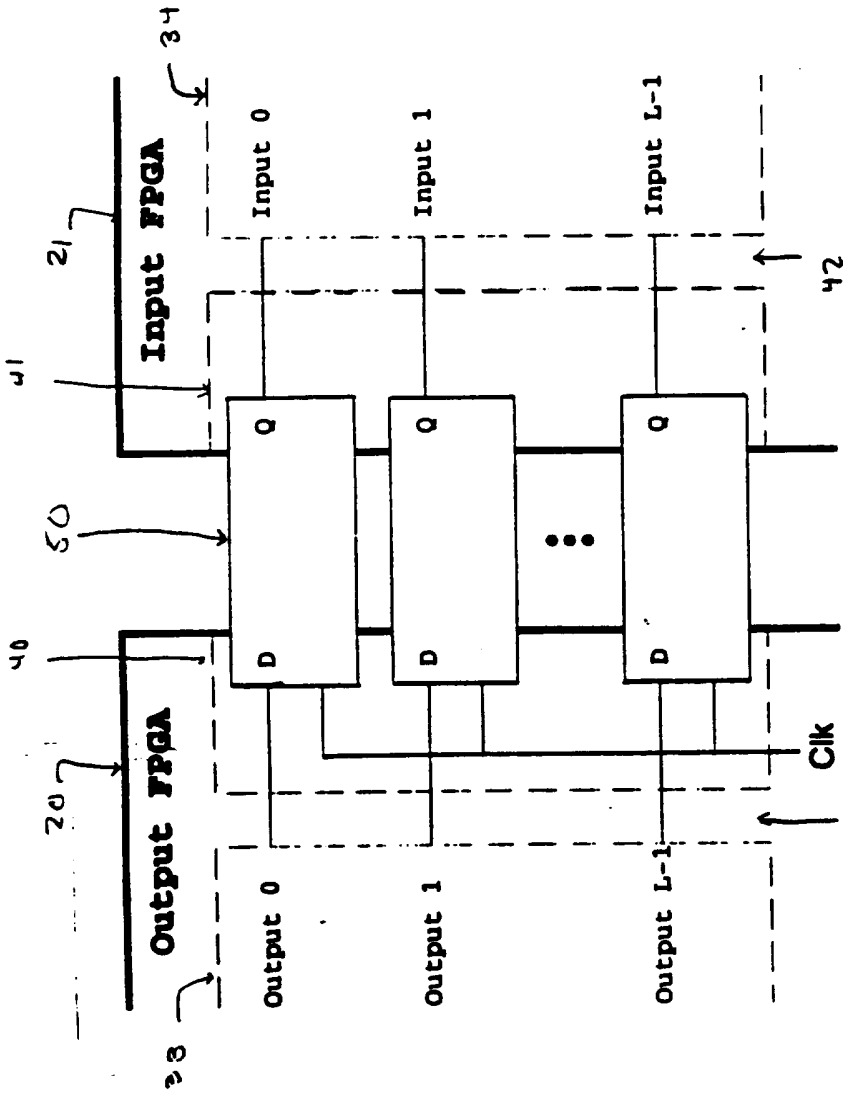


Figure 5 Behavioral Model of Connected Pair of MultiPins

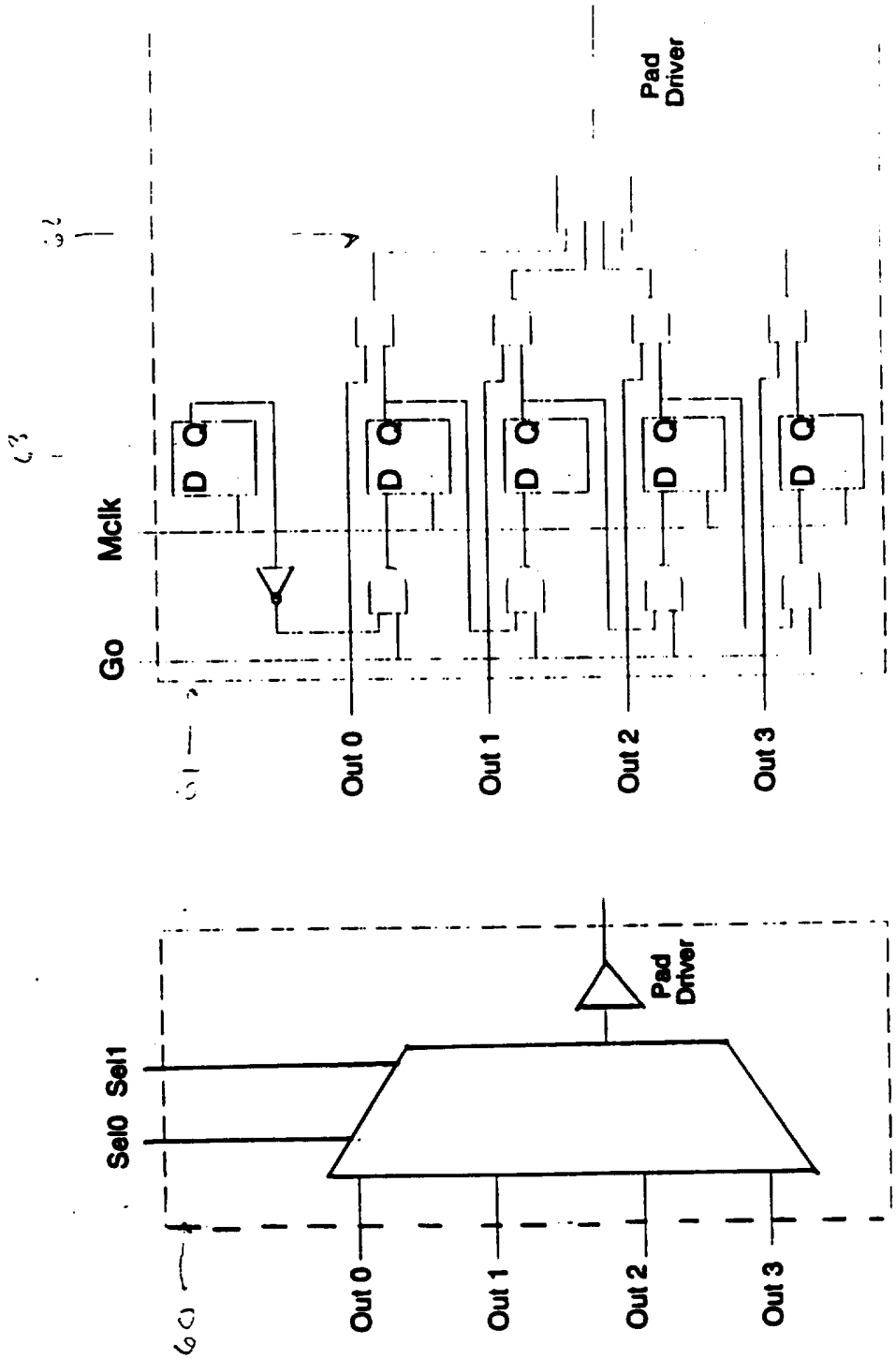


Figure 6 Level-1 MOB Implementations: Global Control and Local Control Multiplexors

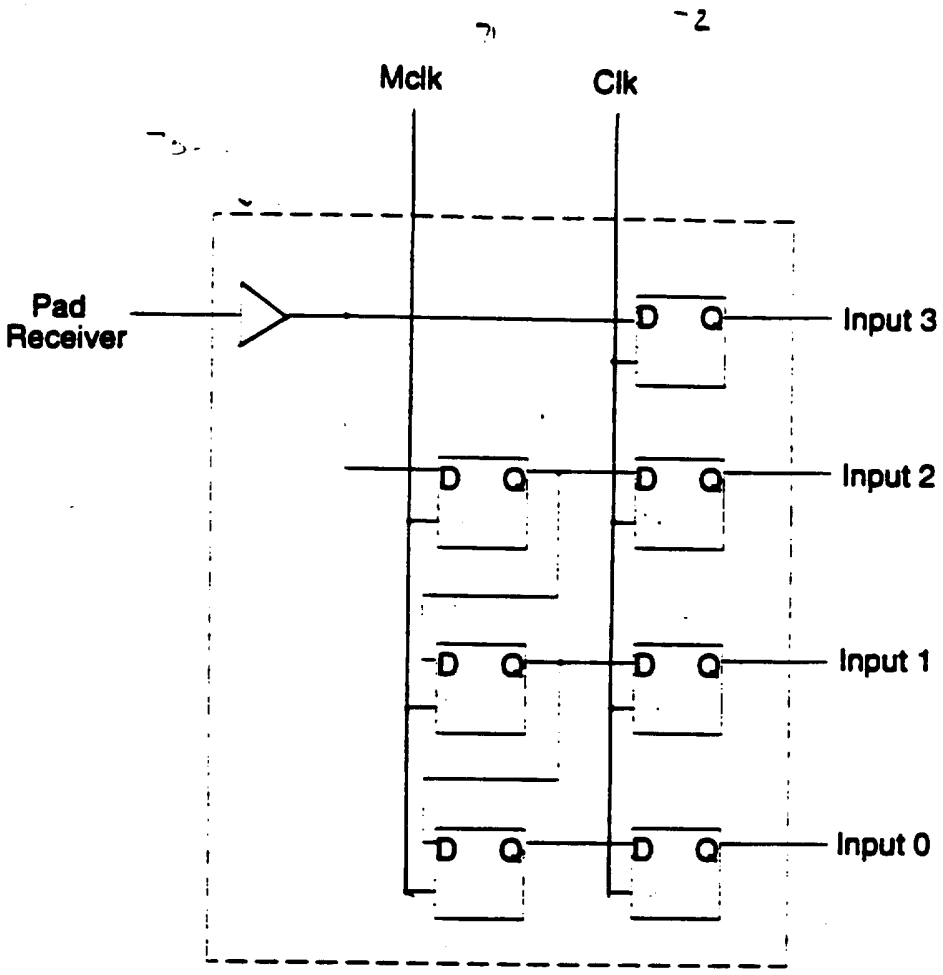


Figure 7 Level-1 MIB Implementation

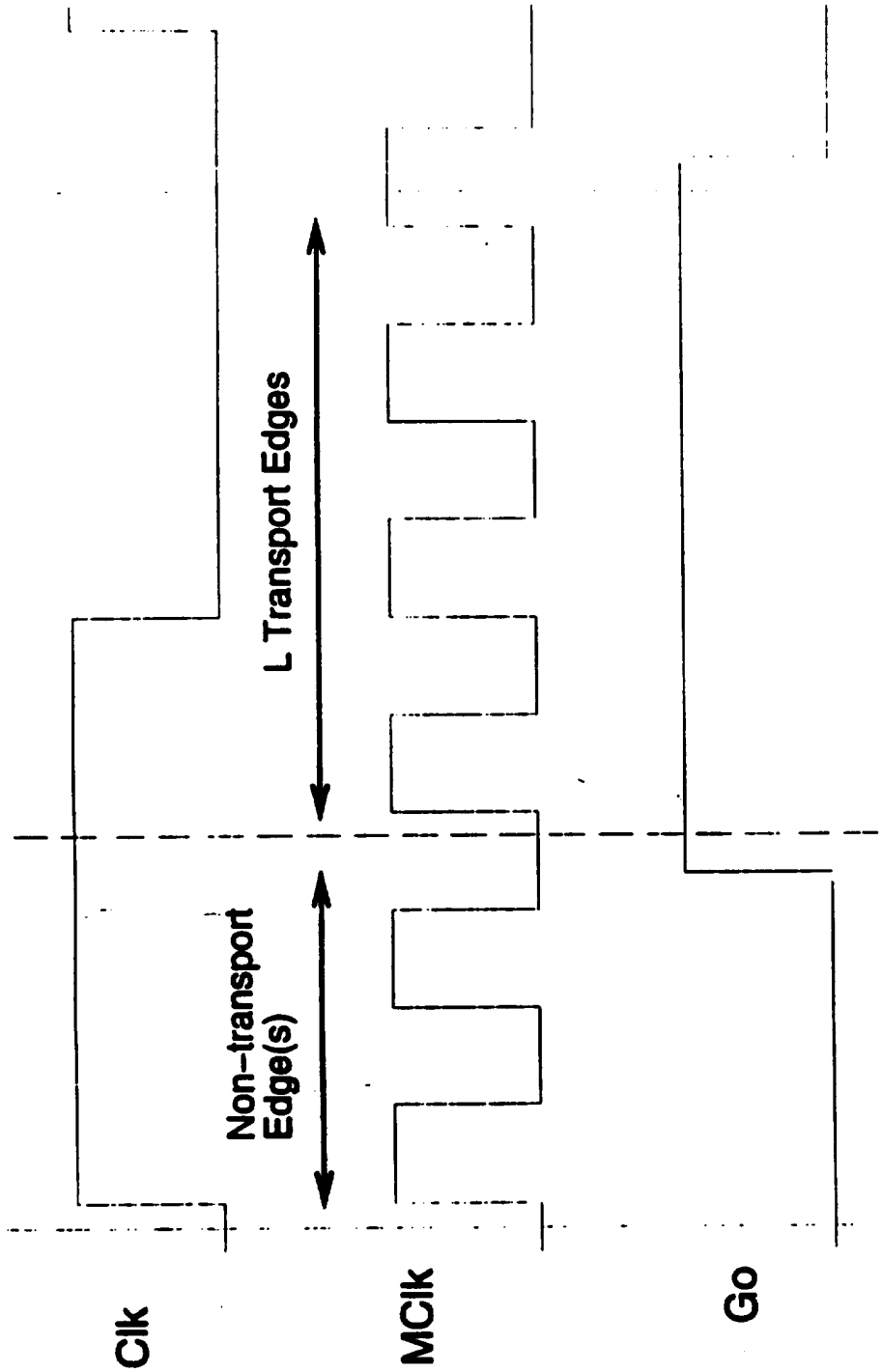


Figure 8 Timing Diagram for Level-1 Clock and Control Signals

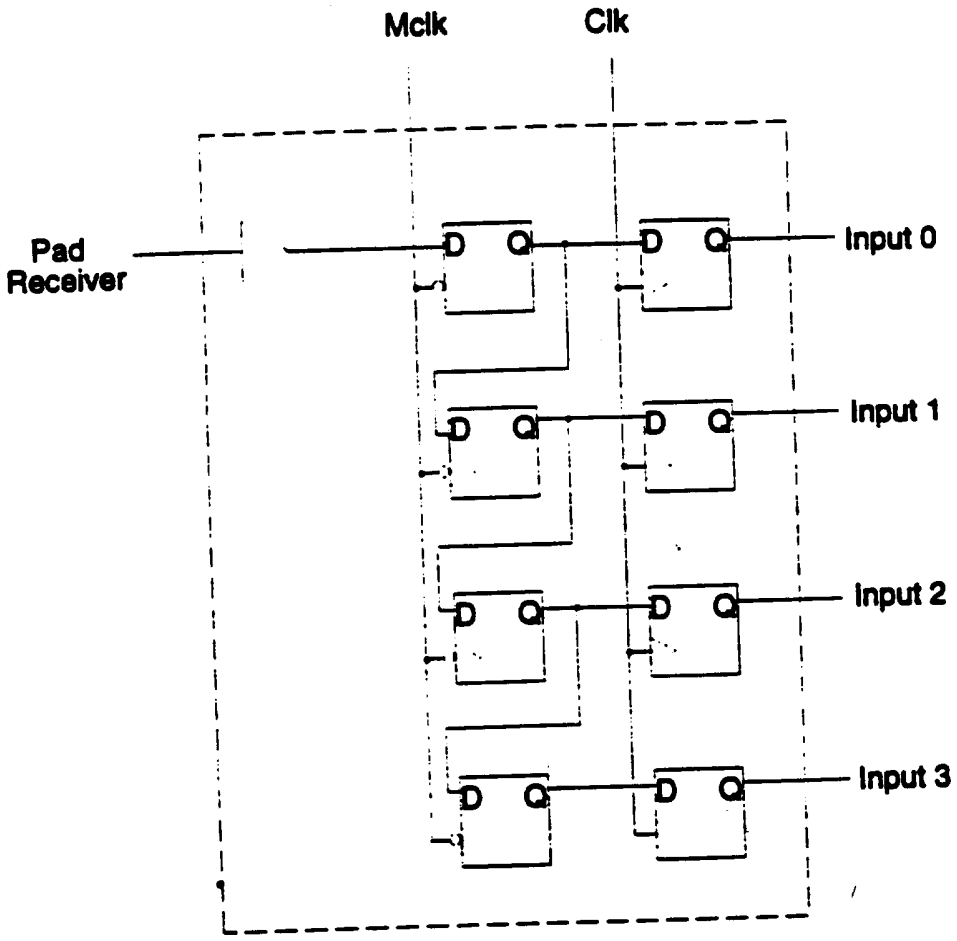


Figure 9 Clock Skew Tolerant MIB Implementation

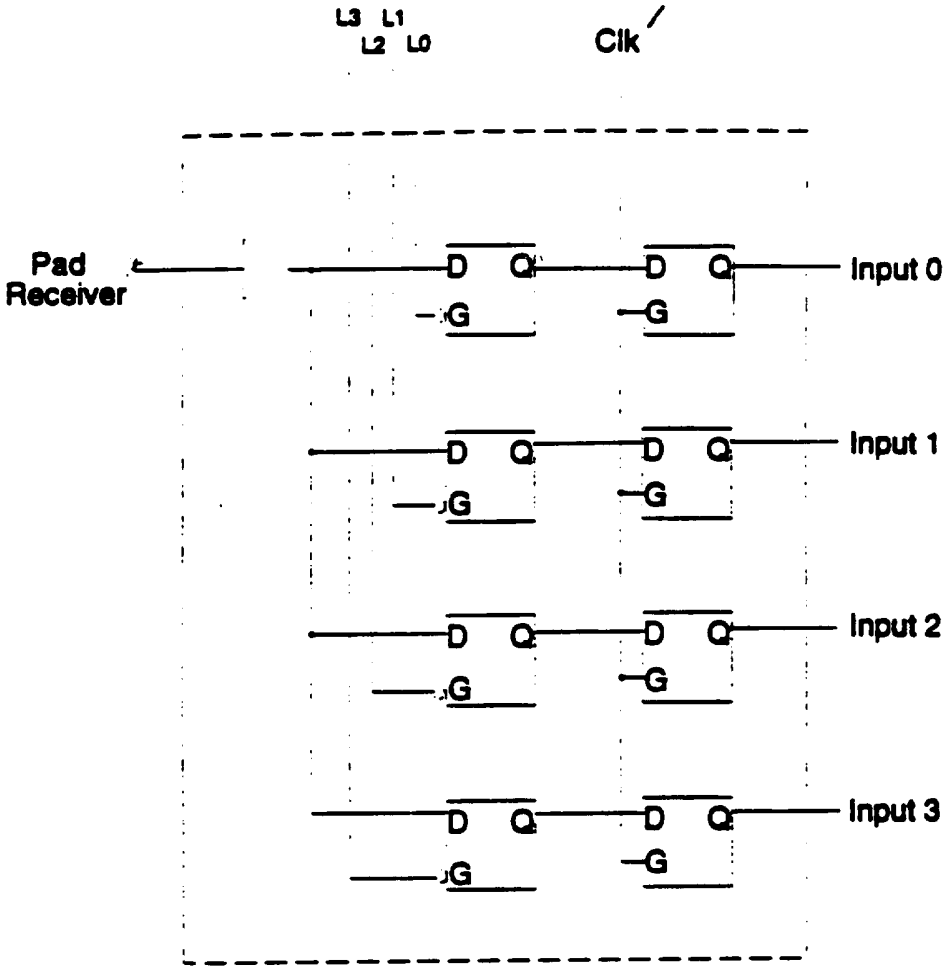
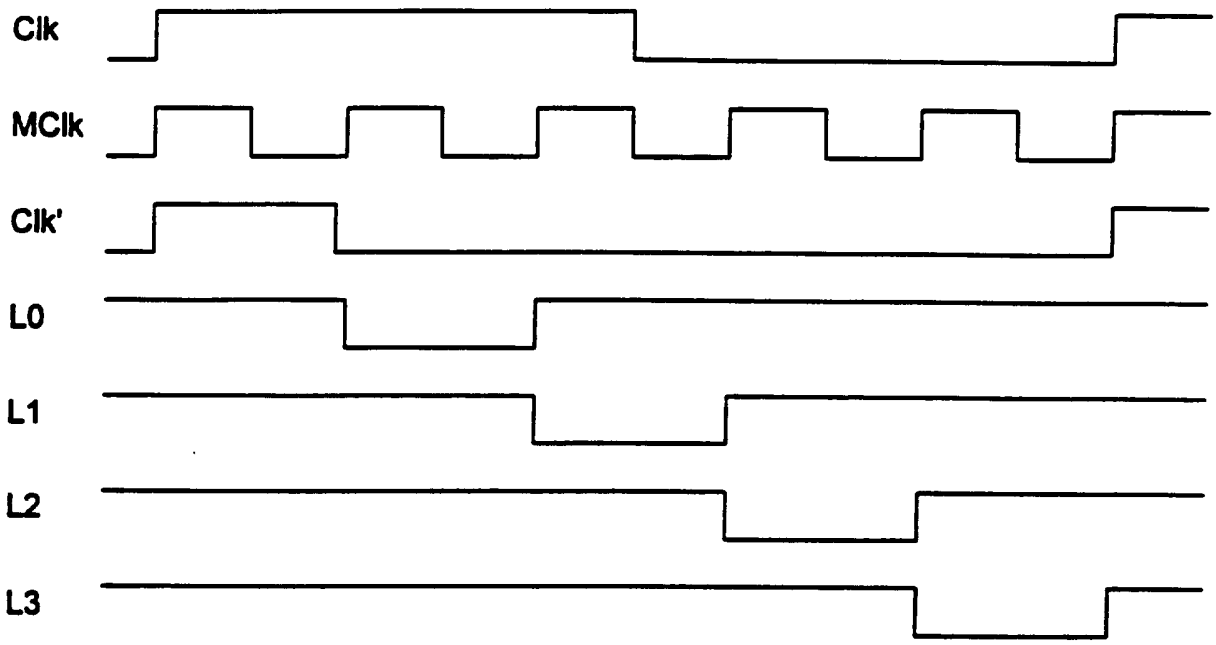


Figure 10 Latch-based MIB Implementation



Latch Control Signal Timing Diagram

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/14094

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :HO3K 19/173; H01L 25/00
US CL : 326/38, 39, 40, 41, 47
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/38, 39, 40, 41, 47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X , P	US, A, 5,402,014 (ZILIK) 28 MARCH 1995 , FIG 4	1-10 AND 15-21
A	US, A 5,136,188 (HA) 04 AUGUST 1992	
A , P	US, A 5,371,422 (PATEL) 06 DECEMBER 1994	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
29 FEBRUARY 1996	08 MAR 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 308-7726	Authorized officer ANDREW SANDERS Telephone No. (703) 308-4832

Form PCT/ISA/210 (second sheet)(July 1992)*