United States Patent

[11] 3,621,221

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[54] **CORRELATOR WITH EQUALIZATION CORRECTION**
2 Claims, 6 Drawing Figs.

[52] **U.S. Cl.** **235/181,** 333/18, 333/28
[51] **Int. Cl.** **G06f 15/34,** H04b 3/04
[50] **Field of Search** 235/181, 150.4; 333;18;28;29;33;70/; 328/37

[56] **References Cited**

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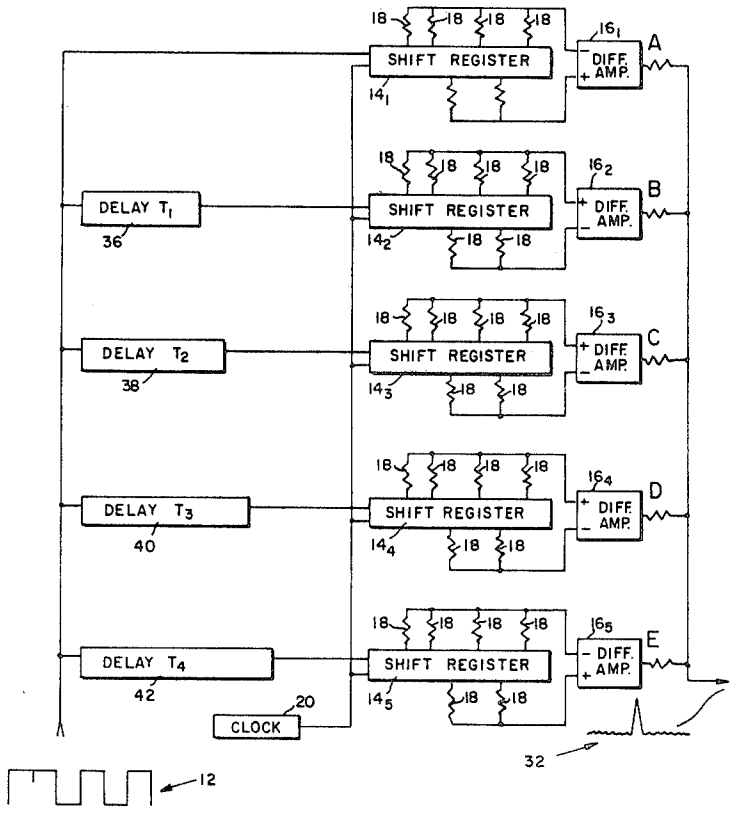
Primary Examiner—Joseph F. Ruggiero
Attorney—Louis Etlinger

ABSTRACT: Apparatus is herein disclosed for providing in a code system correlation in conjunction with equalization correction to reduce the higher sidelobes which appear for certain autocorrelation functions. The signal to be correlated is applied to a shift register or tapped delay line, whose tap outputs are summed with various polarities and weightings to accomplish, simultaneously, correlation and equalization.

The invention herein described was made in the course of or under a contract or subcontract thereunder with the Department of the Navy.



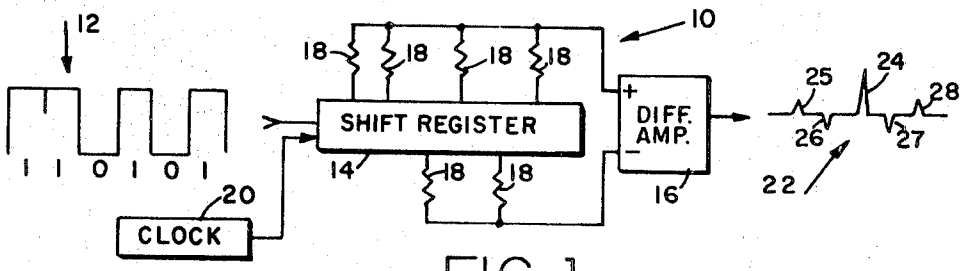


FIG. 1.

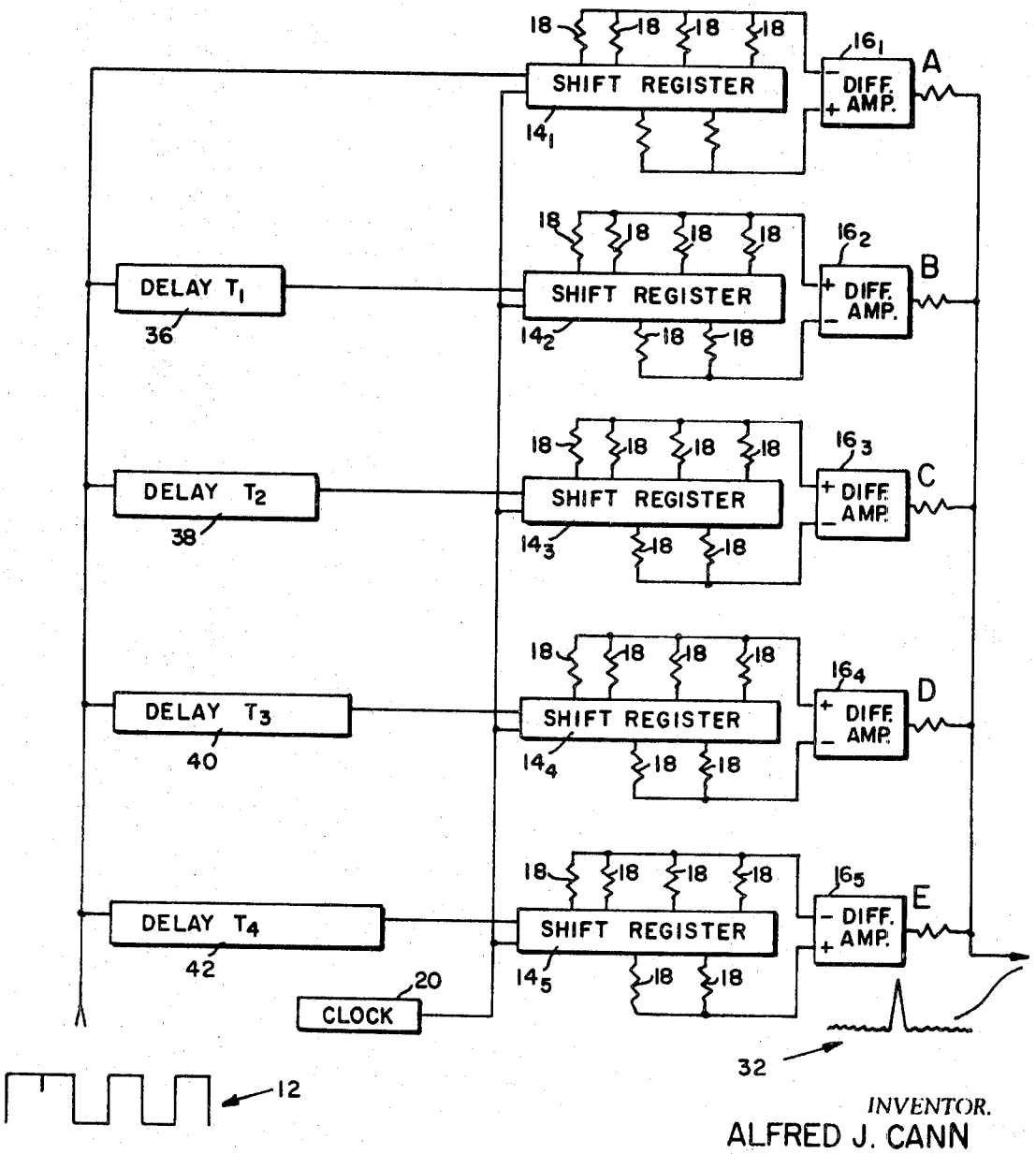


FIG. 3.

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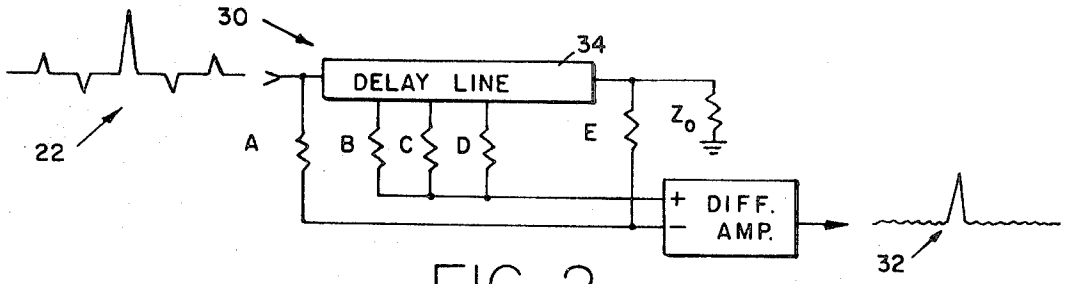

FIG. 2.

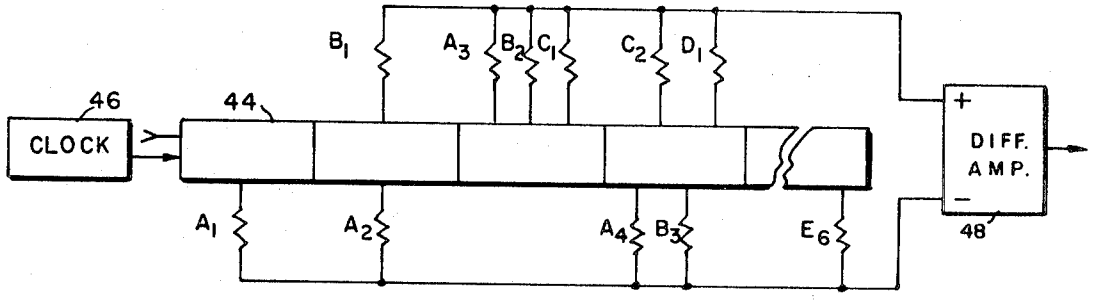

FIG. 4.

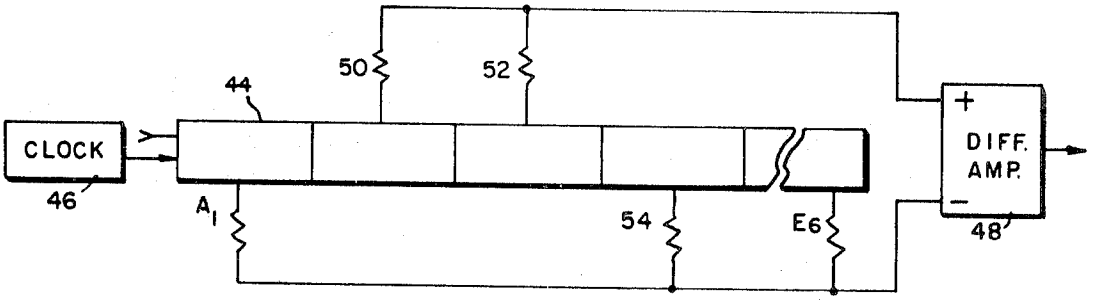

FIG. 5.

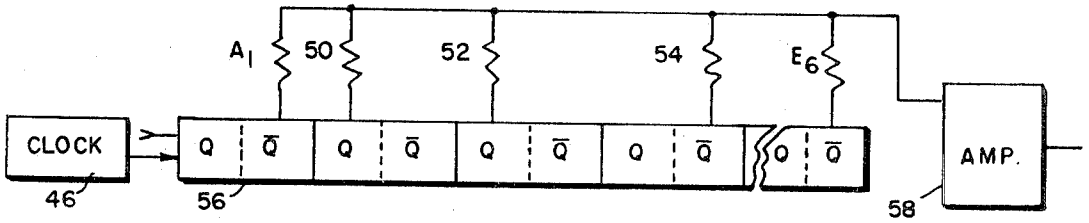

FIG. 6.

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CORRELATOR WITH EQUALIZATION CORRECTION

BACKGROUND OF THE INVENTION

When employing a binary coded system using correlation reception for communication, radar, sonar, telemetry, measurement, etc., there are many instances when constraints operate to require the system to use a code whose autocorrelation function has time sidelobes which are not as low as would be desirable. In such cases a transversal equalizer can be employed to reduce the higher sidelobes and redistribute the energy over many lower sidelobes extending over a wider range (in time). However, the conventional transversal equalizer is a tapped delay line with appropriate attenuations, tap locations and attenuation values being chosen to yield a network whose impulse response is like the function to be corrected but with inverse polarity of the major sidelobes.

The conventional transversal equalizer, thus, is costly and, moreover has limited frequency capabilities occasioned by the delay/risetime ratio of practical delay lines. Furthermore, in many instances the decoding or correlation is accomplished using a shift register which has digital delay capability heretofore ignored.

SUMMARY OF THE INVENTION

Accordingly, it is the object of this invention to provide a digital transversal equalizer in combination with a correlation network.

It is another object of this invention to provide a combined digital transversal equalizer and correlation arrangement employing a single shift register.

Briefly, in one embodiment, a combined code correlator and digital transversal equalizer is disclosed, comprising a shift register with appropriate bits thereof tapped in accordance with the code employed and sidelobes to be corrected.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other features and objects of this invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawings, in which;

FIG. 1 is a block diagram of a simplified code correlating shift register with typical input and output waveforms being illustrated;

FIG. 2 is a block diagram of a conventional transversal equalizer with typical input and output waveforms being illustrated;

FIG. 3 is a block diagram of a correlating arrangement having equalization correction augmentation;

FIG. 4 is a block diagram of a single-shift register correlator having equalization capacity;

FIG. 5 is a block diagram of the shift register of FIG. 4 with only one resistor per stage; and

FIG. 6 is a block diagram of another embodiment of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring not to the drawings; FIG. 1 illustrates a simple correlating arrangement 10 for decoding a binary signal of the form 12. It is to be understood that the code employed was selected for illustration purposes only in order to present a simplified explanation of the invention and in no way is this illustration to be limiting on the scope of the invention. Selected taps of shift register 14 are coupled to a differential amplifier 16 in accordance with the code to be correlated 12. The tap resistors 18 of shift register 14 are of equal ohmic value. A clock 20 is employed to shift signal 12 through the register 14. The output from differential amplifier 16 will take the form of signal 22 which comprises a main pulse 24 and undesirable sidelobes 25–28.

Signal 22 can be applied to a conventional transversal equalizer 30, as shown in FIG. 2, which has an impulse response like the function to be corrected but with inverse polarity of the sidelobes. The output signal 32 from the transversal equalizer of FIG. 2 has the higher sidelobes 25–28 effectively reduced with the energy thereof redistributed over many lower sidelobes over a wide range. The transversal equalizer of FIG. 2, comprises a delay line 34 appropriately tapped with resistors, A, B, C, D, and E, the resistors A, B, C, D, and E having ohmic values corresponding to the amounts of attenuation desired at each delay.

Referring now to FIG. 3 there is illustrated thereby an embodiment of a correlator according to the invention having equalization correction, this embodiment being illustrated for tutorial purposes. The input signal 12 which is to be decoded, is applied to a plurality of shift registers 14_1 through 14_5 which shift registers are shifted by a clock 20 as in the correlator of FIG. 1. The input signal is coupled to the shift register 14_1 directly and to the shift registers 14_2 through 14_5 via a plurality of delays 36 through 42. The delay times T_1–T_4 of delays 36–42 correspond to the time difference between the respective main pulse and sidelobes of the signal 22 of FIG. 2. The delays 36–42 can comprise shift registers instead of delay lines. The shift registers 14 are each tapped with resistors 18, all of like ohmic value as was the case in FIG. 1, the taps of each shift register being applied to a plurality of corresponding differential amplifiers 16_1 through 16_5. Note that the four taps 18 of shift register 14_1 corresponding to "one" bits in the code signal 12 are applied to the negative side of the differential amplifier since the first sidelobe 25 of the signal 22 to be corrected is positive and, thus, a signal of reverse polarity is necessary to compensate therefor. The taps corresponding to the "one" bits of code 12 of shift register 14_2 are applied to the positive side of the differential amplifier 16_2 since this correction will be for the second pulse 26 of the signal 22 and a signal of opposite polarity is necessary to provide correction. The four taps of shift register 14_3 are likewise applied to the positive input of differential amplifier 16_3 since they correspond to the main pulse of signal 22 and, of course, no correction is required for this desired output pulse. In like fashion, the four one-bit taps of shift registers 14_4 and 14_5 are applied to the positive and negative sides of differential amplifier 16_4, 16_5 respectively since these portions of the circuit will correct for a negative and a positive sidelobe of signal 22, respectively.

The outputs from the differential amplifiers are summed via a plurality of summing resistors A, B, C, D, and E corresponding to resistors A, B, C, D, and E of the transversal equalizer of FIG. 2. Of course, these resistors are of different ohmic value depending upon the amount of attenuation desired.

It should be noted at this time that the resistors A–F can be selected to be of the same ohmic value if the resistors 18 of the shift registers are chosen to be of different values whereby they would provide the appropriate equalization compensation. The output signal 32 is derived at the output of the summing resistors A through E and has the sidelobes appropriately corrected to provide many more sidelobes of very small amplitude.

For simplicity, pure signals are used as examples, and of course, in such cases the sidelobes are no problem and can be thresholded out. In actual practice, however, the signals are noisy and, for any chosen threshold level, noise will occasionally suppress a main lobe below threshold and push a sidelobe above threshold. To minimize the frequency of occurrence of such errors one desires to maximize the difference between main and sidelobe signals—hence the desire for equalization.

Referring now to FIG. 4, there is illustrated a more preferred embodiment of the invention wherein the equalization and correlation is accomplished with a single appropriately tapped shift register 44 in conjunction with a clock 46. The cock provides shift pulses at a rate equal to the data input rate of the signal to be correlated. The first stage of shift register 44 is tapped by a resistor designated A_1. This is a resistor having an ohmic value A and corresponding to the first bit of the shift

register 14_1 of FIG. 3. The second stage of the shift register 44 is tapped in accordance with the second bit of shift register 14_1 and the first bit of shift register 14_2, indicated respectively as resistors A_2 and B_1, these resistors having ohmic values equal to resistors A and B of FIG. 3. Likewise, the third stage of shift register 44 is tapped by resistors A_3, B_2 and C_1 which designate the third bit of shift register 14_1, the second bit of shift register 14_2 and the third bit of shift register 14_3. This same sequence is carried out through all the stages of shift register 44 until finally the last stage of shift register 44 is tapped by a single resistor E_6 having an ohmic value E equivalent to the sixth bit of shift register 14_5. These taps are applied to a differential amplifier 48 with the correlated signal appearing at the output therefrom.

In this embodiment, the shift register which was already being used to accomplish the decoding is now used for double duty purposes to also accomplish the equalization function, thus providing a savings in hardware as well as curing the defects of the relatively low frequency delay lines. The shift register length has been increased from that simply required for decoding by an amount equal to the distance between the earliest and latest sidelobes to be corrected. It is at most tripled.

Although the shift register 44 of FIG. 4 is shown as having in some instances more than one resistor at the various stages thereof, of course, it is most likely that a single resistor having equivalent ohmic value would be provided at each stage. This is illustrated in FIG. 5 where the resistors A_2 and B_1 are now replaced by a resistor 50 of equivalent ohmic value. In like fashion resistors A_3, B_2 and C_1 have been replaced by resistor 52 and resistors A_4, B_2, C_2 and D_1 have been replaced by resistors 54. The tying in of resistors 50 and 54 to the plus and minus buses, respectively, has been an arbitrary selection since the example no actual values have been designated for the particular resistors.

In an alternative arrangement, the resistors can be attached to the Q and $\overline{Q}$ sides of the flip flops of the shift register ('-'one" and "zero" sides) and tied to a single summing bus, going to a single-ended amplifier. This is illustrated in FIG. 6 where the resistors A_1, 50, 52, 54 and E_6 are tied to a common bus coupled to amplifier 58. Note that in cases of reasonable delay to risetime ratios the shift register of the embodiments shown can be replaced by delay lines having appropriately weighted taps. Of course, no clock is required. Thus, it is to be understood that the embodiments shown are illustrative only, and that many variations and modifications may be made without departing from the principles of the invention herein disclosed and defined by the appended claims.

I claim:

1. A correlator having equalization correction, comprising:

a shift register having a plurality of stages into which a digital input signal comprising a bit pattern of ones and zeros is shifted;

means for shifting said input signal through said shift register;

a first group of resistors coupled to the outputs of predetermined stages of said shift register, said resistors corresponding to one bits of the signal to be correlated which correspond to the desired output pulse, one bits of the signal which correct negative sidelobes and zero bits of the signal which correct positive sidelobes;

a second group of resistors coupled to the outputs of predetermined stages of said shift register, said resistors corresponding to zero bits of the signal to be correlated which correspond to the desired output pulse, zero bits of the signal which correct positive sidelobes and one bits of the signal which correct negative sidelobes;

the conductance of each resistor of said first and second groups being the sum of a constant conductance for resistors which correlate bits of the signal and a conductance proportional to the degree of transversal filtering at that bit position; and

first means for summing the outputs of said first group of resistors;

second means for summing the outputs of said second group of resistors; and

means for subtracting the second sum from the first turn to obtain the correlated filtered signal.

2. A correlator having equalization correction, comprising:

a shift register having a plurality of stages each with a Q and $\overline{Q}$ output into which a digital input signal comprising a bit pattern of ones and zeros is shifted;

means for shifting said input signal through said shift register;

a first group of resistors coupled to the Q outputs of predetermined stages of said shift register, said resistors corresponding to one bits of the signal to be correlated which correspond to the desired output pulse, one bits of the signal which correct negative sidelobes and zero bits of the signal which correct positive sidelobes;

a second group of resistors coupled to the $\overline{Q}$ outputs of predetermined stages of said shift register, said resistors corresponding to zero bits of the signal to be correlated which correspond to the desired output pulse, zero bits of the signal which correct positive sidelobes and one bits of the signal which correct negative sidelobes;

the conductance of each resistor of said first and second groups being the sum of a constant conductance for resistors which correlate bits of the signal and a conductance proportional to the degree of transversal filtering at that bit position; and

means for summing the outputs of said resistors.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,621,221 Dated November 16, 1971

Inventor(s) Alfred J. Cann

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 2, line 50	The letters "A-F" should read --A-E--
Column 2, line 72	The word "cock" should read --clock--
Column 3, line 34	The word --in-- should be inserted after the word "since"
Column 4, line 26	The word "turn" should read --sum--

Signed and sealed this 3rd day of October 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents