Title: DRIVER CIRCUIT FOR A LIQUID CRYSTAL DISPLAY

Abstract: The driver circuit for a liquid crystal display is essentially a current driven device and preferably comprises digitally controllable current sources or switches (2.1 - 2.N) as column or row drivers connected to the loads (4.1 - 4.N) of the display. The switches are controlled by digital control data (CD) derived via a lookup table (5) from incoming image data (DATA). The driver circuit may further comprise a shift register.
Driver circuit for a liquid crystal display

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The invention relates to a driver circuit for a liquid crystal display and a method for driving a liquid crystal display.

Liquid crystal display systems having thin film transistors (TFTs) are being used more and more in applications which require a visual representation of images and/or data. Since the color depth of such TFTs systems is increasing steadily and the associated liquid crystal technology is getting more and more sophisticated, a very accurate control of the voltages needed for the TFT driving scheme is becoming compulsory. One of the critical blocks in the chain of subsystems involved in the panel driving in the current TFT source driver architecture is the resistor ladder for the digital-analog (D/A) conversion. This ladder shall be abbreviated as RDAC in the following. Conventionally, the RDAC uses resistors sized in order to reduce the process mismatching and the leakage influences. Such a resistor structure unfortunately occupies a large chip area, which is disadvantageous and thus undesirable.

To start with a known design, Fig. 1 shows a conventional architecture for a TFT display driver. The RDAC shown comprises multiple resistors R1 to Rn+1 forming a voltage divider with multiple voltage outputs, providing output voltages V1 to Vn corresponding thereto. Thus, the RDAC forms a simple digital to analog converter creating n discrete voltages V1 to Vn. The output voltages V1 to Vn, in the following also called reference voltages, create the shape of the gamma curve, wherein the gamma curve is a representation of the electrical and optical performance of the TFT display. It describes the transmission of the liquid crystal when applying a voltage to it. Each of the outputs of the RDAC is fed to a switch matrix SM1 to SMn.

Data signals are also fed to the switch matrixes SM1 to SMn, wherein the data is mapped to the corresponding reference voltage. E.g., the magnitude of the data determines the reference voltage V1 – Vn which is then switched to the output of the
switch matrix SM1 to SMn. Afterwards, the voltages switched through are buffered in the output buffers B1 to Bn.

Depending on the required resolution, speed performances, and leakage issues, different parameters of the RDAC underlie various constraints. The color and brightness resolution depends on the number and size of each resistive element R1 to Rn+1 of the resistor ladder RDAC. However, the accuracy of the gamma curve depends on the aspect ratio of the resistive elements R1 to Rn+1 (matching) and the total resistance of the resistor ladder RDAC for current leakage drawbacks. Finally, to minimize the delay caused by the internal parasitic elements an adaptation is made so that each tap in the resitant chain sees the same delay towards the output.

Therefore, to reach the required accuracy, a good tradeoff must be found between the kind of resistor available in the given technology and its parameter dependency. The matching pair spread $\sigma_{AR/R}$ is presented as the standard deviation of the relative difference $\Delta R/R$ between two resistors, e.g. R1 and R2, wherein $\Delta R = R1 - R2$ and $R = R1 + R2$. The resistances of the contacts in the head structures of the resistor, shown in Fig. 3, are considered as parts of the resistor. In addition, when a new D/A conversion is required, the whole resistor chain, i.e. the whole RDAC, has to be redesigned. Often the redesign of the resistor chain ends up in a complete product redesign.

Matsueda shows in US patent application publication 2002/0149556 a liquid crystal display with thin film transistors. A driver circuit for the liquid crystal display is described in figure 1 of this publication. In an active matrix for image display, signal lines and scanning lines are disposed in a matrix manner, and at an intersection thereof a pixel TFT, a hold capacitor, and a liquid crystal capacitor are connected. A shift register and a level shifter form the scanning lines. The level shifter is provided with a buffer circuit at its output section. A data driver section for sending an image signal to the signal lines is formed by a shift register, latches for reading data from a (n+m)-bit digital image signal according to the output timing of the shift register, latches for writing the data stored in the latches at a batch, and by a D/A converter for converting the (n+m)-bit digital image data stored in the latches to an analog signal.
With these two-stage latches, the D/A converter operates with the data stored in the second-stage latch while data is rewritten into the first-stage latch. Thus, sufficient time is available for driving the signal lines. Disadvantageously, the driver circuit works with a resistor-division-type D/A converter, i.e. a RDAC as explained above. Therefore, this driver circuit shows also the problems mentioned above.

An object of the invention is to provide an improved driver circuit and an associated method for driving a liquid crystal display. This novel driver circuit/method allows easy adaption of the image data control signals to the characteristics of the liquid crystal display used without the necessity of redesigning the whole driver circuit. Advantageously, with the driver circuit according to the invention, a desired gamma curve can easily be achieved, or a given curve adjusted.

The solution according to the invention is a driver circuit for a liquid crystal display with the features according to the independent apparatus claim 1 and a method for driving a liquid crystal display with the features according to independent method claim 13.

Essentially, the novel driver circuit according to the invention is a current-driven device wherein appropriately controlled current switches provide the necessary input for the dot generation on the display. It comprises a controllable current reference and current switches controlled by said current reference. It may further comprise digitally controllable current sources/switches connected to the liquid crystal display and controlled by digital control data and/or the inputs by said current reference. It may further comprise a lookup table for converting incoming digital image data to digital control data.

The method for driving a liquid crystal display according to the present invention comprises the following steps:

- Digital image data are converted by means of a lookup table into digital control data.
- Then, using these digital control data, controllable current sources are adjusted to deliver corresponding currents for generating image dots on the liquid crystal display.
In an embodiment of the driver circuit according to the invention, a reference current source is provided and connected to the controllable current sources/switches to supply them with a reference current.

In a further embodiment of the driver circuit, the reference current source is a programmable reference current source. This has the advantage that the driver circuit is very flexible and can easily be adapted to different liquid crystal displays. Advantageously, the driver circuit according to the invention can comprise a pipeline connected between the lookup table and the controllable current sources. In the pipeline, the control data are stored intermediately and then dispatched to the programmable current sources in parallel.

In a still further embodiment of the invention, the pipeline comprises data latches, in which the data are intermediately stored before they are forwarded for example to a shift register.

The lookup table of the driver circuit according to the invention may be stored in an electrically erasable programmable read only memory (EEPROM), a Flash memory, a read only memory (ROM), or a random access memory (RAM).

Furthermore, the driver circuit can comprise a shift register, which is connected with its input to the pipeline and with its outputs to the controllable current sources.

In another aspect of the invention, the liquid crystal display comprises means for generating image dots, and each controllable current source of the driver circuit is connected to one of the means for generating image dots.

In a typical application, the driver circuit according to the invention comprises a clock generator for generating a clock signal which defines when the means for generating image dots of the liquid crystal display are charged.

The driver circuit according to the invention is preferably applicable to a liquid crystal display wherein the image dots are generated by thin film transistors (TFTs).

In a further embodiment of the method according to the invention, a suitable clock signal is provided for controlling the timing when the means for generating image dots are supplied with the current from the current sources.
Subsequently, the invention is further explained with the drawings showing in

Fig. 1 a conventional embodiment of a driver circuit for a thin film transistor display;

Fig. 2 a block diagram of a display driver circuit according to the invention for driving a liquid crystal display; and

Fig. 3 a resistor layout including the head structure of the resistor.

Fig. 1 shows a block diagram of a conventional driver circuit for a liquid crystal display. This conventional driver circuit is explained above in this description in the section "Background of the invention".

The novel source driver architecture using a current based approach is proposed in order to overcome the limitations of the conventional implementation shown in Fig. 1.

Fig. 2 shows the principal structure of an embodiment of the driver circuit 8 for driving a liquid crystal display. The liquid crystal display itself is not fully shown, only parts thereof, namely the means for generating image dots 4.1, 4.2 ... 4.N. These form the loads for the display driver outputs. Usually, three image dots are combined to one pixel, wherein each image dot is driven by one current switch. The number of pixels and thus the number of current switches depends on the resolution of the liquid crystal display. Digital image data DATA entering the driver circuit 8 are fed to a lookup table 5 and control data CD resulting from this lookup operation are stored intermediated in a data pipeline. This data pipeline comprises a series of data latches 6, the number of data latches depending on the number of current switches 2.1, 2.2 to 2.N. A clock generator 3 creates an internal clock signal CLK from an external clock signal EXTCLK, which synchronizes the current switches 2.1 to 2.N and determines the time during which the loads, i.e. the means for generating image dots 4.1 ... 4.N, are charged. Therefore, the internal clock signal CLK is conducted to a clock input of each of the current switches 2.1 to 2.N.
An address generator 9 selects the address of the memory in which the lookup table 5 is stored which is necessary to convert the incoming digital data DATA with the help of the parameters stored in the look-up table 5. By means of a read/write signal R/W it is decided whether the parameters stored in the lookup table 5 shall be read out or not.

Programming of the look-up table 5 is done by hard-programming, the look-up table can be seen as a ROM type. There are of course other possible types of memory so that soft programming is possible (SRAM, EEPROM, etc.)

The driver circuit 8 further comprises a programmable reference current source 1 which can produce different reference currents $I_{ref}$. The set point of the desired current intensity of the current $I_{ref}$ is provided by the incoming digital data DATA, which are also, lead to the programmable reference current source 1.

The principal idea of the driver circuit 8 according to the invention consists in driving the output loads 4.1 to 4.N by means of various currents I1, I2 ... IN.

The necessary reference current $I_{ref}$ is provided by the programmable reference current source 1 and delivered to the column drivers 2.1 to 2.N. Here, the current $I_{ref}$ is replicated and partitioned by a current switch. Each column driver 2.1 to 2.N comprising a current switch and a current replicator produces a current I1, I2 to IN, which, according to the timing imposed by the internal clock generator 3, charges the loads 4.1 to 4.N for a well-defined interval. This interval must be chosen in order to drive the correct voltage onto the load 4.1 to 4.N by means of the partitioned current I1, I2 to IN. How the reference current $I_{ref}$ is split, is stored in the lookup table 5. Here, the incoming digital data DATA are re-mapped into the configuration to be provided to the current switches 2.1 to 2.N. First, this re-mapping allows converting the incoming data DATA into a data format required by the current switches 2.1 to 2.N. Secondly, with the help of the re-mapping the data are adjusted to implement a desired specific gamma curve.

By programming the reference current source 1, the novel architecture allows to drive different loads, giving thus the benefit of being independent from the load conditions once the display panel is chosen.

For incoming data DATA fed through the lookup table 5, the out coming control data CD is temporarily stored in the data latches 6 of the pipeline to interface the
internal and the external time domains. The shift-register 7 stores and delivers the latch signal for each column driver 2.1 to 2.n, and here the image data are stored. After a complete scan of all the columns, an additional pulse is produced, the duration of which being controlled by the clock generator 3. The duration of the pulse accords with the current driving scheme described above. These steps are repeated for all the columns.

The current switch and the current replicator can jointly form a controllable current mirror. The controllable current-mirror is based on a current division technique which allows a basic reference current to be binary weighted and split up so that the output current coming out of driver 2.1 to 2.n is a binary weighted part of the basic current. The current switch and the current replicator are also called column driver or controllable current source.

The lookup table 5 is in principle a [MxN] matrix, where M is the number of bits composing the data and N the required resolution for the current switches 2.1 to 2.n. Since N can be chosen wide enough to implement more than one mapping, simply imposing N > M one can benefit of a digital representation of the gamma curve with the following advantages: 1. The implemented gamma curve can easily be adapted/changed. 2. Production-process-related inaccuracies can easily be corrected by an appropriate adaptation of the parameters stored in the lookup table. 3. The match between the driver output and the load environment can be improved.

Having illustrated and described a preferred embodiment for a novel driver circuit for a liquid crystal display and a method for driving a liquid crystal display, it is noted that variations and modifications in the device and the method can be made without departing from the spirit of the invention or the scope of the appended claims.
REFERENCE NUMBER LIST

R1 – Rn+1  resistors
V1 – Vn  reference voltages
SM1 – Smn  switch matrixes
B1 – Bn  output buffers
Data  Data signal
RDAC resistor ladder for the D/A conversion
1  programmable current reference
2.1 – 2.1N  controllable current source/switch
3  internal clock generator
4  shift register
5  lookup table
6  data latches
I_{ref}  reference current
I1 – IN  output current
DATA  digital input image data
R/W  read/write signal
EXTCLK  external clock signal
CD  control data
CLAIMS:

1. A driver circuit for a liquid crystal display, comprising a current reference (1) providing a plurality of predetermined reference currents (\textit{Iref}), and a plurality of current sources or switches (2.1, 2.2, ... 2.N) as column or row drivers for said display, each said current source/switch receiving a predetermined reference current.

2. The driver circuit according to claim 1, further comprising a lookup table (5) for converting incoming digital image data (DATA) into digital control data (CD) supplied to the current switches (2.1, 2.2, ... 2.N).

3. The driver circuit according to claim 1 or 2, wherein the current reference (1) is a digital device and the current switches (2.1 ... 2.N) are digitally controllable current sources connectable to the liquid crystal display and controllable by digital control data (CD) and/or a predetermined reference current (\textit{Iref}).

4. The driver circuit according to any of the preceding claims, wherein the current reference (1) is programmable.

5. The driver circuit according to any of the preceding claims, wherein the current reference (1) comprises a current mirror.

6. The driver circuit according to any of the preceding claims, wherein a pipeline for the data is provided, connected between the lookup table (5) and the current switches (2.1 ... 2.N).
7. The driver circuit according to claim 6, wherein the pipeline comprises data latches (6).

8. The driver circuit according to claim 6 or 7, further comprising a shift register (7) connected with its input to the pipeline for receiving image data to be displayed and with its outputs to the current switches (2.1 – 2.N).

9. The driver circuit according to any of the preceding claims, wherein the lookup table (5) is stored in an EEPROM, a Flash memory, a ROM, or a RAM.

10. The driver circuit according to any of the preceding claims, wherein the liquid crystal display comprises means for generating image dots (4.1 – 4.N), and each controllable current source (2.1 – 2.N) is connectable to one of said means for generating image dots (4.1 – 4.N).

11. The driver circuit according to claim 10, further comprising a clock generator (3) for generating a clock signal (CLK), which defines when the means for generating image dots (4.1 – 4.N) are charged by the current switches (2.1 – 2.N).

12. The driver circuit according to claim 10, wherein the means for generating image dots (4.1 – 4.N) comprise thin film transistors.

13. A method for driving a liquid crystal display, comprising the following steps: (a) a plurality of predetermined reference currents (I_ref) is generated, each said reference current being provided to an associated current source or switch, (b) each said current source/switch delivers a corresponding current for generating image dots on said liquid crystal display.

14. The method according to claim 13, wherein the current source/switch is digitally controlled and the predetermined reference current is provided as digital signal to an associated current source/switch.
15. The method according to claim 14, wherein incoming image data (DATA) to be displayed are converted into digital control data (CD), and said digital control data control the current switches/sources together with the digital reference current.

16. The method according to claim 14, wherein the conversion of incoming digital image data (DATA) to digital control data (CD) is performed via a lookup table (5).

17. The method according to any or all of claims 13 to 16, wherein a clock signal determines the internal timing of the reference current generation and delivery, the image data conversion, and the image dot generation.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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