

[54] CODE PROGRAMMING DEVICE

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[57]

ABSTRACT

[52] U.S. Cl..... 340/147 P; 328/37; 340/348

[51] **Int. Cl.**..... **G08c 9/00; H03k 21/00**

[58] **Field of Search** 340/147, 164, 149 R, 147 P,
340/147 MD, 168, 348, 168 R, 147 R, 164
R; 328/37, 39, 42

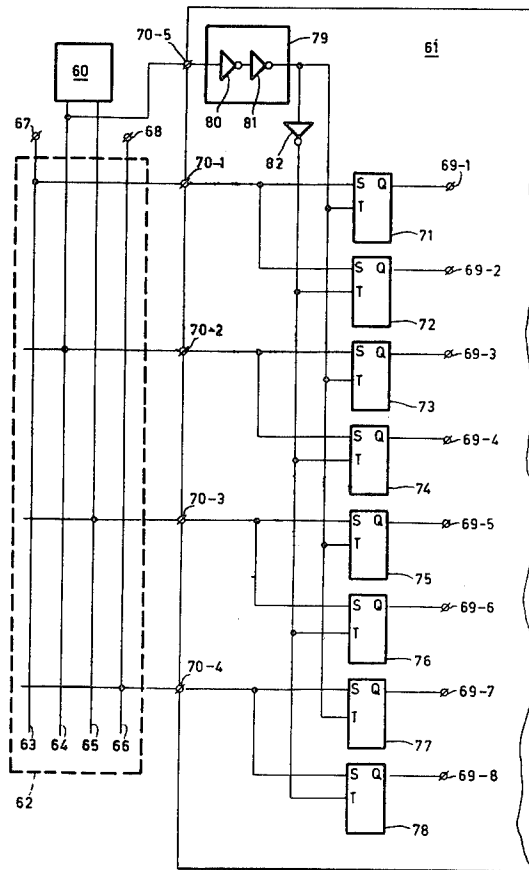
A programming device, comprising an integrated circuit which is provided with an envelope and a coding matrix which comprises code conductors and a code generator which is connected thereto so as to supply each code conductor with its own sub-code. The integrated circuit is coupled to the coding matrix so as to receive a code signal programmed in the coding matrix.

[56] **References Cited**

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5 Claims, 6 Drawing Figures



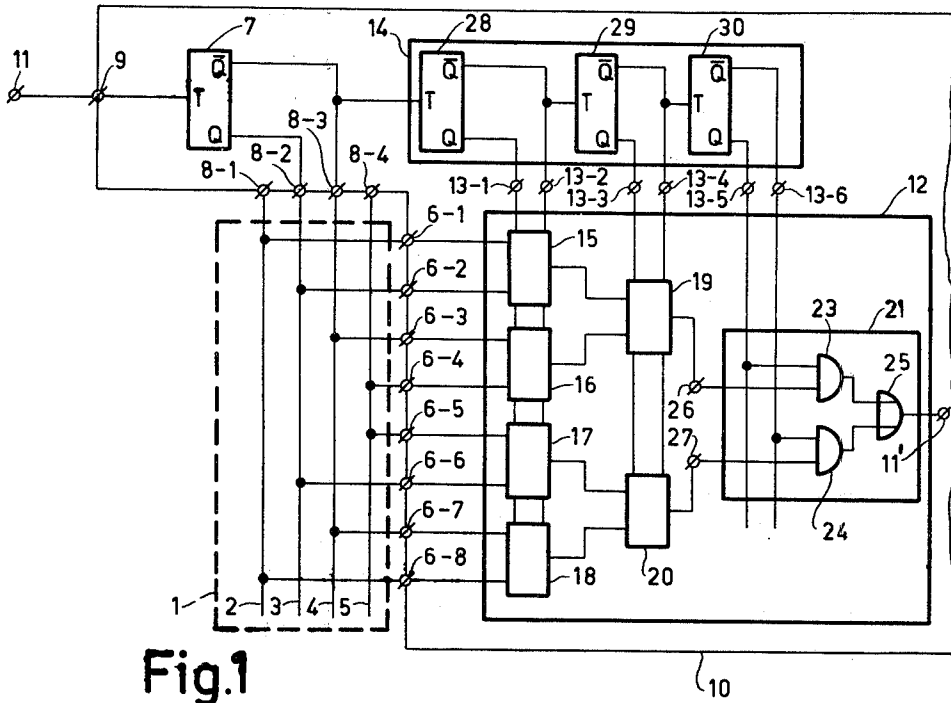


Fig.1

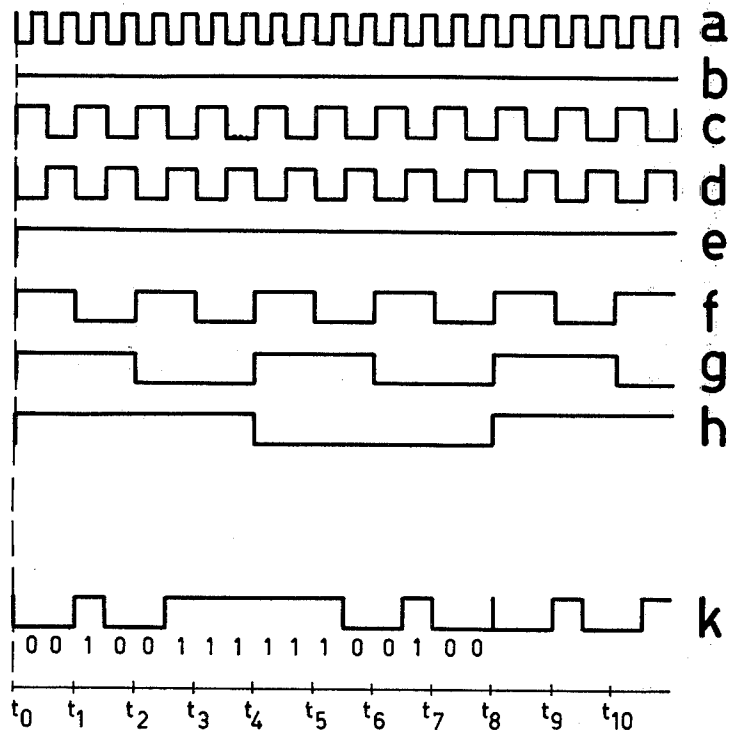


Fig.2

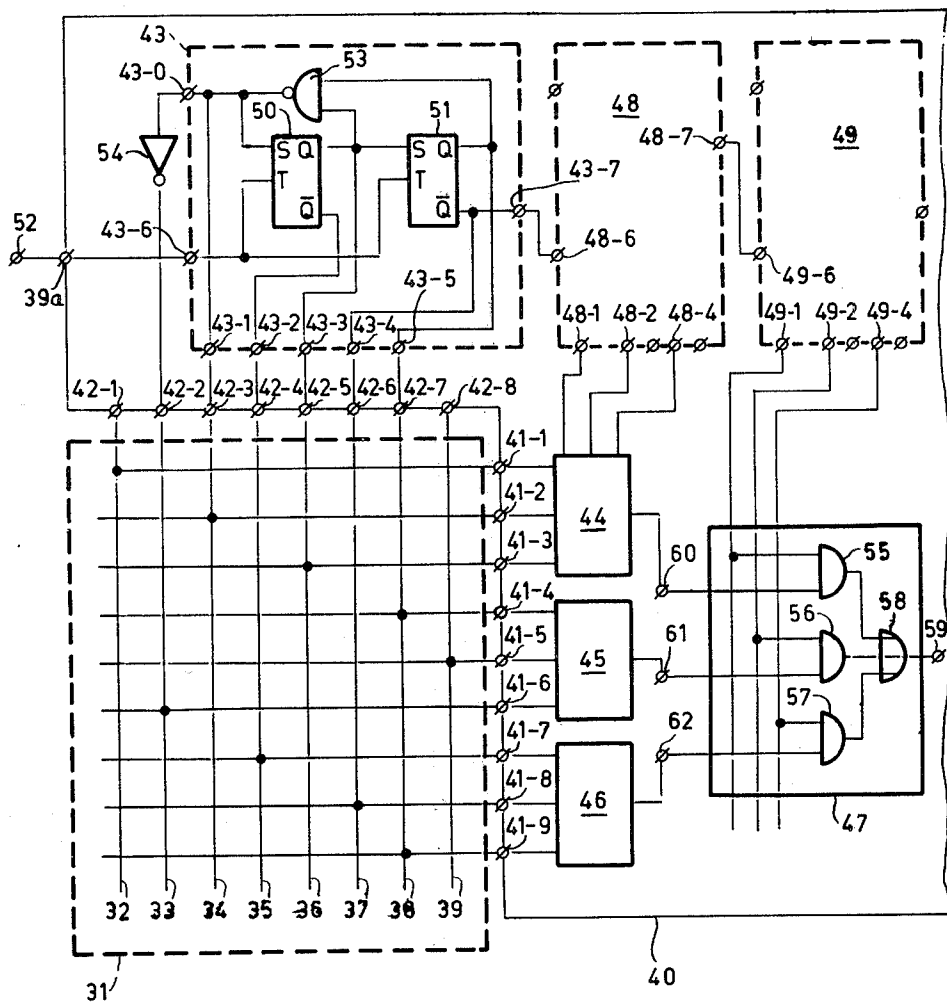


Fig.3

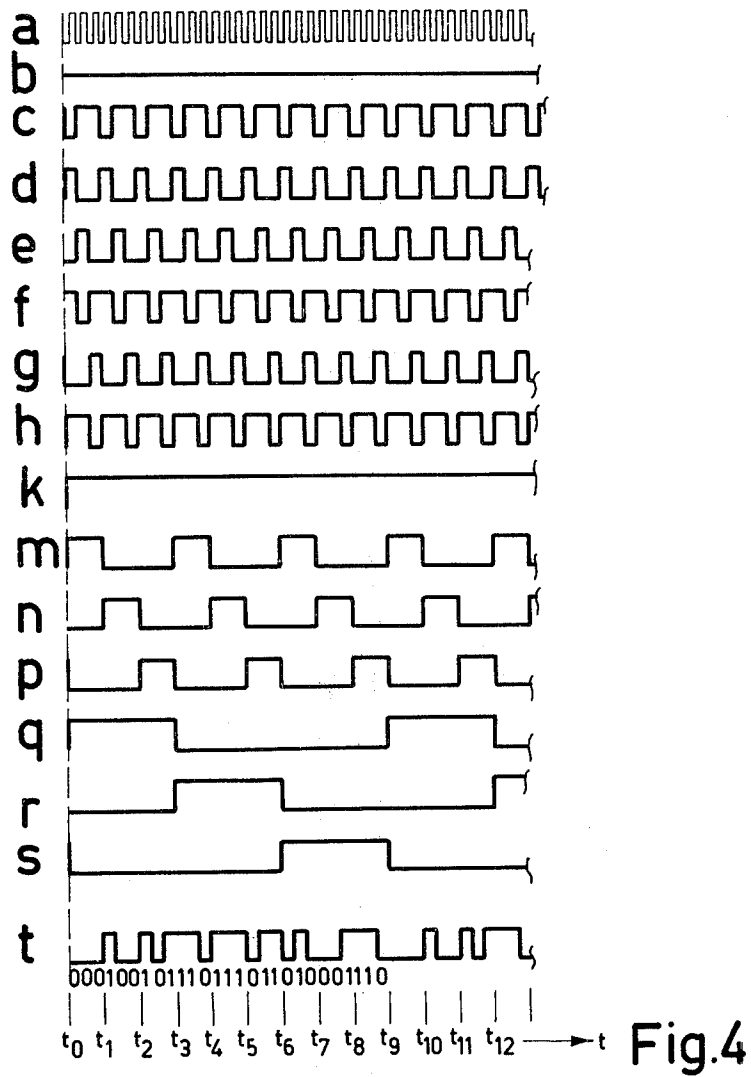


Fig.4

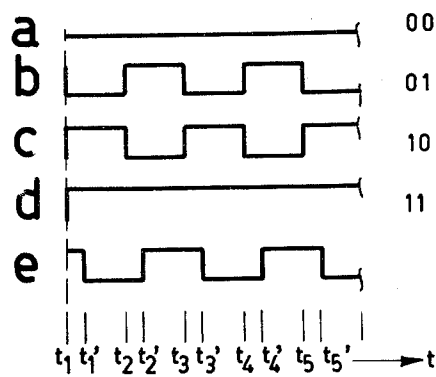


Fig.6

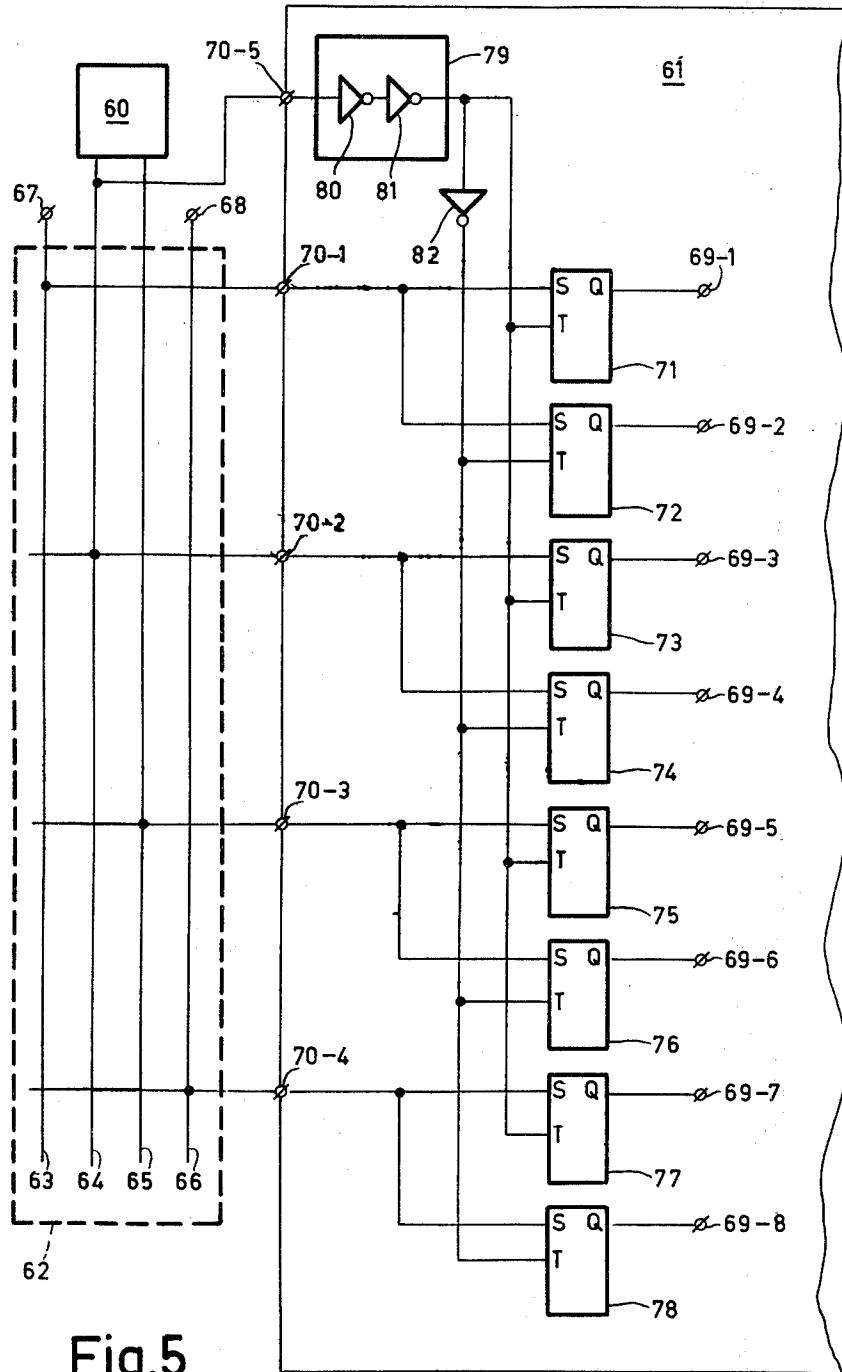


Fig.5

CODE PROGRAMMING DEVICE

The invention relates to a code programming device, comprising a circuit which is provided with an envelope and a coding matrix to which the circuit is coupled so as to supply this circuit with a code signal programmed by means of the coding matrix.

Devices of this kind in which the code signals are address codes are used inter alia in receivers of selective paging systems.

In these known devices, the envelope is provided with a number of connection terminals, corresponding to the number of bits of the address code, for applying a specific address code to the circuit. The coding matrix comprises a conductor which carries a high voltage and a conductor which carries a low voltage, the connection terminals being connected to these conductors in accordance with the address code to be programmed. In selective paging systems by means of which it must be possible to call a very large number of subscribers individually, such as in the case of a "city paging system," the number of connection terminals required for applying an address code to the circuit is accordingly large.

The number of connection terminals of an envelope of a circuit, however, is limited. This implies that the number of connection terminals which can be made available for programming address codes in the described manner for selective paging systems comprising very many subscribers is too small.

The invention has for its object to provide a completely novel concept for the programming of code signals, in which the required number of connection terminals of the envelope of the circuit is small with respect to the number of bits of the code signals.

The device according to the invention is characterized in that the coding matrix comprises code conductors and a code generator which is connected thereto in order to supply each code conductor with its own sub-code. In this context, a sub-code is to be understood to mean a signal which forms a part of a code signal to be programmed.

According to another characteristic, the code generator is arranged within the envelope of the circuit. This offers the advantage that no separate envelope is required for the code generator, whilst the number of connection terminals of the common envelope which must be available for generating a code signal is minimum.

It is to be noted that French Patent Specification No. 2,019,375 describes a circuit where the bits of a code signal are successively applied to a code comparison device. However, by means of this circuit no code signal can be programmed but a given code signal can only be stored.

The invention and its advantages will be described in detail hereinafter with reference to the embodiments shown in the figures.

The FIGS. 1, 3 and 5 show different embodiments of a programming device according to the invention, and

The FIGS. 2, 4 and 6 show signals which can appear in the programming devices shown in the FIGS. 1, 3 and 5, respectively.

The programming device shown in FIG. 1 is used inter alia in a receiver of a selective paging system. In a code comparison device in a receiver of this kind, a received code signal is compared with a specific code

signal present in the receiver. Such code signals are referred to as address codes. In order to achieve manufacturing economy of the receivers, they are uniformly constructed in integrated form. For putting a receiver of this kind into operation in a selective paging system. It must be possible to adjust an address code for the relevant receiver in a simple manner. To this end, the receivers are provided with a coding matrix 1. In known receivers, this matrix is composed of a first conductor 2 which is connected, via a connection terminal 8-1 of the envelope 10, to a voltage source (not shown in the drawing) for supplying this conductor 2 with a low voltage signal, denoted by the logic symbol 0, and a second conductor 5 which is also connected to the voltage source, via a connection terminal 8-4, for supplying this conductor with a high voltage signal which is denoted by the logic symbol 1. The specific address code is applied to the integrated code comparison device, not shown in the figure, by connecting each of the connection terminals 6 of the envelope 10 of the integrated code comparison device to one of the two conductors 2, 5 in accordance with the address code to be programmed. A separate connection terminal 6 must then be available on the envelope for each bit of the address code. For a paging system by means of which individual paging of a large number of subscribers must be possible, the address codes are composed of a correspondingly large number of bits. This implies that an insufficient quantity of connection terminals 6 for applying these long address codes are available on the envelope.

According to the invention, the coding matrix 1 is provided with code conductors 3 and 4, and a code generator 7 is provided which is connected to the code conductors 3 and 4, via connection terminals 8-2 and 8-3, in order to supply each of these code conductors 3, 4 with its own sub-code.

It is to be noted that the code generator (in this embodiment) is accommodated inside the envelope 10. This code generator 7 comprises a bistable element which is provided with a trigger input T, a signal output Q and an inverted signal output $\bar{Q}$. If a voltage changing from high to low appears on the trigger input T, the bistable element is switched over from the set state to the reset state or vice versa, the set state being characterized in that signal output Q carries a high voltage signal 1 and the inverted signal output $\bar{Q}$ carries a low voltage signal 0, and vice versa for the reset state. The trigger input T of the bistable element 7 is connected, via connection terminal 9, to a clock pulse input 11 which receives the clock pulse signal shown in FIG. 2a. The bistable element 7 divides this pulse series by two and supplies the signal output Q and the inverted signal output $\bar{Q}$ with the signals shown in FIGS. 2c and 2d, the said signals representing sub-codes of the code signal to be programmed. Together with the voltage signals on the conductors 2 and 5, four codes having a length of two bits are obtained, i.e., 0,0; 1,0; 0,1 and 1,1, respectively, for the conductors 2 to 5. By connecting these conductors as desired to the connection terminals 6-1 to 6-8, each address code can be applied to an input terminal 11' of an integrated code comparison device (not shown in the figure). In order to apply the address code to this input terminal in a suitable form, a contact pyramid 12 comprising control inputs 13 is provided, and also a control signal generator 14 which is connected to the inverted signal output $\bar{Q}$ of code genera-

tor 7 and which is connected to the control inputs 13-1 to 13-16.

The contact pyramid 12 is composed of identical two-position switches 15 to 21, two-position switch 21 being shown in detail.

The two-position switch comprises two AND-gates 23 and 24, a signal input 26, 27 and a control input 13-5, 13-6 being connected to the inputs of each AND-gate, the AND-gates being connected to input terminal 11' via an OR-gate 25. If a high signal is applied to control input 13-5, the signal on input 26 will be applied to input terminal 11' via AND-gate 23 and OR-gate 25. Similarly, if the control signal on control input 13-6 is high, the signal on input 27 will be applied to input terminal 11' via AND-gate 24 and OR-gate 25.

The control signals are generated in the control signal generator 14. This generator comprises three cascade-connected bistable elements 28, 29 and 30 which are identical to bistable element 7. By means of these elements 28, 29 and 30, control signals are obtained by successive two-division of the pulse series which is supplied by code generator 7 and which is shown in FIG. 2d, the control signal supplied by the signal outputs Q of the elements 28, 29 and 30 being shown in the FIGS. 2f, 2g and 2h.

The connection terminal 6-1, 6-2; 6-3, 6-4; 6-5, 6-6; and 6-7, 6-8 are connected in pairs to the inputs of the two-position switches 15, 16, 17 and 18, which also receive the control signals supplied by element 28. The outputs of the switches are connected to the inputs of the two-position switches 19 and 20, which also receive the control signals supplied by element 29. The outputs of these switches are connected to the signal inputs 26 and 27, the control signals generated by element 30 being applied to the control terminals 13-5 and 13-6.

As appears from the FIGS. 2f, 2g and 2h, the control signals on the control inputs 13-1, 13-3 and 13-5 are high between the instants t_0 and t_1 , with the result that connection terminal 6-1 is connected to input terminal 11' during this period. Between the instants t_1 and t_2 , the control signals on the control inputs 13-2, 13-3 and 13-5 are high, with the result that connection terminal 6-2 is connected to input terminal 11' during this period.

Similarly, between the instants t_2-t_3 , t_3-t_4 , t_4-t_5 , t_5-t_6 , t_6-t_7 and t_7-t_8 , the connection terminals 6-3, 6-4, 6-5, 6-6, 6-7 and 6-8 are successively connected to the input terminal 11'. In the above time intervals the two-bit sub-codes are each time applied to input terminal 11'. As a result of the connections between the conductors 2, 3, 4, 5 and the connection terminals 6-1 to 6-8 shown in the coding matrix 1, a code signal is programmed which is shown in FIG. 2k.

As a result of the realization of the programming device as described above, it is achieved that an address code comprising sixteen bits is applied to the input terminal 11' by means of eight connection terminals 6-1 to 6-8, whilst only two additional connection terminals 8-3 and 8-4 are required to enable application of the codes to the code conductors 3 and 4.

For an address code comprising a much larger number of bits, it is more advantageous to use sub-codes which also comprise a large number of bits.

One embodiment in which sub-codes having a length of three bits are used is illustrated in FIG. 3.

Using three bits, at the most eight different subcodes can be composed. Therefore, the code programming

device shown in FIG. 3 differs from that shown in FIG. 1 in that the coding matrix comprises, in addition to the voltage conductors 32 and 39, six code conductors 33 to 37, in that the code generator 43 is constructed as a three-divider, in that the contact pyramid is realized by means of three-position switches 44, 45, 46 and 47, and in that the control signal generator comprises three-dividers 48 and 49.

The three-dividers, three-divider 43 being shown in detail, comprise two series-connected bistable elements 50 and 51 which are provided with a signal input s in addition to a trigger input T, a signal output Q, and an inverted signal output $\bar{Q}$. At the instant at which the voltage on the trigger input T changes from high to low, the bistable element is set or reset, in accordance with the signal value applied to the signal input s .

The trigger inputs T of these elements 50 and 51 are connected, via terminal 43-6 and connection terminal 39a, to a clock input 52 which receives the clock pulse signal which is shown in FIG. 4a.

Assuming that the elements 50 and 51 are in the set state, a signal having the logic value 0 will be applied to the signal input s of element 50 via the NAND-gate 53 which is connected to the signal outputs Q. Element 50 is reset when the trailing edge of the first clock pulse appears. The NAND-gate 53 then applies a signal having the logic value 1 to signal input s of element 50. Element 51 is reset when the trailing edge of the second clock pulse appears, because the logic value 0 was applied to the signal input e of this element, and element 50 is set, with the result that the NAND-gate 53 supplies the logic value 1. When the trailing edge of the third clock pulse appears, element 51 is set again, with the result that the three-divider 43 returns to its initial position.

Of the signals generated by the three-divider 43, the signal shown in FIG. 4c is applied to code conductor 33 via terminal 43-0, inverter 54 and connection terminal 42-2. The other signals generated by the three-divider 43, shown in the FIGS. 4d to 4h, are applied to the code conductors 34 to 37 via terminals 43-1 to 43-5 and connection terminals 42-3 to 42-7. The voltage conductors 32 and 39 receive their voltages, shown in the FIGS. 4b and 4k, in a manner not shown via the connection terminals 42-1 and 42-8.

The three-position switches 44 to 47 comprise, as is shown in detail for three-position switch 47, three AND-gates 55, 56, 57 which are connected, via an OR-gate 58, to an input terminal 59 of a code comparison device not shown. Connected to inputs of each AND-gate 55, 56 and 57 are a signal input 60, 61 and 62 and a control signal input 49-1, 49-2, 49-4. Depending on whether or not a control signal applied to an AND-gate is high, the signal input connected to the relevant AND-gate is connected to the input terminal 59.

The three-divider 48 derives the signals which are shown in the FIGS. 4m, 4n and 4p from the signal which is supplied by code generator 43 via terminal 43-7 and which is shown in FIG. 4g, the said signals being applied to the three-position switches 44, 45 and 46 via the terminals 48-1, 48-2 and 48-4. Similarly, the three-divider 49 derives the signals shown in the FIGS. 4q, 4r and 4s from the signal supplied via terminal 48-7 and shown in FIG. 4p, the derived signals being applied to the terminals 49-1, 49-2 and 49-4.

The connection terminals 41-1, 41-2, 41-3; 41-4, 41-5, 41-6; and 41-7, 41-8 and 41-9 are connected in

groups of three to the signal inputs of the three-position switches 44, 45 and 46, whilst the outputs of these switches are connected to the signal inputs 60, 61 and 62.

As appears from the FIGS. 4m to 4s, connection terminal 41-1 is connected to the input terminal 59 between the instants t_0 and t_1 , connection terminal 41-2 being connected thereto between t_1 and t_2 , etc. Consequently, the connection terminals 41-1 to 41-9 are thus successively connected to the input terminal 49, each time during one cycle time of the sub-codes.

By connecting each of the connection terminals 41-1 to 41-9 to one of the conductors 32 to 39 in the coding matrix 31, any desired address code can be adjusted. The address code shown in FIG. 4t is adjusted by way of the connections shown in the matrix 31, the said address code having a length of twenty-seven bits. The number of connection terminals required for this address code so as to apply this address code to input terminal 59 amounts to nine, whilst six additional connection terminals 42-2 to 42-7 are required for applying the sub-codes to the coding matrix 31.

The use of sub-codes having a larger number of bits reduces, on the one hand, the number of connection terminals required for applying the sub-codes from the coding matrix to the integrated circuit, whilst on the other hand the number of connection terminals for applying the sub-codes to the coding matrix is increased. It follows that a minimum number of required connection terminals for a code signal of a given length to be programmed can be achieved by a suitable choice of the length of the sub-codes. In the adjoining table the number of bits m of the sub-codes are given for code signals having a length of N bits for which a minimum number of connection terminals suffices. In the embodiment

1 to 4	1
5 to 24	2
25 to 96	3
96 to 288	4

shown in FIG. 5, the code generator 60 is accommodated outside the envelope 61. In this embodiment the subcodes have a length of two bits, so that a coding matrix 62 suffices which contains, in addition the voltage conductors 63 and 66, the code conductors 64 and 65. The voltage conductors 63 and 66 are connected to the terminals 67 and 68 of a voltage source not shown and carry the signals shown in FIGS. 6a and 6d. The code generator 60 is a clock pulse generator which applies the sub-code shown in FIG. 6b to code conductor 64 and which applies the inverted sub-code shown in FIG. 6c to code conductor 65. The envelope 61 is provided with connection terminals 70-1 to 70-5. In order to enable application of a code signal to input terminals 69-1 to 69-8 of a code comparison device not shown, via the connection terminals 70-1 to 70-4, each connection terminal 70-1, 70-2, 70-3, 70-4 is connected to signal inputs s of two storage elements 71, 72; 73, 74; 75, 76 and 77, 78 which are constructed as bistable elements. The input terminals 69-1 to 69-8 are connected to the signal outputs Q of these elements. Furthermore, the code generator 60 applies, on the one side, the pulse sequence shown in FIG. 6e as a control signal to the trigger inputs T of the odd storage elements 71, 73, 75 and 77 via connection terminals 70-5 and via a delay

element 79 comprising the inverters 80 and 81, whilst on the other side this pulse series is applied, after inversion in inverter 82, as a control signal to the trigger inputs T of the even storage elements 72, 74, 76 and 78.

The operation will be described in detail with reference to a specific address code which is determined by the connections established between the connection terminals 70-1 to 70-4 and the conductors 63 to 66.

Immediately after the instant t_1 shown in FIG. 1, the signal values on the conductors 63 to 66 are successively low, high and high.

These values are applied, via the connection terminals 70-1 to 70-4, to the signal inputs s of the bistable elements 71, 72, 73, 74, 75, 76 and 77, 78. The negative voltage variation (FIG. 6e) produced by the delay element 79 at the instant t_1^1 adjusts the odd storage elements 71, 72, 73 and 77 to the reset state, the reset state, the set state and the set state, successively, in accordance with the signal values present on their input terminals.

At the instants t_2 , the signal values of the code conductors 64 and 65 and hence the signal values on the signal inputs s of the storage elements 73, 74 and 75, 76 change from low to high (FIG. 6b) and from high to low (FIG. 6c), respectively. The positive voltage variation (FIG. 6e) produced by the delay element 79 at the instant t_2^1 adjusts the even storage elements 72, 74, 76 and 78 to the reset state, the set state, the reset state and the set state, respectively, via inverter 82, in accordance with the signal values present on their signal inputs s . As a result, after the instant t_2^1 the storage elements 71 to 78 apply an address code to the input terminals 69-1 to 69-8 which has the bit values 0,0,0, 1,1, 0, 1,1, respectively.

The number of input terminals required for writing the above eight-bit address code amounts to one connection terminal for the control signal and four connection terminals for the eight bits.

At the instant t_3^1 the odd storage elements are written in again, and at the instant t_4^1 the even elements again etc. This offers the advantage, on the one hand, that should the address code be mutilated by interference in the storage elements 71 to 78, the correct address code will be adjusted again by the next pulse supplied by the code generator 60, whilst on the other hand it is now possible to use inexpensive storage elements which require only a limited storage time with the result that the programming device can be inexpensively realized.

It is to be noted that if the code comparison device which is not shown is adapted to compare the address codes with a received code signal at the instants t_2^1 , t_4^1 , t_6^1 etc., the even storage elements 72, 74, 76 can be dispensed with, and that if the code comparison device is adapted to compare the address code with a received code signal partly at the instants t_1^1 , t_3^1 , t_5^1 , etc. and partly at the instants t_2^1 , t_4^1 , t_6^1 , etc., all storage elements 71 to 78 can be dispensed with. The control signals supplied by delay unit 79 and/or inverter 82 are then used for controlling the code comparison device.

What is claimed is:

1. A device comprising code-matrix means for generating a fixed code signal comprising a plurality of code conductors, a code generator means having an input means for receiving locally generated identical clock pulses and an output means coupled to said conductors for supplying to each of said conductors a subcode respectively, and a circuit means coupled to said matrix

means for receiving from said matrix means said code signal.

2. A device as claimed in claim 1, wherein the code generator means and the circuit means are integrally formed.

3. A device as claimed in claim 1, further comprising connection terminal means coupled to the code matrix for receiving the sub-codes, the circuit means comprising one code signal output terminal means for providing the code signal in series, a switching device provided with a control input, said switching device being coupled between the connection terminals and the code signal output terminal, the code generator being coupled to the control input, said switching device comprising means for coupling the connection terminals successively to the code signal output terminal under the control of a signal supplied by the code generator.

4. A device as claimed in claim 1, wherein the circuit means comprises a plurality of output terminals which correspond to the number of bits of the code signal, and further comprising connection terminals means coupled to the coding matrix for receiving the sub-codes, storage elements provided with a plurality of control inputs which corresponds to the number of bits of the sub-code, said elements being coupled to each connection terminal, the said storage elements being coupled to the output terminals and comprising means for supplying the output terminals simultaneously with the bits of the sub-codes which are successively applied to the connection terminals, and a control signal generator coupled to said control inputs.

5. A device as claimed in claim 1 further comprising a receiver of a selective paging system.

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