Sept. 9, 1969 L. K. CLARK ET AL 3,466,599
TRAFFIC CONTROLLER HAVING IMPROVED TIME
WAITING-GAP REDUCTION CIRCUIT
Filed Oct. 12, 1966 7 Sheets-Sheet 1

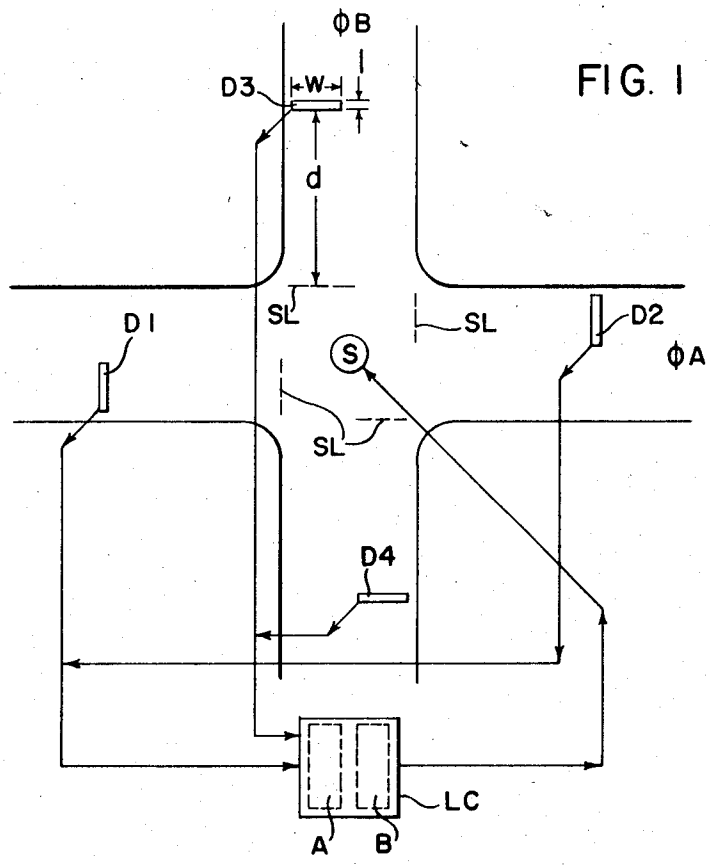


FIG. 1

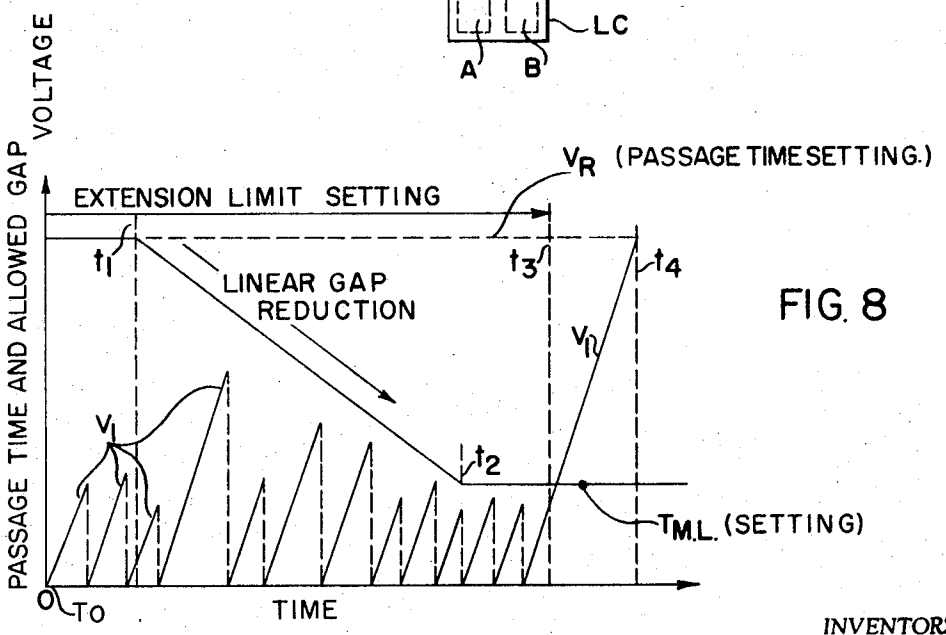


FIG. 8

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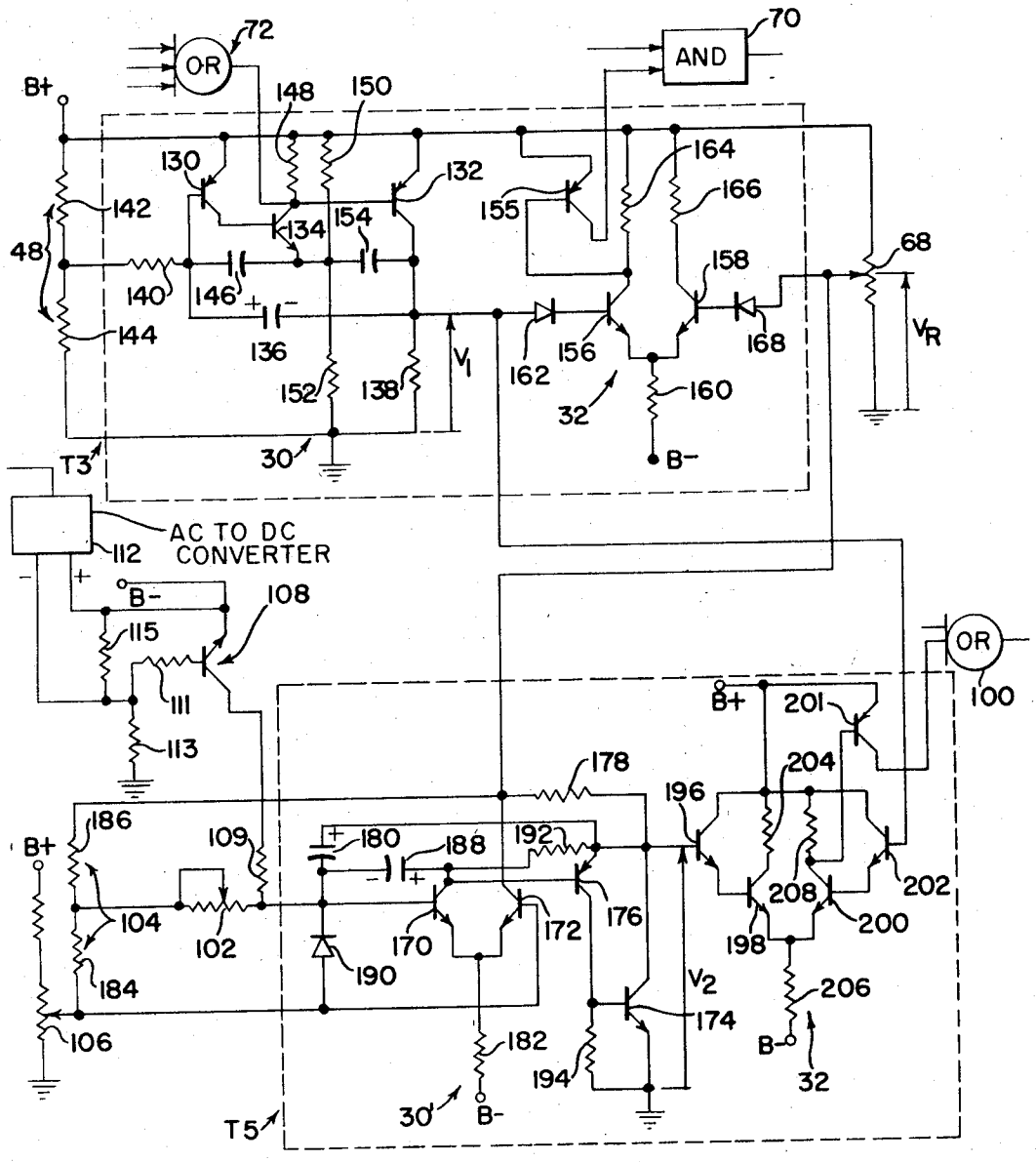


FIG. 2

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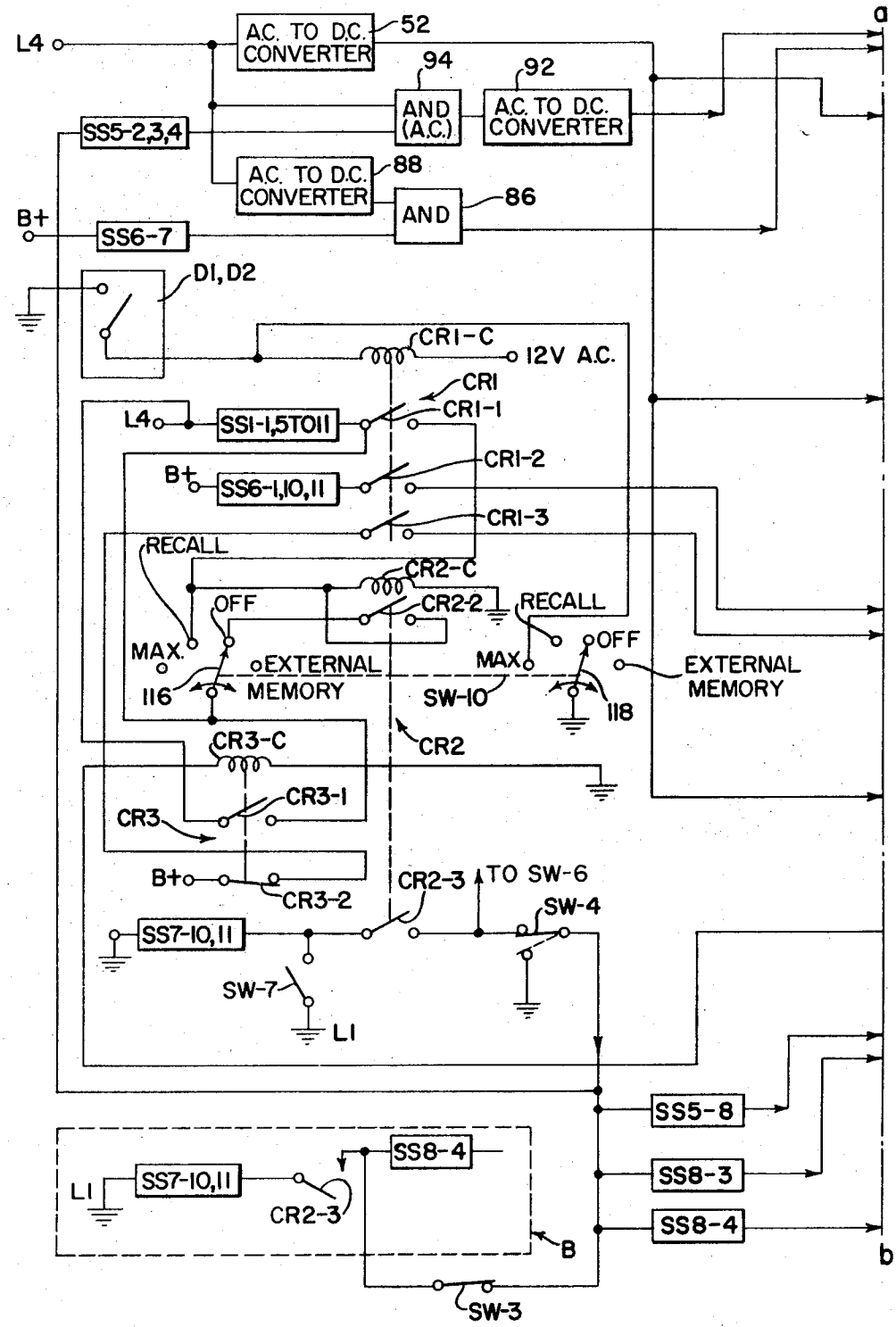


FIG. 3

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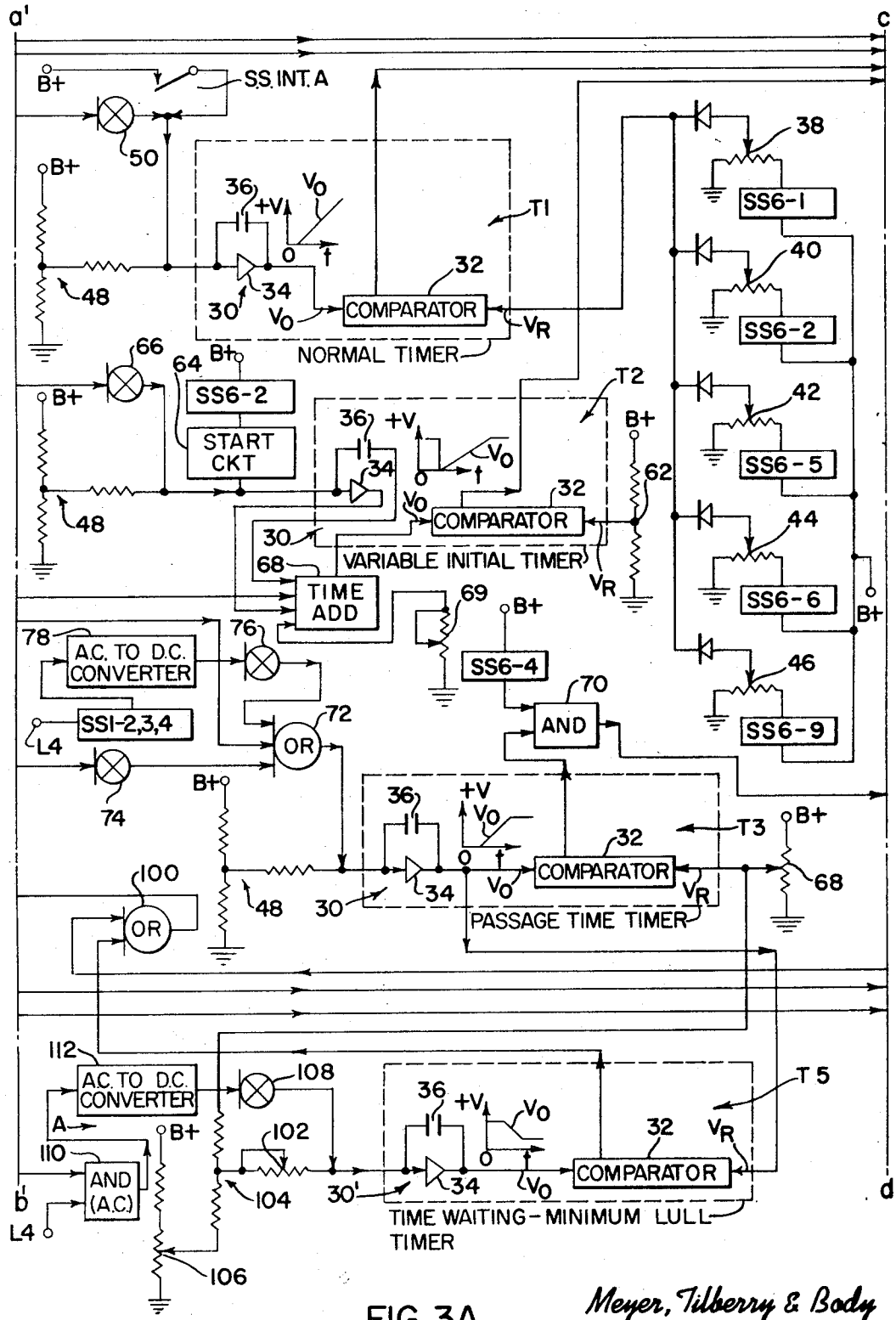


FIG. 3A

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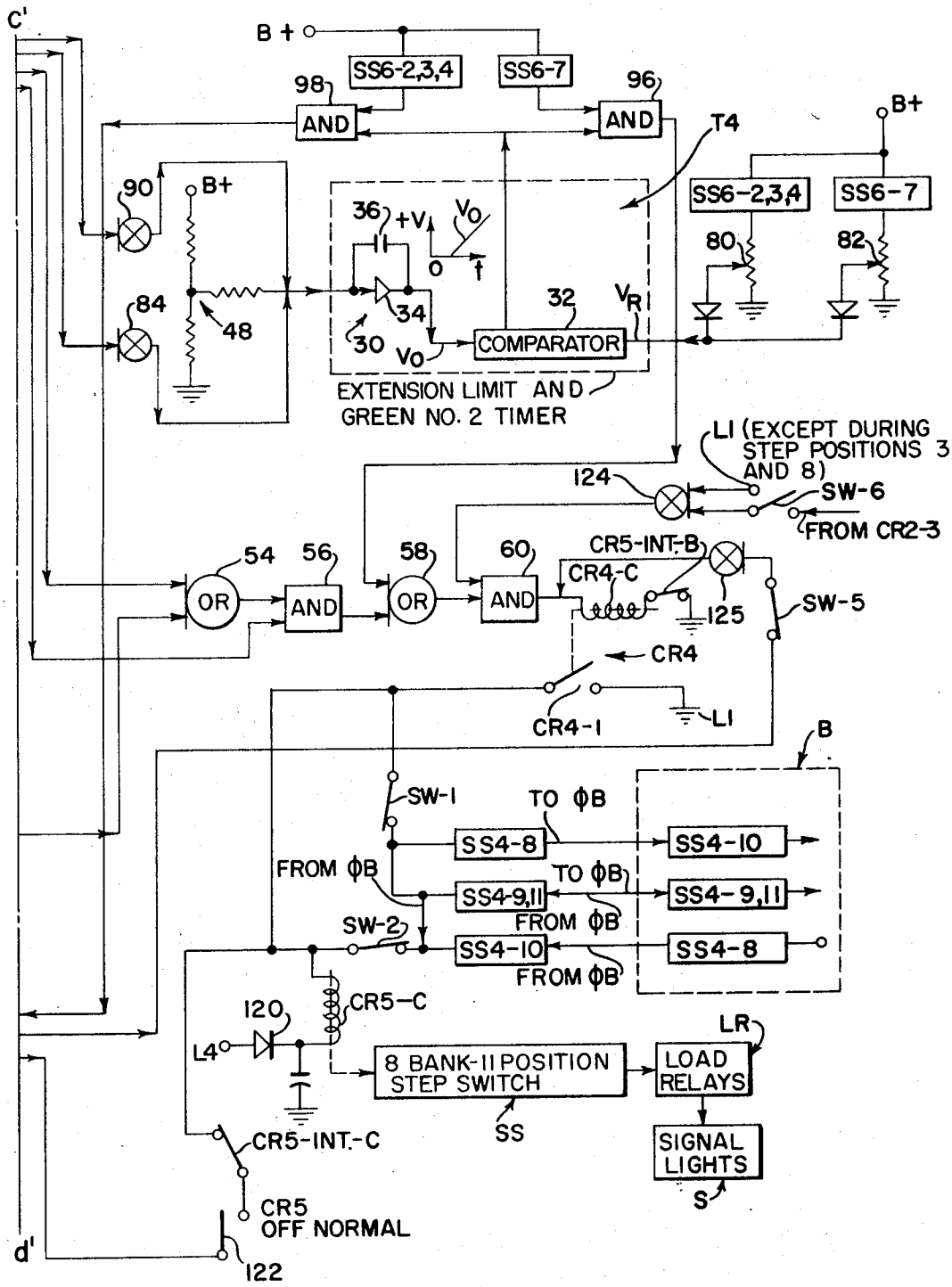


FIG. 3B

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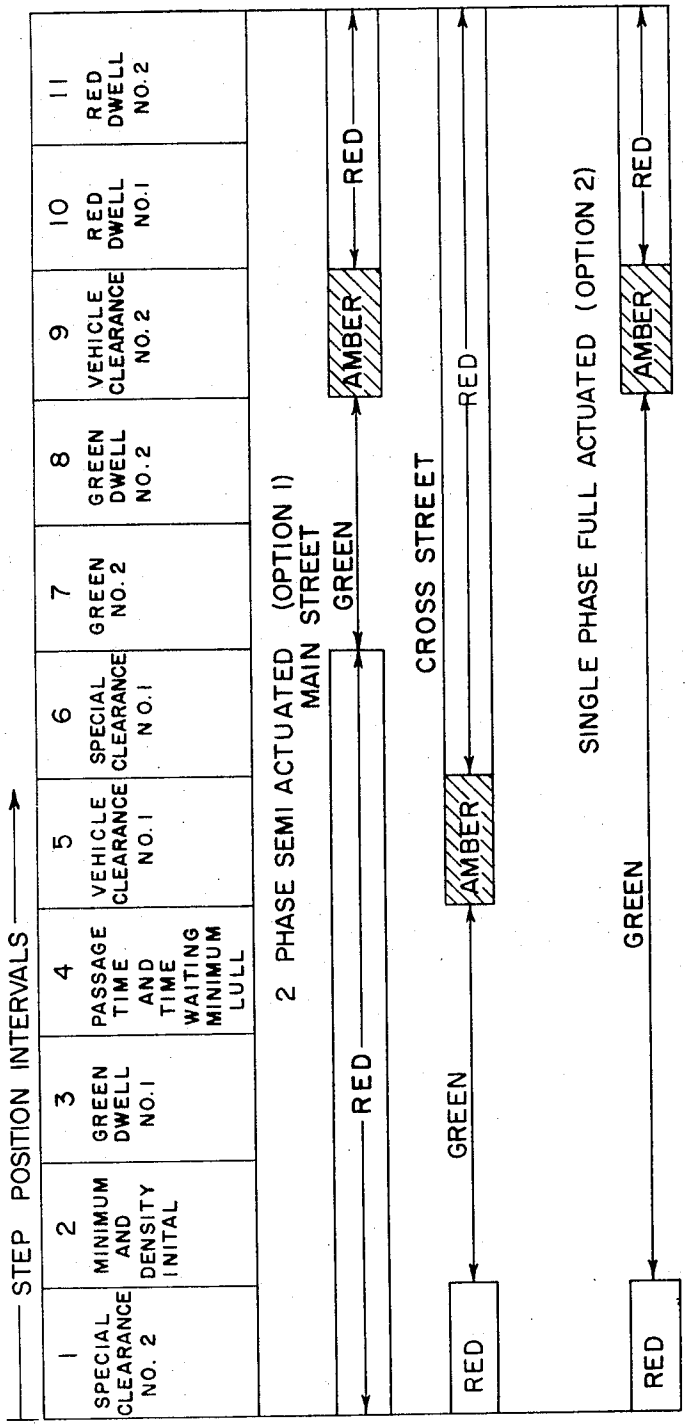


FIG. 4

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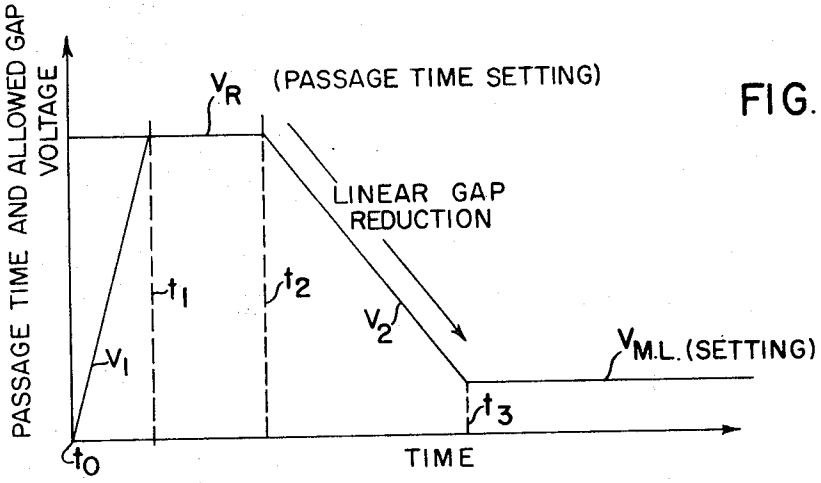


FIG. 5

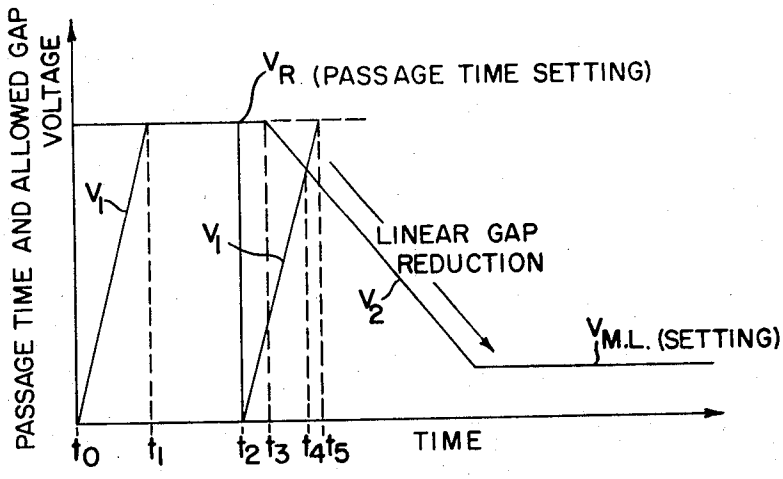


FIG. 6

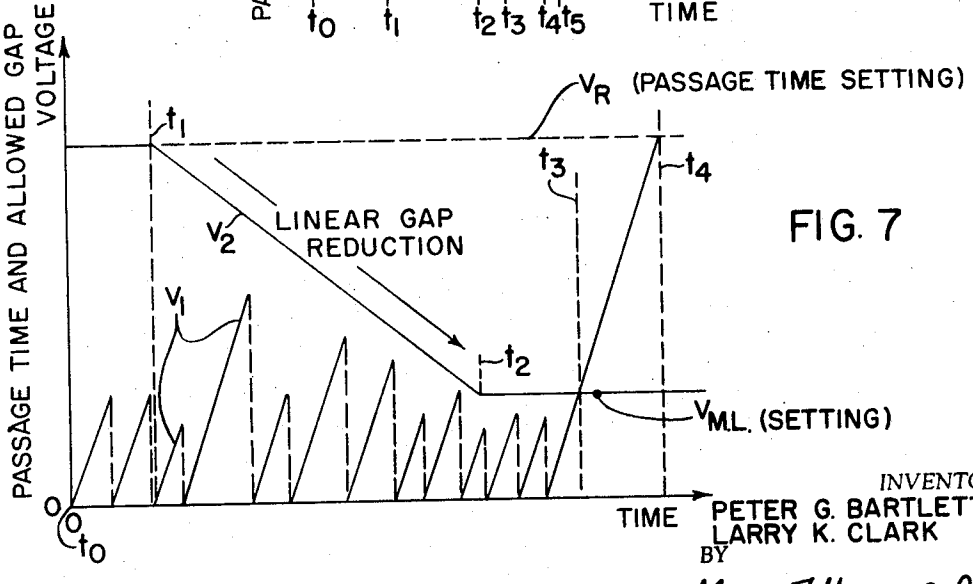


FIG. 7

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United States Patent Office 3,466,599 Patented Sept. 9, 1969

3,466,599

TRAFFIC CONTROLLER HAVING IMPROVED TIME WAITING-GAP REDUCTION CIRCUIT

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Filed Oct. 12, 1966, Ser. No. 586,127
Int. Cl. G08g 1/07
U.S. Cl. 340—37 15 Claims

This invention relates to the art of traffic control and, more particularly, to a traffic controller having an improved time waiting-gap reduction circuit.

The invention is particularly applicable in conjunction with a two or more phase, full actuated traffic controller and will be described with particular reference thereto; although, it is to be appreciated that the invention may be used in conjunction with various types of traffic controllers including, for example, a two phase, semiactuated traffic controller.

Traffic controllers having time waiting-gap reduction circuits are known in the art of traffic control. One purpose of such a circuit is to effect a change in right-of-way signals allocated to two intersecting traffic phases as a function of the elapsed time a vehicle is waiting (known as the time waiting period) on the phase which is denied right-of-way movement, as well as the actual time gap between successive vehicles in the phase to which right-of-way is allocated. Generally, when the actual time gap exceeds a predetermined or reference time gap and/or after a predetermined time waiting period has elapsed, a change in allocation of right-of-way is initiated. Provisions may be made for last car passage time to permit the last vehicle in the phase having right-of-way to reach the intersection before that phase is denied right-of-way movement.

Various aspects of such time waiting-gap reduction circuits are disclosed in C. L. DuVivier's United States Patent Nos. 3,234,505; 3,241,108; and, 3,241,109. The most pertinent disclosure of these patents, with respect to the present invention, is believed to be Patent No. 3,241,109. That patent discloses an actual gap timing circuit which is reset by each vehicle detection occurring in an associated traffic phase so as to time the actual gap time between successive vehicles in that phase; a time waiting circuit for timing the period that a vehicle is waiting for right-of-way movement on the phase to which right-of-way movement is denied; and, a comparator circuit for comparing potentials representative of the actual gap time and the time waiting period and then initiating a change in allocation of right-of-way movement when the two potentials are substantially of equal value.

The actual gap timing circuit disclosed in Patent No. 3,241,109 incorporates a capacitor which is charged in a somewhat linear manner so that the actual gap time that is timed by the timer is represented by the value of the stored voltage which increases with elapsed time. However, the time waiting circuit disclosed in that patent incorporates an RC timing circuit, wherein the time waiting period is represented by the value of the stored voltage of an exponentially charged timing capacitor. Accordingly, at most, this patent discloses a comparison of a somewhat linear function (actual gap time) with an exponential function (time waiting time). Thus, the point in time that the potential representative of the actual gap time and the potential representative of the time waiting time are substantially equal in value and cannot be accurately predicted from cycle to cycle during the operation of the traffic controller.

The present invention is directed toward a traffic controller having an improved time waiting-gap reduction circuit, wherein both the actual gap time and the time waiting time are represented by linear functions, whereby the point in time that the two functions are substantially equal in value is accurately predictable, thereby overcoming the noted disadvantages, as well as others, of previous controllers having time waiting-gap reduction circuits.

The present invention contemplates a traffic controller for controlling allocation of go and stop signals to at least two intersecting traffic phases, means for detecting vehicles in at least one of said phases during the period of time that a stop signal is allocated to the other phase, and a time waiting-gap reduction circuit for initiating a change in allocation of the go and stop signals to the phases as a function of the time waiting time on the other phase and the actual gap time between successive vehicles on the first phase.

In accordance with the present invention, the improved time waiting-gap reduction circuit includes a passage timer having means for developing a first signal which progressively varies in a linear manner with elapsed time between successive vehicle detections, and a time waiting timer having means for developing a second signal which progressively varies in a linear manner with elapsed time during the period that a vehicle is waiting on the phase to which a stop signal is displayed, and means for comparing the first and second signals and developing a go terminating signal when the first and second signals attain a predetermined relationship with respect to each other.

In accordance with a more limited aspect of the present invention, the passage timer and time waiting timer respectively develop the first and second signals as voltage potentials, which linearly vary in value with elapsed time.

Still further in accordance with the invention, the passage timer and time waiting timer develop the actual gap time and time waiting signals as voltage potentials which linearly vary in value toward that of each other with elapsed time, so that after a given period of time the potentials are of substantially equal value.

The primary object of the present invention is to provide an improved time waiting-gap reduction circuit, wherein both the actual gap time and time waiting time are represented by linear functions so that the point in time that the two functions attain a predetermined relationship with respect to each other is accurately predictable from cycle to cycle during the operation of the controller.

It is a still further object of the present invention to provide an improved time waiting-gap reduction circuit which is relatively simple in construction and economical to manufacture.

It is still a further object of the present invention to provide an improved time waiting-gap reduction circuit incorporating solid state components thereby decreasing power requirements for economy of operation.

It is a still further object of the present invention to provide an improved time waiting-gap reduction circuit incorporating linear timers which exhibit output potentials which linearly vary with elapsed time.

A still further object of the present invention is to provide an improved time waiting-gap reduction circuit incorporating linear timers which are less susceptible to transients and therefore more repeatable and accurate in operation than previous time waiting-gap reduction circuits incorporating RC timers.

In accordance with a still further object of the present invention, there is provided a time waiting-gap reduction circuit which incorporates timer circuits which do not charge a capacitor in an exponential manner and, accordingly, do not require large timing capacitors with resultant difficulties in attaining temperature compensation without the use of expensive components.

These and other objects and advantages of the invention will become apparent from the following description of the preferred embodiment of the invention as read in connection with the accompanying drawings in which:

FIGURE 1 is a schematic illustration of a typical intersection to which the present invention may be applied;

FIGURE 2 is a schematic circuit of the preferred embodiment of the invention;

FIGURES 3, 3A and 3B are a block diagram of a traffic controller incorporating the preferred embodiment of the invention illustrated in FIGURE 2;

FIGURE 4 is a chart illustrating traffic intervals corresponding with step switch positions; and,

FIGURES 5, 6, 7 and 8 are charts illustrating various aspects of the operation of the invention.

TRAFFIC CONTROLLER

Referring now to FIGURES 1, 3 and 4 wherein the showings are for purposes of illustrating a preferred embodiment of the invention only, and not for limiting same, there is illustrated in FIGURE 1 a typical intersection of two traffic phases, phase A and phase B. Adjacent the intersection of the two phases there is schematically illustrated stop lines SL which may be located as desired by municipal traffic engineers. At each approach to the intersection there is provided a detector, i.e., detectors D1 and D2 for the approaches of phase A, and detectors D3 and D4 for the approaches of phase B. Detectors D1, D2, D3 and D4 preferably take the form of loop detectors, which are well known in the art of traffic control, and generally comprise a closed wire loop embedded in a roadway, with the loop configuration defining an area under surveillance by the detector, which together with associated circuitry develops an output signal so long as a vehicle is present within the area under surveillance. Alternatively, detectors D1, D2, D3 and D4 may take the form of other detectors, such as overhead mounted ultrasonic detectors which, in a manner similar to that of loop detectors, serve to monitor or survey a predetermined area on the roadbed for the presence of vehicles and provide an output signal as long as a vehicle is present in the area under surveillance. Further, the detectors may also take the form of spot detectors, such as the familiar tread pad, which together with its associated circuitry provides an output signal in response to each actuation by a vehicle momentarily passing over the spot detector. In the event that the detectors take the form of loop detectors, as shown in FIGURE 1, it is preferable that each detector, as illustrated with respect to detector D3 in FIGURE 1, have a width w which is sufficiently wide to detect vehicles in all of the lanes in the approach to the intersection; a length l which extends in the direction of the phase for a distance less than the length of one vehicle, such as, for example, on the order of four feet; and, be located at a distance d from the stop line, which distance may be on the order of two-hundred feet. The detectors D1, D2, D3 and D4 are connected to a local controller LC, which controls the operation of an intersection traffic signal S which displays go, caution and stop signals to phases A and B. Preferably, in accordance with the present invention, loop detectors D1 and D2 are connected to a phase control unit A for controlling the signal displays by traffic signal S to phase A and detectors D3 and D4 are connected to phase control unit B for controlling the signal displays by traffic signal S to phase B.

The traffic controller to be described hereinafter takes the form of a two phase, full actuated, traffic controller including a phase control unit for each traffic phase. The invention is not limited to such a traffic controller but may be used with other controllers, such as, for example, a semiactuated, two phase, traffic controller or a two or more phase, full actuated, traffic controller wherein all of the control circuitry is included within a given unit as opposed to phase control units described with reference to FIGURE 3.

As shown in FIGURE 1, local controller LC includes two phase control units A and B for respectively controling phase A and phase B traffic flow. Phase control units A and B are substantially identical and, accordingly, only phase unit A is described hereinafter in detail, it being understood that the description applies equally to phase unit B.

Referring now to FIGURE 3, phase unit A generally comprises five timers; namely, a normal timer T1, a variable initial timer T2, a passage time timer T3, an extension and green No. 2 timer T4, and a time waiting-minimum lull timer T5; and, an eight bank, eleven position step switch SS for controlling the operation of the phase A signal lights of traffic signal S through load relays LR in response to actuation of the phase A vehicle detectors D1, D2.

As will become evident from the description that follows, phase control unit A includes various TIMER circuits, NOR circuits, AND circuits, OR circuits, and (A.C.) circuits. To facilitate the understanding of this invention, each of these circuits is briefly explained below.

TIMER circuit.—This is a static, solid state means timing circuit having an input circuit and an output circuit. Upon application of the ground potential signal, known as a (0) signal, the timer commences its timing function and upon completion thereof develops at its output circuit a positive potential signal, known as a (1) signal.

NOR circuit.—This is a static, solid state means circuit having one or more input circuits and one output circuit. A (0) signal is present at its output circuit whenever a (1) signal is applied to any of its input circuits. If a (0) signal is present on all of its input circuits, a (1) signal is present on its output circuit.

AND circuit.—This is a direct current static, solid state means circuit having two or more input circuits and one output circuit. A (1) signal is present at its output circuit so long as all of its input circuits receive a (1) signal. If a (0) signal is present at any of its input circuits, a (0) signal is present at its output circuit.

OR circuit.—This is a static, solid state means circuit having two or more input circuits and one output circuit. A (1) signal is present at its output circuit so long as any of its input circuits receive a (1) signal.

AND (A.C.) circuit.—This is a static, solid state means circuit, such as a transformer, having two input circuits and an output circuit which serves to develop an alternating current output signal at its output circuit only when one of its inputs is connected to ground potential and the other of its inputs is connected to the hot side of an alternating current voltage source.

STEP SWITCH

Step switch SS preferably takes the form of an eight bank, eleven position step switch. If desired, the step switch may take the form of an electronic ring counter having the capability of cyclically stepping through eleven positions. As is well known to those skilled in the art, step switch SS cyclically steps through eleven positions, during which various circuits are completed by means of load relays LR for energizing the traffic signal lights S. Various load relay combinations may be made in accordance with a traffic engineer's schedule. From FIGURE 4 it will be noted that step position Nos. **1**, **2**, **3**, **4**, **5**, **6**, **7**, **8**, **9**, **10** and **11** are respectively the special clearance No. **2**, minimum and density initial, green dwell, passage time and time waiting-minimum lull, vehicle clearance No. **1**, special clearance No. **1**, green No. **2**, green dwell, vehicle clearance No. **2**, red dwell No. **1**, and red dwell No. **2** intervals. As will be noted in the description which follows, the phase unit illustrated in FIGURE 3 may be a single phase unit (option **2**) for controlling a single traffic actuated phase, or may be used as a semiactuated, two phase traffic controller (option **1**) for controlling main street in acordance with a pretimed schedule and cross street traffic flow in accordance with traffic demand.

The phase controller may be converted to a semiactuated traffic controller by opening normally closed switches SW–1, SW–2, SW–3, SW–4, SW–5 and closing normally open switches SW–6, SW–7. For semiactuated operation (option 1, see FIGURE 4), step switch intervals 10, 11 and 1 through 6 may be the main street red (stop) period, intervals 7 and 8 may be the main street green (go) period, and interval 9 may be the main street amber (caution) period. Also, step switch positions 6 through 11 and 1 may be the cross street red period, positions 2 through 4 may be the cross street green period, and position 5 may be the cross street amber period. With switches SW–1 through SW–7 in a position as shown in FIGURE 3, the circuit serves as a single phase, full actuated, phase control unit (option 2, see FIGURE 4) during which step positions 10, 11 and 1 serve as the actuated phase red (stop) period, step positions 2 through 8 serve as the actuated phase green (go) period, and step position 9 serves as the actuated phase amber (caution) period.

NORMAL TIMER

Normal timer T1, like timers T2, T3, T4, and T5, generally comprises a linear ramp function generator 30 and a differential amplifier circuit serving as a comparator circuit 32. Generator 30 and comparator circuit 32 are preferably constructed as disclosed in United States patent application, Serial No. 580,809, entitled "Electronic Timer Circuit," and filed on Sept. 20, 1966, in the names of Larry K. Clark and Peter G. Bartlett, which application is assigned to the same assignee as the present invention. Generator 30 includes a D.C. amplifier 34 and a negative feedback capacitor 36. Briefly, upon application of a (0) signal to the input circuit of generator 30, an output voltage V_0 appears at its output circuit, which potential linearly increases in value with elapsed time, as shown by the wave form adjacent generator 30 in FIGURE 3. The comparator 32 serves to compare the value of the linearly increasing output voltage V_0 with a reference voltage V_R and develop a positive direct current voltage output signal, known as (1) signal, when the value of the two potentials is substantially equal.

The reference voltage V_R applied to one of the input circuits of comparator 32 is obtained from one of five potentiometers 38, 40, 42, 44 and 46. Each of the potentiometers has its resistance connected between ground and the B+ voltage supply source through contacts on step switch SS. Accordingly, it is appreciated that the time delay required for the output voltage V_0 of generator 30 to reach the value of the reference voltage V_R is dependent on the adjustment of the particular potentiometer in effect during the appropriate step position.

As discussed above, the various potentiometers 38, 40, 42, 44 and 46 are connected through step switch contacts to the B+ voltage supply source. As is well known to those skilled in the art, each time that a step switch is energized, it steps one step to close one switch in each bank until the step switch is stepped to the next step position. Thus, for example, in step switch position 6 all normally open switch contacts on the eight banks in step position 6 are closed. Reference is now made to potentiometer 38 which has its resistance portion connected between ground and the B+ voltage supply source through normally open step switch contacts located at bank 6, position 1, referred to in the drawings as SS6–1. Similarly, potentiometer 40 is connected to the B+ voltage supply source through step switch contacts at bank 6, position 2, SS6–2. Similarly, potentiometers 42, 44 and 46 are respectively connected to the B+ voltage supply source through step switch contacts SS6–5, SS6–6 and SS6–9. It will be noted that these step switches are closed at different positions of the step switch, no two being closed at the same time. Thus, potentiometer 38 serves to adjust the time duration of special clearance No. 2 interval. Potentiometer 40 serves to adjust the time duration of the minimum initial interval, potentiometer 42 serves to adjust the time duration of vehicle clearance No. 1 interval, potentiometer 44 serves to adjust the time duration of special clearance No. 1 interval, and potentiometer 46 serves to adjust the time duration of a special clearance No. 2 interval. These step switch positions and traffic intervals are illustrated in the chart of FIGURE 4.

The input circuit of ramp function generator 30 is connected through a potential divider 48 to the B+ voltage supply source, as well as through a normally open interrupter contact S.S.INT.A to the B+ voltage supply source. Interrupter contacts A are located on the step switch and momentarily close each time that the step switch is stepped from one position to the next. Thus, each time the step switch is actuated a (1) signal, i.e., B+ voltage, is applied to the input circuit of generator 30 to reset the generator so that its output voltage V_0 is referenced to ground prior to commencing a timing operation.

The input circuit of the normal timer T1, taken at the input of generator 30, is connected to the output circuit of a NOR circuit 50, which, in turn, has its input circuit connected to a source of alternating current voltage L4 through an A.C. to D.C. converter 52. The alternating voltage source L4 is preferably the hot side of an alternating current voltage source, which has its other side connected directly to ground. The ground side of the alternating current voltage source will hereinafter be referred to either as ground or the L1 voltage supply source. The converter 52 serves to convert the alternating current voltage into a positive potential known as a (1) signal for application to NOR circuit 50 so that so long as there is no disruption in the voltage source L4, a (1) signal is applied to the input circuit of NOR circuit 50, whereupon a (0) signal is applied from the output circuit of NOR circuit 50 to the input circuit of timer T1. The output circuit of timer T1, as taken at the output circuit of comparator circuit 32, is connected to the input circuit of an OR circuit 54, having its output circuit connected to the input circuit of an AND circuit 56. The output circuit of AND circuit 56 is connected to an input circuit of an OR circuit 58 having its output circuit connected to the input circuit of another AND circuit 60. The output circuit of AND circuit 60 is connected to ground through relay coil CR4–C of a control relay CR4.

VARIABLE INITIAL TIMER

The variable initial timer T2 is substantially identical to normal timer T1 and, accordingly, like components are identified in FIGURE 3 with like reference characters. The variable voltage V_R for comparator circuit 32 of timer T2 is taken from a voltage divider 62 connected between ground and the B+ voltage supply source. The output circuit of the timer, as taken from the comparator circuit 32, is connected to an input circuit of AND circuit 56. The input circuit of timer T2 is connected to a B+ voltage supply source through a START circuit 64 and normally open step switch contacts SS6–2 at step switch bank 6, position 2. The input circuit of timer T2 is also connected to the output circuit of a NOR circuit 66, which in turn has its input circuit connected to the output circuit of A.C. to D.C. converter 52. The variable initial timer serves to time a variable period of time in accordance with the number of actuations of phase A vehicle detectors D1, D2 and this function is provided by means of a time add circuit 68 connected to the input circuit of amplifier 34. The time add circuit is adjusted by a potentiometer 69 and has its input circuit connected to the B+ voltage supply source through normally open relay contacts CR1–2 of relay CR1, and step switch normally open contacts SS6–1, 10, 11 so that whenever contacts CR1–2 are closed, during step positions 1, 10 and 11, B+ potential is applied to the time add circuit. Preferably, the variable initial timer is set so that it pro-

vides a time increment between one and five seconds for each vehicle actuation.

PASSAGE TIME TIMER

The passage time timer T3 is substantially identical to the normal timer T1 and, accordingly, like components are identified by like reference numerals in FIGURE 3. The passage time timer serves upon actuation to time a passage time, otherwise known as a unit extension time, which is the time required for a vehicle to traverse the distance from the phase A vehicle detectors D1, D2 to the stop line SL at the intersection (see FIGURE 1). This time is normally set in the range from 0 to 30 seconds, according to a traffic engineer's schedule. The reference voltage V_R for comparator circuit 32 of timer T3 is obtained from an adjustable passage time potentiometer 68. The output circuit of the timer is taken from the output circuit of comparator 32 and is connected to the input circuit of an AND circuit 70, having a second input taken from the B+ voltage supply source through normally open step switch contacts SS6–4. The output circuit of AND circuit 70 is connected to the input circuit of OR circuit 54.

The input circuit of timer T3, as taken at the input circuit of the ramp function generator 30, is connected to the output circuit of an OR circuit 72. The input circuit of OR circuit 72 includes one input connected to the output circuit of NOR circuit 74, which in turn has its input circuit connected to the output circuit of the A.C. to D.C. converter 52. A second input circuit of OR circuit 72 is connected to the output circuit of a NOR circuit 76, which in turn has its input circuit connected through an A.C. to D.C. converter 78 to the L4 voltage supply source by means of normally open step switch contacts SS1–2, 3, 4. A third input circuit of OR circuit 72 is connected through normally open relay contacts CR1–3 of relay CR1, to the B+ voltage supply source, through normally closed relay contacts CR3–2 of relay CR3.

EXTENSION LIMIT AND GREEN NO. 2 TIMER

The extension limit and green No. 2 timer T4 is substantially identical to the normal timer T1 and, accordingly, like components are identified with like reference characters in FIGURE 3. The reference voltage V_R for the comparator circuit 32 of timer T4 is obtained in step positions 2, 3, and 4 from the B+ voltage supply source through potentiometer 80 and normally open step switch contacts SS6–2, 3, 4. In step position 7, the reference voltage V_R is obtained from the B+ voltage supply source through potentiometer 82 and normally open step switch contacts SS6–7. Potentiometer 80 serves to adjust the maximum duration of the extension limit period and potentiometer 82 serves to adjust the time duration of the green No. 2 interval (see FIGURE 4).

The input circuit of timer T4, as taken at the input circuit of linear ramp function generator 30, is connected to the output circuit of a NOR circuit 84, having its input circuit connected to the output circuit of an AND circuit 86. One input circuit to AND circuit 86 is connected to the B+ voltage supply source through normally open step switch contacts SS6–7. The other input circuit for AND circuit 86 is connected through an A.C. to D.C. converter 88 to the alternating current voltage supply source L4.

The input circuit of timer T4 is also connected to the output circuit of a NOR circuit 90, having its input circuit connected to the output circuit of an A.C. to D.C. converter 92. The input circuit of the converter 92 is in turn connected to the output circuit of an AND (A.C.) circuit 94. AND circuit 94 may take the form of a transformer having its secondary winding connected to converter circuit 92 and its primary winding serving as an input circuit, with one end of the primary winding being connected to the alternating current voltage source L4 and the other end of the primary winding being connected to ground through step switch contacts SS5–2, 3, 4, a normally closed switch SW–3 and, in phase unit B through normally open relay contacts CR2–3 (which correspond with the like numbered contacts in phase unit A), and thence through the phase B step switch contacts SS7–10, 11. This portion of the circuitry of phase unit B is shown in FIGURE 3 only for purposes of clarifying the manner of interconnection of phase units A and B.

The output circuit of timer T4, taken at the output circuit of comparator 32, is connected to one input circuit of an AND circuit 96, having another input circuit connected to the B+ voltage supply source through normally open switch contacts SS6–7. The output circuit of AND circuit 96 is connected to an input circuit of OR circuit 58. The output circuit of timer T4 is also connected to the input circuit of another AND circuit 98, having a second input circuit connected to the B+ voltage supply source through normally open step switch contacts SS6–2, 3, 4. The output circuit of AND circuit 98 is connected to one input circuit of an OR circuit 100. The output circuit of OR circuit 100 is connected to ground through relay coil CR3–C of relay CR3.

TIME WAITING-MINIMUM LULL TIMER

The time waiting-minimum lull timer T5 is substantially identical to the normal timer T1 and, accordingly, like components in both circuits are identified with like reference characters in FIGURE 3. A major distinction, however, between timer T5 and the normal timer T1 is that the generator 30′ of timer T5 is the complement of generator 30 in timer T1. That is, as will be noted from a comparison of the wave forms associated with the circuitry of timer T1 or T5, the value of output voltage V_o of timer T1 linearly increases in a positive direction with elapsed time, whereas the value of output voltage V_o of timer T5 linearly decreases toward ground potential with elapsed time. The reference voltage V_R for comparator circuit 32 of timer T5 is taken from the output circuit of generator 30 in timer T3 so that the reference voltage V_R is equal to the value of output voltage V_o of generator 30 in timer T3. Accordingly, timer T5 serves to compare the linearly decreasing voltage V_o from generator 30′ with the linearly increasing reference voltage V_R, taken from the generator 30 of timer T3.

The input circuit of timer T5, as taken at the input circuit of generator 30′, is connected through a time waiting adjustable potentiometer 102 to the junction of a potential divider 104. The potential divider 104 is connected between the wiper arm of potentiometer 68 of timer T3, and the wiper arm of a minimum lull adjustable potentiometer 106, which in turn is connected between ground and the B+ voltage supply source.

The input circuit of timer T5 is also connected to the output circuit of a NOR circuit 108, having its input circuit connected to the ouput circuit of an A.C. to D.C. converter 112. Converter 112 is connected to the output circuit of an AND (A.C.) circuit 110. One of the input circuits of AND (A.C.) circuit 110 is connected to power source L4 and the other of its input circuits is connected through normally open step switch contacts SS8–4, normally closed switch SW–3, and in the phase B phase control unit through normally open relay contacts CR2–3 and, thence, through step switch contacts SS7–10, 11 to ground.

RELAY CIRCUITS

To some extent, the description given hereinabove with respect to the timers T1, T2, T3, T4 and T5 has included description as to the circuit interconnection with relays CR1, CR2 and CR3. Relay CR1 may be termed as the vehicle detection relay and includes relay coil CR1–C which is connected between a 12 volt alternating current voltage source, labeled as 12V–A.C. in FIGURE 3, and ground through phase A detectors D1, D2 which are illustrated in the circuit as a normally open switch. Relay

CR1 includes normally open relay contacts CR1–1, CR1–2 and CR1–3. These contacts have been discussed hereinbefore with respect to their interconnection with the timer circuits. In addition to the interconnections previously described with respect to the timer, it will be noted from FIGURE 3 that contacts CR1–1 are connected to ground through relay coil CR2–C of memory relay CR2. Relay CR2 also includes normally open relay contacts CR2–2 and CR2–3. Relay CR3, which includes relay coil CR3–C connected between the output circuit of OR circuit **100** and ground, also includes normally open relay contacts CR3–1 and normally closed relay contact CR3–2. In addition, the relay circuits also interconnect with a recall switch SW–10, which includes a pair of ganged movable contacts **116** and **118**. Movable contacts **116** and **118** are four position contacts, and may be positioned in either one of four positions; namely, maximum, recall, off, and external memory. In the off position, contact **116** serves together with relay contacts CR2–2 to provide a shunt circuit across normally open detector relay contacts CR1–1. Thus, whenever relay coil CR1–C is energized, to energize relay coil CR2–C (when in step positions **1** and **5** through **11**), relay contacts CR2–2 close to provide a shunt path across contacts CR1–1 to maintain relay coil CR2–C energized. With switch SW–10 in its recall position, movable contact **116** connects relay coil CR2–C between ground and the alternating current voltage source L4 (in step positions **1** and **5** through **11**) to maintain the memory coil in a constant recall condition. When switch SW–10 is in its maximum position, movable contact **118** connects detector relay coil CR1–C between ground and the 12 volt alternating current voltage source so as to constantly energize the detector relay coil. When switch SW–10 is in its external memory position, the memory function is performed by external memory means such as a presence detector which, as described hereinbefore, provides an output signal so long as a vehicle is present within its zone of influence. In addition to the foregoing, it will be noted that relay contacts CR3–1 serve, when closed, to provide a shunt between voltage source L4 and relay contacts CR1–1. Also, memory relay contacts CR2–3 serve, when closed during step positions **10** and **11**, to provide a vehicle calling signal, representative that a vehicle on phase A demands right-of-way movement through the intersection, to the phase B phase control unit through normally closed switch SW–3.

STEP SWITCH DRIVER CIRCUIT

The step switch driver circuit includes relay coil CR4–C, of relay CR4, in the output circuit of AND circuit **60**. Relay CR4 includes a set of normally open contacts CR4–1 which serve to connect a step switch driver coil CR5–C between the alternating current voltage source L4 and ground through diode **120**. The step switch SS is driven one step, in a manner well known in the art, in response to each energization of driver coil CR5–C. The step switch is driven from step position **3** to step position **4** when a circuit is completed across coil CR5–C from the alternating current voltage source L4 through normally closed interrupter contacts CR5–INT–C, off normal contact **122**, normally open step switch contacts SS8–3, normally closed switch SW–3, normally open relay contacts CR2–3 (in phase unit B) and normally open phase B step switch contacts SS7–10, **11** to ground. The off normal contacts **122** are controlled by the step switch and are normally open, except in step position **3**. The normally closed interrupter contacts CR5–INT–C are controlled by driver coil CR5–C and are open during the period that the coil is energized.

The input circuit of AND circuit **60** is connected to the output circuit of a NOR circuit **124**. One of the input circuits of NOR circuit **124** is connected to a source of L1 power (ground) except during step positions **3** and **8**. The step switch SS is stepped from its step position **3** to its step position **4** by the circuit described above with respect to the off normal contacts **122** and the interrupter contacts CR5–INT–C. The following description is given with respect to the circuit that is used for stepping the step switch SS from step position **8** to step position **9**. This circuit includes a path taken from an input circuit of another NOR circuit **125**, having its output connected to relay coil CR4–C, through normally closed switch SW–5, normally open step switch contacts SS5–8 and, thence, through normally closed switch SW–3 and into the phase B control unit through normally open relay contacts CR2–3 and step switch contacts SS7–10, **11** to the L1 power source, i.e., ground. Accordingly, it is seen that the step switch cannot be stepped out of its step positions **3** or **8** unless relay contacts CR2–3 in the phase B control unit are closed, representative of a vehicle demanding right-of-way movement on phase B. A second input circuit for NOR circuit **124** is taken through normally open switch SW–6 (which is closed only for semi-actuated operation) and thence to the junction between normally closed switch SW–4 and relay contacts CR2–3.

In local controller LC, which includes phase units A and B for controlling phase A and phase B traffic flow, the phase unit associated with the traffic phase to which a stop signal is displayed normally dwells in red dwell No. **1** interval, at step position **10** (see FIGURE 4). When the phase unit associated with the phase to which a go signal is displayed is stepped from step position **8** to step position **9**, it is desirable that the other phase unit be stepped from step position **10** to step position **11**. Similarly, when the phase unit in control is stepped from step position **9** to step position **10**, the other phase unit is stepped from red dwell No. **2** interval, at step position **11**, to step position **1**. The circuit for accomplishing this function is described below. Normally closed switch SW–1 is connected from the junction of coil CR5–C and relay contacts CR4–1 to normally open phase A step switch contacts SS4–8, and thence to phase B step switch contacts SS4–10. Similarly, switch SW–1 is connected through phase A step switch contacts SS4–9, **11**, and thence to phase B step switch contacts SS4–9, **11**. Switch SW–2 serves to connect the junction of switch SW–1 and coil CR5–C through phase A step switch contacts SS4–10 to the phase B step switch contacts SS4–8. Also, switch SW–2 is connected through phase A step switch contacts SS4–9, **11** to phase B step switch contacts SS4–9, **11**. The operation of these circuits will be appreciated from the detailed description which follows.

OPERATION

Phase A, step position 10.—A cycle of operation for phase unit A of local controller LC commences, for example, when phase unit A is in its red dwell No. **1** interval, i.e., step position **10**. When phase B is stepped from its step position **8** to its step position **9**, L1 power is applied from phase unit B through now closed step switch contacts SS4–8, through now closed phase A step switch contacts SS4–10, and thence through switch SW–2 to complete an energizing circuit for phase A step switch coil CR5–C. Accordingly, this steps the step switch SS in phase unit A from step position **10** to step position **11**, the phase A red dwell No. **2** interval. Simultaneously therewith, the phase B step switch is stepped from its step position **8** to its step position **9**, as will be appreciated from the description which follows with reference to phase unit A.

Phase A, step position 11.—After phase unit B has timed its vehicle clearance No. **2** interval, i.e., step position **9**, L1 power is applied from phase unit B through its now closed step switch contacts SS4–9, through the now closed phase A step switch contacts SS4–11, and thence through switch SW–2 to complete an energizing circuit for phase A step switch coil CR5–C. Thus, the phase A step switch SS is stepped from its step position **11** to step position **1**, the phase A special is above ground potential, i.e., close to B+ potential. Accordingly, in the absence of timer T2 being reset, an output signal, i.e., a (1) signal, is applied from the output circuit of comparator **32**

of timer T2 to the AND circuit 56. AND circuit 56 applies a (1) signal through OR circuit 58 to the input circuit of AND circuit 60. AND circuit 60, in turn, receives a second (1) signal from the output circuit of NOR circuit 124, except during step positions 3 and 8. Thus, a (1) signal is applied from the output circuit of AND circuit 60 to energize control relay coil CR4–C. This closes relay contacts CR4–1, completing an energizing circuit for step switch coil CR5–C. The step switch SS steps from its step position 1 to step position 2, the minimum and density initial interval.

Phase A, step position 2.—As shown in FIGURE 4, step position 2 is a go or green signal interval for phase A traffic. At the commencement of this interval circuits are completed for energizing normal timer T1, the extension limit timer T4, the variable initial timer T2, the passage time timer T3, and relay coil CR3–C. The operation with respect to each of these circuits is described below.

Upon advancement into the minimum initial interval, timer T1 is reset by step switch interrupter contacts SS–INT–A and the timer then commences its timing function. The reference voltage V_R is obtained from potentiometer 40 during step position 2 since normally open stepping switch contacts SS6–2 are now closed. When the output voltage V_0 of generator 30 is substantially equal to the reference V_R a (1) signal is applied through OR circuit 54 to the input circuit of AND circuit 56. AND circuit 56, however, does not apply a (1) signal to OR circuit 58 until a (1) signal is developed by the output circuit of variable initial timer T2. In step position 2, clearance No. 2 (stop) interval. As will be appreciated from the description which follows, phase unit B is also stepped from its step position 9 to its step position 10, the red dwell No. 1 interval, where the phase B unit dwells until it becomes traffic actuated. Phase unit A is now in control.

Phase A, step position 1.—In step position 1, phase A normal timer T1 times a fixed special clearance No. 2 interval, illustrated as a red or stop interval in FIGURE 4. The time duration of this interval is determined by the value of the reference voltage V_R applied to comparator 32, as adjusted by potentiometer 38. As the step switch was stepped into step position 1, step switch interrupter contacts SS–INT–A momentarily closed to apply B+ potential, i.e., a (1) signal, to the input circuit of timer T1. This resets the timer so that as the switch reopens an energizing (0) signal is applied to the timer. In the event that the L4 power source fails, a (1) signal is applied from NOR circuit 50 to the input circuit of timer T1, to constantly maintain the timer reset. In the absence of such power failure, however, timer T1 commences its timing function as the step switch steps to position 1. Accordingly, the output voltage V_0 of generator 30 in timer T1 linearly increases until such time that the value of voltage V_0 is substantially that of the reference voltage V_R, whereupon a (1) signal is applied from the output circuit of comparator 32 to the input circuit of OR circuit 54. The OR circuit applies a (1) signal to the input circuit of AND circuit 56. The AND circuit 56, however, requires a second (1) input signal from the output circuit of comparator circuit 32 of timer T2 before it applies a (1) signal to OR circuit 58. As shown by the wave form associated with generator 30 of timer T2, the output voltage V_0 is normally set so that its START circuit 64 associated with timer T2 is initiated to actuate timer T2 to commence its timing function. The minimum value of voltage V_0 is adjusted by the time add circuit 68 so as to vary the time required for the output voltage V_O to be substantially equal to the reference voltage V_R. The greater the minimum value of voltage V_0, the lesser the time required to obtain an output (1) signal from timer T2 and, conversely, the lesser the minimum value of voltage V_0, the greater the time required for timer T2 to develop an output (1) signal. The time add circuit 68 receives a B+ signal during step positions 1, 10 and 11 for each closure of vehicle detector relay contacts CR1–2. Accordingly, the variable initial time is proportionally increased in accordance with the number of vehicles detected during the preceding period that a stop signal was displayed to phase A traffic. The variable initial timer may be set by potentiometer 69 to provide approximately five seconds for each vehicle detection. When timer T2 completes its timing function, it applies a (1) signal to the input circuit of AND circuit 56, whereupon the AND circuit applies a (1) signal through OR circuit 58 to the input circuit of AND circuit 60. Since a (1) signal is applied to AND circuit 60 from the output circuit of NOR circuit 124, except during step positions 3 and 8, a (1) signal is applied to energize control relay coil CR4–C, thereby completing an energizing circuit for step switch driver coil CR5–C. Thus, the step switch SS is stepped from step position 2 to step position 3, the green dwell interval.

At the commencement of step position 2, a circuit is also completed for energizing the passage time timer T3. More particularly, in step positions 2, 3 and 4 a circuit is completed from the alternating current voltage source L4 through step switch contacts SS1–2, 3, 4, and thence through the A.C. to D.C. converter 78 for developing a (1) signal for application to NOR circuit 76. Accordingly, NOR 76 applies a (0) signal through OR circuit 72 to the input circuit of timer T3. Also, so long as there is not a failure of L4 power, a (0) signal is applied by NOR circuit 74 through OR circuit 72 to the input circuit of timer T3. Thus, the passage time timer commences its timing function so as to time at least one passage time, as adjusted by potentiometer 68. The passage time timer may be reset by vehicle actuations in phase A, since for each actuation relay coil CR1–C is energized to close its contacts CR1–3. Closure of contacts CR1–3 applies a (1) signal from the B+ voltage supply source through normally closed relay contacts CR3–2 to OR circuit 72. This momentary application of a (1) signal through OR circuit 72 resets timer T3 so that it commences to time a second passage time. When the passage time timer completes its timing function, a (1) signal is developed at its output circuit for application to AND circuit 70. However, a (1) signal is not applied from the output circuit of AND circuit 70 to the input circuit of OR circuit 54 in any step switch position other than step switch position 4. Accordingly, if passage time timer completes its timing function in interval 2 or 3, this will not actuate the step switch SS.

During light traffic conditions, the variable initial timer T2 may time out before the normal timer T1 completes its timing function. During heavy traffic conditions, however, the variable initial timer T2 may require considerable time to complete its timing function after the normal timer T1 has timed out. Thus, the phase A traffic would maintain right-of-way to the detriment of the phase B traffic. The extension limit portion of timer T4 serves to time a maximum period of go time for phase A traffic, after a vehicle on phase B has registered its demand for right-of-way movement through the intersection. More particularly, any time during phase A step positions 2, 3 and 4 a circuit is completed for energizing timer T4 when a vehicle actuation has occurred on phase B. Thus, when relay contacts CR2–3 in phase B become closed, representative of a vehicle actuation in phase B during phase B step position 10 or 11, L1 power is applied through the phase B step switch contacts SS7–10, 11, the now closed relay contacts CR2–3 in phase B, and thence to the phase A unit through switch SW–3, through phase A step switch contacts SS5–2, 3, 4, to AND (A.C.) circuit 94. So long as L4 power has not failed, AND (A.C.) circuit 94 applies an A.C. signal to the A.C. to D.C. converter 92. Circuit 92, in turn, applies a (1) signal to the input circuit of NOR circuit 90, which, in turn, applies a (0) signal to the input signal circuit of timer T4 so that timer T4 may commence its timing function. The time duration of the extension limit period is deter-

mined by the adjusted value of the reference voltage V_R, which during step positions 2, 3 and 4 is obtained from potentiometer 80. When the extension limit portion of timer T4 completes its timing function, a (1) signal is applied from its output circuit to the AND circuit 98. During step positions 2, 3 and 4, AND circuit 98 applies a (1) signal through OR circuit 100 to energize relay coil CR3–C of relay CR3. This, in turn, opens normally closed relay contacts CR3–2, thereby preventing further vehicle actuations on phase A from resetting the passage time timer T3. Accordingly, the passage time timer completes timing a passage time and then develops a (1) signal for application to AND circuit 70. If this occurs during step position 2 or 3, then as soon as the step switch is stepped to step position 4, a (1) signal is applied by AND circuit 70 through OR circuit 54 to AND circuit 56.

Phase A, step position 3.—When the step switch is stepped from step position 2 to step position 3, the phase A control unit is in its green dwell interval. This is not a timed interval. In order for the step switch to be stepped from step position 3 to step position 4, a vehicle actuation must occur in phase B. When a vehicle actuation has occurred in phase B, relay contacts CR2–3 in the phase B control unit are closed and L1 power is supplied through phase B step switch contacts SS7–10, 11 through the now closed contacts CR2–3, and thence through switch SW–3 to phase A step switch contacts SS8–3, through the off normal contacts 122, which are closed during step position 3, through the interrupter contacts CR5–INT–C to complete an energizing circuit for step switch driver coil CR5–C. The step switch steps from step position 3 to step position 4. Accordingly, it is seen that if the phase B vehicle actuation took place during the phase A step position 2, the phase A green dwell interval would be substantially eliminated. Otherwise, the phase A control unit dwells in its green dwell interval until such time as a vehicle actuation occurs on phase B.

Phase A, step position 4.—In step position 4, the phase A passage time and time waiting-minimum lull period, the step switch will be stepped to step position 5 as soon as the passage time timer completes its timing function so that AND circuit 70 provides a (1) signal through OR circuit 54 to AND circuit 56. As discussed hereinabove, the passage time timer will be forced to complete its timing function in the event that the extension limit portion of timer T4 completes its timing function. This occurs because when the extension limit timer completes its timing function, it develops an output signal which disables the reset feature of the passage time timer by energizing relay coil CR3–C, causing contacts CR3–2 to open. However, the time waiting-minimum lull timer T5 also serves, during step position 4, to energize relay coil CR3–C and thus disable the reset feature of the passage time timer. During step position 4, L1 potential is applied from phase unit B through phase B step switch contacts SS7–10, 11 and closed relay contacts CR2–3, representative of a phase B vehicle detection, and thence through switch SW–3, and through phase A step switch contacts SS8–4 to AND (A.C.) circuit 110. So long as L4 power has not failed, AND (A.C.) circuit 110 applies an alternating current voltage signal to converter circuit 112. Converter circuit 112 applies a (0) signal to NOR circuit 108 which, in turn, applies a (1) signal to the input circuit of timer T5, causing the timer to commence its timing function. Since ramp function generator 30′ is the complement of generator 30 of the normal timer T1, the output voltage V_0 of generator 30′ linearly decreases, as shown by the wave form associated with timer T5. The reference voltage V_R for comparator circuit 32 of timer T5 is the output voltage V_0 of generator 30 in the passage time timer T3. When the output voltage V_0 of generator 30′ is substantially equal to the reference V_R, comparator 32 of timer T5 develops a (1) signal for application through OR circuit 100, energizing relay coil CR3–C. This opens relay contacts CR3–2, preventing further reset of passage time timer T3. Accordingly, the passage time timer T3 completes its timing of a passage time and applies a (1) signal to AND circuit 70. It is to be appreciated that it is possible for timer T5 to time out after the extension limit portion of timer T4 and, accordingly, the extension limit time will control the point in time that the reset feature of the passage time timer is disabled. A (1) signal is applied through OR circuit 54 to AND circuit 56. Since the variable initial timer has previously timed out, a (1) signal is also applied from timer T2 to AND circuit 56, whereupon the AND circuit applies a (1) signal through OR circuit 58 to AND circuit 60. Since AND circuit 60 receives a (1) signal from NOR circuit 124, except during step positions 3 and 8, a (1) signal is also applied from the output circuit of AND circuit 60 to energize control relay coil CR4–C. This closes relay contacts CR4–1 to complete an energizing circuit for step switch coil CR5–C. Accordingly, step switch SS steps from step position 4 to step position 5, the phase A vehicle clearance No. 1 interval.

Phase A, step position 5.—The phase A vehicle clearance No. 1 interval is a go interval for phase A and is timed by normal timer T1. The time duration of this interval is dependent on the value of the reference voltage V_R applied to comparator 32 of timer T1, which voltage, in turn, is adjusted by potentiometer 42. When the output voltage V_0 of generator 30 of timer T1 is substantially equal to the reference voltage V_R, a (1) signal is applied from the output circuit of timer T1 through OR circuit 54 to the input circuit of AND circuit 56. Since a (1) signal is applied from the output circuit of the variable initial timer T2 to the AND circuit 56, a (1) signal is applied through OR circuit 58 to AND circuit 60. Since a (1) signal is also applied to the AND circuit 60 from the output circuit of NOR circuit 124, except during step positions 3 and 8, a (1) signal is also applied from the output circuit of AND circuit 62 to energize relay coil CR4–C. This closes relay contacts CR4–1 to complete an energizing circuit for step switch driver coil CR5–C. Thus, step switch SS steps from step position 5 to step position 6, the phase A special clearance No. 1 interval.

Phase A, step position 6.—The phase A special clearance No. 1 interval is a go interval for phase A, as indicated in FIGURE 4. This interval is timed by the normal timer T1. The duration of the interval is dependent on the value of the reference voltage V_R as adjusted by potentiometer 44. When the output voltage V_0 of generator 30 is substantially equal to the reference voltage V_R, the comparator circuit 32 of timer T1 applies a (1) signal through OR circuit 54 to the AND circuit 56. Since the variable initial timer T2 has completed its timing circuit, its comparator circuit 32 also applies a (1) signal to AND circuit 56. Accordingly, AND circuit 56 applies a (1) signal through OR circuit 58 to AND circuit 60. Since a (1) signal is also applied to AND circuit 60 from the output circuit of NOR circuit 124, except during step positions 3 and 8, a (1) signal is applied from the output circuit of AND circuit 60 to energize control relay coil CR4–C. This closes relay contacts CR4–1 which, in turn, completes an energizing circuit for step switch driver coil CR5–C. Thus, the step switch SS steps from step position 6 to step position 7, the phase A green No. 2 interval.

Phase A, step position 7.—The green No. 2 interval is a go interval for phase A, as indicated in FIGURE 4, and is timed by the green No. 2 portion of timer T4. The time duration of this interval is dependent on the value of reference voltage V_R which, during step position 7, is dependent on the adjustment of potentiometer 82. In step position No. 7, a B+ potential is applied through step switch contacts SS6–7 to the input circuit of AND circuit 86. In the absence of power failure of alternating current voltage source L4, a (1) signal is also applied to the AND circuit 86 from the A.C. to D.C. converter

circuit 88. Thus, AND circuit 86 applies a (1) signal to NOR circuit 84 which, in turn, applies a (0) signal to the input circuit of timer T4. Thus, timer T4 commences its timing function and, when the output voltage V_0 of generator 30 is substantially equal to the reference voltage V_R, a (1) signal is applied from the output circuit of comparator circuit 32 of timer T4 to the input circuit of AND circuit 96. A (1) signal is also applied to the input circuit of AND circuit 96 from the B+ voltage supply source through step switch contacts SS6–7. Accordingly, AND circuit 96 applies a (1) signal through OR circuit 58 to the AND circuit 60. Since a (1) signal is also applied to the AND circuit 60 from the output circuit of NOR circuit 124, except during step positions 3 and 8, AND circuit 60 applies a (1) signal to relay coil CR4–C. This closes relay contacts CR4–1 for completing an energizing circuit for the step switch driver coil CR5–C. Thus, the step switch SS steps from step position 7 to step position 8, the phase A green dwell interval.

Phase A, step position 8.—The green dwell interval is not a timed interval. The phase A control unit will dwell in this position until such time as a vehicle actuation occurs on phase B. More particularly, it is possible that the traffic actuation on phase B, which caused the phase A control unit to step from step position 3 has been lost, by the time the unit is advanced to step position 8, as by a malfunction in equipment operation. Accordingly, so that stop signals are not displayed to all phases during this condition, phase A control unit remains in step position 8. If the phase B traffic actuation is still in effect, or at such time that a phase B traffic actuation occurs, a circuit is completed for energizing the step switch driver coil CR5–C. Driver coil CR5–C is energized by a circuit which commences in phase unit B from source L1 through phase B step switch contacts SS7–10, 11, through closed relay contacts CR2–3, representative of a phase B traffic actuation, through switch SW–3, and then through phase A step switch contacts SS5–8, switch SW–5 to NOR circuit 125. Thus, a (1) signal is applied from the output circuit of NOR circuit 125 to energize relay coil CR4–C. This closes relay contacts CR4–1 for completing an energizing circuit for the step switch driver coil CR5–C. Thus, the step switch SS steps from step position 8 to step position 9, the phase A vehicle clearance No. 2 interval.

Phase A, step position 9.—The vehicle clearance No. 2 interval is a caution interval for phase A, as indicated by the chart in FIGURE 4, and is timed by normal timer T1. The duration of this interval is dependent on the value of the reference voltage V_R, as adjusted by potentiometer 46. When the output voltage V_0 of generator 30 is substantially equal to the reference voltage V_R the comparator circuit 32 of timer T1 applies a (1) signal through OR circuit 54 to AND circuit 56. Since the variable initial timer T2 has completed its timing function, its comparator circuit 32 also applies a (1) signal to AND circuit 56. Accordingly, AND circuit 56 applies a (1) signal through OR circuit 58 to AND circuit 60. Since a (1) signal is also applied to AND circuit 60 from the output circuit of NOR circuit 124, except in step positions 3 and 8, a (1) signal is applied from the output circuit of AND circuit 60 to energize control relay coil CR4–C. This closes relay contacts CR4–1 which, in turn, completes an energizing circuit for step switch driver coil CR5–C. Thus, the step switch SS steps from step position 9 to step position 10, the phase A red dwell No. 1 interval.

As the step switch SS was stepped from step position 8 to step position 9, ground potential, i.e., L1 power, was applied through relay contacts CR4–1, switch SW–1, phase A step switch contacts SS4–8, and thence through phase B step switch contacts SS4–10 to complete an energizing circuit through phase B switch SW–2 and phase B step switch driver coil CR5–C. Accordingly, this steps the phase B step switch SS from step position 10 to step position 11, the phase B red dwell No. 2 interval.

Phase A, step position 10.—The red dwell No. 1 interval is a stop interval for phase A, as indicated by the chart in FIGURE 4. The phase A unit will dwell in step position 10 until it becomes traffic actuated. As the phase A step switch SS was stepped from step position 9 to step position 10, L1 power was applied through contacts CR4–1 through phase A switch SW–1, phase A step switch contacts SS4–9, and thence in phase B unit through step switch contacts SS4–11 and phase B switch SW–2 to complete an energizing circuit for the phase B step switch driver coil CR5–C. Thus, the phase B step switch is stepped from step position 11 to step position 1, the phase B special clearance No. 2 (stop) interval. Phase unit B is now in control and will commence timing its intervals No. 1 and No. 2 and then dwell in its green dwell interval, i.e., phase B step switch position No. 3, until it receives a call from phase A unit, indicative of a traffic actuation in phase A. The sequence of operation for phase unit B is the same as that just described with respect to phase unit A.

Although the invention has been described thus far in conjunction with a two phase, full actuated traffic control system including separate phase units A and B for controlling traffic flow through an intersection of traffic actuated phases A and B, it is to be appreciated that the invention may also be used in conjunction with a semiactuated, two phase control system including a single control unit. More particularly, the phase unit A described thus far with respect to FIGURE 3, may be converted to a two phase, semiactuated traffic controller. This conversion takes place by merely opening switches SW–1, SW–2, SW–3, SW–4 and SW–5, and closing switches SW–6 and SW–7. In addition to actuating the switches, suitable load relay changes should be made so that step switch SS connects both main street and cross street signal lamps to a source of power during the appropriate step switch intervals. Having made such conversions, a typical traffic interval versus step position may take the form as shown in the chart of FIGURE 4 (option 1) for a two phase, semiactuated controller. More particularly, it will be noted that step switch positions 10, 11 and 1 through 6 constitute a stop period for main street traffic, that step positions 7 and 8 serve as the main street go period, and that step position 9 serves as the main street caution or amber period. Also, under these conditions, it will be noted that step positions 6 through 11 and 1 serve as the cross street red or stop period, that step positions 2 through 4 serve as the cross street green or go period, and step position 5 serves as the cross street caution or amber period. As is common in the art of traffic control for such a two phase, semiactuated controller, the cross street serves as the traffic actuated phase and main street is the nonactuated traffic phase.

TIME WAITING-GAP REDUCTION CIRCUITRY

In accordance with the present invention, the time waiting-gap reduction circuitry includes the passage time timer T3 and the time waiting-minimum lull timer T5, illustrated in block diagram in FIGURE 3. Reference is now made to FIGURE 2, which shows the preferred schematic circuit diagram of these two circuits.

Passage time timer.—The passage time timer T3 includes a linear ramp function generator 30 and a comparator circuit 32. Generator 30 takes the form of an operational D.C. amplifier having negative feedback, and generally comprises PNP transistors 130 and 132, an NPN transistor 134, a negative feedback capacitor 136, and an output resistor 138. Transistor 130 has its emitter connected directly to the B+ voltage supply source and its base connected through an input timing resistor 140 to the junction of resistors 142 and 144. Resistors 142

and 144 are connected together in series and form a voltage divider 48 between the B+ voltage supply source and ground. The collector of transistor 130 is directly connected with the base of transistor 134. A capacitor 146 is connected between the emitter of transistor 134 and the base of transistor 130. The collector of transistor 134 is connected through a resistor 148 to the B+ voltage supply source. The junction of resistor 148 and the collector of transistor 134 is connected to the output circuit of OR circuit 72 (see FIGURE 3), as well as to the base of transistors 132. A voltage divider including series connected resistors 150 and 152 is connected between the B+ voltage supply source and ground for purposes of lowering the collector voltage of transistor 130. The junction of resistors 150 and 152 is connected to the emitter of transistor 134, as well as to the collector of transistor 132 through a capacitor 154. The negative feedback capacitor 136 is connected between the collector of transistor 132 and the junction of resistor 140 and the base of transistor 130. The output resistor 138 is connected between the junction of capacitor 136 and the collector of transistor 132 and ground.

The comparator circuit 32 of the passage time timer T3 preferably takes the form of a differential amplifier including NPN transistors 156 and 158. The emitters of the two transistors are connected together in common and thence through a resistor 160 to a B— voltage supply source. The base of transistor 156 is connected to the junction of resistor 138 and the collector of transistor 132 through a diode 162, poled as shown in FIGURE 2. The collector of transistor 156 is connected to the B+ voltage supply source through a resistor 164. Also, the junction of resistor 164 and the collector of transistor 156 is connected to the input circuit of AND circuit 70 through transistor 155. The collector of transistor 158 is also connected to the B+ voltage supply source through a resistor 166. The base of transistor 158 is connected to the wiper arm of potentiometer 68 (see FIGURE 3), through a diode 168, poled as shown in FIGURE 2.

Time waiting-minimum lull timer.—The time waiting-minimum lull timer generally comprises a linear ramp function generator 30′ which is constructed of circuit components comprising the complement of those in generator 30 of timer T3, and a differential amplifier 32. Generator 30′ includes three NPN transistors 170, 172 and 174; a PNP transistor 176; and, a feedback capacitor 180. The emitters of transistors 170 and 172 are connected together in common and thence through a resistor 182 to a B— voltage supply source. The base of transistor 170 is connected through the time waiting potentiometer 102 to the junction of resistors 184 and 186, which comprise the voltage divider 104. Resistor 186 and potentiometer 102 connect the base of transistor 170 to the wiper arm of potentiometer 68 associated with the passage time timer T3. The collector of transistor 170 is connected to the base of the same transistor through a capacitor 188, and is also connected directly to the base of transistor 176. The base of transistor 172 is connected to the junction of resistor 184 and the wiper arm of minimum lull potentiometer 106. This potentiometer is connected between the B+ voltage supply source and ground. The collector of transistor 172 is connected to the wiper arm of potentiometer 68. A diode 190, poled as shown in FIGURE 2, connects the base of transistor 172 with the base of transistor 170.

The junction of diode 190 and the base of transistor 170 is connected to NOR circuit 108 (see FIGURE 3). NOR circuit 108, as shown in FIGURE 2, includes a NPN transistor having its collector connected to the base of transistor 170 through a resistor 109, its emitter connected to a B— voltage supply source and its base connected to ground through resistors 111 and 113. The negative output of the A.C. to D.C. converter 112 is connected to the junction of resistors 111 and 113 and the positive output of the converter is connected to the emitter. A resistor 115 is connected between the emitter and the junction of resistors 111 and 113.

Capacitor 180 connects the emitter of transistor 176 with the base of transistor 170. Also, the emitter of transistor 176 is connected with the collector of transistor 170 through a resistor 192. The collector of transistor 176 is connected to ground through a resistor 194. Transistor 174 has its emitter connected to ground and its base connected to the junction of resistor 194 and the collector of transistor 176. Also, the collector of transistor 174 is connected to the wiper arm of potentiometer 68 through resistor 178.

The differential amplifier 32 of the time waiting-minimum lull timer T5 includes four NPN transistors 196, 198, 200 and 202. Transistor 196 has its collector connected to the B+ voltage supply source and its base connected to the junction of resistor 178 and the collector of transistor 174. The emitter of transistor 196 is directly connected to the base of transistor 198. The collector of transistor 198 is connected to the B+ voltage supply source through a resistor 204. The emitters of transistors 198 and 200 are connected together in common and thence through a resistor 206 to the B— voltage supply source. The collector of transistor 200 is connected to the B+ voltage supply source through a resistor 208. Also, the collector of transistor 200 is connected to the input circuit of OR circuit 100 (see FIGURE 3), through PNP transistor 201. Transistor 201 has its collector connected to OR circuit 100, its emitter connected to the B+ voltage supply source, and its base connected to the collector of transistor 200. Transistor 202 has its collector connected to the B+ voltage supply source and its emitter directly connected to the base of transistor 200. In addition, the base of transistor 202 is connected to the junction of resistor 138 and the collector of transistor 132 in the passage time timer T3.

Detailed description of operation of time waiting-gap reduction circuit.—As long as OR circuit 72 applies a (1) signal, i.e., a positive potential signal, to the base of transistor 132, the output voltage V_I of generator 30 of the passage time timer T3 is substantially at ground potential. The adjustment of the wiper arm of potentiometer 68 adjusts the passage time setting, see setting V_R (passage time setting) in FIGURES 5, 6, 7 and 8. During the period that OR circuit 72 applies a (1) signal to the base of transistor 132, the negative side of capacitor 136 is referenced to ground and the capacitor is charged by the current flowing from the emitter to base of transistor 130. The value of the charge stored by the capacitor 130 is, therefore, the value of the B+ potential minus the voltage drop between the emitter and base of transistor 130.

When OR circuit 72 applies a (0) signal, i.e., a potential between B+ and ground potential, to the base of transistor 132, the transistor becomes conductive. A potential is developed across input timing resistor 140. The value of this potential is determined by the potential stored by the capacitor 136 and the setting of the potential divider comprised of resistors 142 and 144. Capacitor 136 commences to discharge through resistors 140, 144 and 138, thereby slightly decreasing the potential stored by the capacitor. As the value of the potential stored by capacitor 136 decreases, transistor 130 begins to conduct. Current flows from the B+ voltage supply source through the emitter to collector of transistor 130 to the base of transistor 134, causing transistor 134 to conduct. As transistor 134 begins to conduct, the potential appearing on its collector decreases toward ground potential. As this occurs, transistor 132 begins to conduct. Current, therefore, commences to flow from the emitter to collector of transistor 132, whereupon a voltage begins to build up across the output resistor 138. This voltage increase across resistor 138 lifts the potential on the negative end of capacitor 136 to a point above ground potential. Since the voltage across capacitor 136 cannot change instantaneously, the potential at the positive end

of the capacitor is also raised instantaneously the same amount as on the negative end. This tends to turn off transistors **130**, **134** and **132**. Capacitor **136** then discharges through resistors **140** to **144** and **138**. Again, transistors **130**, **134** and **132** begin to conduct, applying more potential across output resistor **138**. The circuit continues to function in this manner so that for a square wave input a linear ramp function is produced, appearing as output voltage V_1 across resistor **138**. Voltage V_1 increases in a linear manner with elapsed time from ground potential toward the value of the B+ voltage supply source. So long as timer T3 is not reset, as by momentary application of a (1) signal from OR circuit **72** to the base of transistor **132**, this linear ramp function will continue until transistor **132** is completely saturated.

The output voltage V_1 of generator **30** is continuously compared with the reference voltage V_R, as adjusted by potentiometer **68**, with comparator circuit **32** of timer T3. Initially, the output voltage V_1 is at ground potential. At this point in time, potentiometer **68** provides positive reference potential to the anode of diode **168**. The magnitude of this potential is reflected through the diode to the emitter of transistor **158**, such that a positive potential appears at the junction of the emitters of transistors **156** and **158**. This potential is equal to the value of the voltage applied to the base of transistor **158** minus the base to emitter voltage drop of transistor **158**. Since the output voltage V_1 is initially at ground potential and a positive potential appears at the junction of emitters of transistors **156** and **158**, transistor **156** is reversed biased. Transistor **158**, on the other hand, is forward biased and is conducting. Under these conditions, the value of the voltage appearing on the collector of transistor **156** is essentially equal to that of the B+ voltage supply source, and the voltage appearing on the collector of transistor **158** is at a value somewhere between ground and B+ voltage supply source. Accordingly, transistor **155** is reversed biased so that a (1) signal is not applied to the input circuit of AND circuit **70** (see FIGURE 3).

When OR circuit **72** applies a (0) signal to the base of transistor **132**, the output voltage V_1 is a linear ramp function increasing in value from ground potential toward the value of the B+ voltage supply source with elapsed time. After a predetermined period of time the value of voltage V_1 is substantially equal to, or slightly greater than, that of the reference potential V_R, whereupon transistor **156** becomes forward biased and begins to conduct. This, in turn, causes transistor **155** to be forward biased, applying a (1) signal to the input circuit of AND circuit **70** for initiating interval terminating action.

The passage time timer T3, however, is reset in response to each vehicle detection occurring in the associated phase A. That is, for each actuation of detectors D1, D2 (see FIGURE 3) relay coil CR1–C is energized to close its contacts CR1–3. Closure of contacts CR1–3 applies a (1) signal from the B+ voltage supply source through the normally closed relay contacts CR3–2, through contacts CR1–3 to the input circuit of OR circuit **72**. OR circuit **72**, in turn, applies a (1) signal to the base of transistor **132**, thereby referencing the output voltage V_1 to ground potential. The passage time timer T3 is effective during step positions **2**, **3** and **4**. More particularly, during step positions **2**, **3** and **4**, L4 potential, i.e., the hot side of the alternating current voltage source, is applied through the phase A step switch contacts SS1–2, **3** or **4** and, thence, through the A.C. to D.C. converter **78**, whereupon a (1) signal is applied to NOR circuit **76**. NOR circuit **76**, in turn, applies a (0) signal to the input circuit of OR circuit **72**. During the remaining step switch positions, NOR circuit **76** applies a (1) signal through or circuit **72** to the input circuit of timer A3 to maintain the timer reset so that the output voltage V_1 is referenced to ground potential. In addition, the passage timer is reset in the event that a failure occurs in the alternating current voltage source; that is, in the event that L4 power is lost, NOR circuit **74** applies a (1) signal through OR circuit **72** to maintain the timer reset.

Referring now to FIGURE 2, and more particularly to the time waiting-minimum lull timer T5, potentiometers **106** and **102** serve to respectively adjust the setting of the time waiting and minimum lull periods. The function of these two potentiometers is to establish a minimum allowable gap in the time between vehicle detector actuations that must not be exceeded in order to retain control of the go signal. This function minimizes the length of time one or more vehicles on an opposing phase must wait on a stop signal, therefore eliminating undue delay and increasing intersection efficiency.

Timer T5 is operative during phase A position **4**, providing there is a call received from another phase representative that the other phase has been traffic actuated. More particularly, with reference to FIGURE 3, it will be noted that when phase unit B is traffic actuated so that its contacts CR2–3 are closed, L1 potential is applied from phase unit B through step switch contacts SS7–10, **11** and relay contacts CR2–3, through switch SW–3, and through phase A's step switch contacts SS8–4 to the AND (A.C.) circuit **110**. So long as L4 power has not failed, AND (A.C.) circuit **110** applies an alternating current voltage signal to converter circuit **112**. Converter circuit **112** applies a (0) signal to NOR circuit **108** which, in turn, applies a (1) signal to the input circuit of timer T5, causing the timer to commence its timing function. As stated hereinbefore, generator **30'** of timer T5 includes components which constitute the complement of those in generator **30** of timer T3, and, accordingly, the output voltage V_2 of generator **30'** decreases linearly with elapsed time from a value between ground and the B+ voltage supply source toward ground potential.

During the reset condition of timer T5, i.e., when no voltage is present on the output circuit of converter **112**, transistor **108** is forward biased and conductive since its base is referenced to ground and its emitter is referenced to the B— voltage supply source. Accordingly, the negative feedback capacitor **180** charges in accordance with the polarity shown in FIGURE 2. This charge is limited by the setting of minimum lull potentiometer **106**. The value of the charge is substantially equal to the value of the reference voltage V_R, as adjusted by potentiometer **68**, less the value of the voltage on the wiper arm of the minimum lull potentiometer **106**. Transistor **172** is forward biased by the setting of the wiper arm of potentiometer **106** so that the transistor is conducting. Accordingly, the potential on the emitters of transistors **170** and **172** is raised to a sufficiently high positive value that transistor **170** is reversed biased. Transistor **176** is reversed biased due to the positive potential on its base with respect to that on its emitter. Since transistor **176** is not conducting, transistor **174** does not conduct. Accordingly, voltage V_2 taken between ground and the junction of collector **174** and resistor **178** is at a value substantially that of the value of the reference voltage V_R, as adjusted by the passage time timer potentiometer **68**.

When a traffic actuation occurs on another phase during the period that phase unit A is in step position **4**, a circuit is completed to AND (A.C.) circuit **110** so that this circuit applies an alternating current voltage signal to the A.C. to D.C. converter **112**. Thus, converter **112** applies negative voltage to the junction of resistors **111** and **113**, whereby the voltage on the base of transistor **108** is driven sufficiently negative to reverse bias the transistor. Since transistor **108** is now reversed biased, this removes the reverse bias on transistor **170**. That is, the potential on the base of transistor **170** becomes positive with respect to that on its emitter, whereby the transistor becomes forward biased and conducts. This, in turn, applies a sufficiently negative voltage to the base

of transistor **176** so that this transistor becomes forward biased and conductive. Since transistor **176** is conductive, sufficient positive voltage is applied to the base of transistor **174** so that this transistor also becomes conductive. Accordingly, the output voltage V_2 decreases. This voltage decrease lowers the potential on the positive end of feedback capacitor **180** toward the level of ground potential. Since the voltage across capacitor **180** cannot change instantaneously, the potential at the negative end of the capacitor is also driven more negatively the same amount as on the positive end. This tends to turn off transistors **170, 176** and **174**. Capacitor **180** then discharges somewhat. Again, transistor **170** begins to conduct thereby further lowering the output voltage V_2. The circuit continues to function in this manner so that for a square wave input, a linear ramp function is produced appearing as output voltage V_2. Voltage V_2 decreases in a linear manner with elapsed time from the value between ground potential and the B+ voltage supply source, as determined by the adjustment of potentiometer **68**, toward ground potential, but limited at a lower limit as adjusted by the minimum lull potentiometer **106**.

The output potential V_2 of generator **30'** and the output potential V_1 of generator **30** of timer **T3** are continuously compared by comparator circuit **32** in timer **T5**. The comparator circuit **32** in timer **T5** operates in substantially the same manner as the capacitor circuit **32** in timer **T3**, described hereinabove, and, accordingly, no further detailed description is believed necessary for complete understanding of the invention. Initially, the output potential V_1 is at ground potential, and potential V_2 is at a potential between ground and the B+ voltage supply source. Accordingly, transistor **200** will be reversed biased. However, when voltage V_2 decreases to the point that it is of less value than potential V_1, transistor **200** will conduct applying forward biasing potential to the base of transistor **201**. Thus, transistor **201** conducts and applies B+ potential, i.e., a (1) signal, to the input of OR circuit **100**.

Reference is now made to the charts illustrated in FIGURES 5, 6, 7 and 8 of voltage versus time for various operational conditions of the time waiting-gap reduction circuitry. In FIGURE 5 the level of the voltage V_R is the passage time setting as adjusted by potentiometer **68**. The voltage level V_{ML} may be reduced, as adjusted by the minimum lull potentiometer **106**. The slope of the wave form for the output voltage V_2 is determined by the setting of the time waiting potentiometer **102**. At time t_0, during step switch position **2**, the passage time timer **T3** is energized and the output voltage V_1 increases linearly with elapsed time toward the value of the passage time setting V_R. At time t_1 the passage timer times out, which may take place during step position **2** or **3**, but its output signal performs no control function since AND circuit **70** (see FIGURE 3) will not provide an output signal until the step switch is in step position **4**. At time t_2 the passage timer has not been reset and a call has been received from another phase unit, whereupon the step switch is immediately stepped from step position **3** to step position **4**. Since the passage timer has timed out, AND circuit **70** will apply a (1) signal through OR circuit **54**, causing the step switch to step from step position **4** to step position **5**.

Reference is now made to the chart of FIGURE 6 which illustrates a more complicated situation than that posed in FIGURE 5. Again, the passage timer **T3** is energized to time t_0, during step position **2**. At point in time t_1 the passage timer times out in either step position **2** or **3**, but performs no control function. At time t_2 the passage timer is reset by a vehicle actuation occurring in phase A, whereupon the passage timer commences its timing function and output voltage V_1 increases linearly toward the value of the reference voltage V_R. At time t_3 a traffic actuation has occurred on another phase, stepping phase unit A from step position **3** to step position **4**, and energizing the time waiting-minimum lull timer **T5**. At time t_4 the value of voltage V_1 is substantially equal to that of voltage V_2, whereupon timer **T5** applies a (1) signal to OR circuit **100** to disable the reset feature of the passage timer. That is, OR circuit **100** applies a (1) signal to energize relay coil **CR3-C** (see FIGURE 3) to open contacts **CR3-2**. Thus, further actuation of phase A detectors **D1, D2** will not reset the passage time timer **T3**. Accordingly, the output voltage V_1 continues to increase in value until it is substantially equal to the value of the reference voltage V_R. This occurs at time t_5 and the passage time timer applies a (1) signal to AND circuit **70**. Since the step switch is in step position **4**, AND circuit **70** applies a (1) signal to OR circuit **54** causing the step switch to be advanced from step switch position **4** to step switch position **5**.

Reference is now made to FIGURE 7 which illustrates a more complicated condition than that posed in FIGURE 6. Again, the passage time timer **T3** is energized at time t_0, during step switch position **2**. At time t_1 a call has been received from another phase, whereupon phase A unit is stepped to step position **4**. The time waiting-minimum lull timer **T5** is energized and commences linear gap reduction. It will be noted that during the period from time t_1 to time t_2 the actual gap between successive vehicles on phase A to retain right-of-way must continuously reduce with the waiting time of a vehicle on the actuated or calling phase. At time t_2, the time waiting period, as adjusted by potentiometer **102**, has been reduced to the preset minimum lull voltage V_{ML}, as adjusted by potentiometer **106**. The flow of traffic in phase A has been such that the lull being sought has not been found. Accordingly, phase A traffic is allowed to continue under these conditions. At time t_3 the lull condition has been found. That is, the output voltage V_2 is now stabilized at the value of voltage V_{ML}, and this value has been reached by voltage V_1. Accordingly, timer **T5** applies a (1) signal through OR circuit **100** to disable the reset feature of the passage time timer **T3**. The unit remains in interval **4** until the passage time interval is completed at time t_4. During this period, additional actuations of phase A detectors **D1, D2** will not reset the passage time timer. At time t_4, the passage timer has timed out and applies a (1) signal to AND circuit **70**. Accordingly, the step switch is advanced from step switch position **4** to step switch position **5**.

Reference is now made to the chart illustrated in FIGURE 8 which presents a somewhat more complicated condition than that posed in FIGURE 7. As will be recalled from the chart in FIGURE 7, the minimum lull setting V_{ML} was reached at time t_2 without the passage time timer timing out. It will be appreciated that during heavy traffic conditions on phase A it is possible that the actual time gaps between successive vehicles will be sufficiently small that the output voltage V_1 of the passage time timer would never reach the level of voltage V_{ML}. This condition is overcome by the setting of potentiometer **80** associated with the extension limit timer **T4** (see FIGURE 3). As shown in FIGURE 8, the conditions at time t_2 are the same as those set forth in FIGURE 7. However, at time t_3 the setting of the extension limit timer is such that the extension limit timer **T5** has timed out, applying a (1) signal through AND circuit **98** to OR circuit **100**, thereby disabling the reset feature of the passage time timer. Accordingly, the passage time timer completes its timing function during step position **4**, and at time t_4 voltage V_1 has reached the value of the passage time reference voltage V_R. Thus, timer **T3** applies a (1) signal to the AND circuit **70** causing the step switch to advance from step position **4** to step position **5**.

Once the step switch has been advanced to step position **5**, the vehicle clearance No. 1 interval, the normal timer **T1** commences its timing function, as discussed hereinbefore.

The invention has been described in connection with a particular preferred embodiment, but is not limited to same. Various modifications may be made without departing from the scope and spirit of the present invention as defined by the appended claims.

Having thus described our invention, we claim:

1. In a traffic controller for alternately allocating go and stop signals to at least two intersecting traffic phases, each having vehicle detection means associated therewith for detecting vehicles in an associated said phase, said controller including a time waiting-gap reduction circuit for initiating a change in allocation of said go and stop signals to said phases as a function of the actual gap time between successively detected vehicles in one of said phases and the time that a detected vehicle is waiting in the other of said phases to which a stop signal is allocated; the improvement wherein said time waiting-gap reduction circuit comprises:

first timing means including first generating means for generating an actual time gap signal which progressively varies in a linear manner with elapsed time between successively detected vehicles in said one phase;

second timing means including second generating means for generating a time waiting signal which progressively varies in a linear manner with the elapsed time that a detected vehicle is waiting in said other phase to which a stop signal is allocated; and,

means for comparing said actual time gap signal and said time waiting signal and developing a signal for initiating termination of said go signal allocation to said one phase when said actual gap signal and said time waiting signal attain a predetermined relationship with respect to each other.

2. In a traffic controller as set forth in claim 1, wherein said first and second timing means respectively develop said actual gap and time waiting signals as voltage potentials which linearly vary in value with elapsed time.

3. In a traffic controller as set forth in claim 1, wherein said first and second timing means develop said actual gap and time waiting signals as voltage potentials which linearly vary in value toward that of each other with elapsed time so that after a given period of time said potentials are of substantially equal values.

4. In a traffic controller as set forth in claim 1, including means for resetting said first generating means for each detection of a vehicle in said one phase.

5. In a traffic controller as set forth in claim 4, including third timing means for timing a predetermined maximum period of time concurrently with the timing function of said second timing means and then developing a first reset disable signal;

reset disable means coupling said third timing means with said resetting means for resetting said first generating means in response to a said first reset disable signal, whereupon further detections of vehicles in said one phase do not result in resetting said first generating means.

6. In a traffic controller as set forth in claim 1, wherein said first timing means includes comparator means for comparing said actual time gap signal with a reference signal and then developing an output signal for terminating said go signal allocation to said one phase when said actual time gap signal and said reference signal attain a predetermined relationship with respect to each other.

7. In a traffic controller as set forth in claim 6, including adjustable means for providing said reference signal, whereby the time delay between energization of said first generating means and development of said output signal by said comparator means of said first timing means is directly proportional to the adjusted reference signal.

8. In a traffic controller for alternately allocating go and stop signals to at least two intersecting traffic phases, each having vehicle detection means associated therewith for detecting vehicles in an associated said phase, said controller including a time waiting-gap reduction circuit for initiating a change in allocation of said go and stop signals to said phases as a function of the actual gap time between successively detected vehicles on one of said phases and the time that a detected vehicle is waiting on the other of said phases, when a stop signal is allocated thereto; the improvement wherein said time waiting-gap reduction circuit comprises:

first and second linear timers, each including:

generating means for generating a first signal which progressively varies in a linear manner with elapsed time;

comparing means for comparing said first signal with a reference signal and developing an output signal when said first and reference signals attain a predetermined relationship with respect to each other;

means for resetting said generating means of said first timer for each detection of a vehicle in said one phase to which a go signal is allocated, whereby said first signal generated by said first timer progressively varies in a linear manner with elapsed time between successively detected vehicles in said one phase;

means for energizing said generating means for said second timer in response to a detected vehicle in said other phase to which a stop signal is allocated, whereby said first signal generated by said second timer progressively varies in a linear manner with the elapsed time that said detected vehicle in said other phase is waiting on a said stop signal;

said comparing means of said second timer being coupled to said generating means of said first timer to receive said first signal generated thereby so that said first signal from said first timer serves as the reference signal for the said comparing means of said second timer;

means for disabling said resetting means in response to a said output signal from the comparing means of said second timer, whereby further detections of vehicles in said one phase do not result in resetting the generating means of said first timer; and

means responsive to a said output signal from the comparing means of said first timer to initiate a change in the allocation of said go and stop signals to said phases.

9. In a traffic controller as set forth in claim 8, including maximum timing means coupled to said energizing means for timing a predetermined maximum period of time concurrently with the operation of said generating means of said second timer and then developing a reset disable signal, said disabling means being coupled to said maximum timing means for receiving said disabling signal to disable said resetting means independently of whether an output signal has been developed by the comparing means of said second timer.

10. In a traffic controller as set forth in claim 8, including means for limiting the value of the said first signal generated by the generating means of said second timer to a predetermined value so that said signal progressively varies in value in a linear manner with elapsed time until it attains a value equal to said predetermined value whereupon said signal becomes a steady state signal at said predetermined value.

11. In a traffic controller as set forth in claim 8, wherein said generating means of said second timer is comprised of components which essentially constitute the complement of those of the generating means of said first timer, whereby the first signal from said first timer and the first signal from said second timer progressively vary in value in a linear manner with elapsed time toward the value of each other.

12. In a traffic controller as set forth in claim 11, wherein each of said first signals is a voltage potential and wherein the comparing means of said second timer

includes a differential amplifier for comparing said potentials.

13. In a traffic controller as set forth in claim 12, including means for providing a said reference signal for the comparing means of said first timer as a voltage potential.

14. In a traffic controller as set forth in claim 13, wherein said reference signal providing means is adjustable, whereby the time delay between energization of the generating means of said first timer and development of a said output signal by the comparing means of said first timer is directly proportional to the adjusted value of said reference signal.

15. In a traffic controller as set forth in claim 11, wherein each said generating means includes:

first and second transistors of the same conductivity type;

a third transistor of an opposite conductivity type than said first and second transistors;

each of said transistors having first, second and control electrodes with the first electrodes of said first and third transistors being respectively directly coupled to the control electrodes of the said third and second transistors; and

a capacitor coupling said first electrode of said second transistor with the control electrode of said first transistor.

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