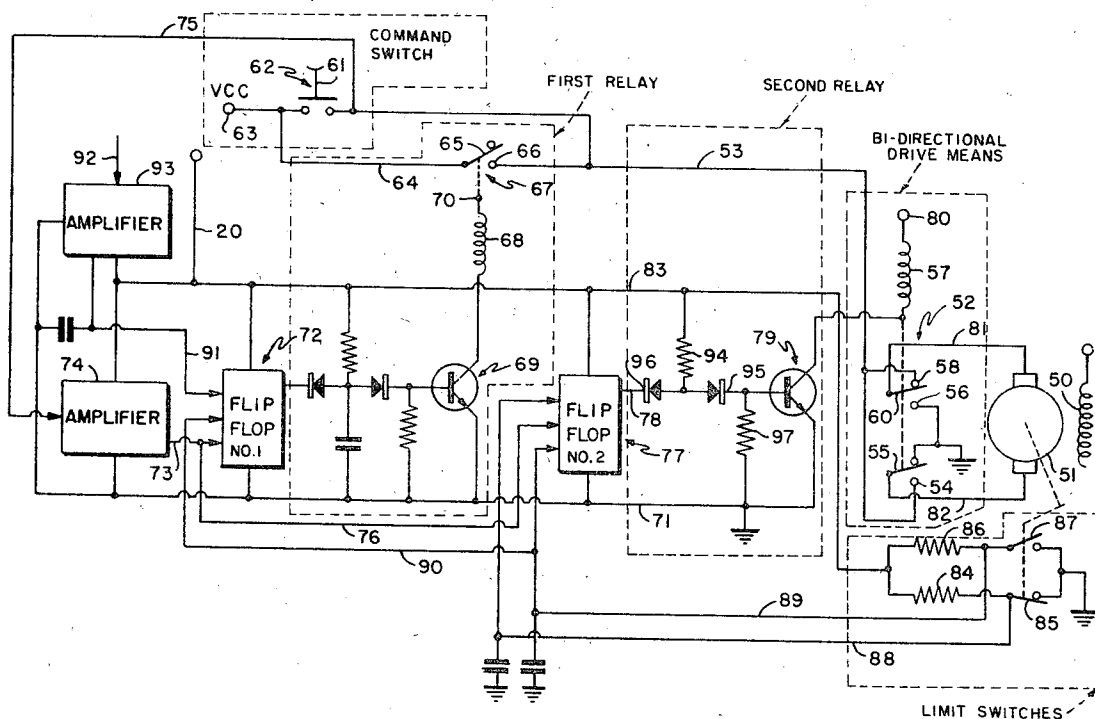


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|------|-----------|--------------------------------------------------------------------------|
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| [21] | Appl. No. | 844,982                                                                  |
| [22] | Filed     | July 25, 1969                                                            |
| [45] | Patented  | June 29, 1971                                                            |
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|-----------|----------------------------------------------------------------------------------------------|--------------|----------------------------------------------------------------------------------|
| [54]      | <b>SEMI-AUTOMATIC TUNING CIRCUIT FOR AN<br/>ANTENNA COUPLER</b><br>3 Claims, 3 Drawing Figs. |              |                                                                                  |
| [52]      | U.S. Cl.....                                                                                 |              | <b>325/174,</b><br>325/177, 334/22, 334/24, 334/71                               |
| [51]      | Int. Cl.....                                                                                 |              | <b>H04b 1/04</b>                                                                 |
| [50]      | Field of Search.....                                                                         |              | 325/127,<br>128, 160, 171—179; 307/265; 334/17—25, 61,<br>62, 71, 72, 22, 24, 71 |
| [56]      | <b>References Cited</b>                                                                      |              |                                                                                  |
|           | <b>UNITED STATES PATENTS</b>                                                                 |              |                                                                                  |
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**ABSTRACT:** In response to a manual "tune" order, this system drives the inductance in an antenna matching network to the maximum inductance position, whereupon the drive is reversed and control of the adjustment of the inductor is assumed by the processed output of a mismatch sensing device. The system comprises a first binary device which determines whether or not power will be rendered available to energize the driving circuits for the inductance, together with a second binary device which determines the direction in which the inductance is driven. The system includes a signal processing network which first receives a signal indicative of the desired matched condition, inverts that signal, converts the resultant into a staircase signal, inverts and shapes the staircase signal into one having a smooth slope, and finally, through the use of an operational amplifier, converts the indication of zero-slope attainment into a pronounced negative-going signal or "tuned" indication which is utilized to control the binary devices in such a way that the toward minimum drive on the inductance is arrested substantially at the point of attainment of the desired match.



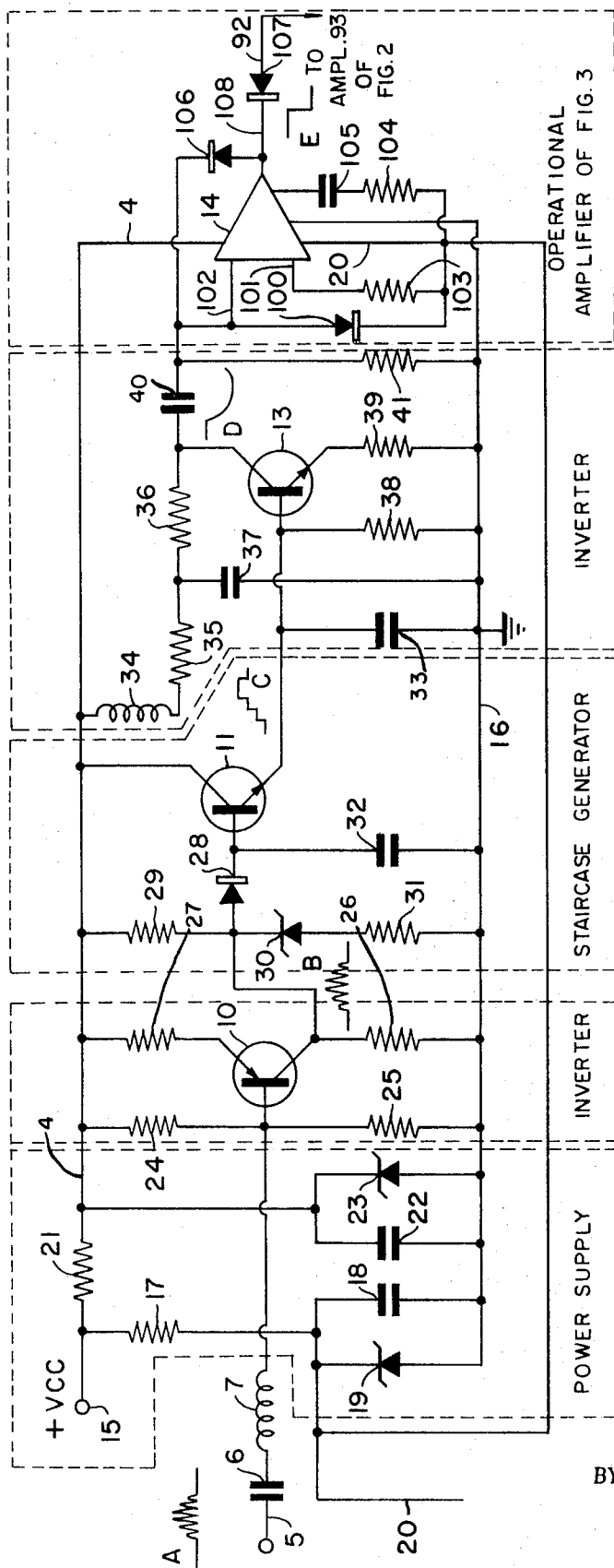


**Fig 1**

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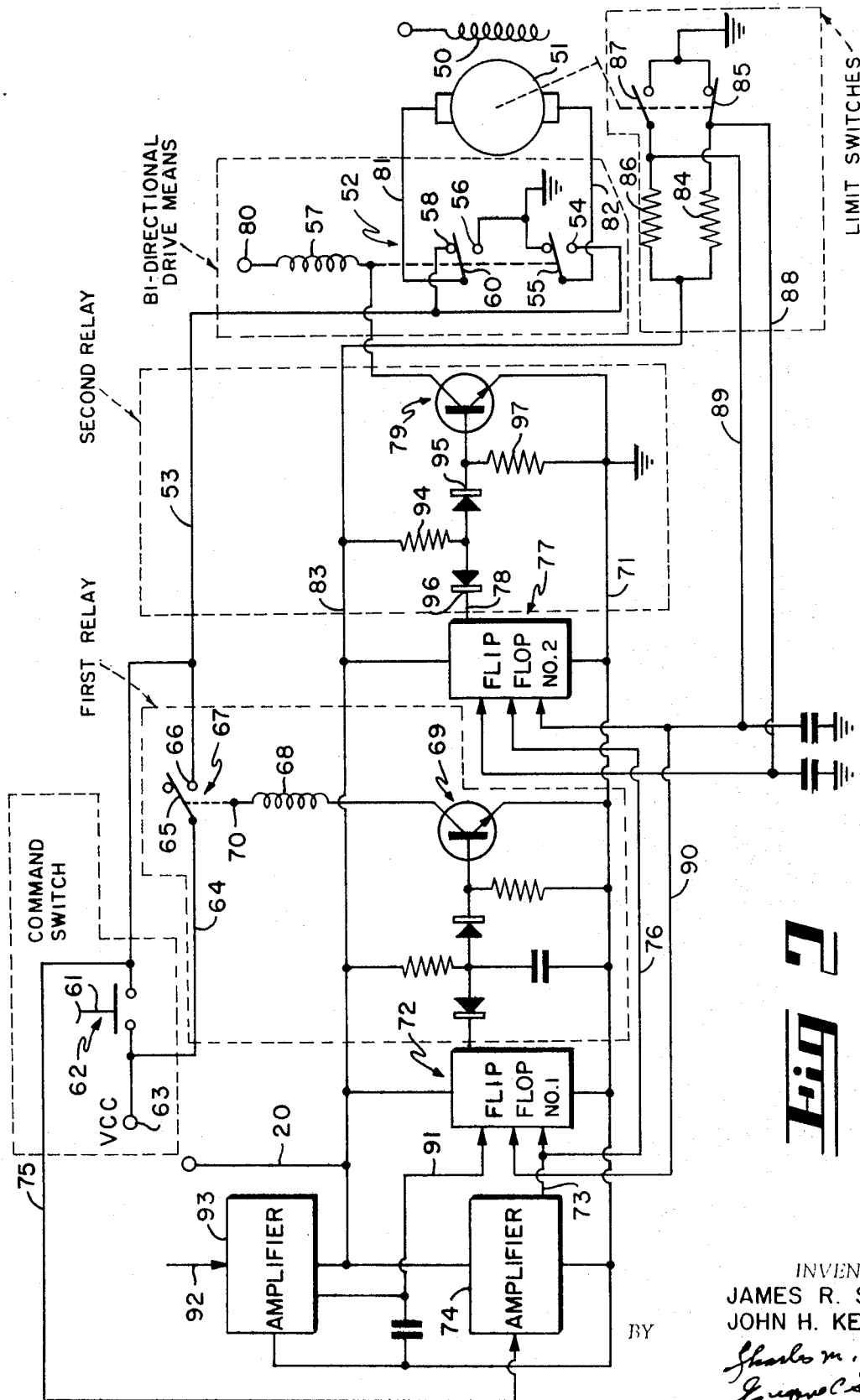
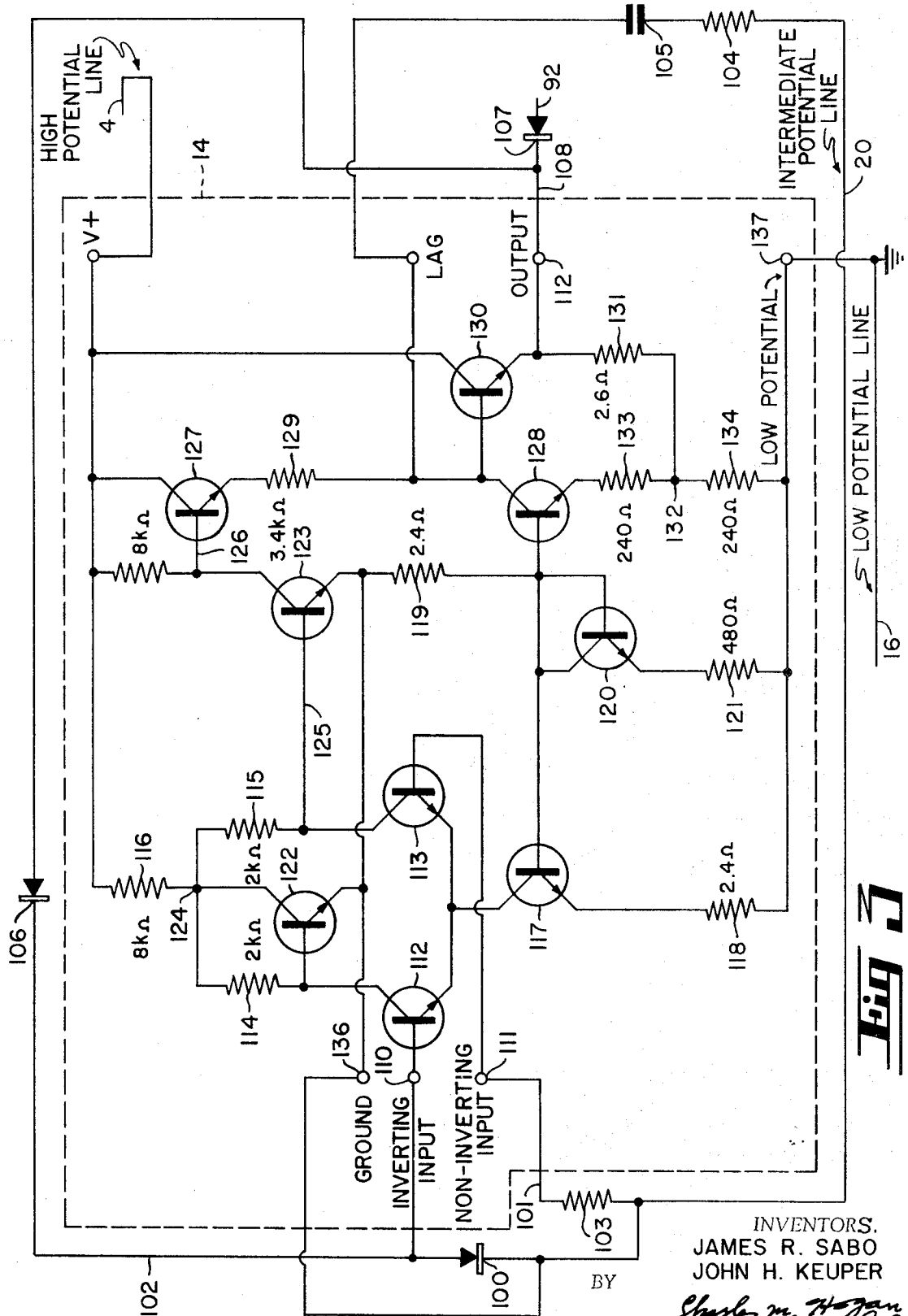


**Fig. 2**

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## SEMI-AUTOMATIC TUNING CIRCUIT FOR AN ANTENNA COUPLER

### BACKGROUND OF THE INVENTION

The present invention relates generally to impedance matching networks. A matching network is a combination of electrical and/or electronic elements useful in coupling a source impedance or a driver output line to a load input line, for efficient energy transfer—as for example, in coupling the output of a transmitter to an antenna load. The invention relates more specifically to antenna matching networks. In the preferred embodiment herein shown, the network responds to a manual “tune” order or instruction to drive an adjustable inductance in such a manner that a transmitter is coupled to an antenna load with the desired match. When match is achieved the drive on the inductance is arrested.

The invention is an improvement in the field of antenna coupling networks. This field includes substantial literature, of which an example is U.S. Pat. No. 3,390,337, issued June 25, 1968 to B. J. Beitman, Jr., entitled “Band Changing and Automatic Tuning Apparatus for Transmitter T-pad Output Filters,” assigned to the same assignee, Avco Corporation, as the present application and invention.

The primary object of the present invention is to provide a semiautomatic tuning system, which processes a signal obtained from a reflected radio frequency watt meter, by integrating it into a smooth waveform, then by using an operational amplifier, set up as a differentiator, produces a step function when the input signal passes through zero slope. The system includes binary devices and relays so constructed and arranged that, when the proper match is sensed, the drive on the inductance in the tuning network is arrested.

For a better understanding of the invention, together with other and further objects, advantages and capabilities thereof, reference is made to the following description of the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1, 2 and 3 are circuit schematics, of the major subsystems of a tuning system in accordance with the invention, FIG. 1 pertaining to the sensing and detector circuitry, FIG. 2 showing the inductance drive circuitry, and FIG. 3 being a prior art form of the operational amplifier shown generally in block form as a part of FIG. 1.

### DESCRIPTION OF THE INVENTION

First advertng briefly to FIG. 2, there is shown an inductance 50, adjusted to constitute the inductance parameter of the tuning circuit included in an antenna coupling system. This inductance is adjusted by a bidirectional electric motor 51 in such manner that an antenna coupler including the tuning network is appropriately matched to an antenna (not shown). Inductances adjustable in this manner and various types of antenna coupling networks are per se well known, as shown in the above-mentioned Bietman U.S. Pat. No. 3,390,337. Suffice it for the present to say that, in response to a manual order, motor 51 drives inductance 50 to the maximum value position, whereupon the inductance is driven in the reverse direction until it is arrested due to the action of an input signal appearing on line 5 (FIG. 1). This signal is in the form of a succession of lobes (see waveform A) which gradually increase in magnitude, so that the envelope assumes a zero slope at its maximum, and then diminishes in magnitude. The attainment of the zero slope signifies that a match occurs, the inductance then being of the proper value. Therefore the signal just referred to is processed in such a manner as to provide, at the output of amplifier 14 (FIG. 1) a sharply negative-going signal which is utilized to control the motor drive circuitry of FIG. 2 in such a manner as immediately to arrest the drive on the inductance. As previously indicated, the drive on the inductance, once the maximum is achieved, is

toward the minimum inductance position, until this arresting action occurs.

Attention is now specifically invited to FIG. 1, which comprises the following principal stages, in cascade: a phase inverter including transistor 10, a staircase signal generator including transistor 11, an inverting and smoothing network including transistor 13, and finally an operational amplifier 14 generally set up as a differentiator in such manner as, in response to the attainment of a zero slope and a slight rise in the signal at the output of transistor stage 13, to produce a negative-going signal indicated by the waveform E.

In FIG. 1 the conductor 16 is a ground line. Terminal 15 is the positive bias supply terminal, as indicated by the legend +V<sub>cc</sub>. A series combination of filter resistor 17 and Zener diode 19 comprises a voltage divider disposed between terminal 15 and ground 16, providing a stable direct current voltage on line 20, which constitutes a supply line for the motor driving subsystem of FIG. 2. Zener diode 19 is shunted by a filter capacitor 18.

Disposed between terminal 15 and ground is a voltage divider comprising resistor 21 and Zener diode 23, the latter being shunted by a filter capacitor 22, thereby to provide a stable potential on bus bar 4. A direct current bias potential for the base of inverter transistor stage 10 is provided by a voltage divider comprising resistors 24 and 25, connected between lines 4 and 16, the junction of these resistors being connected to the base of transistor 10. Emitter load resistor 27, the emitter collector circuit of PNP transistor 10, and collector load resistor 26 comprise a series circuit between lines 4 and 16.

Input waveform A is a semisinusoidal envelope containing a plurality of gradually ascending lobes, followed by gradually descending lobes. The maximum or zero slope portion of this envelope indicates a match. Waveform A represents the output of a reflected rf wattmeter output. This wattmeter (not shown) is so associated with the tuning network (in a manner well known to those skilled in the art) that, when the reflected wattmeter output is a minimum, corresponding to a minimum standing wave ratio, the FIG. 1 system issues a “tuned” command, indicated by the wave form E. This command indicates that the antenna has been properly matched to the output of the transmitter. The “tuned” command arrests the adjustment of the inductance 50 (FIG. 2) and prevents any further automatic tuning of the antenna coupler network. Fine tuning can be accomplished by a manual control (not shown).

The use of rf reflected power wattmeters to measure standing wave ratios, to sense mismatched and matched conditions, and to issue a signal or command when match is achieved, is well known to those skilled in the art. Reference is made, for example, to U.S. Pat. No. 3,366,883, issued Jan. 30, 1968, to Noel J. Griffin and George A. Perrero, entitled “Automatic Broad Band VSWR Power Control” and assigned to the same assignee as the present application and invention. Also to an article by Warren B. Bruene entitled “An Inside Picture of Directional Wattmeters” published in the Apr. 1959 issue of QST magazine.

The input signal, as indicated, appears at terminal 5 and is coupled into the base of PNP transistor by a series combination of capacitor 6 and rf choke 7. The inverter stage including transistor 10 inverts the waveform A so that the resultant waveform B appears on the collector of transistor 10. This waveform is applied to a staircase generator comprising diode 28, in series between the collector of transistor 10 and the base of transistor 11, a shunt capacitor 32 being connected on the cathode or output side of the diode, and a combination of Zener diode 30 and resistor 31 functioning as a limiter on the anode or input side of the diode 28. A resistor 29 is connected between high potential bus bar 4 and the junction of Zener diode 30 and detector diode 28. The network comprising the elements 28, 30 and 32 and current amplifier 11 transforms waveform B into a staircase waveform C which consists in steplike increments followed by a plateau and finally a descent, the significant portion of the wave form C being the

initiation of the descent. The NPN transistor 11, the base of which is connected to the junction between capacitor 32 and the cathode of diode 28, functions as a current amplifier. The purpose of capacitor 32 is to hold the ascending charge on the detector diode 28.

The collector of transistor 11 is connected to bus bar 4 and the emitter to the base of transistor 13. This base is provided with a base resistor 38 shunted by a filter capacitor 33. The element 39 is an emitter load resistor for transistor 13, the collector of which is in circuit with bus bar 4, via choke 34 and resistors 35 and 36. Resistors 35 and 36 comprise the collector load resistors for transistor 13. Series choke 34, series resistor 35, and shunt capacitor 37 comprise a filter. The output of the inverter stage comprising transistor 13 is an inverted and rounded form of wave form C. This output is shown at D. The significant portion of the output wave form is that portion, following the zero slope, when it begins to rise. This waveform is applied to an operational amplifier circuit generally indicated by the reference numeral 14 via a coupling network comprising a coupling capacitor 40 and a shunt resistor 41.

The operational amplifier is described in detail in the discussion of the FIG. 3 circuitry. Suffice it for the present to say that in response to the significant portion of waveform D there appears on output line 92 the negative-going portion of waveform E, and it is that portion which accomplishes the desired arrest of the adjustment of the inductance.

In the overall operation of the FIG. 1 circuit the voltage representing reflected power is coupled through capacitor 6 and RF choke 7 to the base of transistor 10. The base of transistor 10 is biased at 0.5 volt below the voltage on line 4. When transistor 10 conducts, the inverted output is fed to the base of emitter follower of transistor 11. Diode 28 and capacitor 32 filter out the pulsating voltage caused by the lack of a discharge path for capacitor 32. The voltage at the base of transistor 11 is then a voltage representing the peaks of the pulsating voltage. The output of transistor 13 is capacitively coupled from the collector, through capacitor 40 to input 102 of operational amplifier 14 (FIG. 3). Resistor 103 functions as a swamping resistor.

The operational amplifier does not respond to a negative-going voltage, but as the antenna matching network is driven through the correct tune point of the voltage, representing lowest reflected power at the input to the operational amplifier, the envelope slope changes toward a positive direction (see waveform A). When the voltage present at the output of transistor 13 attains zero slope, the output of the operational amplifier drops (see waveform E), causing voltage applied by amplifier 93 (FIG. 2) to "set" input 91 of flip-flop 72 to be low, in turn causing transistor 69 to cut off. Thus the tune relay 67 is deenergized and the drive motor is stopped.

The description now proceeds to FIG. 2 which shows the circuitry for adjusting the tuning inductor. The forward (toward maximum inductance) driving circuit comprises conductor 53, fixed contact 54 of relay 52, movable contact 55, and motor 51, and contacts 60 and 56 and ground. This circuit is in closed condition when coil 57 is energized. On the other hand, when coil 57 is deenergized the circuit for driving the motor in the reverse direction (so that the inductance is driven toward its minimum value) is closed. This circuit comprises conductor 53, fixed contact 58 of relay 52, movable contact 60, motor 51, contact 55, and ground. Therefore it will be seen that the conductor 53 and the relay 52, controlled by coil 57, in terms of immediate functionality, comprise means for causing the motor to drive in either selected direction. In terms of ultimate functionality they comprise means for driving the inductance toward either its maximum or minimum value.

The circuitry now under description operates in this general manner: when button 61 of a "tune" switch 62 is depressed, the operator thereby issues a "tune" command for the inductance to be adjusted to a desired value. As a preliminary to such adjustment, the inductance is always first placed in its maximum inductance position. Therefore the arrangements

are such that the depression of button 61 makes power available to the forward driving circuits. Now depression of the button 61 would accomplish this only instantaneously. A hold circuit is provided by a connection from the high potential terminal 15 of a source of power, via conductor 64, and movable contact 65 and fixed contact 66 of a relay 67, to conductor 53. That is, when relay 67 is energized, so as to close contact 65 on contact 66, then power is made available for the driving circuits of the motor 51.

The description now proceeds to the arrangements for energizing coil 68 of relay 67. The collector-emitter circuit of a transistor 69 is in series with coil 68 and the two elements are connected between a power source terminal 70 and a low potential line 71. When the collector-emitter circuit of transistor 69 is conductive the relay 67 is energized and contacts 65-66 are closed. The transistor 69 is rendered conductive by reason of the resetting of a flip-flop 72 which is coupled to the base of PNP type transistor 69. When this flip-flop 72 is reset to apply a positive going potential to the base of transistor 69, then transistor 69 is energized. The flip-flop has a resetting input conductor 73 from the output of an amplifier 74. When the tune button 61 is depressed an input conductor 75 to an amplifier 74 is energized so that the output lead 73 applies a resetting potential to the flip flop 72. Additionally, the lead 73 is connected by wire 76 to an additional flip-flop 77 and causes it to be reset. It is the resetting of flip-flop 77 that causes the forward driving circuit of the motor 51 to be closed.

Now the immediate function of the flip-flop 72 is to determine whether or not contacts 65 and 66 will be closed and therefore whether or not power will be available to energize the motor driving circuit. In other words, all that the flip-flop 72 does is to determine whether or not conductor 53 will be "hot."

Summarizing, a "tune" command by depression of button 61 energizes input 75 to amplifier 74 so that output 73 of the amplifier resets flip-flop 72 to energize transistor 69 to cause contacts 65 and 66 to be closed. Therefore it will be seen that the flip-flop 72 simply constitutes means for setting up a source of power for the motor driving circuitry, thereby determining whether or not power will be available to drive the motor.

The events which occur in response to a "tune" command have now been described with one exception. It has been stated that flip-flop 77 is reset by issuance of the command. The output 78 of flip-flop 77 is coupled to the base of transistor 79, the collector-emitter circuit of which is in series with coil 57, both the coil and the transistor being connected in series between a power terminal 80 and ground line 71. When flip-flop 77 is reset it causes coil 57 of relay 52 to be energized, whereby contacts 54 and 55 are closed to drive the inductance toward maximum value. In other words, the flip-flop 77 simply constitutes means for determining whether the motor will be driven in the forward or reverse direction. When coil 57 is energized the forward driving circuit is closed. When coil 57 is deenergized the reverse driving circuit is closed. While flip-flop 72 is a means for determining whether or not power will be available, flip-flop 77 is a means for determining whether wire 81 or wire 82 will have the higher voltage.

For the reasons stated the issuance of a command will cause the motor to drive the inductance to its maximum value position.

Now let it be assumed that such maximum value position is reached, i.e. the order to proceed to the maximum position has been complied with. Under that assumed condition, then flip-flop 77 should be set so that any further driving must be in the reverse direction. The circuitry is then put under the control of the detector and it is therefore necessary that driving power remain available. These requirements are tantamount to setting of flip-flop 77 and permitting flip-flop 72 to remain in its reset condition.

After the drive to maximum inductance has been attained, it has been shown that flip-flop 77 is set so that the inductance is driven toward minimum inductance.

The function of the detector circuitry of FIG. 1 is to continue this drive until a match is detected, so that the inductance driving motor should stop.

Upon the attainment of such match the detector output 92 (FIG. 1) furnishes to an amplifier 93 a signal (waveform E) of negative potential which is applied to input 91 of flip-flop 72 to set the flip-flop, whereupon wire 53 deenergized and the motor stops at the desired value of adjustment of the inductor.

It has been shown that flip-flop 72 has a reset input 73 which responds to a command from the tune switch (via amplifier 74) to make wire 53 hot and therefore make power available for driving the motor. Also that in response to a "tuned" signal on line 92 the set input 91 of flip-flop 72 causes the flip-flop to be set and wire 53 to become cold.

The flip-flop also has an inhibiting input 90 which operates in such a way that when the inductance is in its maximum inductance position flip-flop 72 is told to "stay put."

Flip-flop 77 has a "reset" input 76 which in response to a command from the tune switch closes the forward motor drive circuitry. It also has a "reset" input 88 which in response to the attainment of minimum inductance likewise causes to be closed the forward drive circuitry. It further has a "set" input 89 which causes flip-flop 77 to be "set" to close the reverse driving circuitry under the condition that the inductance is at maximum.

Attention is now invited to a bus bar 83, which is in series with line 20. There is a substantial positive potential on bus bar 83. That bus bar is in series with two series pairs of resistors and switches, those series pairs being in parallel. One pair comprises resistor 84 and switch 85. The other pair comprises resistor 84 and resistor 86 and switch 87. The switches 85 and 87 are, respectively, minimum and maximum limit switches. When the position of the motor and the inductor are such that a maximum inductance has been achieved, then the switch 87 closes, grounding input 89 to flip-flop 77, thereby setting flip-flop 77. Additionally, the input 90 to flip-flop 72 is grounded. This is an inhibiting input and it "tells" the flip-flop 72 to remain in reset condition.

Various means and methods for supplying limit switches to indicate positions of maximum and minimum inductance are well known to those skilled in the art, so that the mechanical construction and relationships of such switches to the motor and inductance need not be here shown.

The description will now be diverted to the events which occur if the inductance at any time happens to attain the minimum inductance position. For this hypothesis switch 85 closes and grounds input 88 to flip-flop 77, causing it to reset, thus assuring that any further drive on the inductance can only be toward maximum value.

The couplings between the flip-flops 72 and 77 and the respective transistors 69 and 79 are similar, so that only one will be described. Power for energizing transistor 79 flows from bus bar 83 via resistor 94 and diode 95, into the base of transistor 79, under the condition that the flip-flop 77 is reset, making output 78 more positive in potential. When the flip-flop 77 is set, the power flows through resistor 94 and diode 96 and flip-flop 77. That is, the flip-flop 77 does not apply the power for the transistor 79. It only controls such power and this is the reason for the provision of the steering network 94, 95, 96. Connected between the base of transistor 79 and line 71 is a resistor 97.

FIG. 3 shows a suitable form of operational amplifier for use in the system in accordance with the invention, together with associated connections establishing the relationship between FIGS. 1 and 3. The operational amplifier here shown is a Fairchild type  $\mu A702A$  arranged as a zero-crossing detector. The associated connections are similar to those described and shown at pages 166 and 167, particularly FIG. 3, of the publication entitled "Fairchild Semiconductor Linear Integrated Circuits Applications Handbook" published by Fairchild Semiconductor, 313 Fairchild Drive, Mountain View, California, in 1967 (Library of Congress Catalog No. 67-27446), the subject matter of said pages 166 and 167 being referred to and incorporated herein as fully as if set forth in full herein, in so far as it is under the caption "Zero-Crossing Detector."

A zero-crossing detector is a device that changes state immediately upon the passing through zero value (or through some average reference level) of an input signal. Note that a resistor 103 is connected by conductor 101 between the noninverting input 111 and a supply line of intermediate potential 20. The intermediate potential supply input 136 is connected to the intermediate potential line 20. Additionally, the lowest potential supply input 137 is connected to lowest potential line 16. Note further that there is a limiting diode 100 between the inverting input 110 and the intermediate potential line 20. A diode 106 is connected between the signal output line 108 and line 102 into inverting input 110. The output line 108 is coupled to line 92 via diode 107. External frequency compensation is provided between the "lag" terminal and the intermediate potential line 20 by a series combination of capacitor 105 and resistor 104. The relationship between FIGS. 1 and 3 of the drawings of the instant patent application will now be understood.

The block 14 in FIG. 1 corresponds to the block 14 in FIG. 3 which is substantially identical to the schematic diagram of the prior art Fairchild unit shown in FIG. 3 at page 35 of the aforementioned publication, incorporated herein by reference. This type of amplifier unit 14 is described in detail at pages 33-35 of said publication and the pin connections and characteristics are shown in the pamphlet entitled " $\mu A702A$  High Gain Wide Band DC Amplifier" published by Fairchild Semiconductor, 313 Fairchild Drive, Mountain View, California, in 1967.

The elements 104 and 105 provide frequency compensation of the lag-type. The diode 100 is a limiter diode to prevent latchup conditions. The diode 106 constitutes a feedback circuit.

The operational amplifier of FIG. 3 has a differential input 110, 111 and a single-ended output 108, the differential input terminals being designated at 110 and 111 and the single-ended output having the reference numeral 108. The positive-going trailing portion of waveform D at the inverting input 110 produces the negative output (waveform E) at the output line 92. This operational amplifier is characterized by a high input impedance, a very low output impedance, and high voltage gain and bandwidth. The differential input stage of this operational amplifier comprises transistors 112 and 113, having their emitters connected together and their bases individually connected to the inverting input 110 and the noninverting input 111, respectively. The collectors are provided with load resistors 114 and 115, respectively, and the other leads of these load resistors are connected to resistance 116, which goes to the high potential line 4. The emitters of the NPN transistors 112 and 113 are fed from a current source comprising NPN transistor 117, the emitter-collector circuit of which is connected, in series with a resistor 118, between the low potential line 16 and the emitters of transistors 112 and 113. This current source is biased from a voltage divider comprising resistor 119, a diode-connected NPN transistor 120, and a resistance 121. The transistor 120 provides compensation for the base-emitter voltage of the current source transistor 117.

NPN transistors 122 and 123 are identical transistors, the bases of which are fed from the common voltage point 124 through the identical input stage load resistors 114 and 115. When the input stage collector circuits are equal the collector currents of transistors 122 and 123 will likewise be equal. Transistor 122 functions as a unity gain amplifier which inverts the output of transistor 112 and combines it with the output of transistor 113 at the base of transistor 123. Therefore the differential gain of the input stage is used and a single-ended output 125 is obtained. Parenthetically the emitters of transistors 122 and 123 are in circuit with the intermediate potential line 20. The transistor 123 constitutes the second stage of the operational amplifier. Its gain is stable over a wide range of temperatures. The output 126 of the second stage cannot swing negative. Therefore a level shifting circuit incorporating NPN transistors is provided. That is, the output of the second stage is buffered with an emitter follower transistor 127. A current source comprising transistor 128 provides a

voltage drop across emitter resistor 129 of the buffer stage to cause the level shifting. An additional emitter follower transistor 130 is used in order to provide a low output impedance on line 108, in circuit with its emitter. The load resistor 131 of the emitter of transistor 130 is connected to the junction point 132 of the load resistors 133 and 134 of the emitter of transistor 128 to provide positive feedback.

While there has been shown and described what is at present considered to be the preferred embodiment of the invention, it will be understood by those skilled in the art that various changes and modifications may be made therein without departing from the scope of the invention as defined by the appended claims.

Having described our invention, we claim:

1. In a system in which an inductance is tuned to a value appropriate to a sensed matched condition, the combination of:
  - a command switch adapted to be closed to issue an electrical "tune" command;
  - a sensing device adapted to issue a "tuned" command;
  - a first binary device having a reset input, coupled to the command switch, and a set input, coupled to said sensing device,
 means, including a first relay having an output line and controlled by said first binary device, for making power available on said output line when said first binary device is reset and for shutting off power when said first binary device is set,
- a variable inductance,
- a two-state bidirectional drive means for said inductance, said drive means having forward and reverse states and being coupled to said output line, said drive means being normally in its reverse state,
- a second binary device having a first reset input, coupled to the command switch, and a second reset input and a set input,
- a second relay coupling said second binary device and said bidirectional drive means, said second binary device being reset and said second relay energized for forward

drive on the inductance and said second binary device set and said second relay deenergized for reverse drive on the inductance,

- the issuance of a command causing the first and second binary devices to be reset and power to be available on said output line and said second relay device to be energized and the drive means to change to its forward state and said inductance to be driven towards its maximum value,
- a first limit switch means coupled to the set input of the second binary device for setting the second binary device when the inductance attains its maximum value, whereby said second relay is deenergized and the drive means returns to its reverse state so that the inductance is then driven towards its minimum value,
- and a second limit switch means coupled to the second reset input of the second binary device for resetting the second binary device in the event that the inductance attains its minimum value, whereby the inductance is then driven towards maximum value,
- the issuance of a "tuned" command by the sensing device causing the first binary device to be set so that power is shut off and the drive on the inductance stops.
2. The combination in accordance with claim 1 in which the sensing device is adapted to receive a signal having a zero crossing characteristic, upon the attainment of the matched condition and in which the sensing device comprises:
  - means for inverting and transforming this signal into an amplified signal having a more pronounced zero crossing characteristic and
  - means including an operational amplifier for transforming the more pronounced signal into a triggered signal having a very sharp characteristic.
3. The combination in accordance with claim 2 in which the first binary device has an inhibiting input coupled to the first limit switch means so that when the inductance is driven to its maximum value the first binary device is ordered to remain in its reset condition.