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13/413,284 6 March 2012 (06.03.2012) US(71) Applicant: MEMC ELECTRONIC MATERIALS, INC.
[US/US]; 501 Pearl Drive, St. Peters, Missouri 63376 (US).

(72) Inventors: ZHANG, Guoqiang, D.; c/o MEMC Electronic Materials, Inc., 501 Pearl Drive, St. Peters, Missouri 63376 (US). LIBBERT, Jeffrey, L.; c/o MEMC Electronic Materials, Inc., 501 Pearl Drive, St. Peters, Missouri 63376 (US).

(74) Agents: KEPPEL, Nicholas, A. et al.; Armstrong Teasdale LLP, 7700 Forsyth Blvd., Suite 1800, St. Louis, Missouri 63105 (US).

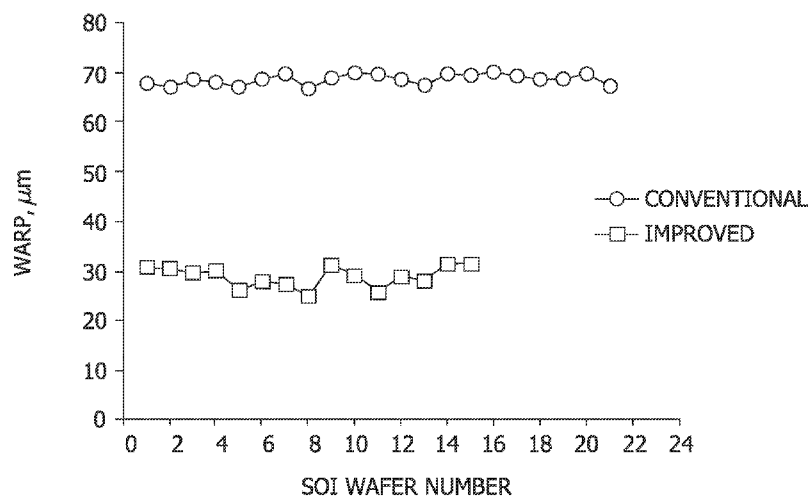
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(54) Title: A METHOD OF MANUFACTURING SILICON-ON-INSULATOR WAFERS



(57) Abstract: A method is provided for preparing multilayer semiconductor structures, such as silicon-on-insulator wafers, having reduced warp and bow. Reduced warp multilayer semiconductor structures are prepared by forming a dielectric structure on the exterior surfaces of a bonded pair of a semiconductor device substrate and a semiconductor handle substrate having an intervening dielectric layer therein. Forming a dielectric layer on the exterior surfaces of the bonded pair offsets stresses that may occur within the bulk of the semiconductor handle substrate due to thermal mismatch between the semiconductor material and the intervening dielectric layer as the structure cools from process temperatures to room temperatures.

A METHOD OF MANUFACTURING SILICON-ON-INSULATOR WAFERS

FIELD OF THE INVENTION

[0001] The field of the invention relates generally to a method of manufacturing multilayer semiconductor structure, e.g., silicon-on-insulator wafers, having reduced warp and bow.

BACKGROUND OF THE INVENTION

[0002] Semiconductor wafers are generally prepared from a single crystal ingot (e.g., a silicon ingot) which is trimmed and ground to have one or more flats or notches for proper orientation of the wafer in subsequent procedures. The ingot is then sliced into individual wafers. While reference will be made herein to semiconductor wafers constructed from silicon, other materials may be used to prepare semiconductor wafers, such as germanium, silicon carbide, silicon germanium, or gallium arsenide.

[0003] Semiconductor wafers (e.g., silicon wafers) may be utilized in the preparation of composite layer structures. A composite layer structure (e.g., a silicon-on-insulator (SOI) structure) generally comprises a handle wafer or layer, a device layer, and an insulating (i.e., dielectric) film (typically an oxide layer) between the handle layer and the device layer. Generally, the device layer is between 0.05 and 20 micrometers thick. In general, composite layer structures, such as silicon-on-insulator (SOI), silicon-on-sapphire (SOS), and silicon-on-quartz, are produced by placing two wafers in intimate contact, followed by a thermal treatment to strengthen the bond.

[0004] After thermal anneal, the bonded structure undergoes further processing to remove a substantial portion of the donor wafer to achieve layer transfer. For example, wafer thinning techniques, e.g., etching or grinding, may be used, often referred to as back etch SOI (i.e., BESOI), wherein a silicon wafer is bound to the handle wafer and then slowly etched away until only a thin layer of silicon on the handle wafer remains. (See, e.g., U.S. Pat. No. 5,189,500, which is incorporated in its entirety herein by reference.) A particular challenge in the preparation of SOI structures is the presence of warp or bow, particularly when a portion of the buried oxide (BOX) is contributed from the bonding surface of the device wafer. If the BOX

thickness is different from (typically more than) the thickness of the oxide on the backside of the support wafer, the SOI wafer will have high warp or bow which can be over the acceptable limit. High warp or bow can cause serious problems, such as handling in SOI wafering and fabrication lines.

BRIEF DESCRIPTION OF THE INVENTION

[0005] Briefly, therefore, the present invention is directed to a method of preparing a multilayer semiconductor structure. The method comprises the following steps in order: (a) forming a dielectric layer on a front surface of a semiconductor device substrate, the semiconductor device substrate comprising two major, generally parallel surfaces, one of which is the front surface of the semiconductor device substrate and the other of which is a back surface of the semiconductor device substrate, a circumferential edge joining the front and back surfaces of the semiconductor device substrate, and a central plane between the front and back surfaces of the semiconductor device substrate; (b) bonding the front surface of the semiconductor device substrate having the dielectric layer to a front surface of a handle substrate to thereby form a bonded structure, wherein the handle substrate comprises two major, generally parallel surfaces, one of which is the front surface of the handle substrate and the other of which is a back surface of the handle substrate, a circumferential edge joining the front and back surfaces of the handle substrate, and a central plane between the front and back surfaces of the handle substrate; and (c) forming a dielectric layer on the back surface of the handle substrate.

BRIEF DESCRIPTION OF THE DRAWING(S)

[0006] FIG. 1 is a graph depicting the measured warp in SOI structures prepared according to a conventional process (●) and the measured warp in SOI structures prepared according to the method of the present invention (■). The SOI structures were prepared according to the method described in Example 1.

DETAILED DESCRIPTION OF THE EMBODIMENT(S) OF THE INVENTION

[0007] The present invention is directed to a method for manufacturing a multilayer semiconductor structure, e.g., a silicon-on-insulator (SOI) multilayer structure, with overall reduced warp and bow in the final semiconductor composite multilayer structure. The multilayer semiconductor structure comprises a device substrate, a handle substrate, and an intervening dielectric layer. In some embodiments, the method of the present invention is directed to the manufacture of a silicon-on-insulator structure comprising an oxide layer in between an active silicon layer of a device substrate and a handle substrate. The oxide layer is commonly referred to as Buried Oxide (or "BOX"). According to the method of the present invention, the BOX may be prepared on the device substrate, the handle substrate, or on both substrates prior to substrate bonding.

[0008] During manufacture of a silicon-on-insulator multilayer structure, a dielectric layer, e.g., an oxide layer, may be prepared on the front surface of the handle substrate. The formation of a dielectric layer on the surface of a semiconductor substrate, i.e., the front surface of either or both of the device substrate and the handle substrate, may cause stresses in the bulk of the substrate, which may or may not be sufficiently offset in the bulk of the substrate. The dielectric layer may thus induce stresses that may result in a final SOI having warp and bow. Stresses may form in a device and/or handle substrate as the wafer cools from the temperature of dielectric formation to room temperature.

[0009] A dielectric layer, typically an oxide layer, may be formed one or both of the front surfaces of the device substrate and the handle substrate at high temperature. Herein, the front surfaces of the substrate refer to the major surfaces of the substrates that, when bonded, form the interior surfaces of the bonded structure. Back surfaces thus refer to the major surfaces that become the exterior surfaces of the bonded structure. The temperature of deposition generally exceeds 500°C and may even exceed 1000°C. In some embodiments, the dielectric layer(s), e.g., oxide layer(s), may be deposited to substantially equal thickness and density on both of the front surfaces of the device and handle substrates. When the substrates with dielectric deposited on the front surfaces is moved into a room temperature environment, both the

substrate (e.g., silicon) and the dielectric layer (e.g., silicon dioxide) contract, but at different rates. The different rates of contraction are due to the different coefficients of thermal expansion of the native substrate material and the deposited dielectric layer. Silicon, for example, has a coefficient of thermal expansion of 2.6 ppm/°C. Silicon dioxide has a coefficient of thermal expansion of 0.5 ppm/°C. In view of these different coefficients, silicon expands or contracts more than silicon dioxide in response to changes in temperature. The contraction differential inputs stress into the substrate as the substrate having dielectric deposited thereon cools from the temperature of deposition to room temperature.

[0010] In some manufacturing processes, a substrate, either the device or handle or both, may be prepared with dielectric layers (e.g., oxide layers) on both the front and the back surfaces. In such embodiments, the stresses induced by differential contraction in front surface dielectric layer may be offset by the stress from the backside surface dielectric layer. The overall stress on the substrate may thus be minimized. However, when the dielectric layer is removed from one side of the substrate while the opposite surface of the substrate has dielectric layer, stresses may input in the substrate during subsequent high temperature process steps due the difference in contraction between the native substrate structure and the remaining dielectric on the surface having dielectric.

[0011] In still other manufacturing processes, stress may be inputted into a substrate after bonding of the device and handle wafers and during the thinning process. Herein, the oxide layer on the backside surface of the device wafer is removed, the buried oxide (BOX) contributed partially from the device wafer is thicker than the oxide layer on the backside surface of the handle wafer. In this case, the stress from the BOX may not be fully offset by the stress from the backside oxide of the handle wafer. Unbalanced stresses on both surfaces may result in warp or bow in the substrate.

[0012] According to the method of the present invention, stresses induced by an intervening dielectric layer in a bonded structure may be offset by oxidizing the back, exterior surface of the handle substrate after the handle substrate is bonded to the device substrate to form a bonded structure. Offsetting the stresses induced by thermal expansionary mismatch between the native silicon substrate and a dielectric layers by

depositing dielectric on both the front and back surfaces of the bonded pair results in a final SOI structure exhibiting minimum amount of warp or bow, approximating that of the support substrate before oxidation. In some embodiments, the method of the present invention is therefore directed to offsetting the stresses contributed by the dielectric layer, e.g., the BOX layer, thus enabling the preparation of low warp or bow semiconductor multilayer structures.

[0013] In some embodiments in which a silicon-on-insulator multilayer structure is manufactured, dielectric layers, e.g., oxide layers, may be prepared on both the front surface of the handle substrate and on the front surface of the device substrate. Accordingly, the BOX layer may comprise a combination of oxide layers from the handle substrate and device substrate. A BOX layer prepared by combining two oxide layers may be preferable in some manufacturing processes due to, e.g., a desire to provide space between the active silicon layer and the bonding interface since the bonding interface may be contaminated with metals and/or particles, which may diffuse into the active silicon layer, thereby impairing the device's electrical properties. A BOX layer may be prepared by combining oxide layers from the handle substrate and device substrate also due to certain applications, wherein the device surface is roughened or uneven due to processing or patterning before bond. In order to cover the uneven or rough front surface on the device wafer, oxide, such as chemical vapor deposition oxide (CVD oxide), may be deposited on the device wafer prior to bonding. In embodiments wherein the BOX is formed from oxide layers deposited on the front surfaces of both the device substrate and the handle substrate, the resultant multilayer SOI structure may have a BOX that contributes stresses to the structure that may not be sufficiently offset by dielectric on the back surface(s) of the handle and/or device substrates since the BOX layer may be significantly thicker than the oxide layer on the back surface(s) of the handle and/or device substrates. The inability of dielectric on the back surface(s) of the device and/or handle substrates to offset the stresses contributed by the BOX may result in an SOI multilayer structure having warp or bow over an acceptable limit, and the structure may take a domed warp shape. SOI structures with high warp or bow pose serious problems in SOI wafering line and in fabrication line, such as handling. For example, a chip manufacturer's maximum tolerance may allow

warp no greater than about 60 micrometers, while some manufacturing processes may allow warp no greater than 30 micrometers. The method of the present invention enables the manufacture of SOI structures having warp within these chip manufacturing process tolerances. Stated another way, multilayer semiconductor structures, such as SOI structures, prepared according to the method of the present invention have warp no greater than 35 about micrometers, no greater than about 30 micrometers, no greater than about 28 micrometers, or even no greater than about 25 micrometers.

[0014] In some embodiments, the present invention is directed to a method of preparing semiconductor multilayer structures comprising a dielectric layer having low warp and bow. The dielectric layer intervening a handle substrate and a device substrate is generally a source of stress that may contribute to the warp and bow of the final multilayer structure. According to the method of the present invention, stresses contributed by a dielectric layer, e.g., a relatively thick BOX layer, may be offset by the deposition of a dielectric layer, e.g., an oxide layer, on the back surfaces of the device substrate, the handle substrate, or on both back surfaces of the device substrate and the handle substrate. The oxide layers deposited on the back surfaces of the device substrate and/or the handle substrate may be deposited after bonding and before thinning the device wafer of the bonded pair. In preferred embodiments, oxide is deposited on both backside surfaces of the device substrate and the handle substrate. Through the method of the present invention, backside oxide on the handle substrate may be adjusted to counter-balance stresses contributed by the BOX. Therefore, the final SOI structure warp or bow may be maintained within a tolerable level. As an added advantage, the bond between the substrates may be strengthened during the furnace cycle where thermal oxide is grown on the bonded pairs of wafers or densification of chemical vapor deposition oxide (CVD oxide) on the bonded pairs of wafers. The strengthened bond may help the thinning process on the device wafers during SOI wafering, for instance reducing active silicon layer delamination.

[0015] The substrates for use in the present invention include a monocrystalline donor substrate and a monocrystalline handle substrate. In general, the monocrystalline substrates comprises two major, generally parallel surfaces, one of which is a front surface of the substrate and the other of which is a back surface of the

substrate, a circumferential edge joining the front and back surfaces, and a central plane between the front and back surfaces. Prior to any operation as described herein, the front surface and the back surface of the substrate may be substantially identical. A surface is referred to as a "front surface" or a "back surface" merely for convenience and generally to distinguish the surface upon which the operations of method of the present invention are performed. In the context of the present invention, "front surface" refers to the major surface of the substrate that becomes an interior surface of the bonded structure. "Back surface" refers to the major surface that becomes an exterior surface of the bonded structure.

[0016] The monocrystalline donor and handle substrates may be semiconductor wafers. In preferred embodiments, the semiconductor wafers comprise a material selected from the group consisting of silicon, silicon carbide, silicon germanium, silicon nitride, silicon dioxide, gallium arsenic, gallium nitride, indium phosphide, indium gallium arsenide, germanium, and combinations thereof. In particularly preferred embodiments, the semiconductor wafers comprise a wafer sliced from a single crystal silicon wafer which has been sliced from a single crystal ingot grown in accordance with conventional Czochralski crystal growing methods. Such methods, as well as standard silicon slicing, lapping, etching, and polishing techniques are disclosed, for example, in F. Shimura, *Semiconductor Silicon Crystal Technology*, Academic Press, 1989, and *Silicon Chemical Etching*, (J. Grabmaier ed.) Springer-Verlag, N.Y., 1982 (incorporated herein by reference). Preferably, both device wafer and support wafer have mirror-polished front surface finishes that are free from surface defects, such as scratches, large particles, etc. Wafer thickness generally varies from about 250 micrometers to about 1500 micrometers, with thicknesses in the range of about 500 micrometers to about 1000 micrometers, such as about 725 micrometers, being preferred.

[0017] According to the method of the present invention, a dielectric layer, e.g., an oxide layer or a nitride layer, may be formed on a front surface of a device substrate, a front surface of a handle substrate, or on both front surfaces of a device substrate and a handle substrate. Dielectric layers prepared by oxidation generally deposit a layer of silicon dioxide (SiO_2) on the wafer surface while nitridation generally

deposits a layer of silicon nitride (Si_3N_4) on the wafer surface. In general, an oxide layer may be formed on a silicon substrate generally by thermal oxidation or chemical vapor deposition.

[0018] In some embodiments, the dielectric layer comprises a silicon oxide (SiO_2) layer formed on a front surface of a device substrate, a front surface of a handle substrate, or on both front surfaces of a device substrate and a handle substrate by thermally growing oxide on the silicon wafer surface in a furnace at elevated temperature. The thermal oxidation of a front surface of a device substrate, a front surface of a handle substrate, or on both front surfaces of a device substrate and a handle substrate is generally performed in a vertical furnace with steam (H_2O or mixture of hydrogen and oxygen gas) and/or oxygen at a temperature in excess of about 700°C , generally between 800°C and about 1200°C . The thermal oxidation is typically performed in a vertical furnace, e.g., commercially available AMS400. The oxidizing ambient may also contain several percent of hydrochloric acid (HCl). The chlorine removes metal ions that may occur in the oxide. Thermal oxidation of a front surface of a device substrate, a front surface of a handle substrate, or on both front surfaces of a device substrate and a handle substrate generally proceeds until a silicon dioxide layer is formed having a thickness between about 50 nanometers and about 5000 nanometers, preferably between about 100 nanometers and about 2000 nanometers.

[0019] In some embodiments, the dielectric layer comprises a silicon oxide (SiO_2) layer formed on a front surface of a device substrate, a front surface of a handle substrate, or on both front surfaces of a device substrate and a handle substrate by chemical vapor deposition. The deposition of CVD oxide on the front surface of the device substrate, the handle substrate or both may be performed in a furnace in an ambient comprising a silicon-containing gas and an oxidant. In some embodiments, the ambient atmosphere comprises silane (SiH_4) and oxygen (O_2). In some embodiments, the ambient atmosphere comprises dichlorosilane (SiCl_2H_2) and nitrous oxide (N_2O). In some embodiments, the ambient atmosphere comprises tetraethylorthosilicate ($\text{Si}(\text{OC}_2\text{H}_5)_4$). CVD oxide may be deposited on the wafers in a CVD tool, e.g., commercial available Walker Johnson. Chemical vapor deposition of the oxide layer generally occurs at temperatures between about 300°C and about 900°C . The

temperature may vary depending upon the particular recipe selected for CVD oxide. For example, silane (SiH_4) and oxygen (O_2) generally deposits silicon dioxide at temperatures between about 300°C and about 500°C . Dichlorosilane (SiCl_2H_2) and nitrous oxide (N_2O) generally deposits silicon dioxide at temperatures between about 700°C and about 900°C . Tetraethylorthosilicate ($\text{Si}(\text{OC}_2\text{H}_5)_4$) generally deposits silicon dioxide at temperatures between about 600°C and about 800°C . Chemical vapor deposition of the oxide layer on a front surface of a device substrate, a front surface of a handle substrate, or on both front surfaces of a device substrate and a handle substrate generally proceeds until a silicon dioxide layer is formed having a thickness between about 50 nanometers and about 5000 nanometers, preferably between about 300 nanometers and about 2000 nanometers. The chemical vapor deposition oxide layer is generally densified by annealing the substrate in a furnace to increase the strength of the oxide layer. Densification generally occurs at a temperature between about 1000°C and about 1200°C for several hours, typically 2 hours.

[0020] The front surfaces of substrates may be oxidized by either thermal oxidation or densified CVD oxide. The proper oxidation technique may depend, at least in part, on the requirements of the SOI device fabrication process. For example, if the device is highly sensitive to electrical properties and/or metals between the silicon (device layer) and the silicon dioxide interface, thermal oxidation is generally applied. In some embodiments in which high uniformity (e.g. < 100 Angstroms) of the oxide layer is required, the device and/or handle substrate surfaces may be thermally oxidized.

[0021] According to the method of the present invention, the front surface of the device substrate and the front surface of the handle substrate are bonded. Herein, the front surface of the device substrate, the front surface of the handle substrate, or both may contain a dielectric layer, e.g., a silicon dioxide layer, deposited by thermal oxidation and/or chemical vapor deposition. The silicon dioxide layer may have a thickness generally between about 50 nanometers and about 5000 nanometers, such as between about 100 nanometers and about 2000 nanometers. Bonding occurs by bringing the front surfaces of the device substrate and the handle substrate together into intimate contact to thereby form a bonded structure. Bonding takes part in a bonding

tool, for example, a commercially available EV850 (made by Electronic Vision), in which a device substrate and a support substrate are bonded together. Since the mechanical bond is relatively weak, the bonded structure is further annealed to solidify the bond between the donor wafer and the handle wafer. Post bond heat treatment can be performed in an electric oven, such as a commercially available Blue M. The bonded structure may be heat-treated at a temperature between about 200°C and about 1000°C, preferably at a temperature of about 500°C. The thermal treatment may have a duration between about 1 hour and about 12 hours, preferably for about 6 hours.

[0022] In some embodiments, the bonded multilayer structure is subjected to a post bond anneal. A post-bond anneal further increases the bonding strength as anneal temperature is significantly higher than that of post-bond heat treatment. The post-bond anneal may occur in a temperature between about 800°C and about 1200°C, preferably at a temperature of about 1150°C. The post-bond anneal may have a duration between about 1 hour and about 10 hours, preferably for about 4 hours.

[0023] After the front surfaces of the device substrate and the handle substrate have been bonded, a dielectric layer, e.g., an oxide layer, is formed on the back surface of the device substrate, the back surface of the handle surface, or both back surfaces of the device substrate and the handle substrate. The back surface of the device substrate, the handle substrate, or both may be oxidized by thermal oxidation or chemical vapor deposition. The same thermal oxidation and CVD oxidation processes may be used to oxidize the back surfaces of the substrates in the multilayer structure which were employed to oxidize the front surfaces of the handle substrate, device substrate, or both. In general, the thickness of the oxide layers on the back surface of the device substrate, the back surface of the handle surface, or both back surfaces of the device substrate and the handle substrate may be between about 50 nanometers and about 5000 nanometers, preferably between about 500 nanometers and about 2000 nanometers. The thickness of the oxide layer or layers deposited on one or both back surfaces are determined in part by the thickness of the BOX layer bonding the front surfaces of the device substrate and handle substrate. The thickness of the BOX layer and the cumulative thickness of the backside surface silicon dioxide layer(s) are preferably comparable in thickness in order to adequately offset stresses induced by the differential coefficients

of thermal expansion of the native silicon and the silicon dioxide. In embodiments wherein the BOX layer is prepared by densified CVD oxide, the cumulative thickness of the backside surface silicon dioxide layers may be determined empirically by a calibration method in order to optimize the cumulative thickness necessary to offset stresses induced by the densified CVD oxide BOX layer.

[0024] In some embodiments, the back surface of the device substrate, the handle substrate, or both may be oxidized by thermal oxidation. In embodiments wherein intervening dielectric layer, e.g., a BOX layer, and the back surface of the device substrate, the handle substrate, or both were oxidized by thermal oxidation, the thermal oxide thickness to be grown on the bonded pair generally equal to the thickness of thermal oxide used to form the BOX layer between the bonded front surfaces. Simply stated, the process recipe of thermal oxidation on the bonded pair is about the same as the process recipe that is used to grow thermal oxide on the device wafer prior to bonding.

[0025] In some embodiments in which the dielectric layer, e.g., the BOX layer, is prepared by densified chemical vapor deposition oxidation, the proper thickness of the thermal oxide formed on the back surface of the device substrate, the handle substrate, or both to counter-balance the stress of the CVD oxide layer should be determined empirically since densified CVD oxide has less stress while compared with thermal oxide. The proper thickness of thermal oxide that is needed to counter-balance densified CVD oxide is determined experimentally. For instance, if the densified CVD oxide layer thickness is about 1 micrometer, a calibration series of back surface oxide thicknesses (e.g. 0.3 μm , 0.5 μm , 0.7 μm , etc.) may be grown on the surfaces of the tested substrates. Warp/bow is measured to determine which thickness of thermal oxide gives the lowest warp/bow. The lowest warp/bow translates into the proper backside surface oxide thickness to properly offset the stresses induced by the CVD oxide layer. Generally, the thickness of thermal oxide to be grown on the bonded pair is somewhat less than the thickness of the densified oxide on the bonding surface of the device wafer.

[0026] Upon formation of a dielectric layer, e.g., a silicon oxide layer, on the back surface of the back surface of the device substrate, the back surface of the handle

surface, or both back surfaces of the device substrate and the handle substrate, the back surface of the device substrate is thinned by grinding, polishing, etching, or any combination of surface treatments. In general, the device substrate is thinned until the device substrate has a thickness between about 1 micrometer and about 300 micrometers, such as between about 3 micrometers and about 300 micrometers, or about 3 micrometers and 70 micrometers, such as about 7 micrometers. The thickness of thinned device substrate depends upon the final end use of the SOI structure and is determined by customer specifications. Surface grinding typically uses a single-side grinder, such as Disco grinder DFG-830 made by Disco Incorporation. In the surface grinding, most materials of the device wafer are removed from the backside of the device wafer after bonded. Edge treatment could include several steps, for instance, edge grinding and device wafer edge etching. Edge grinding uses typically an edge profiler, such as STC EP-5800RHO.

[0027] In embodiments wherein the back surface of the semiconductor device substrate is etched, alkali etchants or acidic etchant are applicable. Alkali etchants are preferred. Acidic etchants include, e.g., a mixture of hydrochloric acid, nitric acid, phosphoric acid, and hydrofluoric acid. Alkali etchants include KOH and NaOH. Etching processes are generally known in the art.

[0028] In embodiments wherein the back surface of the semiconductor device substrate is polished, either a single-side or double-side polishing or both can be applied to polish the back surface. Single-side polishing may be accomplished using a commercially available tool such as Strasbaugh Mark 9-K, while double-side polishing use a commercially available tool such as PeterWolters AC2000-P.

[0029] After all process steps are completed, the SOI wafers are inspected for all the required parameters, such as flatness, particles, etc. before final package for customers. In general, multilayer semiconductor structures, such as SOI structures, prepared according to the method of the present invention have warp no greater than 35 micrometers, no greater than 30 micrometers, no greater than about 29 micrometers, or even no greater than about 28 micrometers. In some embodiments the warp may be less than about 26 micrometers, less than about 25 micrometers, or even less than about 24 micrometers.

[0030] Having described the invention in detail, it will be apparent that modifications and variations are possible without departing from the scope of the invention defined in the appended claims.

[0031] The following non-limiting examples are provided to further illustrate the present invention.

Example 1. Preparation of Reduced Warp/Bow SOI Structures

[0032] Multiple device wafers and the handle wafers were bonded. The bonded structures were heat-treated in a Blue M oven for 6 hours at the temperature of 500°C. The post heat-treated bonded structures were coated with CVD oxide on both exterior, major surfaces. More specifically, the back surfaces of the bonded device wafer and handle wafer were both oxidized by CVD oxidation. CVD oxidation was carried out by decomposing tetraethyl orthosilicate ($\text{Si}(\text{OC}_2\text{H}_5)_4$) in an CVD tool (AMAT Precision 5000, SVG Thermal Vertical Furnace) at a temperature of about 700°C. The CVD oxide thickness was about 1 micrometer. The bonded structures were annealed at a temperature of 1000°C for about 2 hours in an anneal furnace (AMS 400, SVG Thermal Vertical Furnace). The total thickness of the oxide layers on the back surfaces of the device and handle wafers was substantially the same as the thickness of the BOX layer. The device layer was thinned, including grinding, etching, polishing and cleaning to achieve the top silicon layer thickness, uniformity and surface quality per customer specifications. See FIG. 1, which is a graph depicting the measured warp in several bonded structures prepared according to the conventional process in which the exterior major surfaces of the bonded structure were not subjected to an additional oxidation process (●) and the measured warp in several bonded structures prepared according to the above-described process of the invention (■). The measured warp in conventionally prepared bonded structures average about 69 micrometers, with some structures exhibiting warp over 70 micrometers. In contrast, the measured warp in bonded structures prepared according to the method of Example 1 averaged about 29 micrometers, with some structures exhibiting warp less than 27 micrometers, or even less than 25 micrometers.

[0033] This written description uses examples to disclose the invention, including the best mode, and also to enable any person skilled in the art to practice the invention, including making and using any devices or systems and performing any incorporated methods. The patentable scope of the invention is defined by the claims, and may include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims if they have structural elements that do not differ from the literal language of the claims, or if they include equivalent structural elements with insubstantial differences from the literal languages of the claims.

WHAT IS CLAIMED IS:

1. A method of preparing a multilayer semiconductor structure, the method comprising the following steps in order:

(a) forming a dielectric layer on a front surface of a semiconductor device substrate, the semiconductor device substrate comprising two major, generally parallel surfaces, one of which is the front surface of the semiconductor device substrate and the other of which is a back surface of the semiconductor device substrate, a circumferential edge joining the front and back surfaces of the semiconductor device substrate, and a central plane between the front and back surfaces of the semiconductor device substrate;

(b) bonding the front surface of the semiconductor device substrate having the dielectric layer to a front surface of a handle substrate to thereby form a bonded structure, wherein the handle substrate comprises two major, generally parallel surfaces, one of which is the front surface of the handle substrate and the other of which is a back surface of the handle substrate, a circumferential edge joining the front and back surfaces of the handle substrate, and a central plane between the front and back surfaces of the handle substrate; and

(c) forming a dielectric layer on the back surface of the handle substrate.

2. The method of claim 1 wherein the semiconductor device substrate comprises a material selected from the group consisting of silicon, silicon carbide, silicon germanium, silicon nitride, silicon dioxide, gallium arsenic, gallium nitride, indium phosphide, indium gallium arsenide, germanium, and combinations thereof.

3. The method of claims 1 or 2 wherein the semiconductor device substrate comprises a silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method.

4. The method of claim 3 wherein the dielectric layer formed on the front surface of the semiconductor device substrate comprises silicon dioxide.

5. The method of claim 4 wherein the dielectric layer comprising silicon dioxide has a thickness between about 50 nanometers and about 5000 nanometers.
6. The method of any of claims 1-5 wherein the handle substrate is a silicon wafer.
7. The method of claim 6 wherein the handle substrate further comprises a dielectric layer on the front surface thereof.
8. The method of claim 7 wherein the dielectric layer comprises silicon dioxide and has a thickness between about 50 nanometers and about 5000 nanometers.
9. The method of claim 6 wherein the dielectric layer formed on the back surface of the handle substrate during step (c) comprises silicon dioxide.
10. The method of claim 9 wherein the dielectric layer comprising silicon dioxide has a thickness between about 50 nanometers and about 5000 nanometers.
11. The method of any of claims 1-10 wherein step (c) further comprises concurrent formation of a dielectric layer on the back surface of the semiconductor device substrate.
12. The method of claim 11 wherein the dielectric layers formed on the back surfaces of both the handle substrate and the semiconductor substrate comprises silicon dioxide.
13. The method of claim 12 wherein the dielectric layers comprising silicon dioxide have thicknesses between about 50 nanometers and about 5000 nanometers.
14. The method of any of claims 1-13 further comprising step (d) thinning the semiconductor device substrate.

15. The method of claim 14 wherein the semiconductor device substrate is thinned by grinding, etching, polishing or any combination of such techniques the back surface of the semiconductor device substrate.

16. The method of claim 15 wherein after step (d), the thinned semiconductor device substrate has a thickness between about 3 micrometers and about 70 micrometers.

17. The method of any of claims 1-16 wherein the multilayer semiconductor structure has warp no greater than 30 micrometers.

FIG. 1

