(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 January 2020 (30.01.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/023907 A1

(51) International Patent Classification:
H01L 21/768 (2006.01) *H01L 21/027* (2006.01)

(21) International Application Number:
PCT/US2019/043729

(22) International Filing Date:
26 July 2019 (26.07.2019)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/703,762 26 July 2018 (26.07.2018) US

(71) Applicant: **LAM RESEARCH CORPORATION** [US/US]; 4650 Cushing Parkway, Fremont, California 94538 (US).

(72) Inventors: **OBERST, Justin**; 11608 SW Willet Terrace, Beaverton, Oregon 97007 (US). **BUCKALEW, Bryan L.**; 10170 SW Hedges Court, Tualatin, Oregon 97062 (US). **BANIK, Stephen J.**; 3833 SW Bond Avenue #512, Portland, Oregon 97239 (US).

(74) Agent: **SCHEER, Bradley W.** et al.; Schwegman, Lundberg & Woessner, P.A., P.O. Box 2938, Minneapolis, Minnesota 55402 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: ALTERNATIVE INTEGRATION FOR REDISTRIBUTION LAYER PROCESS

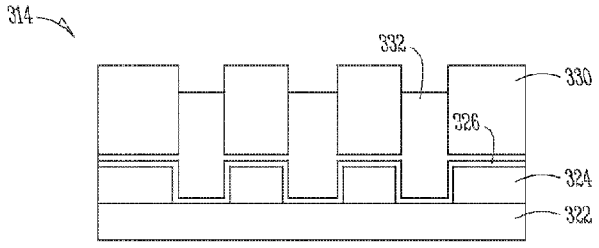


Fig. 3G

(57) **Abstract:** In one example, a method for redistribution layer (RDL) process is described. A substrate is provided. A dielectric layer is deposited on top of the substrate. The dielectric layer is patterned. A barrier and copper seed layer are deposited on top of the dielectric layer. A photoresist layer is applied on top of the barrier and copper seed layer. The photoresist layer is patterned to correspond with the dielectric layer pattern. Copper is electrodepositing in the patterned regions exposed by the photoresist layer. The photoresist layer is removed. The copper and seed barrier are etched.

WO 2020/023907 A1

ALTERNATIVE INTEGRATION FOR REDISTRIBUTION LAYER PROCESS

RELATED APPLICATION

[0001] The present application claims priority from United States Provisional Patent Application No. 62/703,762, filed July 26, 2018, which is herein incorporated by reference in its entirety.

FIELD

[0002] The present disclosure relates generally to a redistribution layer (RDL) process, and in particular to systems and methods for alternative integration for RDL.

BACKGROUND

[0003] In a conventional RDL process flow, both a thin barrier and copper seed layer are deposited onto an incoming substrate (most often silicon). A photoresist layer is applied, via spin coating or lamination. The photoresist is exposed, developed, and descummed to expose the copper seed in an RDL pattern. This patterned area is then filled with copper via an electroplating process. After electroplating, the photoresist is then removed. To electrically isolate the electroplated RDL patterns, the copper seed and barrier layer are removed last. During the seed removal step (via wet chemical etch), the etchant attacks the copper seed at the pattern/seed interface producing undercut beneath the RDL pattern. Undercut can reduce the mechanical integrity of the RDL pattern and produce poor signal integrity. There are two types of undercut that can occur: (1) seed underneath the RDL pattern is etched and (2) both seed and base of electroplated RDL are etched. As RDL dimensions continue to shrink, this issue is becoming more prominent as the undercut occurs under a larger area of the RDL.

[0004] The present disclosure seeks to address these drawbacks. It should be noted that the information described in this section is provided to provide the

skilled artisan some context for the following disclosed subject matter and should not be considered as admitted prior art.

DESCRIPTION OF THE DRAWINGS

[0005] Some embodiments are illustrated by way of example and not limitation in the views of the accompanying drawings.

[0006] **FIG. 1A** is a picture of a cross section of a substrate before a conventional redistribution layer (RDL) process.

[0007] **FIG. 1B** is a picture of a cross section of a substrate after a conventional RDL process.

[0008] **FIG. 2** is a block diagram of a cross section of a substrate after a conventional RDL process.

[0009] **FIGS. 3A-3J** are block diagrams illustrating a partially embedded alternative integration RDL process, according to a first example embodiment.

[0010] **FIGS. 4A-4J** are block diagrams illustrating a partially embedded alternative integration RDL process, according to a second example embodiment.

[0011] **FIGS. 5A-5G** are block diagrams illustrating a fully embedded alternative integration RDL process, according to an example embodiment.

[0012] **FIG. 6A** is cross-sectional depiction of a substrate illustrating an example of engineered copper RDL post-seed etch.

[0013] **FIG. 6B** is cross-sectional depiction of a substrate illustrating a conventional copper RDL post-seed etch.

[0014] **FIG. 7** is flow diagram illustrating a method for a partially embedded RDL process, according to an example embodiment.

[0015] **FIG. 8** is flow diagram illustrating a method for a fully embedded RDL process, according to an example embodiment.

DESCRIPTION

[0016] The description that follows includes systems, methods, techniques, instruction sequences, and computing machine program products that embody illustrative embodiments of the present inventive subject matter. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of example embodiments. It will be evident, however, to one skilled in the art, that the present embodiments may be practiced without these specific details.

[0017] A portion of the disclosure of this patent document contains material that is subject to copyright protection. The copyright owner has no objection to the facsimile reproduction by anyone of the patent document or the patent disclosure, as it appears in the Patent and Trademark Office patent files or records, but otherwise reserves all copyright rights whatsoever. The following notice applies to any data as described below and in the drawings that form a part of this document: Copyright LAM Research Corporation, 2018, All Rights Reserved.

[0018] In the present disclosure, various terms are used to describe a semiconductor processing surface: "wafer" and "substrate" may be used interchangeably. The process of depositing, or plating, metal onto a conductive surface of the wafer via an electrochemical reaction may be referred to generally as "electrodeposition" or "electroplating."

[0019] The present document describes several alternatives to the conventional redistribution layer (RDL) process: three integration schemes and one electroplating process that result in minimized undercut during seed etch. **FIG. 1A** is a picture of a cross section of a substrate before a convention RDL process. **FIG. 1B** is a picture of a cross section of a substrate after a convention RDL process. The after picture illustrates the undercut problem.

[0020] **FIG. 2** is a block diagram of a cross section of a substrate after an RDL process. The substrate 202 is deposited with a barrier 204, a copper seed 206, and ECD copper 208. In the first issue type, the copper seed 206 underneath the ECD copper 208 is etched resulting in an undercut. In the second issue type,

both the copper seed 206 and the base of electroplated RDL (ECD copper 208) are etched.

[0021] **FIGS. 3A-3J** are block diagrams illustrating a partially embedded alternative integration RDL process, according to a first example embodiment. In this process flow, a substrate 322 is provided at operation 302 in **FIG. 3A**. At operation 304 in **FIG. 3B**, a dielectric (polyimide, nitride, etc.) layer 324 is applied to the incoming substrate 322. At operation 306 in **FIG. 3C**, the dielectric layer 324 is patterned. For photosensitive polymeric material (polyimide), this would require exposure, develop, and descum steps. At operation 308 in **FIG. 3D**, a barrier layer 326 and a copper seed layer 328 are applied on top of this layer dielectric layer 324. A photoresist layer 330 may be applied to the substrate 322 at operation 310 in **FIG. 3E**. Depending on the photoresist material (spin on vs. laminate), the photoresist layer 330 could fill the underlying features or just lay atop. The photoresist layer 330 is then exposed, developed, and descummed at operation 312 in **FIG. 3E**. In this process flow, the patterned feature size matches that in the underlying dielectric as illustrated in operation 312 in **FIG. 3F**. At operation 314 in **FIG. 3G**, a copper layer 322 is electroplated in the patterned regions. At operation 316 in **FIG. 3H**, the photoresist layer 330 is removed. At operation 318 in **FIG. 3I**, the copper seed layer 328 and the barrier layer 326 is etched and removed. At operation 320 in **FIG. 3J**, optionally, the dielectric layer 324 can be removed as well. In this integration scheme, the seed etch does not create an undercut. A seed etch may only remove a small amount of material in the electroplated RDL side. It may remove the seed between the RDL structure and the barrier.

[0022] Electroplated RDL thickness can range from 2μm to 10μm. For partially embedded, the dielectric layer has at least about 0.5μm minimum thickness. The thickness range may be between 5-50% depending on the RDL final thickness.

[0023] **FIGS. 4A-4J** are block diagrams illustrating a partially embedded alternative integration RDL process, according to a second example embodiment. The flow of **FIGS. 4A-4J** differs from the flow of **FIGS. 3A-3J** for RDL dimensions in the photoresist layer. At operation 402 of **FIG. 4A**, a substrate 422 is provided. At operation 404 of **FIG. 4B**, a dielectric layer 424 is deposited onto the substrate 422. At operation 406 of **FIG. 4C**, the dielectric

layer 424 is patterned (for polymers: expose, develop, descum). At operation 408 of **FIG. 4D**, both a barrier layer 426 and a seed layer 428 are deposited on the dielectric layer 424 and the substrate 422.

[0024] At operation 410 of **FIG. 4E**, a photoresist layer 430 is applied to the substrate 422. At operation 412 of **FIG. 4F**, the photoresist layer 430 is patterned similarly to the dielectric layer 424. However, the features in the photoresist layer 430 have larger critical dimensions (CDs) or widths than the corresponding ones in the dielectric layer 424. At operation 414 of **FIG. 4G**, copper 432 is electrodeposited. At operation 416 of **FIG. 4H**, the photoresist 430 is removed. At operation 418 of **FIG. 4I**, the copper seed 426 and the barrier layer 424 are etched. At operation 420 of **FIG. 4J**, the dielectric layer 424 is optionally removed.

[0025] This flow process results in RDL patterns with thicker dimensions near the top. This can be beneficial to maintain RDL dimensions post-copper seed etch. This flow may also minimize side-wall cut in after seed etch resulting in RDL structures of excellent mechanical integrity.

[0026] **FIGS. 5A-5G** are block diagrams illustrating a fully embedded alternative integration RDL process, according to an example embodiment. In this process flow, a substrate 516 is provided at operation 502 of **FIG. 5A**. At operation 504 of **FIG. 5B**, a dielectric (polyimide, nitride, etc.) layer 518 is applied to the incoming substrate 516. At operation 506 of **FIG. 5C**, the dielectric layer 518 is patterned. For photosensitive polymeric material (polyimide), this process includes exposure, develop, and descum steps. At operation 508 of **FIG. 5D**, a barrier layer 520 and a copper seed layer 522 are applied on top of the patterned dielectric layer 518 and exposed surface of the substrate 516. At operation 510 of **FIG. 5E**, copper 524 is electroplated in the patterned regions. At operation 512 of **FIG. 5F**, the copper 524 is planarized. The plating evolution is illustrated by operation 514 in **FIG. 5G**.

[0027] **FIG. 6A** is a cross-sectional depiction of a substrate illustrating an example of grain engineering. Cross-section 604 illustrates a substrate 610, a barrier 608, and a copper layer 606. To minimize seed etch effect, a stronger, more robust electroplated copper may be required. This can be engineered using various process parameters including waveform, convection, and chemistry.

[0028] Some copper grain structures that can be engineered to exhibit etch resistance include large grains, columnar grains, and nanotwinned grains. As an example, nanotwinned copper has previously been shown to have high tensile strength, excellent electrical conductivity, and high electromigration resistance. If formed early in the electroplating process, the engineered grain structure (including nanotwins) could reduce the attack on the electroplated copper although not reducing the undercut to the copper seed layer beneath the RDL structure. In the above alternative process schemes detailed above, grain engineered copper could minimize etch into the side of the electroplated RDL structure. This would maintain the pattern dimensions and mechanical integrity of the RDL

[0029] **FIG. 6B** is a cross-sectional depiction of a substrate illustrating an example of a conventional copper RDL post-seed etch. Cross-section 604 illustrates an undercut 612 in the copper 606 in a conventional copper RDL post-seed etch.

[0030] **FIG. 7** is flow diagram illustrating a method for a partially embedded RDL process, according to an example embodiment. At operation 702, a substrate is provided. At operation 704, a dielectric (polyimide, nitride, etc.) is applied to the substrate. At operation 706, the dielectric layer is patterned. For photosensitive polymeric material (polyimide), this would require exposure, develop, and descum steps. At operation 708, a barrier and copper seed layer is applied on top of the layer dielectric layer. At operation 710, a photoresist process is applied to the substrate. The photoresist is exposed, developed, and descummed at operation 710. In this process flow, the patterned feature size would match that in the underlying dielectric. At operation 712, copper is electroplated in the patterned regions. At operation 714, the photoresist is removed. At operation 716, the copper seed and barrier etch is removed. At operation 718, optionally, the dielectric layer can be removed as well. In this integration scheme, the seed etch does not create an undercut.

[0031] **FIG. 8** is flow diagram illustrating a method for a fully embedded RDL process, according to an example embodiment. At operation 802, a substrate is provided. At operation 804, a dielectric (polyimide, nitride, etc.) is applied to the substrate. At operation 806, the dielectric layer is patterned. For

photosensitive polymeric material (polyimide), this would require exposure, develop, and descum steps. At operation 808, a barrier and copper seed layer is deposited on top of this layer dielectric layer. At operation 810, copper is electroplated in the patterned regions. At operation 812, the copper (or copper/dielectric layer) is planarized.

[0032] Although an embodiment has been described with reference to specific example embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the scope of the disclosure. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense. The accompanying drawings that form a part hereof show by way of illustration, and not of limitation, specific embodiments in which the subject matter may be practiced. The embodiments illustrated are described in sufficient detail to enable those skilled in the art to practice the teachings disclosed herein. Other embodiments may be utilized and derived therefrom, such that structural and logical substitutions and changes may be made without departing from the scope of this disclosure. This Detailed Description, therefore, is not to be taken in a limiting sense, and the scope of various embodiments is defined only by the appended claims, along with the full range of equivalents to which such claims are entitled. Such embodiments of the inventive subject matter may be referred to herein, individually and/or collectively, by the term "invention" merely for convenience and without intending to voluntarily limit the scope of this application to any single invention or inventive concept if more than one is in fact disclosed. Thus, although specific embodiments have been illustrated and described herein, it should be appreciated that any arrangement calculated to achieve the same purpose may be substituted for the specific embodiments shown. This disclosure is intended to cover all adaptations or variations of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will be apparent to those of skill in the art upon reviewing the above description.

[0033] Examples:

[0034] Example 1 is a method for redistribution layer (RDL) process, the method comprising: depositing a dielectric layer on a surface of a substrate; patterning the dielectric layer, the patterned dielectric layer exposing a region of

the surface of the substrate; depositing a protective layer on the patterned dielectric layer and the exposed region of the surface of the substrate; depositing a photoresist layer on the protective layer; patterning the photoresist layer, the patterned photoresist layer exposing a first region of the protective layer; electrodepositing a copper layer on top of the exposed first region of the protective layer; removing the patterned photoresist layer to expose a second region of the protective layer; and removing the exposed second region of the protective layer to expose the patterned dielectric layer.

[0035] Example 2 includes the method of example 1, further comprising: removing the exposed patterned dielectric layer to expose a region of the surface of the substrate.

[0036] Example 3 includes the method of example 2, wherein a size of a feature in the patterned photoresist layer is larger than a size of a feature in the patterned dielectric layer.

[0037] Example 4 includes the method of example 1, wherein a size of a feature in the patterned photoresist layer is smaller than a size of a feature in the patterned dielectric layer.

[0038] Example 5 includes the method of example 1, wherein the protective layer comprises a barrier layer and a copper seed layer, the copper seed layer being on top of the barrier layer.

[0039] Example 6 includes the method of example 1, wherein the dielectric layer comprises a photosensitive polymide layer or a nitride layer.

[0040] Example 7 includes the method of example 6, wherein patterning the dielectric layer further comprises: forming the patterned dielectric layer using expose, develop, and descum processes.

[0041] Example 8 includes the method of example 1, wherein a feature size of the patterned photoresist layer matches a feature size of the underlying patterned dielectric layer.

[0042] Example 9 includes the method of example 1, wherein depositing the photoresist layer on top of the protective layer further comprises: filling features of the patterned dielectric layer with the photoresist layer.

[0043] Example 10 includes the method of example 1, wherein the photoresist layer lays on top of the features of the patterned dielectric layer and does not fill the features of the patterned dielectric layer.

CLAIMS

What is claimed is:

1. A method for redistribution layer (RDL) process, the method comprising:

depositing a dielectric layer on a surface of a substrate;

patterning the dielectric layer, the patterned dielectric layer exposing a region of the surface of the substrate;

depositing a protective layer on the patterned dielectric layer and the exposed region of the surface of the substrate;

depositing a photoresist layer on the protective layer;

patterning the photoresist layer, the patterned photoresist layer exposing a first region of the protective layer;

electrodepositing a copper layer on top of the exposed first region of the protective layer;

removing the patterned photoresist layer to expose a second region of the protective layer; and

removing the exposed second region of the protective layer to expose the patterned dielectric layer.

2. The method of claim 1, further comprising:

removing the exposed patterned dielectric layer to expose a region of the surface of the substrate.

3. The method of claim 1, wherein a size of a feature in the patterned photoresist layer is larger than a size of a feature in the patterned dielectric layer.

4. The method of claim 1, wherein a size of a feature in the patterned photoresist layer is smaller than a size of a feature in the patterned dielectric layer.

5. The method of claim 1, wherein the protective layer comprises a barrier layer and a copper seed layer, the copper seed layer being on top of the barrier layer.

6. The method of claim 1, wherein the dielectric layer comprises a photosensitive polyimide layer or a nitride layer.

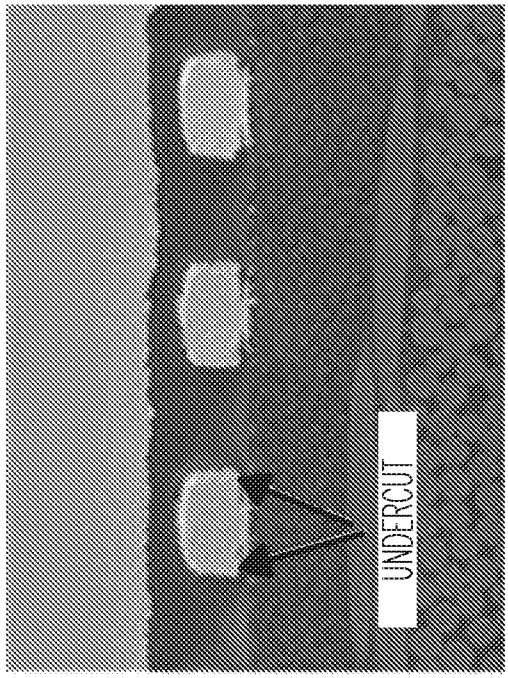
7. The method of claim 6, wherein patterning the dielectric layer further comprises:

forming the patterned dielectric layer using expose, develop, and descum processes.

8. The method of claim 1, wherein a feature size of the patterned photoresist layer matches a feature size of the underlying patterned dielectric layer.

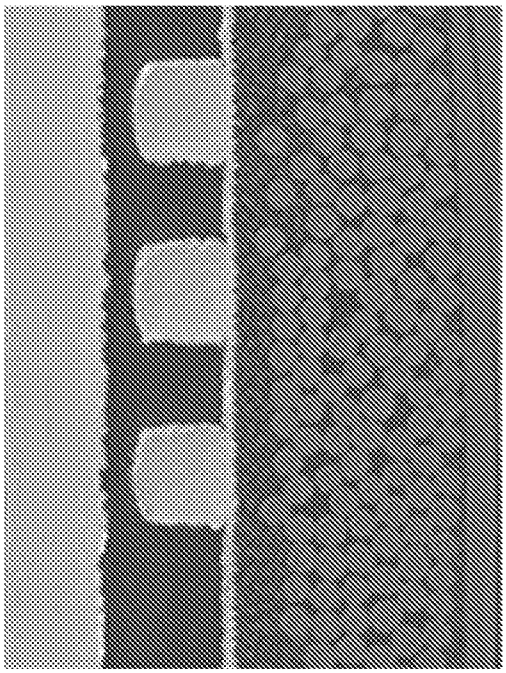
9. The method of claim 1, wherein depositing the photoresist layer on top of the protective layer further comprises: filling features of the patterned dielectric layer with the photoresist layer.

10. The method of claim 1, wherein the photoresist layer lays on top of the features of the patterned dielectric layer and does not fill the features of the patterned dielectric layer.



AFTER ETCHING

Fig. 1B



BEFORE ETCHING

Fig. 1A

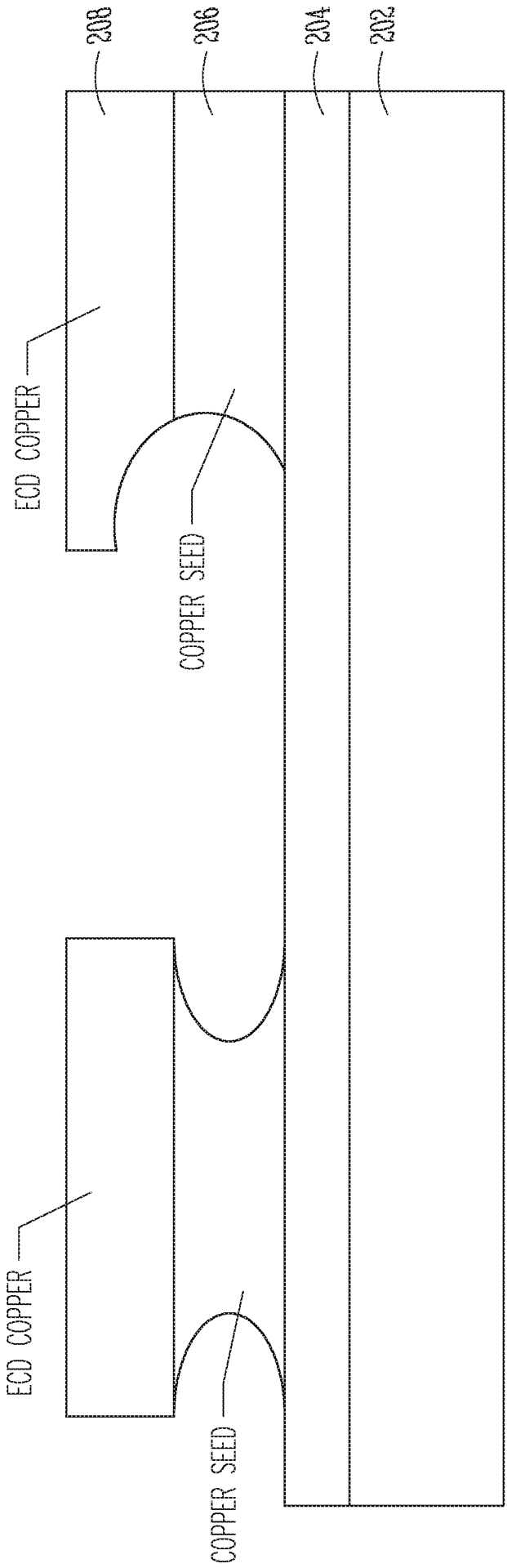

208
206
204
202
ECD COPPER
COPPER SEED
ECD COPPER
COPPER SEED

Fig.2

302

Fig. 3A

304

Fig. 3B

306

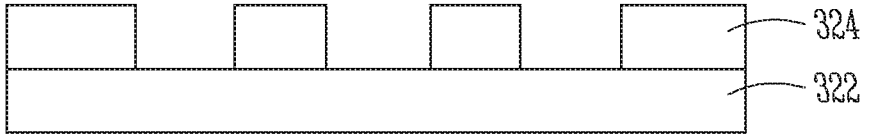


Fig. 3C

308

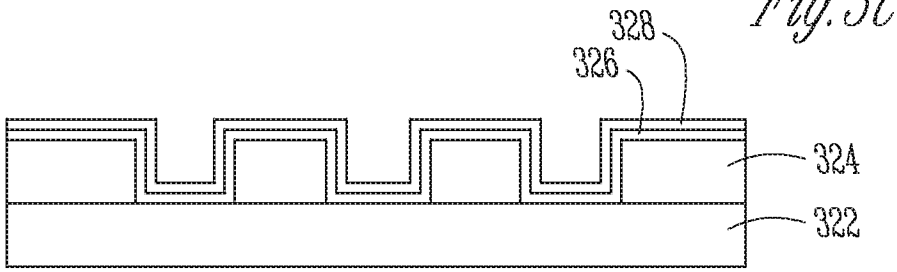


Fig. 3D

310

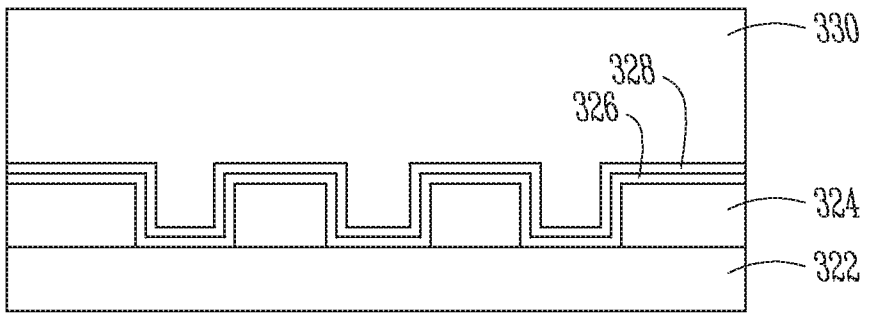


Fig. 3E

312

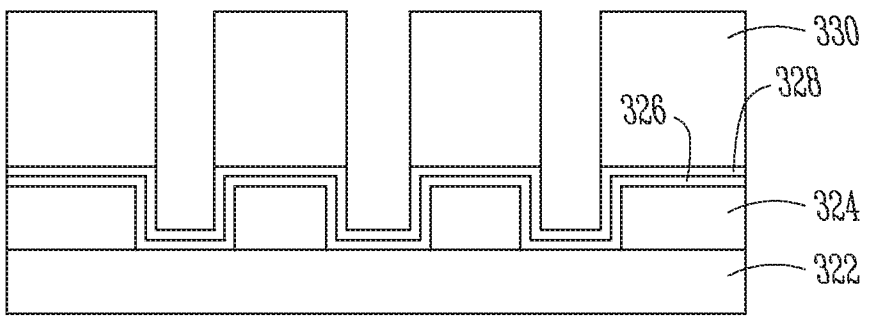


Fig. 3F

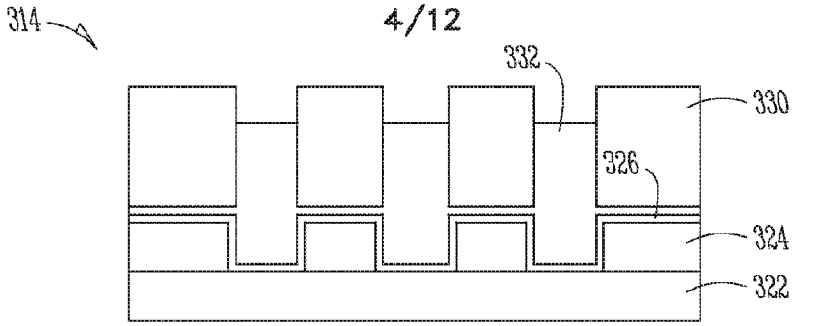


Fig. 3G

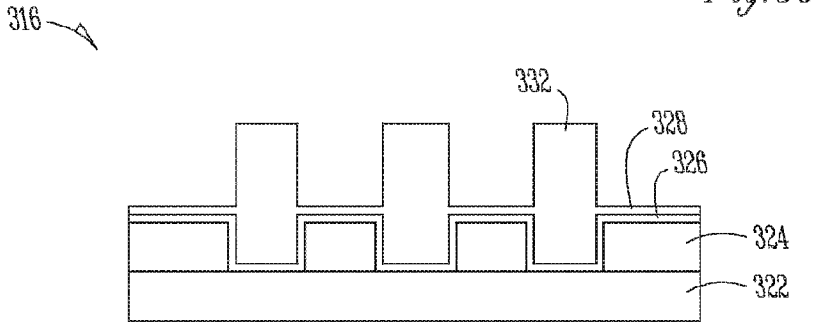


Fig. 3H

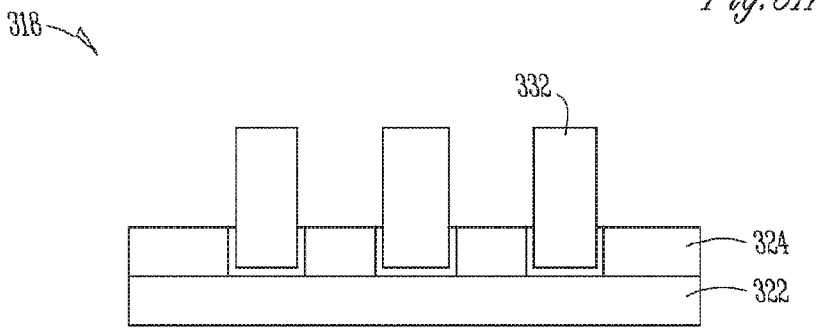


Fig. 3I

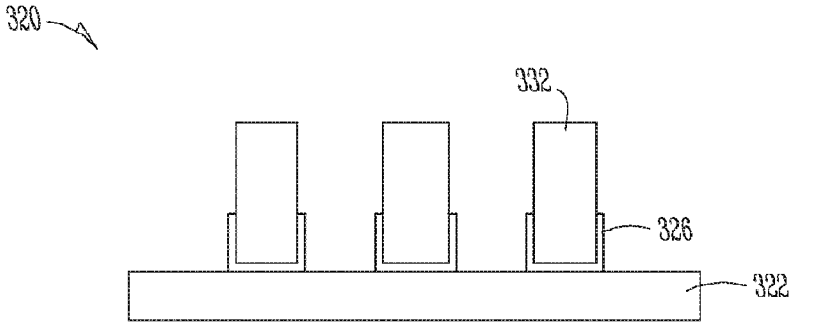


Fig. 3J

402

Fig. 4A

404

Fig. 4B

406

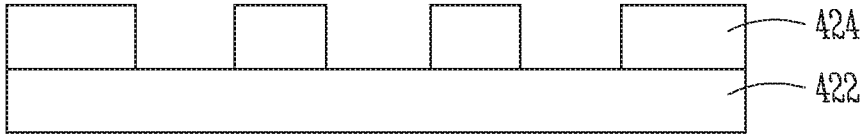


Fig. 4C

408

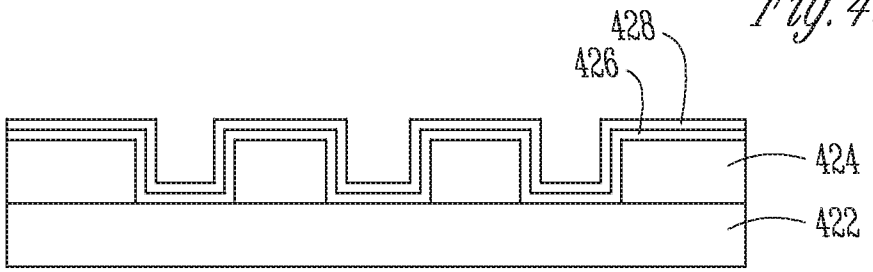


Fig. 4D

410

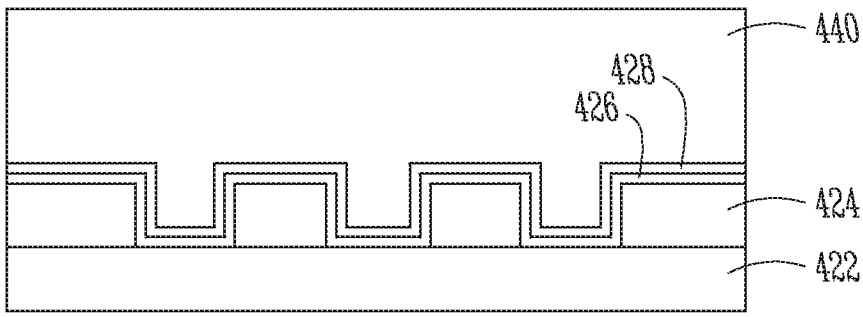


Fig. 4E

412

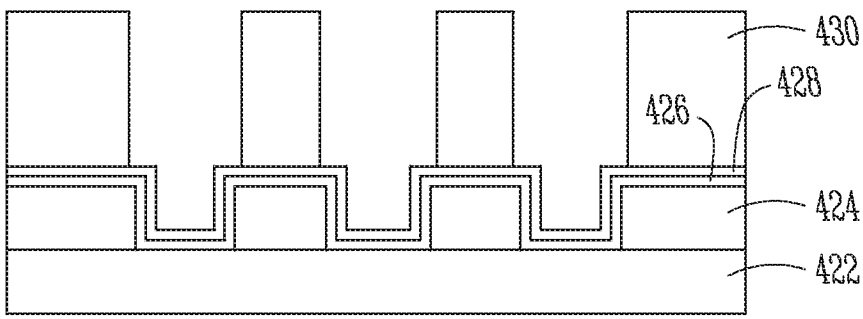


Fig. 4F

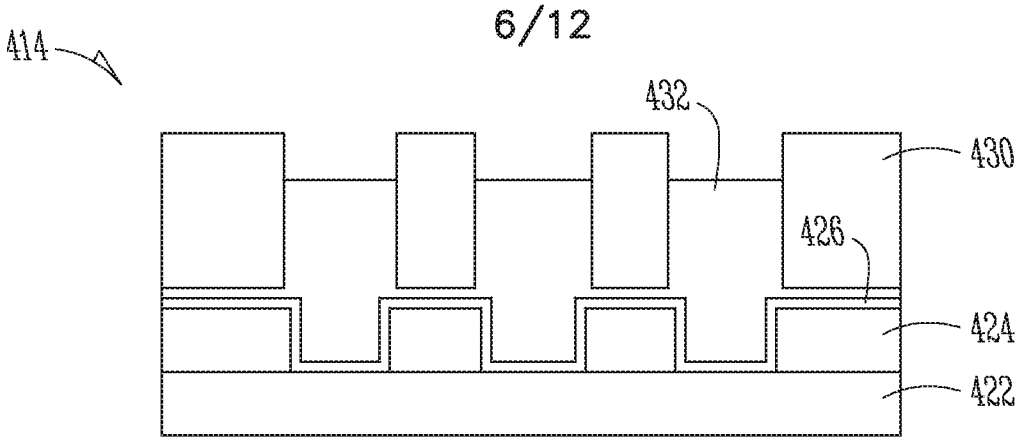


Fig. 4G

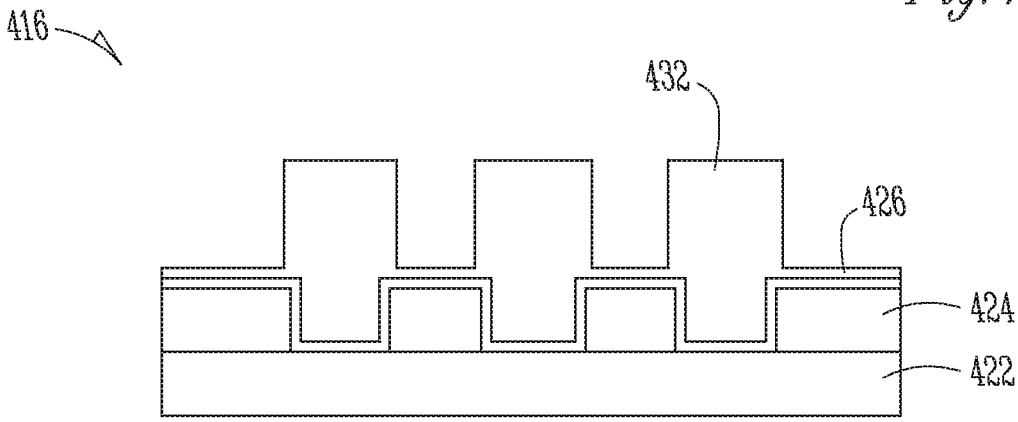


Fig. 4H

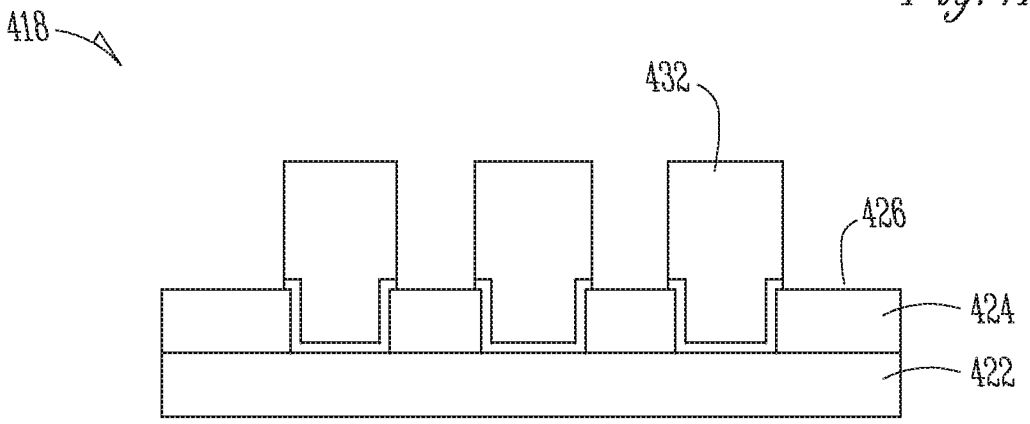


Fig. 4I

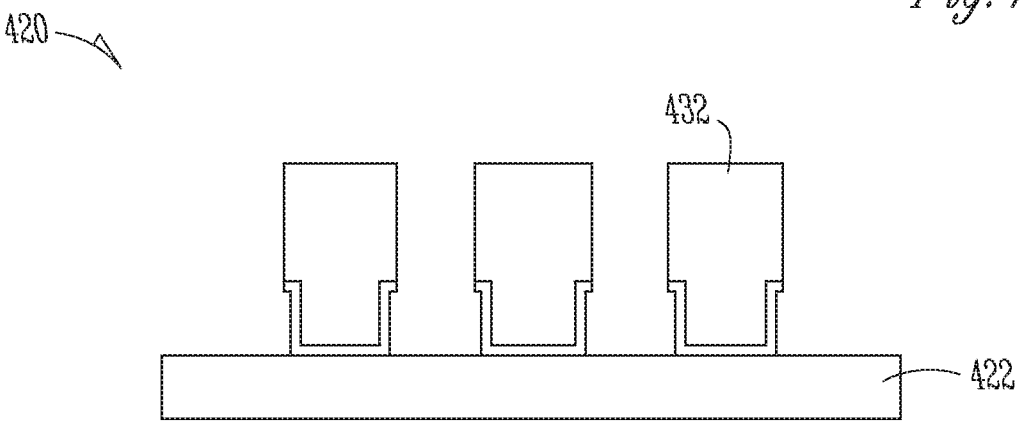


Fig. 4J

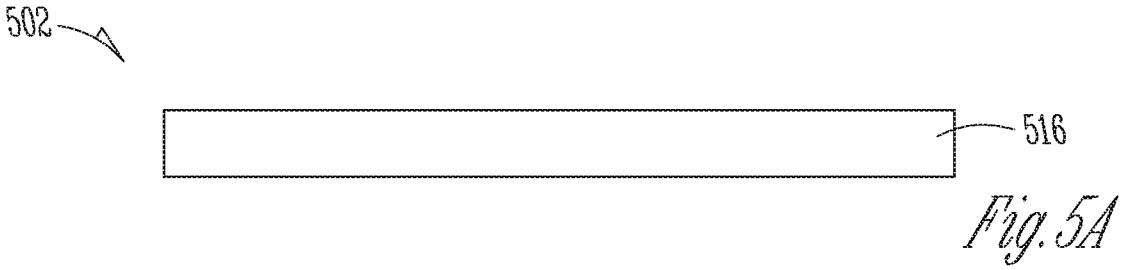


Fig. 5A

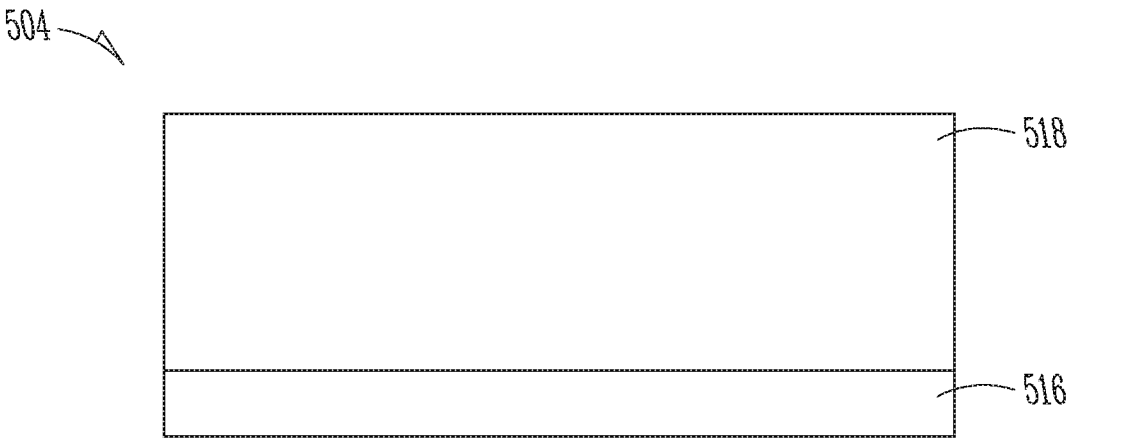


Fig. 5B

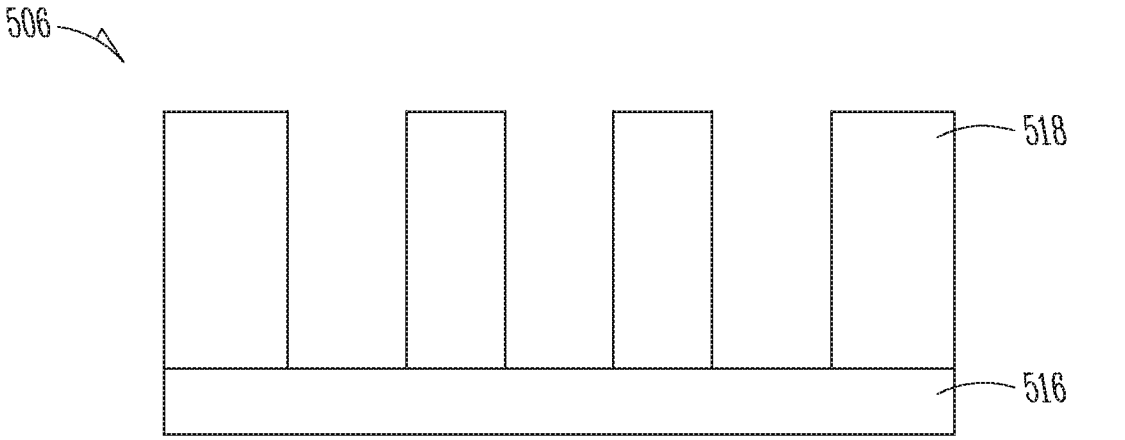


Fig. 5C

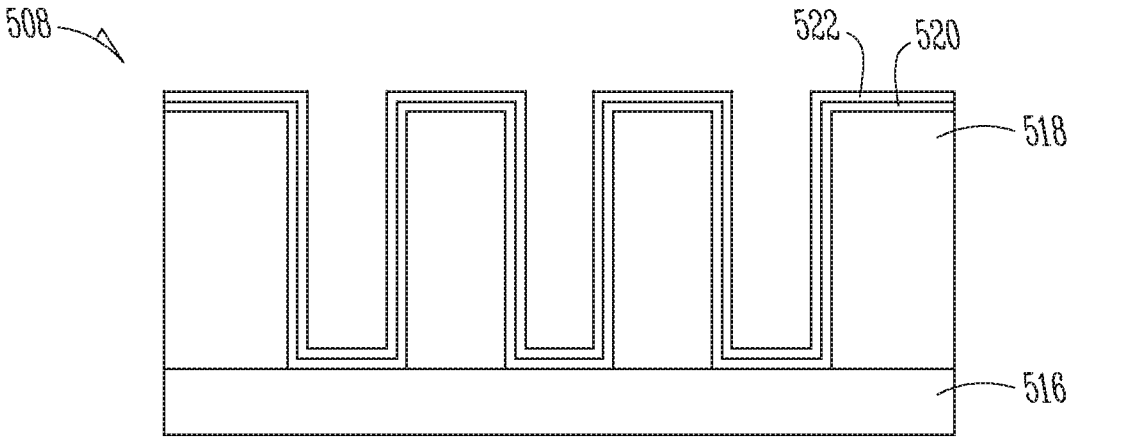


Fig. 5D

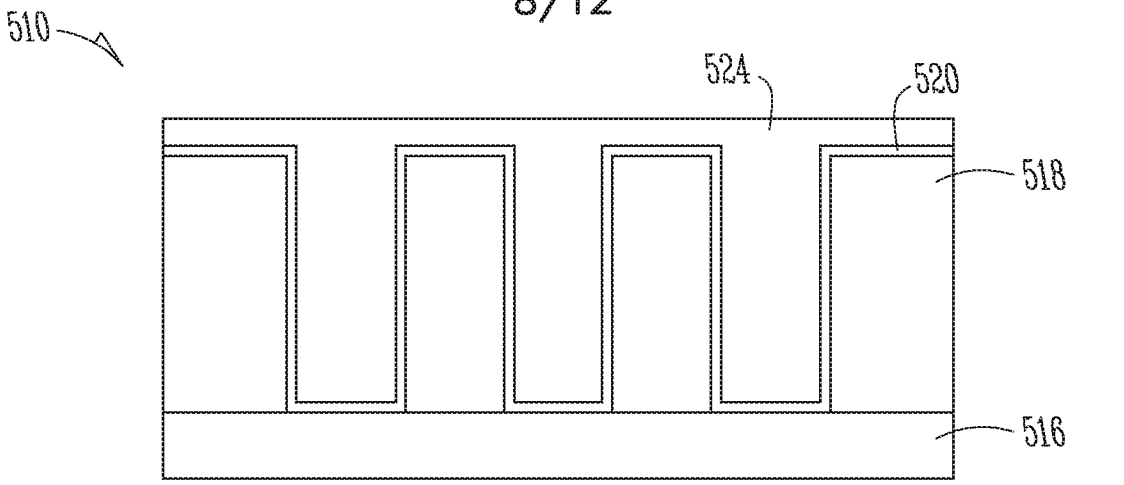


Fig. 5E

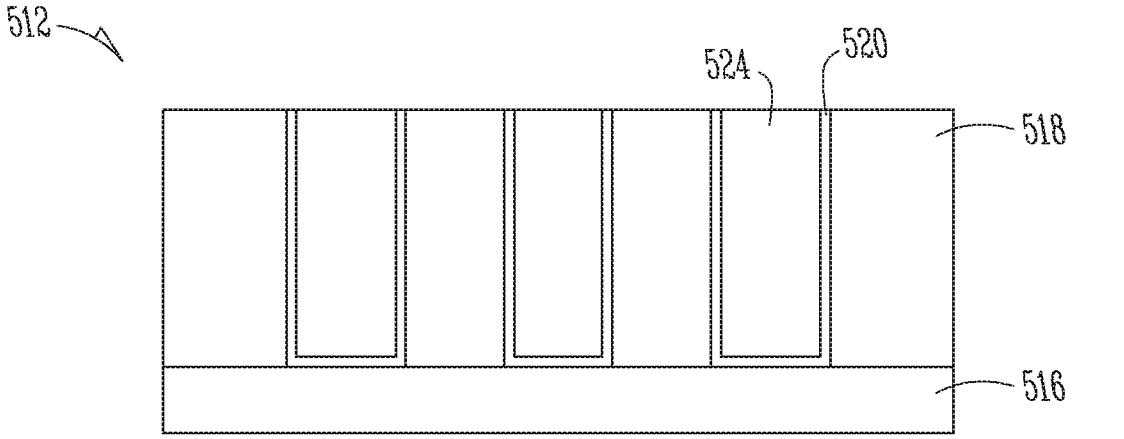


Fig. 5F

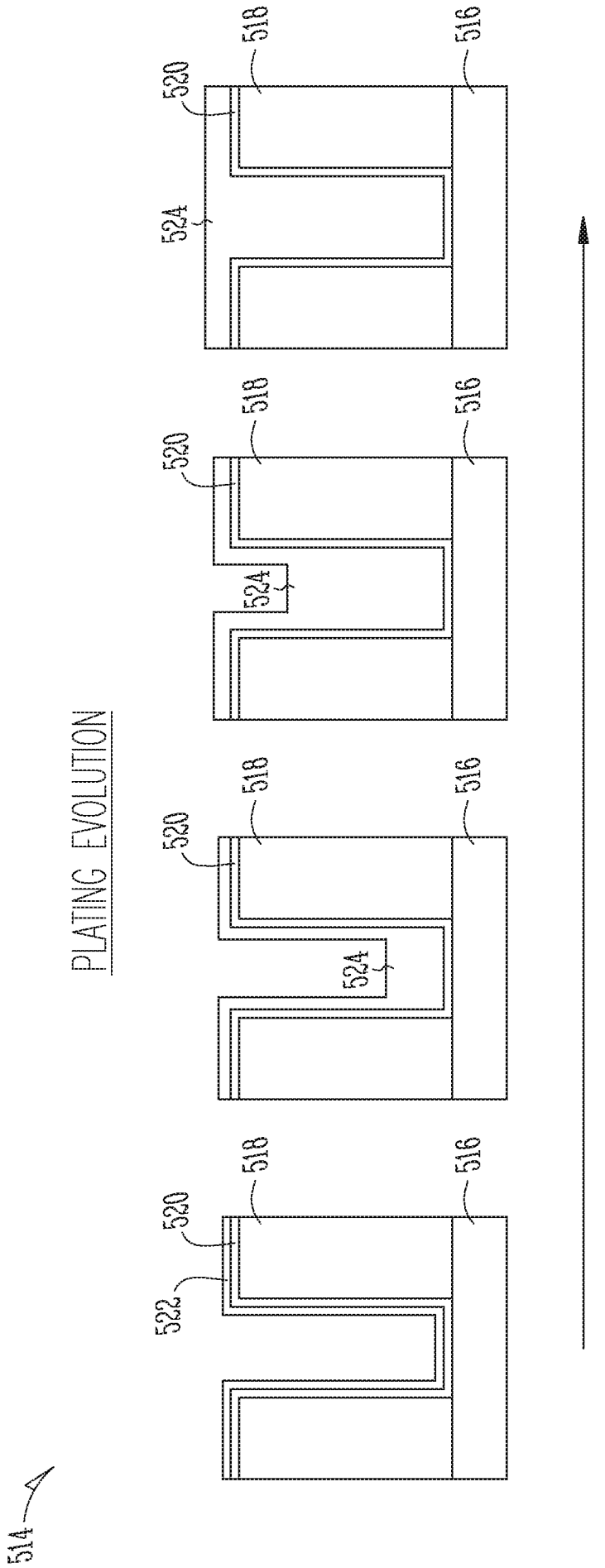

PLATING EVOLUTION
LONGER PLATING TIME
514
516
518
520
522
524

Fig. 5C

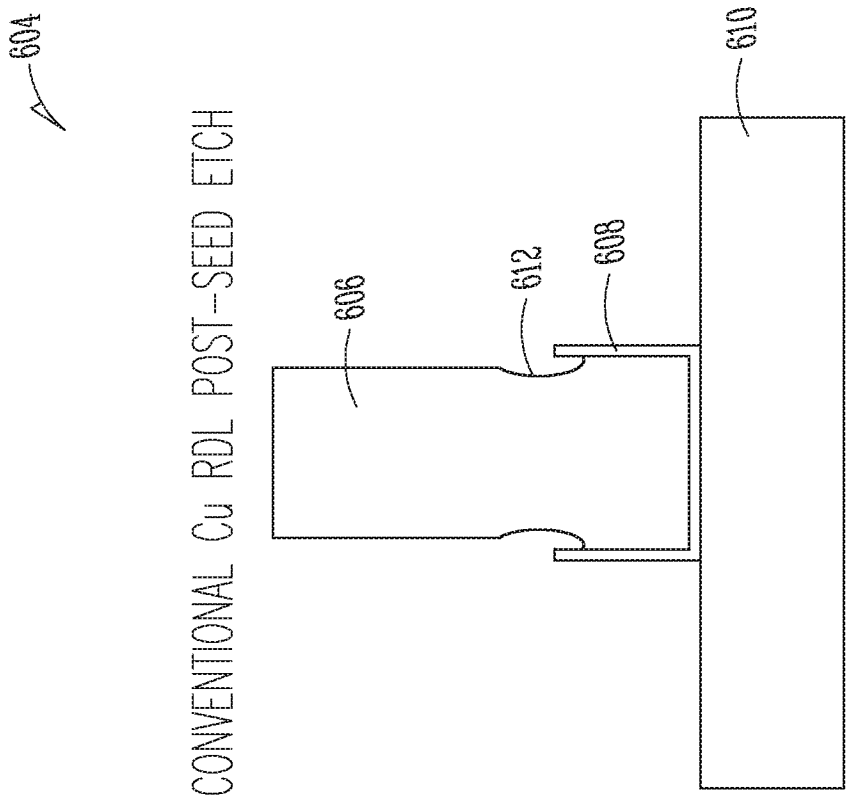

604
CONVENTIONAL Cu RDL POST-SEED ETCH
606
612
608
610

Fig. 6B

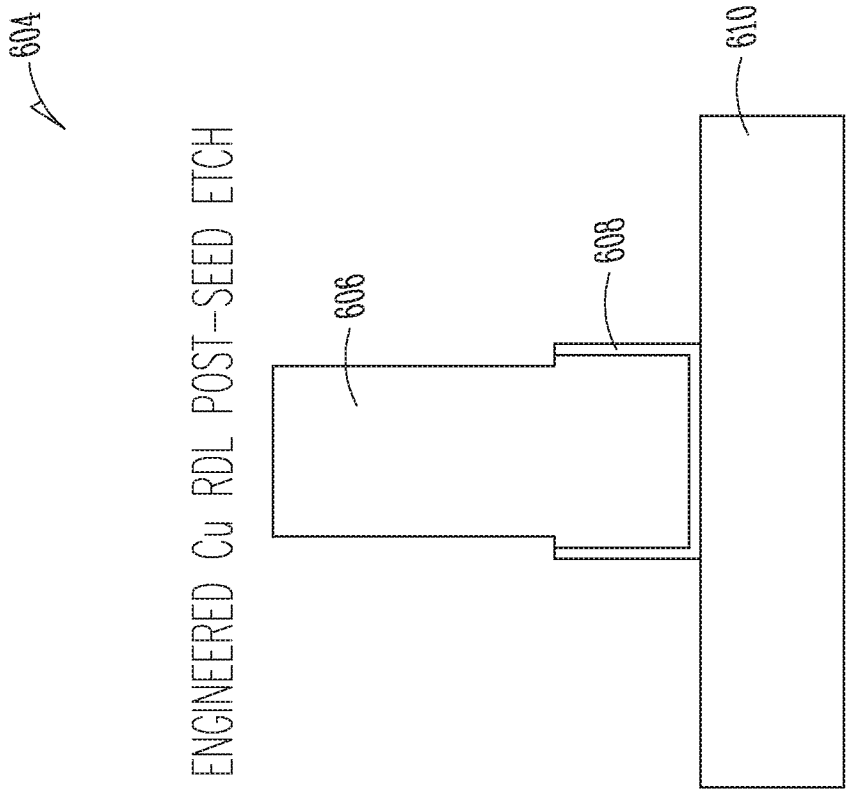

604
ENGINEERED Cu RDL POST-SEED ETCH
606
608
610

Fig. 6A

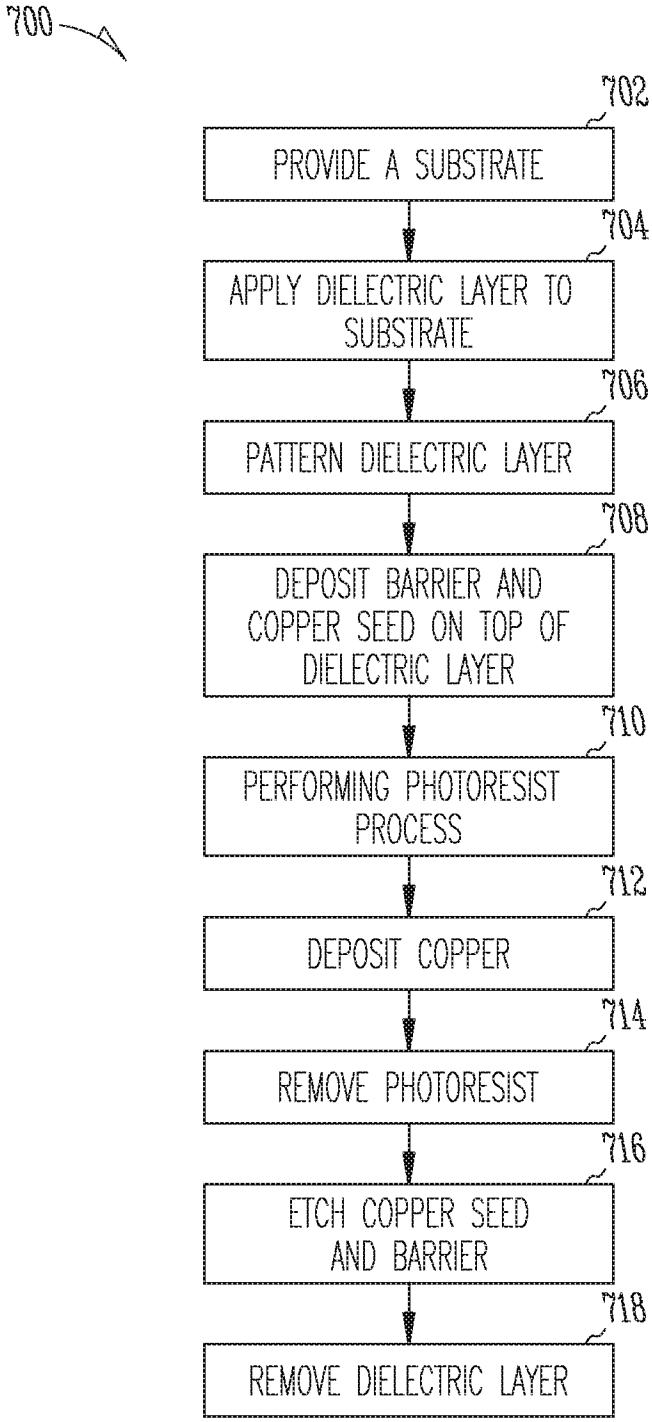

700
702
PROVIDE A SUBSTRATE
704
APPLY DIELECTRIC LAYER TO SUBSTRATE
706
PATTERN DIELECTRIC LAYER
708
DEPOSIT BARRIER AND COPPER SEED ON TOP OF DIELECTRIC LAYER
710
PERFORMING PHOTORESIST PROCESS
712
DEPOSIT COPPER
714
REMOVE PHOTORESIST
716
ETCH COPPER SEED AND BARRIER
718
REMOVE DIELECTRIC LAYER

Fig. 7

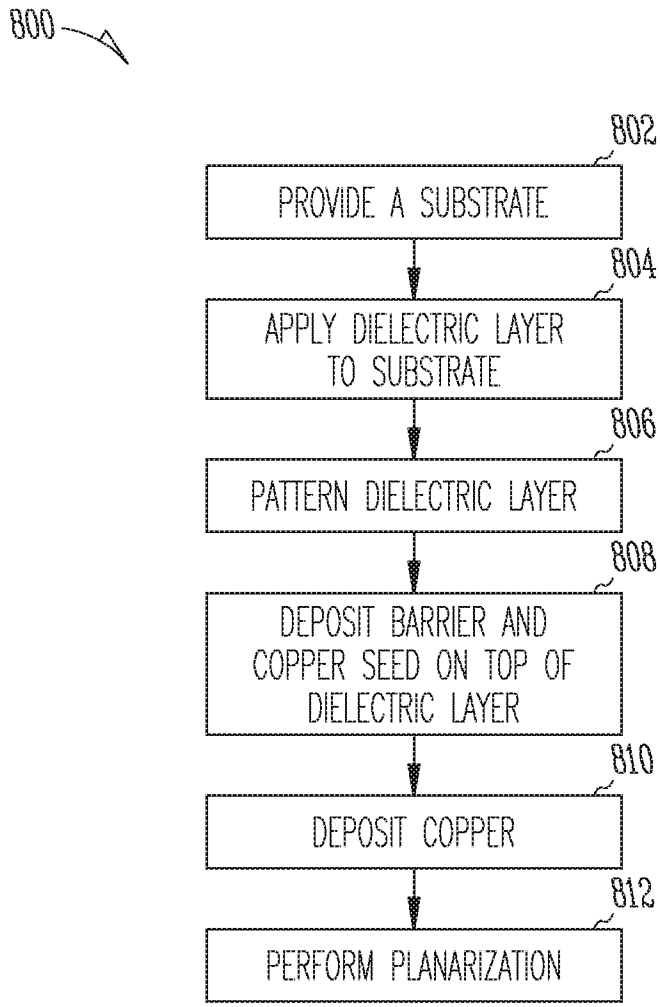

800
802
PROVIDE A SUBSTRATE
804
APPLY DIELECTRIC LAYER TO SUBSTRATE
806
PATTERN DIELECTRIC LAYER
808
DEPOSIT BARRIER AND COPPER SEED ON TOP OF DIELECTRIC LAYER
810
DEPOSIT COPPER
812
PERFORM PLANARIZATION

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/043729

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/027(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/441; H01L 23/00; H01L 23/528; H01L 25/00; H01L 21/027

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: redistribution layer, RDL, seed, barrier, undercut, etch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017-0243839 A1 (LAM RESEARCH CORPORATION) 24 August 2017 See paragraphs [0020]-[0024], claim 1 and figures 1-4.	1-3,5-7,9
A		4,8,10
A	US 2016-0181196 A1 (INTEL CORPORATON) 23 June 2016 See paragraph [0043] and figure 2.	1-10
A	US 2015-0348843 A1 (INVENSAS CORPORATION) 03 December 2015 See paragraph [0007] and figures 1A-1B.	1-10
A	US 2015-0126030 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 07 May 2015 See the entire document.	1-10
A	US 2008-0113504 A1 (JIN-YUAN LEE et al.) 15 May 2008 See the entire document.	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 December 2019 (19.12.2019)	**19 December 2019 (19.12.2019)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
PARK, Hye Lyun
Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/043729

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017-0243839 A1	24/08/2017	AT 514042 A2	15/09/2014
		AT 514042 A3	15/12/2015
		AT 514042 B1	15/12/2015
		CN 102330140 A	25/01/2012
		CN 102330140 B	07/12/2016
		CN 103866374 A	18/06/2014
		CN 103866374 B	06/06/2017
		CN 106480481 A	08/03/2017
		CN 106480481 B	09/07/2019
		CN 106637363 A	10/05/2017
		CN 106637363 B	15/01/2019
		CN 106947997 A	14/07/2017
		CN 107452632 A	08/12/2017
		JP 2014-118634 A	30/06/2014
		JP 2017-216443 A	07/12/2017
		JP 6494910 B2	03/04/2019
		KR 10-1809751 B1	15/12/2017
		KR 10-1860670 B1	23/05/2018
		KR 10-1931035 B1	19/12/2018
		KR 10-2012-0003405 A	10/01/2012
		KR 10-2013-0127400 A	22/11/2013
		KR 10-2014-0076524 A	20/06/2014
		KR 10-2017-0026215 A	08/03/2017
		KR 10-2017-0057217 A	24/05/2017
		KR 10-2017-0131258 A	29/11/2017
		KR 10-2017-0139477 A	19/12/2017
		SG 10201509320 A	30/12/2015
		SG 10201704130 A	28/12/2017
		SG 195480 A1	30/12/2013
		TW 201204877 A	01/02/2012
		TW 201410925 A	16/03/2014
		TW 201437439 A	01/10/2014
		TW 201612367 A	01/04/2016
		TW 201718954 A	01/06/2017
		TW 201802299 A	16/01/2018
		TW 201806037 A	16/02/2018
		TW I504786 B	21/10/2015
		TW I572749 B	01/03/2017
		TW I589734 B	01/07/2017
		TW I606154 B	21/11/2017
		TW I640661 B	11/11/2018
		US 10094034 B2	09/10/2018
		US 10190230 B2	29/01/2019
		US 10233556 B2	19/03/2019
		US 2012-0000786 A1	05/01/2012
		US 2013-0313123 A1	28/11/2013
		US 2014-0183049 A1	03/07/2014
		US 2014-0299477 A1	09/10/2014
		US 2014-0299478 A1	09/10/2014

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/043729

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2016-0265132 A1	15/09/2016
		US 2016-0376722 A1	29/12/2016
		US 2017-0029973 A1	02/02/2017
		US 2017-0058417 A1	02/03/2017
		US 2017-0175286 A1	22/06/2017
		US 2018-0105949 A1	19/04/2018
		US 8795480 B2	05/08/2014
		US 9394620 B2	19/07/2016
		US 9464361 B2	11/10/2016
		US 9523155 B2	20/12/2016
		US 9624592 B2	18/04/2017
		US 9834852 B2	05/12/2017
US 2016-0181196 A1	23/06/2016	CN 105814679 A	27/07/2016
		DE 112013007166 T5	03/03/2016
		GB 2534262 A	20/07/2016
		KR 10-2016-0052463 A	12/05/2016
		RU 2015151166 A	01/06/2017
		RU 2631911 C2	28/09/2017
		US 9721886 B2	01/08/2017
		WO 2015-195067 A2	23/12/2015
		WO 2015-195067 A3	14/04/2016
US 2015-0348843 A1	03/12/2015	US 2013-0015585 A1	17/01/2013
		US 2013-0214429 A1	22/08/2013
		US 2014-0346646 A1	27/11/2014
		US 8431431 B2	30/04/2013
		US 8829683 B2	09/09/2014
		US 9142511 B2	22/09/2015
		US 9515024 B2	06/12/2016
US 2015-0126030 A1	07/05/2015	US 2015-0255334 A1	10/09/2015
		US 2016-0240434 A1	18/08/2016
		US 2017-0236750 A1	17/08/2017
		US 9054163 B2	09/06/2015
		US 9324608 B2	26/04/2016
		US 9640431 B2	02/05/2017
US 2008-0113504 A1	15/05/2008	EP 1359682 A2	05/11/2003
		EP 1359682 A3	09/02/2005
		JP 2004-007636 A	08/01/2004
		US 106126367 A	03/10/2000
		US 2003-0206560 A1	06/11/2003
		US 2004-0032024 A1	19/02/2004
		US 2005-0189650 A1	01/09/2005
		US 2005-0215043 A1	29/09/2005
		US 2008-0099928 A1	01/05/2008
		US 2008-0111236 A1	15/05/2008
		US 2008-0113503 A1	15/05/2008
		US 2009-0137110 A9	28/05/2009

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/043729

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2010-0038803 A9	18/02/2010
		US 6642136 B1	04/11/2003
		US 6917119 B2	12/07/2005
		US 7099293 B2	29/08/2006
		US 7338890 B2	04/03/2008
		US 7355288 B2	08/04/2008
		US 8178967 B2	15/05/2012
		US 8481418 B2	09/07/2013
		US 9369175 B2	14/06/2016