



Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

POST TREATMENT OF LOW K DIELECTRIC FILMS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the present invention relate to the fabrication of integrated circuits. More particularly, embodiments of the present invention relate to a process for depositing and post-treating low dielectric constant films.

Description of the Related Art

[0002] Semiconductor device geometries have dramatically decreased in size since such devices were first introduced several decades ago. Since then, integrated circuits have generally followed the two year/half-size rule (often called Moore's Law), which means that the number of devices that will fit on a chip doubles every two years. Today's fabrication plants are routinely producing devices having 0.13 μm and even 0.1 μm feature sizes, and tomorrow's plants soon will be producing devices having even smaller geometries.

[0003] In order to further reduce the size of devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and to use insulators having low dielectric constants (k) to reduce the capacitive coupling between adjacent metal lines. Recent developments in low dielectric constant insulating films have focused on incorporating silicon (Si), carbon (C), and oxygen (O) atoms into the films. One challenge in this area has been to develop a Si, C, and O containing film that has a low k value and also exhibits desirable thermal and mechanical properties. Often Si, C, and O containing films that have a desirable dielectric constant exhibit poor mechanical strength and are easily damaged by etch chemistry and plasma exposure during subsequent processing, causing failure of the integrated circuit.

[0004] Thermal and plasma annealing processes have been developed in attempts to improve the properties of low dielectric constant films. Thermal and plasma annealing processes have typically been performed at temperatures of less than about 400°C in order to prevent damage to other components of the substrate

or device on which the low dielectric constant film is deposited. It has been found that thermal and plasma annealing processes can densify low dielectric constant films containing Si, C, and O. However, such annealing processes typically are performed for about 30 minutes to 2 hours, and thus significantly increase substrate processing times. Also, further improvements in the mechanical and dielectric properties of the low dielectric constant films are still desired.

[0005] Thus, there remains a need for a method of post-treating low dielectric constant films to improve the properties of the low dielectric constant films.

SUMMARY OF THE INVENTION

[0006] Embodiments of the invention provide a method of processing a substrate, comprising depositing a low dielectric constant film comprising silicon and carbon on a substrate in the presence of RF power and post-treating the deposited low dielectric constant film by a process comprising heating the low dielectric constant film to a desired temperature of at least about 600°C at a rate of at least about 10°C/sec, wherein the low dielectric constant film is maintained at the desired temperature for about five seconds or less, and then cooling the low dielectric constant film at a rate of at least about 10°C/sec. In one embodiment, the low dielectric constant film is heated and cooled within a time period of about 0.5 minutes to about 5 minutes.

[0007] In one embodiment, the low dielectric constant film is heated from a temperature of between about 25°C and about 250°C to a desired temperature of between about 600°C and about 1000°C, wherein the low dielectric constant film is heated at the desired temperature for about five seconds or less, and then cooled from the desired temperature, wherein the low dielectric constant film is heated and cooled within a time period of about 0.5 minutes to about 5 minutes.

[0008] Further embodiments of the invention include post-treating a low dielectric constant film by heating the low dielectric constant film to a desired temperature at a rate of at least about 10°C/sec, wherein the low dielectric constant film is maintained at the desired temperature for about five seconds or less, cooling the low dielectric

constant film at a rate of at least about 10°C/sec, and treating the low dielectric constant film with one or more processes selected from the group consisting of an electron beam treatment and UV radiation treatment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0010] Figure 1 is a cross-sectional diagram of an exemplary CVD reactor configured for use according to embodiments described herein.

[0011] Figure 2 is a diagrammatic view in vertical cross-section of a portion of a rapid thermal processing (RTP) chamber according to an embodiment of the present invention.

[0012] Figure 3 is an electron beam chamber in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0013] Embodiments of the present invention provide a method of depositing a low dielectric constant film on a substrate and post-treating the low dielectric constant film by a process comprising rapidly heating the low dielectric constant film to a desired high temperature, such as between about 600°C and about 1000°C, and then rapidly cooling the low dielectric constant film such that the low dielectric constant film is exposed to the desired high temperature for about five seconds or less. Preferably, the low dielectric constant film is exposed to the desired high temperature for about one second or less. In one aspect, the process of rapidly heating and cooling the low dielectric constant film is a spike annealing process.

[0014] Depositing the low dielectric constant film

[0015] The low dielectric constant film has a dielectric constant of less than about 4 and comprises silicon and carbon, and preferably, oxygen. The low dielectric constant film is deposited from a mixture comprising one or more organosilicon compounds in the presence of RF power. The one or more organosilicon compounds used to deposit the low dielectric constant layer may be organosilanes, organosiloxanes, or combinations thereof. The term "organosilicon compound" as used herein is intended to refer to compounds containing carbon atoms in organic groups, and can be cyclic or linear. Organic groups may include alkyl, alkenyl, cyclohexenyl, and aryl groups in addition to functional derivatives thereof. Preferably, the organosilicon compounds include one or more carbon atoms attached to a silicon atom such that the carbon atoms are not readily removed by oxidation at suitable processing conditions. The organosilicon compounds may also preferably include one or more oxygen atoms.

[0016] Suitable cyclic organosilicon compounds include a ring structure having three or more silicon atoms, and optionally one or more oxygen atoms. Commercially available cyclic organosilicon compounds that may be used include rings having alternating silicon and oxygen atoms with one or two alkyl groups bonded to the silicon atoms. Some exemplary cyclic organosilicon compounds include:

1,3,5-trisilano-2,4,6-trimethylene,	$-(\text{-SiH}_2\text{CH}_2\text{-})_3\text{-}$ (cyclic)
1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS),	$-(\text{-SiHCH}_3\text{-O-})_4\text{-}$ (cyclic)
octamethylcyclotetrasiloxane (OMCTS),	$-(\text{-Si(CH}_3)_2\text{-O-})_4\text{-}$ (cyclic)
1,3,5,7,9-pentamethylcyclopentasiloxane,	$-(\text{-SiHCH}_3\text{-O-})_5\text{-}$ (cyclic)
1,3,5,7-tetrasilano-2,6-dioxy-4,8-dimethylene,	$-(\text{-SiH}_2\text{-CH}_2\text{-SiH}_2\text{-O-})_2\text{-}$ (cyclic)
hexamethylcyclotrisiloxane	$-(\text{-Si(CH}_3)_2\text{-O-})_3\text{-}$ (cyclic).

[0017] Suitable linear organosilicon compounds include aliphatic organosilicon compounds having linear or branched structures with one or more silicon atoms and

one or more carbon atoms. The organosilicon compounds may further include one or more oxygen atoms. Some exemplary linear organosilicon compounds include:

methylsilane,	$\text{CH}_3\text{-SiH}_3$
dimethylsilane,	$(\text{CH}_3)_2\text{-SiH}_2$
trimethylsilane,	$(\text{CH}_3)_3\text{-SiH}$
ethylsilane,	$\text{CH}_3\text{-CH}_2\text{-SiH}_3$
disilanomethane,	$\text{SiH}_3\text{-CH}_2\text{-SiH}_3$
bis(methylsilano)methane,	$\text{CH}_3\text{-SiH}_2\text{-CH}_2\text{-SiH}_2\text{-CH}_3$
1,2-disilanoethane,	$\text{SiH}_3\text{-CH}_2\text{-CH}_2\text{-SiH}_3$
1,2-bis(methylsilano)ethane,	$\text{CH}_3\text{-SiH}_2\text{-CH}_2\text{-CH}_2\text{-SiH}_2\text{-CH}_3$
2,2-disilanopropane,	$\text{SiH}_3\text{-C}(\text{CH}_3)_2\text{-SiH}_3$
diethylsilane,	$(\text{C}_2\text{H}_5)_2\text{-SiH}_2$
propylsilane,	$\text{C}_3\text{H}_7\text{-SiH}_3$
vinylmethylsilane,	$(\text{CH}_2=\text{CH})\text{-SiH}_2\text{-CH}_3$
1,1,2,2-tetramethyldisilane,	$(\text{CH}_3)_2\text{-SiH-SiH}(\text{CH}_3)_2$
hexamethyldisilane,	$(\text{CH}_3)_3\text{-Si-Si}(\text{CH}_3)_3$
1,1,2,2,3,3-hexamethyltrisilane,	$(\text{CH}_3)_2\text{-SiH-Si}(\text{CH}_3)_2\text{-SiH}(\text{CH}_3)_2$
1,1,2,3,3-pentamethyltrisilane,	$(\text{CH}_3)_2\text{-SiH-SiH}(\text{CH}_3)\text{-SiH}(\text{CH}_3)_2$
1,3-bis(methylsilano)propane,	$\text{CH}_3\text{-SiH}_2\text{-(CH}_2)_3\text{-SiH}_2\text{-CH}_3$
1,2-bis(dimethylsilano)ethane,	$(\text{CH}_3)_2\text{-SiH}(\text{CH}_2)_2\text{-SiH}(\text{CH}_3)_2$
1,3-bis(dimethylsilano)propane,	$(\text{CH}_3)_2\text{-SiH}(\text{CH}_2)_3\text{-SiH}(\text{CH}_3)_2$
diethoxymethylsilane (DEMS),	$\text{CH}_3\text{-SiH}(\text{O-CH}_2\text{-CH}_3)_2$
1,3-dimethyldisiloxane,	$\text{CH}_3\text{-SiH}_2\text{-O-SiH}_2\text{-CH}_3$
1,1,3,3-tetramethyldisiloxane,	$(\text{CH}_3)_2\text{-SiH-O-SiH}(\text{CH}_3)_2$
hexamethyldisiloxane (HMDS),	$(\text{CH}_3)_3\text{-Si-O-Si}(\text{CH}_3)_3$
1,3-bis(silanomethylene)disiloxane,	$(\text{SiH}_3\text{-CH}_2\text{-SiH}_2)_2\text{-O}$
bis(1-methyldisiloxanyl)methane,	$(\text{CH}_3\text{-SiH}_2\text{-O-SiH}_2)_2\text{-CH}_2$
2,2-bis(1-methyldisiloxanyl)propane,	$(\text{CH}_3\text{-SiH}_2\text{-O-SiH}_2)_2\text{-C}(\text{CH}_3)_2$
dimethyldimethoxysilane (DMDMOS),	$(\text{CH}_3\text{O})_2\text{-Si}(\text{CH}_3)_2$
phenyldimethoxysilane,	$\text{C}_6\text{H}_5\text{-SiH}(\text{O-CH}_3)_2$
diphenylmethylsilane,	$(\text{C}_6\text{H}_5)_2\text{-SiH-CH}_3$

dimethylphenylsilane, $(\text{CH}_3)_2\text{-SiH-C}_6\text{H}_5$
dimethoxymethylvinylsilane (DMMVS), $(\text{CH}_3\text{O})_2\text{-Si}(\text{CH}_3)\text{-CH}_2\text{=CH}_3$.

[0018] In one embodiment, the low dielectric constant film is deposited from a mixture comprising one or more organosilicon compounds and one or more oxidizing gases in the presence of RF power. Oxidizing gases that may be used include oxygen (O_2), ozone (O_3), nitrous oxide (N_2O), carbon monoxide (CO), carbon dioxide (CO_2), water (H_2O), 2, 3-butane dione, or combinations thereof. When ozone is used as an oxidizing gas, an ozone generator converts from 6% to 20%, typically about 15%, by weight of the oxygen in a source gas to ozone, with the remainder typically being oxygen. However, the ozone concentration may be increased or decreased based upon the amount of ozone desired and the type of ozone generating equipment used. Disassociation of oxygen or the oxygen containing compounds may occur in a microwave chamber prior to entering the deposition chamber to reduce excessive dissociation of the silicon containing compounds. Preferably, radio frequency (RF) power is applied to the reaction zone to increase dissociation.

[0019] Optionally, in addition to the one or more organosilicon compounds and the optional one or more oxidizing gases, one or more hydrocarbon compounds may be included in the mixture for depositing the low dielectric constant film. Hydrocarbon compounds that may be used include aliphatic hydrocarbon compounds having between one and about 20 adjacent carbon atoms. The hydrocarbon compounds can include adjacent carbon atoms that are bonded by any combination of single, double, and triple bonds. For example, the organic compounds may include alkenes and alkynes having two to about 20 carbon atoms, such as ethylene, propylene, acetylene, and butadiene.

[0020] One or more hydrocarbon compounds having a cyclic group may also be used. The term "cyclic group" as used herein is intended to refer to a ring structure. The ring structure may contain as few as three atoms. The atoms may include carbon, silicon, nitrogen, oxygen, fluorine, and combinations thereof, for example. The cyclic group may include one or more single bonds, double bonds, triple bonds,

and any combination thereof. For example, a cyclic group may include one or more aromatics, aryls, phenyls, cyclohexanes, cyclohexadienes, cycloheptadienes, and combinations thereof. The cyclic group may also be bi-cyclic or tri-cyclic. Further, the cyclic group is preferably bonded to a linear or branched functional group. The linear or branched functional group preferably contains an alkyl or vinyl alkyl group and has between one and twenty carbon atoms. The linear or branched functional group may also include oxygen atoms, such as in a ketone, ether, and ester. Some exemplary hydrocarbon compounds having at least one cyclic group include alpha-terpinene (ATP), vinylcyclohexane (VCH), and phenylacetate.

[0021] Optionally, one or more carrier gases may be included in the mixture used to deposit the low dielectric constant film. Carrier gases that may be used include argon, helium, carbon dioxide, and combinations thereof.

[0022] The film may be deposited using any processing chamber capable of chemical vapor deposition (CVD). Figure 1 illustrates a vertical, cross-section view of a parallel plate CVD processing chamber 10 that may be used. The chamber 10 includes a high vacuum region 15 and a gas distribution manifold 11 having perforated holes for dispersing process gases therethrough to a substrate (not shown). The substrate rests on a substrate support plate or susceptor 12. The susceptor 12 is mounted on a support stem 13 that connects the susceptor 12 to a lift motor 14. The lift motor 14 raises and lowers the susceptor 12 between a processing position and a lower, substrate-loading position so that the susceptor 12 (and the substrate supported on the upper surface of susceptor 12) can be controllably moved between a lower loading/off-loading position and an upper processing position which is closely adjacent to the manifold 11. An insulator 17 surrounds the susceptor 12 and the substrate when the susceptor 12 and the substrate are in an upper processing position.

[0023] Gases introduced to the manifold 11 are uniformly distributed radially across the surface of the substrate. A vacuum pump 32 having a throttle valve controls the exhaust rate of gases from the chamber 10 through a manifold 24. Deposition and carrier gases, if needed, flow through gas lines 18 into a mixing

system 19 and then to the manifold 11. Generally, each process gas supply line 18 includes (i) safety shut-off valves (not shown) that can be used to automatically or manually shut off the flow of process gas into the chamber, and (ii) mass flow controllers (also not shown) to measure the flow of gas through the gas supply lines 18. When toxic gases are used in the process, several safety shut-off valves are positioned on each gas supply line 18 in conventional configurations.

[0024] In one aspect, an organosilicon compound is introduced into the mixing system 19 at a flowrate for a 200 or 300 mm substrate of about 100 sccm to about 10,000 sccm. The optional hydrocarbon compound is introduced into the mixing system 19 at a flowrate of about 100 sccm to about 10,000 sccm. The optional oxidizing gas has a flowrate of about 100 sccm to about 6,000 sccm. The carrier gas has a flowrate of about 100 sccm to about 5,000 sccm. In a preferred embodiment, the organosilicon compound is octamethylcyclotetrasiloxane, and the hydrocarbon compound is ethylene.

[0025] The deposition process is preferably a plasma enhanced process. In a plasma enhanced process, a controlled plasma is typically formed adjacent the substrate by RF energy applied to the gas distribution manifold 11 using a RF power supply 25. Alternatively, RF power can be provided to the susceptor 12. The RF power to the deposition chamber may be cycled or pulsed to reduce heating of the substrate and promote greater porosity in the deposited film. The power density of the plasma for a 200 or 300 mm substrate is between about 0.03 W/cm^2 and about 3.2 W/cm^2 , which corresponds to a RF power level of about 10 W to about 1,000 W for a 200 mm substrate and about 20 W to about 2,250 W for a 300 mm substrate. Preferably, the RF power level is between about 200 W and about 1,700 W for a 300 mm substrate.

[0026] The RF power supply 25 can supply a single frequency RF power between about 0.01 MHz and 300 MHz. Preferably, the RF power may be delivered using mixed, simultaneous frequencies to enhance the decomposition of reactive species introduced into the high vacuum region 15. In one aspect, the mixed frequency has a lower frequency of about 12 kHz and a higher frequency of about

13.56 mHz. In another aspect, the lower frequency may range between about 300 Hz to about 1,000 kHz, and the higher frequency may range between about 5 mHz and about 50 mHz. Preferably, the low frequency power level is about 150 W. Preferably, the high frequency power level is between about 200 W and about 750 W, more preferably, about 200 W to about 400 W.

[0027] During deposition, the substrate is maintained at a temperature between about -20°C and about 500°C, preferably between about 100°C and about 450°C. The deposition pressure is typically between about 1 Torr and about 20 Torr, preferably between about 4 Torr and about 7 Torr. An exemplary chamber that may be used to deposit a low dielectric constant layer according to embodiments described herein is provided below.

[0028] When remote dissociation of the oxidizing gas is desired, an optional microwave chamber 28 can be used to input power from between about 50 Watts and about 6,000 Watts to the oxidizing gas prior to the gas entering the processing chamber 10. The additional microwave power can avoid excessive dissociation of the organosilicon compounds prior to reaction with the oxidizing gas. A gas distribution plate (not shown) having separate passages for the organosilicon compound and the oxidizing gas is preferred when microwave power is added to the oxidizing gas.

[0029] Typically, any or the entire chamber lining, distribution manifold 11, susceptor 12, and various other reactor hardware are made out of materials such as aluminum or anodized aluminum. An example of such a CVD reactor is described in U.S. Patent No. 5,000,113, entitled "A Thermal CVD/PECVD Reactor and Use for Thermal Chemical Vapor Deposition of Silicon Dioxide and In-situ Multi-step Planarized Process," issued to Wang et al., and assigned to Applied Materials, Inc., the assignee of the invention, and is incorporated by reference herein to the extent not inconsistent with the invention.

[0030] A system controller 34 controls the motor 14, the gas mixing system 19, and the high frequency power supply 25, which are connected therewith by control

lines 36. The system controller 34 controls the activities of the CVD reactor and typically includes a hard disk drive, a floppy disk drive, and a card rack. The card rack contains a single board computer (SBC), analog and digital input/output boards, interface boards, and stepper motor controller boards. The system controller 34 conforms to the Versa Modular Europeans (VME) standard, which defines board, card cage, and connector dimensions and types. The VME standard also defines the bus structure having a 16-bit data bus and a 24-bit address bus. The system controller 34 operates under the control of a computer program stored on a hard disk drive 38.

[0031] The low dielectric constant films described herein may be deposited using a computer storage medium containing a software routine that, when executed, causes a general purpose computer to control a deposition chamber. The software routine may comprise instructions for depositing any of the films according to any of the embodiments described herein.

[0032] Post-treating the low dielectric constant film

[0033] After the low dielectric constant film is deposited, the low dielectric constant film is post-treated by a process comprising rapidly heating the low dielectric constant film to a desired high temperature and then rapidly cooling the low dielectric constant film. The desired high temperature may be between about 600°C and about 1000°C, such as about 800°C. Preferably, the low dielectric constant film is heated from a temperature of between about 25°C and about 250°C at a rate of at least about 10°C/sec to the desired high temperature. For example, the low dielectric constant film may be heated at a rate between about 10°C/sec and about 300°C/sec. Preferably, the low dielectric constant film is heated at a rate between about 100°C/sec and about 300°C/sec, e.g., about 250°C/sec. After the low dielectric constant film reaches the desired temperature, the heat source(s) used to heat the low dielectric constant film are turned off, and the low dielectric constant film is cooled at a rate of at least about 10°C/sec, such as at a rate between about 10°C/sec and about 100°C/sec. The cooling of the low dielectric constant film may be enhanced by the presence of a reflective plate in the post-treatment chamber.

Preferably, the cooling rate is enhanced by both the presence of a reflective plate in the post-treatment chamber and by exposing the backside of the substrate on which the low dielectric constant film is deposited to a flow of an inert gas such as helium. For example, the backside of the substrate may be exposed to a flow of helium at a rate of between about 10 sccm and about 500 sccm. Since the low dielectric constant film is rapidly heated and rapidly cooled, the length of time between the initiation of the heating of the low dielectric constant film and the termination of the cooling of the low dielectric constant film is typically between about 0.5 minutes and about 5 minutes.

[0034] Generally, the low dielectric constant film is heated and cooled in a chamber atmosphere that may include argon (Ar), nitrogen (N₂), helium (He), oxygen (O₂), hydrogen (H₂), water vapor (H₂O), nitrous oxide (N₂O), or combinations thereof. The chamber pressure may be between about 100 Torr and about 760 Torr. The chamber pressure may be adjusted to change the cooling rate of the low dielectric constant film.

[0035] In one embodiment, the low dielectric constant film is heated and cooled in an argon environment. In one embodiment, argon is introduced into the chamber at a rate between about 10 sccm and about 100 sccm.

[0036] Any chamber that is capable of rapidly heating a low dielectric constant film to a desired high temperature for about five seconds or less, preferably one second or less, and then rapidly cooling the low dielectric constant film may be used to post-treat the low dielectric constant film. An exemplary chamber that may be used to post-treat a low dielectric constant film according to embodiments described herein is provided below.

[0037] One chamber that may be used is the Radiance™ RTP chamber, available from Applied Materials, Inc. of Santa Clara, CA. Figure 2 illustrates a chamber 200 that is an embodiment of the Radiance™ RTP chamber. Chamber 200, as shown in FIG. 2, includes a process region 213 enclosed by a sidewall 214

and a bottom wall 215. The upper portion of sidewall 214 of chamber 200 is sealed to a window 248 by "O" rings 216.

[0038] A substrate or wafer 261 is supported on its edge inside region 213 by a support ring 262 typically made up of silicon carbide. Support ring 262 is mounted on a rotatable quartz cylinder 263. By rotating quartz cylinder 263 support ring 262 and wafer 261 can be caused to rotate. An additional silicon carbide adapter ring can be used to allow wafers of different diameters to be processed (e.g., 150 mm, 200 mm and 300 mm). The outside edge of support ring 262 preferably extends less than two inches from the outside diameter of wafer 261. The volume of chamber 200 is approximately nine liters for a 300 mm system.

[0039] Chamber 200 includes a gas inlet 269 formed through sidewall 214 for injecting process gas into region 213 to allow various processing steps to be carried out in region 213. Positioned on the opposite side of gas inlet 269, in sidewall 214, is a gas outlet 268. Gas outlet 268 is coupled to a vacuum source 286, such as a pump, to exhaust process gas from chamber 200 and to reduce the pressure in chamber 200. The vacuum source 286 maintains a desired pressure while process gas is fed into the chamber during processing.

[0040] A radiant energy assembly 218 is positioned over the window 248. The radiant energy assembly 218 includes a plurality of tungsten halogen lamps 219, for example Sylvania EYT lamps, each mounted into a light pipe 221 which can be a stainless steel, gold, brass, aluminum or other metal. Lamps 219 include a filament wound as a coil with its axis parallel to that of the lamp envelope. Most of the light is emitted perpendicular to the axis towards the wall of the surrounding light pipe 221. The light pipe length is selected to at least be as long as the associated lamp. The light pipe 221 may be longer provided that the power reaching the wafer is not substantially attenuated by increased reflection. The lamps 219 are positioned in a hexagonal array or in a "honeycomb shape." Lamps 219 are positioned to adequately cover the entire surface area of wafer 261 and support ring 262. Lamps 219 (which may be on the order of hundreds) are grouped in zones which can be

independently controlled to provide for extremely uniform or non-uniform heating of wafer 261, as is desired according to the process.

[0041] The radiant energy source 218 comprising the plurality of light pipes 221 and associated lamps 219 allows the use of a thin quartz window 248 to provide an optical port for heating a substrate within the evacuative process chamber. A primary purpose of the window 248 is to isolate the process environment from the lamps 219 as the lamps 219 can get too hot and react with the process gases. Light pipes 221 can be cooled by flowing a coolant, such as water, between the various heat pipes.

[0042] While the radiant energy source 218 is described above as including a plurality of tungsten halogen lamps 219, in another embodiment, the radiant energy source 218 includes ultraviolet lamps.

[0043] The bottom wall 215 of chamber 200 includes a top surface 211 for reflecting energy onto the backside of wafer 261. Additionally, chamber 200 includes a plurality of optical temperature probes 270 positioned through the bottom wall 215 of chamber 200 in order to detect the temperature of wafer 261 at a plurality of locations across its bottom surface. Reflections between the backside of the silicon wafer 261 and reflecting surface 211 create a blackbody cavity which makes temperature measurement independent of wafer backside emissivity and thereby provides accurate temperature measurement capability.

[0044] In one embodiment, the reflective surface 211 is in the form of an absorbing reflector plate that is reflective at wavelengths of 0.7-0.96 μm and reflective at other wavelengths emitted by the radiant energy assembly 218. The absorbing property of the reflector plate enhances the cooling rate of the low dielectric constant film. The cooling rate of the low dielectric constant film may be further enhanced by exposing the backside of the substrate on which the low dielectric constant film is deposited to a flow of an inert gas, such as by introducing inert gas around the edge of the reflector plate or through holes in the reflector plate to the backside of the substrate.

[0045] Aspects of the chamber 200 are operated by a control system (not shown). The control system may include any number of controllers, processors and input/output devices. In one embodiment, the control system is a component of a closed loop feedback system which monitors various parameters within the process chamber 200 while processing a substrate, and then issues one or more control signals to make necessary adjustments according to various setpoints. In general, the parameters being monitored include the temperature, pressure, and gas flow rates.

[0046] In a further embodiment, post-treating the low dielectric constant film comprises rapidly heating the low dielectric constant film to a desired high temperature, rapidly cooling the low dielectric constant film from the desired high temperature, and treating the low dielectric constant film with an electron beam treatment. The low dielectric constant film may be treated with an electron beam treatment before or after the rapid heating and cooling.

[0047] The electron beam (e-beam) treatment typically has a dose between about 50 and about 2000 micro coulombs per square centimeter ($\mu\text{C}/\text{cm}^2$) at about 1 to 20 kiloelectron volts (KeV). The e-beam current typically ranges from about 1 mA to about 40 mA, and is preferably about 1 to about 20 mA. The e-beam treatment is typically operated at a temperature between about room temperature and about 450°C for about 10 seconds to about 15 minutes. In one aspect, the e-beam treatment conditions include 6 kV, 10-18 mA and 50 $\mu\text{C}/\text{cm}^2$ at 350°C for about 15 to about 30 seconds to treat a film having a thickness of about 1 micron. In another aspect, the e-beam treatment conditions include 4.5 kV, 10-18 mA and 50 $\mu\text{C}/\text{cm}^2$ at 350°C for about 15 to about 30 seconds to treat a film having a thickness of about 5000 Å. Argon or hydrogen may be present during the electron beam treatment. Although any e-beam device may be used, one exemplary device is the EBK chamber, available from Applied Materials, Inc. Treating the low dielectric constant film with an electron beam after the low dielectric constant film is deposited will volatilize at least some of the organic groups in the film and thus may form voids in the film.

[0048] Figure 3 illustrates an e-beam chamber 300 in accordance with an embodiment of the invention. The e-beam chamber 300 includes a vacuum chamber 320, a large-area cathode 322, a target plane 330 located in a field-free region 338, and a grid anode 326 positioned between the target plane 330 and the large-area cathode 322. The e-beam chamber 300 further includes a high voltage insulator 324 and an accelerating field region 336 which isolate the grid anode 326 from the large-area cathode 322, a cathode cover insulator 328 located outside the vacuum chamber 320, a variable leak valve 332 for controlling the pressure inside the vacuum chamber 320, a variable high voltage power supply 329 connected to the large-area cathode 322, and a variable low voltage power supply 331 connected to the grid anode 326.

[0049] In operation, the substrate (not shown) with the low dielectric constant film thereon to be exposed with the electron beam is placed on the target plane 330. The vacuum chamber 320 is pumped from atmospheric pressure to a pressure in the range of about 1 mTorr to about 200 mTorr. The exact pressure is controlled by the variable rate leak valve 332, which is capable of controlling pressure to about 0.1 mTorr. The electron beam is generally generated at a sufficiently high voltage, which is applied to the large-area cathode 322 by the high voltage power supply 329. The voltage may range from about -500 volts to about 30,000 volts or higher. The high voltage power supply 329 may be a Bertan Model #105-30R manufactured by Bertan of Hickville, N.Y., or a Spellman Model #SL30N-1200X 258 manufactured by Spellman High Voltage Electronics Corp., of Hauppauge, N.Y. The variable low voltage power supply 331 applies a voltage to the grid anode 326 that is positive relative to the voltage applied to the large-area cathode 322. This voltage is used to control electron emission from the large-area cathode 322. The variable low voltage power supply 331 may be an Acopian Model #150PT12 power supply available from Acopian of Easton, Pa.

[0050] Other details of the e-beam chamber 300 are described in U.S. Pat. No. 5,003,178, entitled "Large-Area Uniform Electron Source", issued to William R. Livesay, assigned to Electron Vision Corporation (which is currently owned by the

assignee of the present invention) and is incorporated by reference herein to the extent not inconsistent with the invention.

[0051] In another embodiment, post-treating the low dielectric constant film comprises rapidly heating the low dielectric constant film to a desired high temperature, rapidly cooling the low dielectric constant film from the desired high temperature, and treating the low dielectric constant film with UV radiation. Preferably, the low dielectric constant film is treated with UV radiation simultaneously with at least a portion of the rapid heating and/or cooling of the low dielectric constant film. However, the low dielectric constant film may be treated with UV radiation before or after the low dielectric constant film is rapidly heated and cooled. In embodiments in which the low dielectric constant film is treated with UV radiation before or after the low dielectric constant film is rapidly heated and cooled, preferably, the low dielectric constant film is heated at a temperature between about 200°C and about 600°C during the UV radiation. For example, the low dielectric constant film may be exposed to UV radiation in a chamber such as a furnace having a UV source. The chamber may have either a vacuum or atmospheric ambient during the UV radiation treatment.

[0052] The low dielectric constant film may be exposed to one or more wavelengths of UV radiation. An example of a chamber and a method that may be used to expose the low dielectric constant film to UV radiation is provided in commonly assigned U.S. Patent No. 6,614,181, which is incorporated by reference herein.

[0053] In a further embodiment, the low dielectric constant film is post-treated by a method comprising rapidly heating and cooling the low dielectric constant film, treating the low dielectric constant film with UV radiation, and treating the low dielectric constant film with an electron beam. The post-treatment processes may be performed in any order. However, preferably, the low dielectric constant film is post-treated by rapidly heating and cooling the low dielectric constant film according to embodiments described herein and simultaneously UV radiating the low dielectric constant film and then treating the low dielectric constant film with an electron beam.

[0054] It is believed that post-treatments that include both rapidly heating and cooling the low dielectric constant film and UV radiating and/or treating the low dielectric constant film with an electron beam enhance the properties of the low dielectric constant film. For example, it is believed that a post-treatment that includes rapid heating and cooling and UV radiation lowers the dielectric constant of the deposited film. It is believed that a post-treatment that includes rapid heating and cooling, an electron beam treatment, and optionally UV radiation lowers the dielectric constant of the deposited film and increases the film's hardness and modulus.

[0055] In any of the embodiments described herein, the low dielectric constant films may be deposited and post-treated within an integrated processing system, such as the Centura[®] or Producer[®] platform, available from Applied Materials, Inc. Thus, the low dielectric constant film can be deposited and post-treated without exposing the film to atmosphere. In embodiments in which more than one post-treatment process is performed, the low dielectric constant film may be protected from atmosphere between the different post-treatment processes. For example, the low dielectric constant film may be transferred to an electron beam chamber after being rapidly heated and cooled and optionally UV radiated in another chamber without being exposed to atmosphere between the rapid heating and cooling and the electron beam treatment.

[0056] The following examples illustrate methods of processing substrates having low dielectric constant films deposited thereon. The films were deposited on 300 mm substrates using a Producer[®] CVD chamber, available from Applied Materials, Inc.

[0057] **Comparison Example 1**

[0058] A low dielectric constant film comprising silicon, carbon, and oxygen was deposited on a substrate from a gas mixture comprising OMCTS, trimethylsilane, and ethylene. The OMCTS was introduced into the chamber at a rate of 520 sccm, the trimethylsilane was introduced into the chamber at a rate of 300 sccm, and the

ethylene was introduced into the chamber at a rate of 2200 sccm. Helium was introduced into the chamber at a rate of 1000 sccm, and oxygen was introduced into the chamber at a rate of 1000 sccm. The film was deposited for 20 seconds at 400°C at a pressure of 5.7 Torr using 800 W RF power at 13.56 MHz. As deposited, the low dielectric constant film had a thickness of 5,043 Å, a dielectric constant (k) of 2.77, and a hardness of 0.59 gPa.

[0059] Comparison Example 2

[0060] A low dielectric constant film was deposited on a substrate as described in Comparison Example 1. The low dielectric constant film was post-treated by thermally annealing the low dielectric constant film at a temperature of 800°C for 1 minute. As deposited, the low dielectric constant film had a thickness of 5,085 Å. After the post-treatment, the low dielectric constant film had a thickness of 4,463 Å (shrinkage of 12.2%). After the post-treatment, the low dielectric constant film had a dielectric constant (k) of 3.35, and a hardness of 1.82 gPa.

[0061] Comparison Example 3

[0062] A low dielectric constant film was deposited on a substrate as described in Comparison Example 1. The low dielectric constant film was post-treated by an electron beam treatment at a current of 3 mA and a dose of 100 $\mu\text{C}/\text{cm}^2$ at 4.5 kV and 400°C. As deposited, the low dielectric constant film had a thickness of 5,074 Å. After the post-treatment, the low dielectric constant film had a thickness of 4,763 Å (shrinkage of 6.1%). After the post-treatment, the low dielectric constant film had a dielectric constant (k) of 2.74, and a hardness of 1.14 gPa.

[0063] Example 1

[0064] A low dielectric constant film was deposited on a substrate as described in Comparison Example 1. The low dielectric constant film was post-treated in a Radiance™ RTP chamber by rapidly heating the dielectric constant film from room temperature to a temperature of 800°C and then immediately cooling the low dielectric constant film to a temperature of 120°C such that the film is heated and

cooled within 30 seconds. As deposited, the low dielectric constant film had a thickness of 5,036 Å. After the post-treatment, the low dielectric constant film had a thickness of 5,021 Å (shrinkage of 0.3%). After the post-treatment, the low dielectric constant film had a dielectric constant (k) of 2.53, and a hardness of 0.62 gPa.

[0065] Example 2

[0066] A low dielectric constant film was deposited on a substrate as described in Comparison Example 1. The low dielectric constant film was post-treated in a Radiance™ RTP chamber by rapidly heating the dielectric constant film from room temperature to a temperature of 800°C and then immediately cooling the low dielectric constant film to a temperature of 120°C such that the film is heated and cooled within 30 seconds. As deposited, the low dielectric constant film had a thickness of 5,011 Å. After the post-treatment, the low dielectric constant film had a thickness of 4,996 Å (shrinkage of 0.3%). After the post-treatment, the low dielectric constant film had a dielectric constant (k) of 2.44.

[0067] Examples 1 and 2 show that post-treating low dielectric constant films by rapidly heating and cooling the low dielectric constant films according to embodiments described herein resulted in films having a lower dielectric constant than films that were not post-treated or films that were post-treated by an electron beam treatment or a conventional annealing process. It is believed that the low dielectric constant of films treated with the post-treatments provided herein may be achieved by the release of porogens, such as organic groups, from the low dielectric constant films upon post-treatment of the low dielectric constant films.

[0068] Example 1 further demonstrates that the rapid heating and cooling of the low dielectric constant films according to embodiments described herein did not substantially affect the hardness of the deposited film. The Examples also show that post-treating low dielectric constant films according to embodiments described herein resulted in less film shrinkage than other post-treatment processes.

[0069] Thus, embodiments of the invention provide a method of post-treating a low dielectric constant film that lowers the dielectric constant of the film without

reducing the hardness of the film and minimizes film shrinkage from the post-treatment. Other advantages of the rapid heating and cooling post-treatment of embodiments of the invention include a higher substrate throughput resulting from the quick post-treatment process and a lower thermal budget for substrates processed according to the embodiments.

[0070] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of processing a substrate, comprising:
depositing a low dielectric constant film comprising silicon and carbon on a substrate in the presence of RF power; and
post-treating the deposited low dielectric constant film by a process comprising:
heating the low dielectric constant film to a desired temperature of at least about 600°C at a rate of at least about 10°C/sec, wherein the low dielectric constant film is maintained at the desired temperature for about five seconds or less; and
then
cooling the low dielectric constant film at a rate of at least about 10°C/sec.
2. The method of claim 1, wherein the post-treating is performed under conditions sufficient to lower the dielectric constant of the low dielectric constant film.
3. The method of claim 1, wherein the low dielectric constant film is heated at a rate between about 10°C/sec and about 300°C/sec and cooled at a rate between about 10°C/sec and about 100°C/sec.
4. The method of claim 1, wherein the post-treating further comprises treating the low dielectric constant film with UV radiation.
5. The method of claim 4, wherein the process comprising heating and cooling the low dielectric constant film is performed simultaneously with the treating the low dielectric constant film with UV radiation.
6. The method of claim 5, wherein the post-treating further comprises treating the low dielectric constant film with an electron beam.

7. The method of claim 6, wherein the low dielectric constant film is post-treated in an integrated processing system such that the low dielectric constant film is not exposed to atmosphere between the heating and the treating of the low dielectric constant film with an electron beam.
8. The method of claim 4, wherein the process comprising heating and cooling the low dielectric constant film and the treating the low dielectric constant film with UV radiation are performed sequentially.
9. The method of claim 1, wherein the post-treating further comprises treating the low dielectric constant film with an electron beam.
10. The method of claim 9, wherein the low dielectric constant film is post-treated in an integrated processing system such that the low dielectric constant film is not exposed to atmosphere between the heating and the treating the low dielectric constant film with an electron beam.
11. The method of claim 1, wherein the low dielectric constant film further comprises oxygen.
12. A method of processing a substrate, comprising:
 - depositing a low dielectric constant film comprising silicon and carbon on a substrate in the presence of RF power; and
 - post-treating the deposited low dielectric constant film by a process comprising:
 - heating the low dielectric constant film from a temperature of between about 25°C and about 250°C to a temperature of between about 600°C and about 1000°C, wherein the low dielectric constant film is heated at the temperature of between about 600°C and about 1000°C for about five seconds or less; and then
 - cooling the low dielectric constant film from a temperature of between about 600°C and about 1000°C, wherein the low dielectric constant film is heated and cooled within a time period of about 0.5 minutes to about 5 minutes.

13. The method of claim 12, wherein the low dielectric constant film is heated at a rate between about 10°C/sec and about 300°C/sec and cooled at a rate between about 10°C/sec and about 100°C/sec.

14. The method of claim 12, wherein the post-treating further comprises treating the low dielectric constant film with UV radiation.

15. The method of claim 12, wherein the post-treating further comprises treating the low dielectric constant film with an electron beam.

16. The method of claim 12, wherein the cooling the low dielectric constant film comprises exposing the substrate to backside gas.

17. A method of processing a substrate, comprising:

depositing a low dielectric constant film comprising silicon and carbon on a substrate in the presence of RF power; and

post-treating the deposited low dielectric constant film by a process comprising:

heating the low dielectric constant film to a desired temperature at a rate of at least about 10°C/sec, wherein the low dielectric constant film is maintained at the desired temperature for about five seconds or less; and then

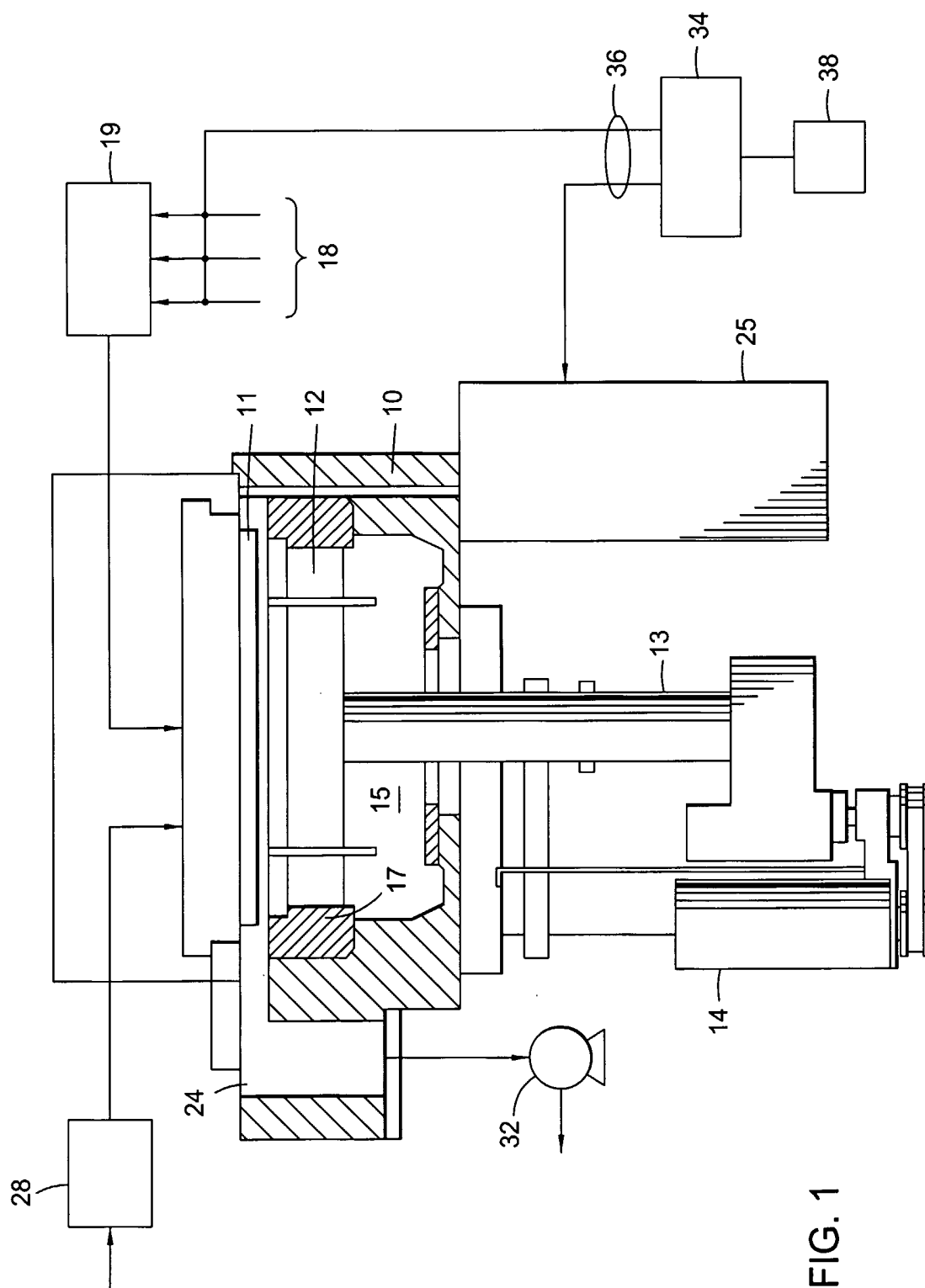
cooling the low dielectric constant film at a rate of at least about 10°C/sec, wherein the low dielectric constant film is heated and cooled within a time period of about 0.5 minutes to about 5 minutes.

18. The method of claim 17, wherein the low dielectric constant film is heated from a temperature of between about 25°C and about 250°C, and the desired temperature is between about 800°C and about 900°C.

19. The method of claim 17, wherein the post-treating further comprises treating the low dielectric constant film with UV radiation.

20. The method of claim 17, wherein the post-treating further comprises treating the low dielectric constant film with an electron beam.

1/3



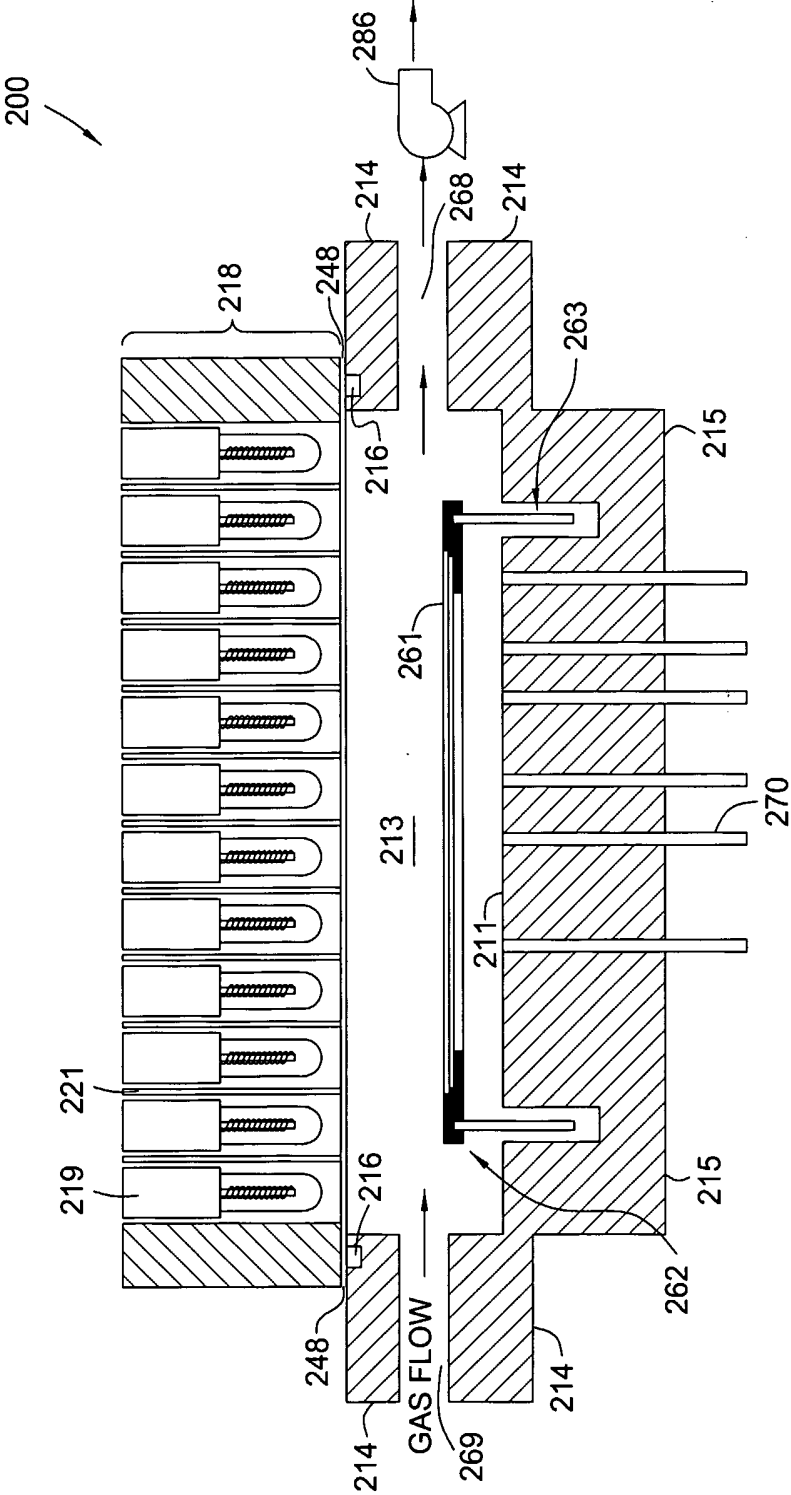


FIG. 2

3/3

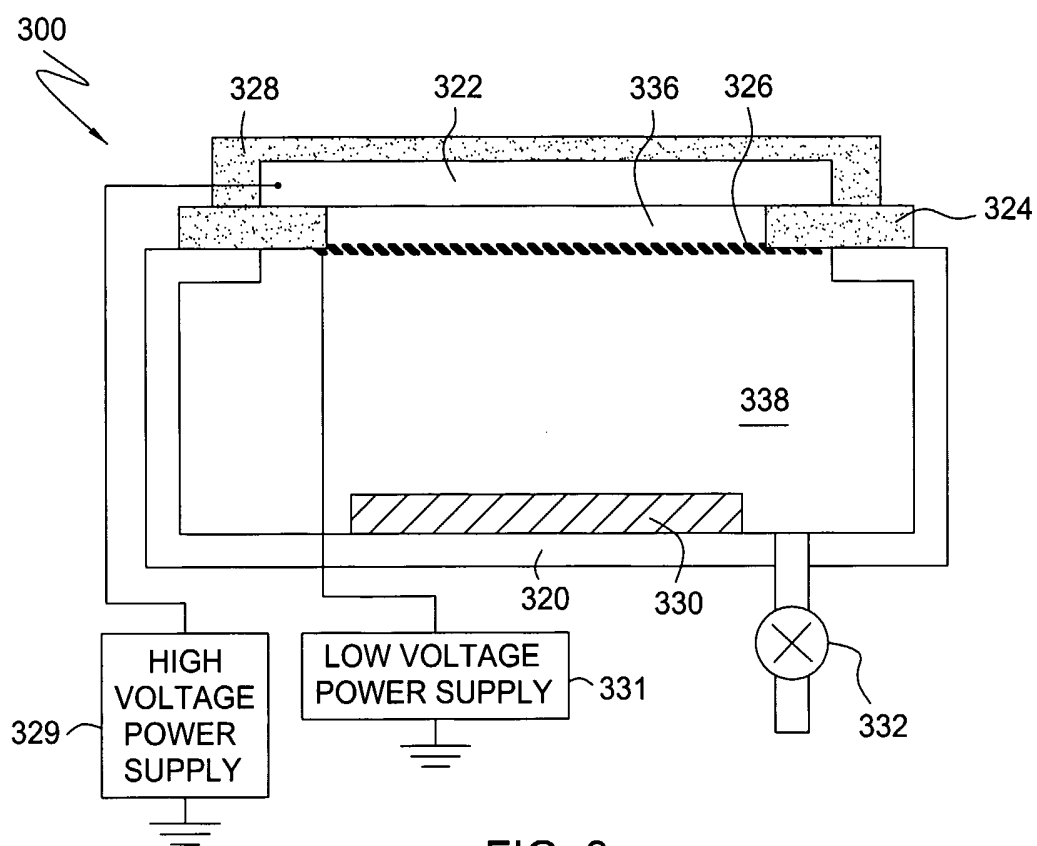


FIG. 3

INTERNATIONAL SEARCH REPORT

PCT/US2005/002927

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H01L21/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 033 999 A (WU ET AL) 7 March 2000 (2000-03-07) column 2, line 29 - line 64 -----	1-20
Y	US 2004/002226 A1 (BURNHAM JAY S ET AL) 1 January 2004 (2004-01-01) paragraph '0025! - paragraph '0032!; figure 9 -----	1-3,6,7, 9-13,15, 17,20
Y	US 6 566 278 B1 (HARVEY KEITH R ET AL) 20 May 2003 (2003-05-20) column 1, line 43 - column 2, line 18; table 2 -----	4,5,8, 14,19
Y	US 2002/110934 A1 (UCHIYAMA KIYOSHI ET AL) 15 August 2002 (2002-08-15) paragraph '0087! -----	16
	-/--	



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

° Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
 "E" earlier document but published on or after the international filing date
 "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
 "O" document referring to an oral disclosure, use, exhibition or other means
 "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
 "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
 "&" document member of the same patent family

Date of the actual completion of the international search

6 April 2005

Date of mailing of the international search report

19/04/2005

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Bakker, J

INTERNATIONAL SEARCH REPORT

PCT/US2005/002927

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 025 279 A (CHIANG ET AL) 15 February 2000 (2000-02-15) claims 1,5,6; table 2 -----	18
A	US 2002/162500 A1 (HONG SOONIL ET AL) 7 November 2002 (2002-11-07) Radiance chamber paragraph '0026! - paragraph '0046! -----	1,12,16, 17
A	US 2003/143865 A1 (GRILL ALFRED ET AL) 31 July 2003 (2003-07-31) paragraphs '0036!, '0037!, '0050! -----	1-20
A	US 2001/004479 A1 (CHEUNG DAVID ET AL) 21 June 2001 (2001-06-21) the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

PCT/US2005/002927

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6033999	A	07-03-2000	NONE
US 2004002226	A1	01-01-2004	JP 2004048001 A 12-02-2004
US 6566278	B1	20-05-2003	NONE
US 2002110934	A1	15-08-2002	TW 518696 B 21-01-2003 WO 02065536 A2 22-08-2002
US 6025279	A	15-02-2000	NONE
US 2002162500	A1	07-11-2002	WO 02089186 A2 07-11-2002
US 2003143865	A1	31-07-2003	US 2002180051 A1 05-12-2002 US 2002137359 A1 26-09-2002 CN 1479804 A 03-03-2004 EP 1352107 A2 15-10-2003 JP 2004515057 T 20-05-2004 WO 0243119 A2 30-05-2002 US 2003234450 A1 25-12-2003 US 2003139062 A1 24-07-2003 US 2002098714 A1 25-07-2002 TW 563202 B 21-11-2003
US 2001004479	A1	21-06-2001	US 6054379 A 25-04-2000 US 6072227 A 06-06-2000 US 6287990 B1 11-09-2001 EP 1055012 A2 29-11-2000 JP 2002503879 T 05-02-2002 TW 408369 B 11-10-2000 WO 9941423 A2 19-08-1999 US 2003064610 A1 03-04-2003 US 2001005546 A1 28-06-2001 US 2003162410 A1 28-08-2003 US 6593247 B1 15-07-2003 US 6562690 B1 13-05-2003 US 6541282 B1 01-04-2003 US 2004029400 A1 12-02-2004 US 2004082199 A1 29-04-2004 US 2004038545 A1 26-02-2004 US 6627532 B1 30-09-2003 US 2004166665 A1 26-08-2004 US 2005023694 A1 03-02-2005 US 6596655 B1 22-07-2003 US 2002074309 A1 20-06-2002 US 2002084257 A1 04-07-2002 US 2003113992 A1 19-06-2003 US 6340435 B1 22-01-2002 US 6413583 B1 02-07-2002 US 6511909 B1 28-01-2003 US 6511903 B1 28-01-2003 US 2002000670 A1 03-01-2002 US 6660663 B1 09-12-2003 US 6537929 B1 25-03-2003 US 2004147109 A1 29-07-2004 US 2004201103 A1 14-10-2004 US 2002045361 A1 18-04-2002 US 2002111042 A1 15-08-2002

INTERNATIONAL SEARCH REPORT

PCT/US2005/002927

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001004479 A1		US 2003124859 A1	03-07-2003
		US 2005059264 A1	17-03-2005
