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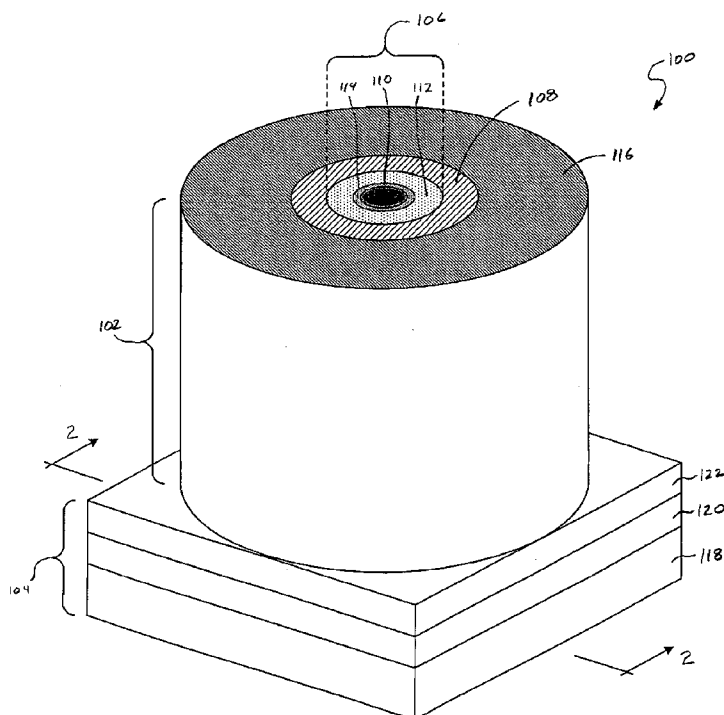


Figure 1A

(57) Abstract: Various embodiments of the present invention are directed to surface-plasmon-enhanced electromagnetic-radiation-emitting devices and to methods of fabricating these devices. In one embodiment of the present invention, an electromagnetic-radiation-emitting device (100) comprises a multilayer core (106), a metallic device layer (108), and a substrate (104). The multilayer core (106) has an inner layer (110) and an outer layer (112), wherein the outer layer is configured to surround at least a portion of the inner layer. The metallic device layer (108) is configured to surround at least a portion of the outer layer. The substrate (104) has a bottom conducting layer (118) in electrical communication with the inner layer (110) and a top conducting layer (122) in electrical communication with the metallic device layer (108) such that the exposed portion emits surface-plasmon-enhanced electromagnetic radiation when an appropriate voltage is applied between the bottom conducting layer and the top conducting layer.



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PLASMON-ENHANCED ELECTROMAGNETIC-RADIATION-EMITTING DEVICES AND METHODS FOR FABRICATING THE SAME

TECHNICAL FIELD

5 Embodiments of the present invention are directed to electromagnetic-radiation-emitting devices, and, in particular, to plasmon-enhanced electromagnetic-radiation-emitting devices that can be implemented in photonic devices.

BACKGROUND

10 In recent years, the increasing density of microelectronic devices on integrated circuits has lead to a technological bottleneck in the density of metallic signal lines that can be used to interconnect these devices. In addition, the use of metallic signal lines yields a significant increase in power consumption and difficulties with synchronizing the longest links positioned on top of most circuits. Rather than transmitting information as
15 electrical signals via signal lines, the same information can be encoded in electromagnetic radiation ("ER") and transmitted via waveguides, such as optical fibers, ridge waveguides, and photonic crystal waveguides. Transmitting information encoded in ER via waveguides has a number of advantages over transmitting electrical signals via signal lines. First, degradation or loss is much less for ER transmitted via waveguides
20 than for electrical signals transmitted via signal lines. Second, waveguides can be fabricated to support a much higher bandwidth than signal lines. For example, a single Cu or Al wire can only transmit a single electrical signal, while a single optical fiber can be configured to transmit about 100 or more differently encoded ER.

 Recently, advances in materials science and semiconductor fabrication techniques
25 have made it possible to develop photonic devices that can be integrated with electronic devices, such as CMOS circuits, to form photonic integrated circuits ("PICs"). The term "photonic" refers to devices that can operate with either classically characterized electromagnetic radiation or quantized electromagnetic radiation with frequencies that span the electromagnetic spectrum. PICs are the photonic equivalent of electronic
30 integrated circuits and may be implemented on a wafer of semiconductor material. In

order to effectively implement PICs, passive and active photonic components are needed. Waveguides and attenuators are examples of passive photonic components that can typically be fabricated using conventional epitaxial and lithographic methods and may be used to direct the propagation of ER between microelectronic devices. Physicists and engineers have recognized a need for active photonic components, such as ER emitting devices and modulators, that can be implemented in PICs and other photonic devices.

SUMMARY

Various embodiments of the present invention are directed to surface-plasmon-enhanced electromagnetic-radiation-emitting devices and to methods of fabricating these devices. In one embodiment of the present invention, an electromagnetic-radiation-emitting device comprises a multilayer core, a metallic device layer, and a substrate. The multilayer core has an inner layer and an outer layer, wherein the outer layer is configured to surround at least a portion of the inner layer. The metallic device layer is configured to surround at least a portion of the outer layer. The substrate has a bottom conducting layer in electrical communication with the inner layer and a top conducting layer in electrical communication with the metallic device layer such that the exposed portion emits surface-plasmon-enhanced electromagnetic radiation when an appropriate voltage is applied between the bottom conducting layer and the top conducting layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A shows an isometric view of an electromagnetic-radiation-emitting device in accordance with embodiments of the present invention

Figure 1B shows a top view of the electromagnetic-radiation-emitting device shown in Figure 1A in accordance with embodiments of the present invention.

Figure 2 shows a cross-sectional view of the electromagnetic-radiation-emitting device, along a line 2-2 shown in Figure 1, in accordance with embodiments of the present invention.

Figure 3 shows a cross-sectional view of a multilayer core and a metallic device layer in accordance with embodiments of the present invention.

Figures 4A-4I show isometric and cross-sectional views that correspond to steps of a method for fabricating the electromagnetic-radiation-emitting device, shown in Figures 1-2, in accordance with embodiments of the present invention.

5 DETAILED DESCRIPTION

Various embodiments of the present invention are directed to surface-plasmon-enhanced electromagnetic-radiation-emitting ("SPE ERE") devices and to methods of fabricating the SPE ERE devices. An SPE ERE device includes an ER source that can generate modulated ER with greater speed and efficiency than typical ER emitting
10 sources, such as light emitting diodes. SPE ERE devices can be used as sources of modulated ER in a variety of different PICs. In the various device and fabrication embodiments described below, a number of structurally similar components comprising the same materials have been provided with the same reference numerals and, in the interest of brevity, an explanation of their structure and function is not repeated.

15 Figure 1A shows an isometric view of an SPE ERE device 100, respectively, in accordance with embodiments of the present invention. SPE ERE device 100 comprises a multilayer ER source 102 that is supported by and in electrical communication with a layered substrate 104. ER source 102 includes a multilayer core 106 and a metallic device layer 108 which is configured to surround at least a portion of multilayer core 106.
20 Multilayer core 106 includes an inner layer 110 and an outer layer 112 surrounding at least a portion of inner layer 110. Multilayer core 106 may also include an intermediate layer 114 positioned between inner layer 110 and outer layer 112 and an optional outer layer 116 surrounding at least a portion of metallic device layer 108. Layered substrate 104 may include a bottom conducting layer 118, a middle dielectric layer 120, and a top
25 conducting layer 122. Middle dielectric layer 120 serves as a layer of insulation between top conducting layer 122 and bottom conducting layer 118. Top conducting layer 122 can be an extended portion of metallic device layer 108, or top conducting layer 122 can be comprised of a semiconductor or conductor that is in electrical communication with metallic device layer 108. Bottom conducting layer 118 can be the Si layer of a silicon-

on-insulator substrate where the Si layer is in electrical communication with inner layer 110 as described below with reference to Figure 2.

Figure 1B shows a top view of ER source 102 in accordance with embodiments of the present invention. As shown in Figures 1A-1B, layers 108, 110, 112, and 114 of multilayer core 106 are exposed in order to emit electromagnetic radiation generated within ER source 102, as described below with reference to Figure 3. Note that ER source 102 shown in Figure 1 is not limited to a cylindrical configuration. For example, ER source 102 can have an elliptical, a square, a rectangular, hexagonal an irregular, or any other suitable cross-sectional shape.

Optional outer layer 116 can be composed of a metal or semiconductor, and both optional outer layer 116 and middle layer 120 can be comprised of SiO_2 , Si_3N_4 , or another suitable dielectric material. Metallic device layer 108 can be comprised of gold, titanium, nickel, chromium, platinum, palladium, aluminum, or another suitable metal conductor or metal alloy. Multilayer core 106 and bottom conducting layer 118 can be comprised of an indirect bandgap elemental semiconductor or a direct or indirect bandgap compound semiconductor. Elemental semiconductors include Si and Ge. Compound semiconductors are typically III-V materials, where Roman numerals III and V represent elements in the third and fifth columns of the Periodic Table of the Elements. Compound semiconductors can be classified according the quantities of III and V elements comprising the semiconductor. For example, binary semiconductor compounds include GaAs, InP, InAs, and GaP; ternary semiconductor compounds include $\text{GaAs}_y\text{P}_{1-y}$, where y ranges between 0 and 1; and quaternary semiconductor compounds include $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$, where both x and y range between 0 and 1.

Elemental composition of compound semiconductor can be varied in order to emit electromagnetic radiation with a particular wavelength. For example, GaAs is a direct bandgap III-V semiconductor that emits electromagnetic radiation with wavelengths in the infrared portion of the electromagnetic spectrum, while GaP is an indirect bandgap semiconductor that emits electromagnetic radiation with wavelengths in a different portion of the electromagnetic spectrum. Quaternary semiconductors can be used to emit electromagnetic radiation over other portions of the electromagnetic spectrum. For

example, the elemental quantities in InAlGaP semiconductors can be varied to emit electromagnetic radiation with wavelengths in the red, yellow, and orange visible portions of the electromagnetic spectrum, and the elemental quantities of AlGaInN semiconductors can be varied to emit electromagnetic radiation with wavelengths in the blue and green visible portions of the electromagnetic spectrum.

In certain embodiments of the present invention, inner layer 110 can be a *p*-type semiconductor, and outer layer 112 can be an *n*-type semiconductor. In other embodiments of the present invention, inner layer 110 can be an *n*-type semiconductor, and outer layer 112 can be a *p*-type semiconductor. In other words, inner layer 110 and outer layer 112 form two layers of a *pn* diode. The terms "*p*-type semiconductor" refer to intrinsic semiconductors that have been doped with an electron acceptor impurity, such as boron in silicon, in order to increase the number of free positive carrier called "holes," and the terms "*n*-type semiconductor" refer to intrinsic semiconductors that have been doped with an electron donor impurity, such as arsenic in silicon, in order to increase the number of free electrons. Holes and electrons are two types of charge carriers. Intermediate layer 114 can be a depletion region which forms across the junction or interface of a *p*-type semiconductor and an *n*-type semiconductor. The carrier concentration difference between inner layer 110 and outer layer 112 creates an electric field across the depletion region, as described below. Carriers diffuse from regions of high concentration to regions of low concentration. In particular, holes originating in a *p*-type semiconductor of multilayer core 106 diffuse part way into the *n*-type semiconductor of multilayer core 106, which has a lower concentration of holes than the *p*-type semiconductor. Similarly, electrons from the *n*-type semiconductor of multilayer core 106 diffuse part way into the *p*-type semiconductor of multilayer core 106, which has a higher concentration of electrons than the *p*-type semiconductor. As charge carriers diffuse, they leave behind the ionized dopants that created them. This charge carrier migration stops when the electric field created between the *n*-type and *p*-type semiconductor layers of multilayer core 106 force a number of charge carriers to drift back at the same rate charge carriers diffuse, which, in turn, leaves a depletion region represented by intermediate layer 114. The thickness of intermediate layer 114 depends

upon the dopant concentrations in inner layer 110 and outer layer 112. In other embodiments of the present invention, intermediate layer 114 can be comprised of an intrinsic semiconductor, in which case, inner layer 110, intermediate layer 114, and outer layer 112 form the three layers of a *p-i-n* diode.

5 Figure 2 shows a cross-sectional view of SPE ERE device 100, along a line 2-2 shown in Figure 1, in accordance with embodiments of the present invention. As shown in Figure 2, ER source 102 is supported by substrate 104. The inner surface of metallic device layer 108 is in contact with the outer surface of outer layer 112, and metallic device layer 108 extends horizontally outward at the bottom to form top conducting layer 122 of substrate 104. Top conducting layer 122 and metallic device layer 108 can be formed from a single piece of metal, as shown in Figure 2. However, in other embodiments of the present invention, top conducting layer 122 can be formed from a separate metallic layer or semiconductor layer. In these embodiments, metallic device layer 108 and top conducting layer 122 are in electrical communication with one another. 10 A portion of inner layer 110 passes through an opening 202 in middle dielectric layer 120, and the bottom surface of inner layer 110 is in contact with bottom conducting layer 118 so that inner layer 110 can be in electrical communication with bottom conducting layer 118. As mentioned above with reference to Figure 1, bottom conducting layer 118 can be the Si layer of a silicon-on-insulator substrate. Middle dielectric layer 120 provides a layer of electrical insulation between top conducting layer 122 and bottom conducting layer 118. Top conducting layer 122 and bottom conducting layer 118 are in electrical communication with a voltage source 204. 15 20

Figure 3 shows a cross-sectional view of multilayer core 106 and metallic device layer 108 in accordance with embodiments of the present invention. Rather than referring to the cross-sectional view shown in Figure 2, for the sake of simplicity in describing the operation of SPE ERE device 100, voltage source 204 is connected directly to inner layer 110 and metallic device layer 108. Assuming that inner layer 110 is a *p*-type semiconductor and outer layer 112 is an *n*-type semiconductor, a positive voltage applied to inner layer 110 and a negative voltage applied to outer layer 112 causes the electrons in outer layer 112 to flow toward intermediate layer 114 and the 25 30

holes in inner layer 110 to flow toward intermediate layer 114. As a result, the width of intermediate layer 114 narrows. When the level of the applied voltage is large enough, the electrons combine with the holes in or near intermediate layer 114 releasing energy in a process called "recombination." As long as the voltage is applied, electrons and holes
5 continue to flow through the layers 110 and 112 and undergo recombination in or near intermediate layer 114. For a multilayer core 106 comprised of an indirect semiconductor, a portion of the energy released is non-radiative, and the remainder is emitted as photons. By contrast, for a multilayer core 106 comprised of a direct semiconductor, most of the energy is released as photons. This is the same process by
10 which ER is typically emitted from a light emitting diode.

Instead of forming photons in the multilayer core 106, an electron-hole pair can recombine into a surface plasmon propagating along interface 302 between outer layer 112 and metallic device layer 108. Plasmons are modes of ER that correspond to quantized states of electron plasma oscillations in a metal. A surface plasmon is a mode
15 of electron excitation existing on the surface of a metal and has both longitudinal and transverse components. Surface plasmons can feature a high density electric field and slow group velocities leading to a substantial increase in the radiative recombination rate of an electron-hole pair. Under the right design, an electron-hole pair will most of the time decay into a surface plasmon mode, rather than into a photon or through a non-
20 radiative channel. The recombination rate and the radiative efficiency of the device will be increased as a result. After propagating along the wire, the surface plasmon will itself decay into free space radiation upon reaching the edge of the wire.

Figure 3 includes a schematic representation of portions 304 and 306 of a surface plasmon propagating upward along interface 302 of multilayer core 106 and metallic
25 device layer 108. Surface plasmons have both transverse and longitudinal electromagnetic field components. The magnetic field component is parallel to interface 302 and perpendicular to the propagation direction, and the electric field component is parallel to the direction of the surface plasmon propagation and perpendicular to interface 302. Curve 308 represents the extent to which the electric field component extends into
30 metallic device layer 108, and curve 310 represents the extent to which the electric field

component extends into multilayer core 106. Curves 308 and 310 show how the electric field components decay exponentially away from interface 302. Because the dielectric constant associated with metallic device layer 108 is greater than the dielectric constant associated with multilayer core 106, the electric field component has shorter penetration
5 depth in metallic device layer 108 than in multilayer core 106.

SPE ERE device 100 embodiments can more efficiently generate ER and more quickly modulate ER than typical light emitting diodes. The surface plasmon speeds up the electron/hole recombination process taking place within the multilayer core 106. As a result, ER source 102 can be operated as a high-speed ER emitting modulator by varying
10 the voltage applied to ER source 102. In other words, by varying the voltage applied to the ER source 102, the ER output can be modulated such that analog or digital information appears in the emitted ER, which can be directed at a detector. In addition, ER source 102 can be modulated at a much higher rate than can a typical electromagnetic-radiation-emitting diode, such as a light emitting diode. In addition, ER
15 source 102 may be more efficient at emitting ER than a typical ER emitting diode, such as a light emitting diode, since the ratio of radiative to non-radiative recombination rates may be substantially increased. In other words, by forming surface plasmons along interface 302, ER source 102 may emit higher intensity ER which can be modulated more quickly than ER generated from a typical ER emitting diode.

Figures 4A-4I show isometric and cross-sectional views that correspond to steps of a method for fabricating the SPE ERE device 100, shown in Figure 1, in accordance with embodiments of the present invention. Initially, as shown in an isometric view of Figure 4A and a cross-sectional view of Figure 4B, middle dielectric layer 120 can be formed on bottom conducting layer 118 using chemical vapor deposition ("CVD"),
25 physical vapor deposition, thermal oxidation, or spin on glass.

Next, as shown in an isometric view of Figure 4C and in a cross-sectional view of Figure 4D, opening 202 can be formed in middle dielectric layer 120 by first defining opening 202 using, for example, block-copolymer lithography, nanoimprint lithography, or electron beam lithography followed by removing the dielectric material from the
30 region defining opening 202 using reactive ion etching, chemically assisted ion beam

etching, or wet etching. In other embodiments of the present invention, opening 202 can be formed by focused ion beam milling. Opening 202 exposes a portion of the top surface of bottom conducting layer 118.

Next, as shown in Figure 4E, using well-known methods, such as galvanic displacement, a seed particle 402 can be formed in opening 202. Seed particle 402 can be a gold, titanium, nickel, chromium, platinum, palladium, aluminum, or another suitable metal conductor or metal alloy. Next, as shown in Figure 4F, using CVD, inner layer 110 can be grown in accordance with well-known vapor-liquid-solid ("VLS") growth mechanism or vapor-solid-solid ("VSS") growth mechanism. For example, in order to form an inner layer 110 composed of InAs, CVD can be used with vapor-phase reactants $\text{In}(\text{CH}_3)_3$ and AsH_3 . Continued supply of the vapor-phase reactants $\text{In}(\text{CH}_3)_3$ and AsH_3 results in supersaturation, which eventually causes precipitation of excess liquid-phase InAs beneath seed particle 202. The excess InAs material precipitates from the supersaturated seed particle 202 onto the substrate, pushing seed particle 202 away from the substrate and forming the column of material, which is inner layer 110. The length of inner layer 110 can be controlled by varying the length of exposure time to the vapor-phase reactants. While inner layer 110 is growing, a *p*-type or an *n*-type dopant can be added to the CVD reaction chamber forming a *p*-type semiconductor inner layer 110 or an *n*-type semiconductor inner layer 110. Alternatively, inner layer 110 can be doped with a *p*-type or an *n*-type dopant after formation using implantation or dopant diffusion or implantation followed by annealing.

Next, as shown in Figure 4G, outer layer 112 surrounding the outer surface of inner layer 110 can be formed using CVD. Outer layer 112 can be doped during formation by introducing a *p*-type or an *n*-type dopant to the reaction chamber while outer layer 112 is forming. Alternatively, a dopant can be added to already formed outer layer 112 using dopant diffusion or implantation followed by annealing. Intermediate layer 114 can be formed as a result of depletion, as described above, or intermediate layer 114 can be formed prior to forming outer layer 112 by depositing an intrinsic semiconductor layer 114 (not shown) over inner layer 110 using CVD followed by forming outer layer 112.

Next, as shown in Figure 4H, a metallic layer 404 is deposited over substantially the entire exposed surface using CVD or MBD. As shown in Figure 4I, an optional layer 406 can be deposited over metallic layer 404. Optional layer 406 can be composed of a metal, semiconductor, or dielectric material and can be deposited using CVD, physical vapor deposition, such as sputtering, electron-beam evaporation, MBD, or spin on glass. Planarization techniques can be used to expose a portion of metallic device layer 108 and expose portions of inner layer 110 and out layer 112 in order to obtain SPE ERE device 100, shown in Figures 1-2.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. The foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive of or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations are possible in view of the above teachings. The embodiments are shown and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents:

CLAIMS

1. An electromagnetic-radiation-emitting device (100) comprising:
 - a multilayer core (106) having an inner layer (110) and an outer layer (112), wherein the outer layer is configured to surround at least a portion of the inner layer;
 - a metallic device layer (108) configured to surround at least a portion of the outer layer; and
 - a substrate (104) having a bottom conducting layer (118) in electrical communication with the inner layer and a top conducting layer (122) in electrical communication with the metallic device layer such that the exposed portion emits surface-plasmon-enhanced electromagnetic radiation when an appropriate voltage is applied between the bottom conducting layer and the top conducting layer.
2. The device of claim 1 wherein the multilayer core (106) further comprises one of:
 - the inner layer (110) is a *p*-type semiconductor and the outer layer (112) is an *n*-type semiconductor; and
 - the inner layer (110) is an *n*-type semiconductor and the outer layer (112) is a *p*-type semiconductor.
3. The device of claim 1 further comprises an intermediate layer (114) located between the inner layer (110) and the outer layer (112) such that the intermediate layer can be a depletion region or composed of an intrinsic semiconductor.
4. The device of claim 1 wherein the top conducting layer (122) further comprises one of:
 - a metallic layer; and
 - a semiconductor layer.
5. The device of claim 1 wherein the bottom conducting layer (118) further comprises one of:
 - a Si layer of silicon-on-insulator substrate; and

a semiconductor layer.

6. A method of fabricating an electromagnetic-radiation-emitting device (100), the method comprising:

forming a dielectric layer (120) on a semiconductor substrate (118), the dielectric layer having a top surface and a bottom surface attached to the semiconductor substrate;

forming a multilayer core (106) on the top surface of the dielectric layer, the multilayer core including an inner layer and an outer layer surrounding at least a portion of the inner layer, the inner layer extends through the dielectric layer and is in electrical contact with the semiconductor substrate; and

depositing a metallic layer (108) over the multilayer core.

7. The method of claim 6 further comprising forming a top surface by planarizing the electromagnetic-radiation-emitting device to expose the portions of the inner layer, the outer layer, and the metallic layer that form the exposed portion of the multilayer core.

8. The method of claim 10 wherein forming the multilayer core further comprises:

forming a opening (202) in the dielectric layer (120);

depositing a seed material (402) in the opening ;

growing the inner layer (110) in the form of a column in the opening wherein the seed material in the opening serves as a nucleus for forming the column;

depositing the outer layer (112).

9. The method of claim 8 further comprises depositing an optional layer of metal, semiconductor, or dielectric material over the metallic layer using one of:

chemical vapor deposition; and

physical vapor deposition.

10. The method of claim 14 wherein growing the inner layer in the form of a column in the opening further comprises vapor-liquid-solid processing.

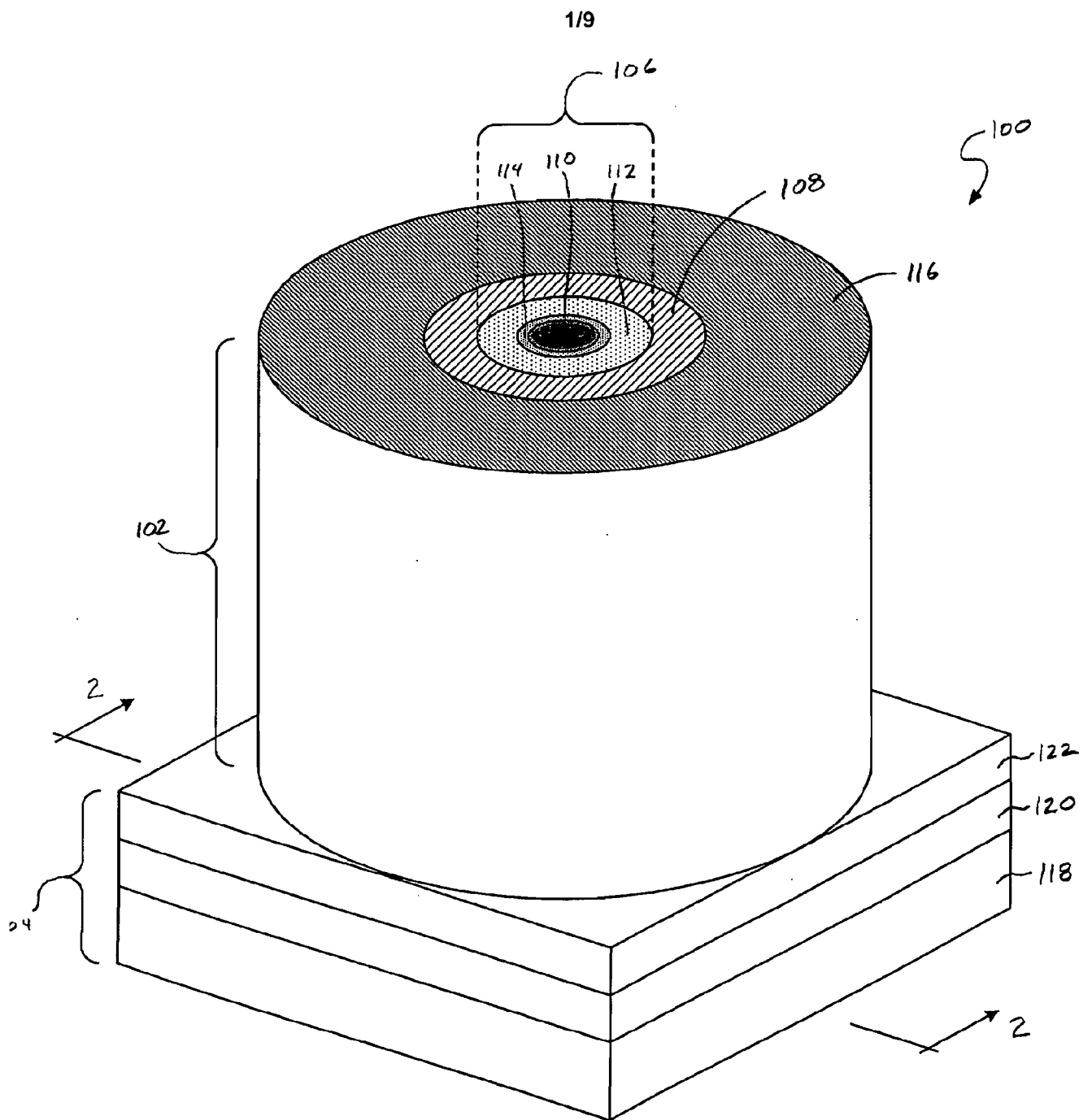


Figure. 1A

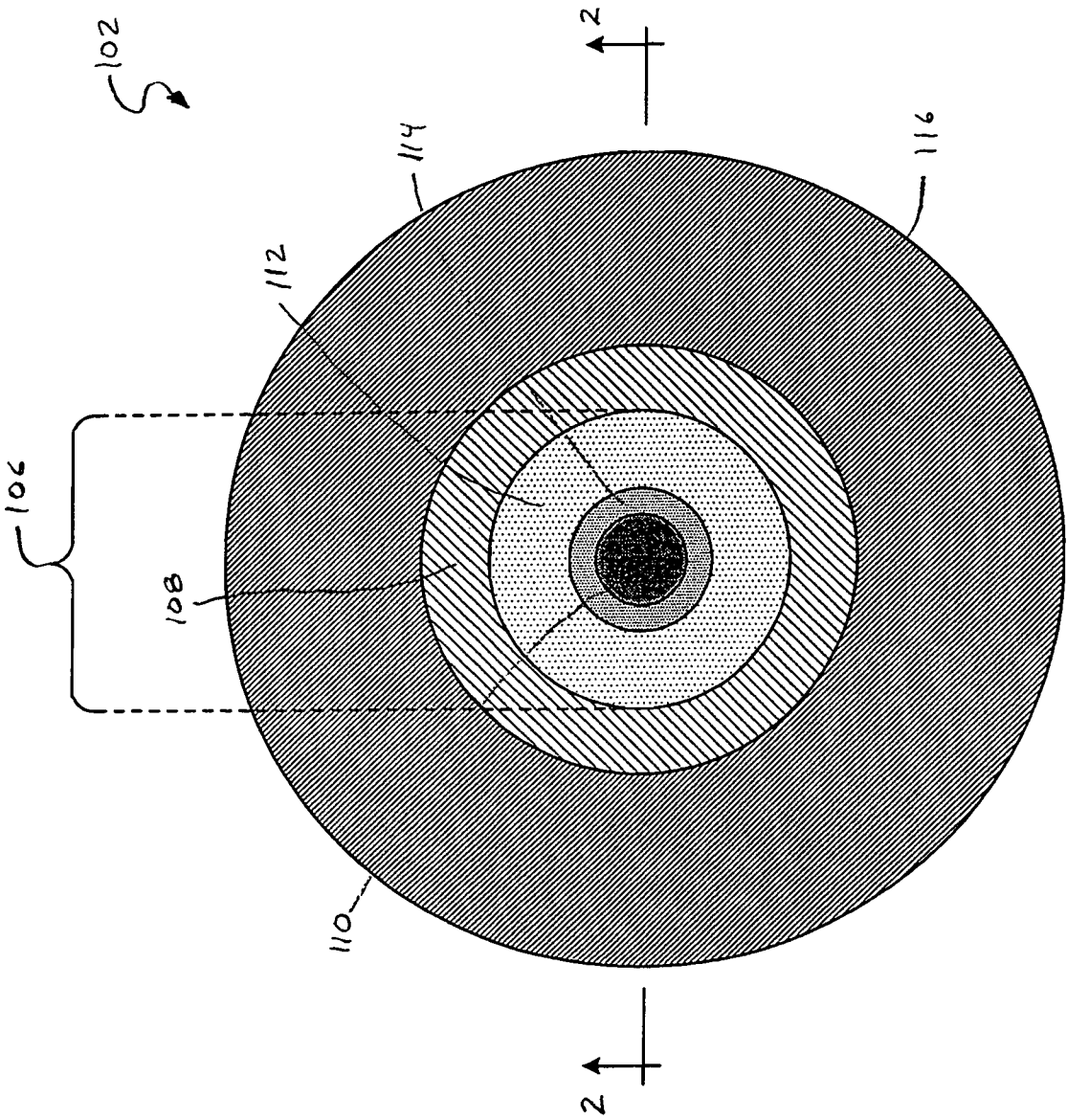


Figure. 1B

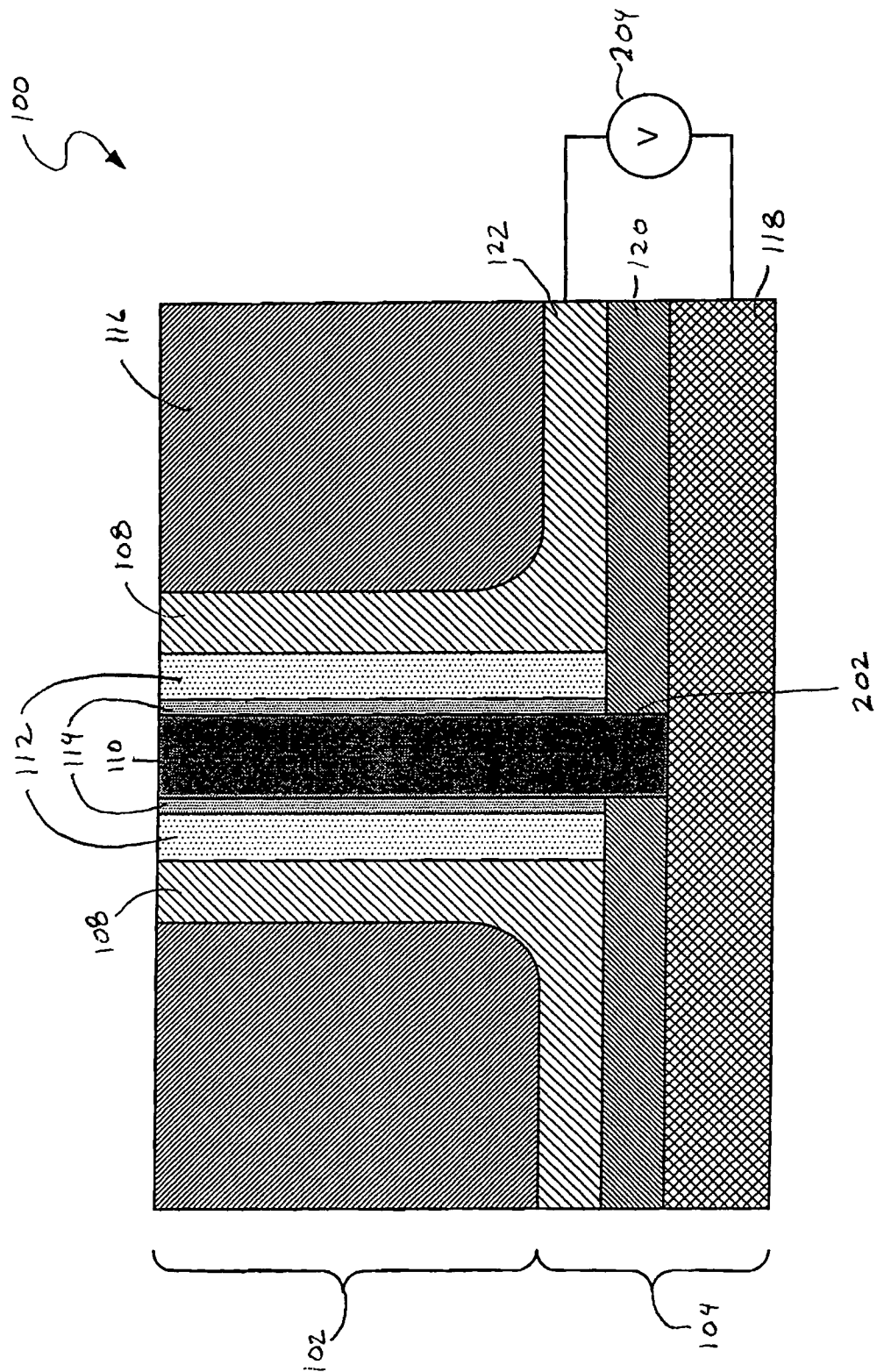


Figure 2

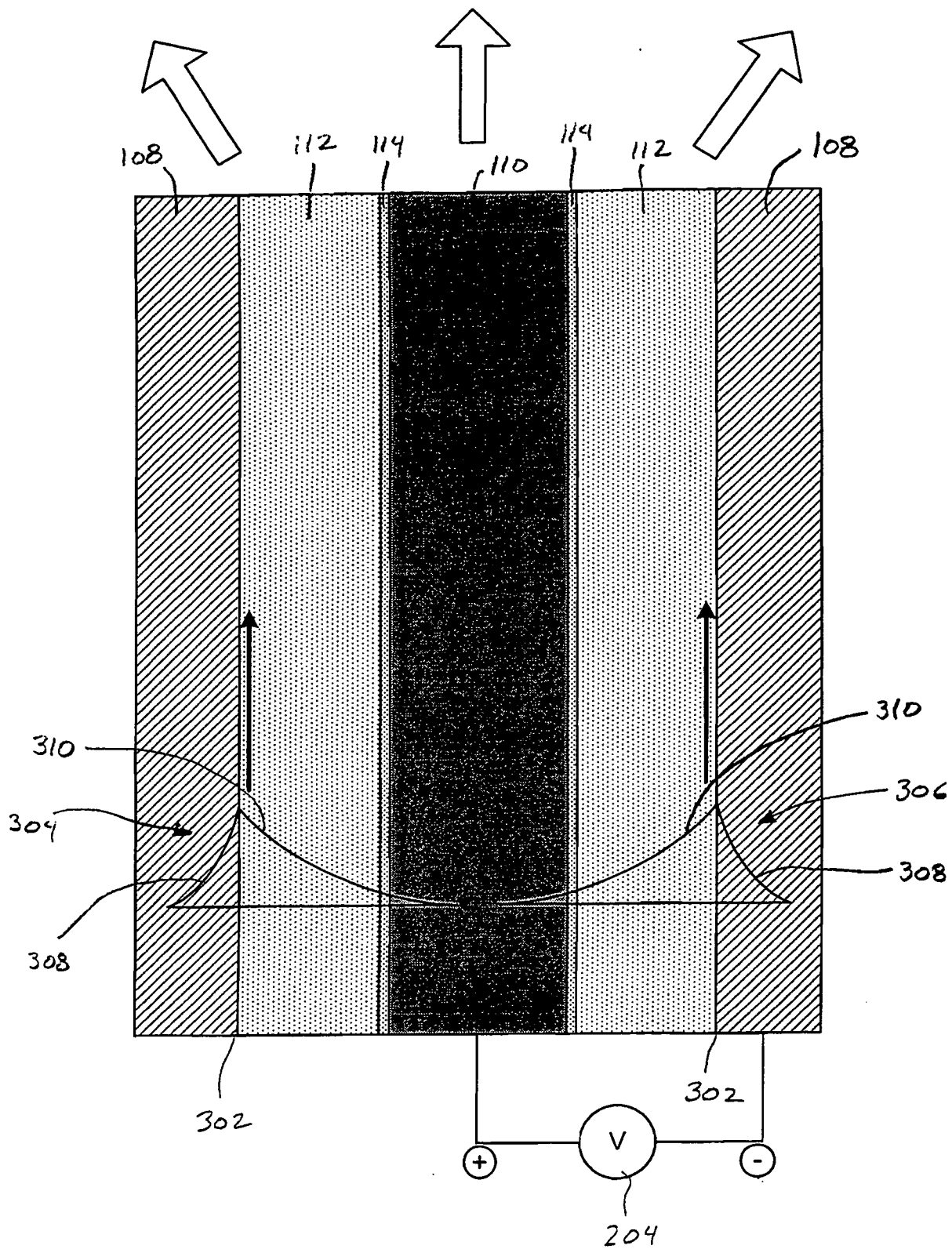


Figure 3

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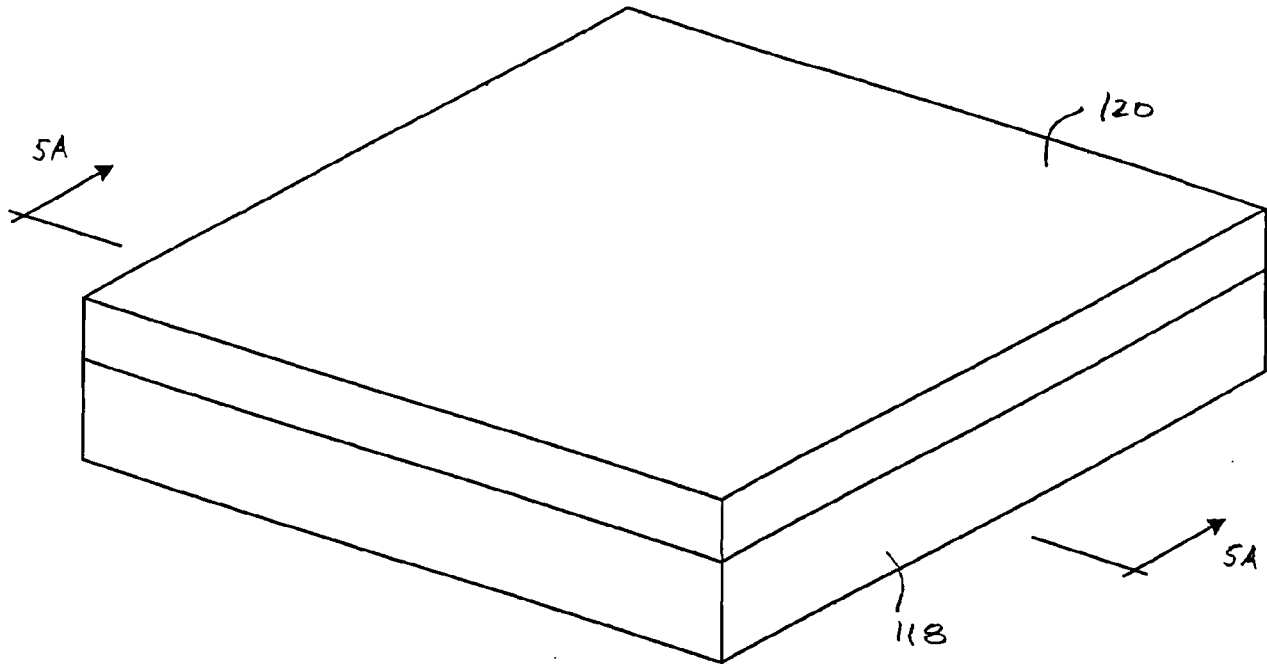


Figure. 4A

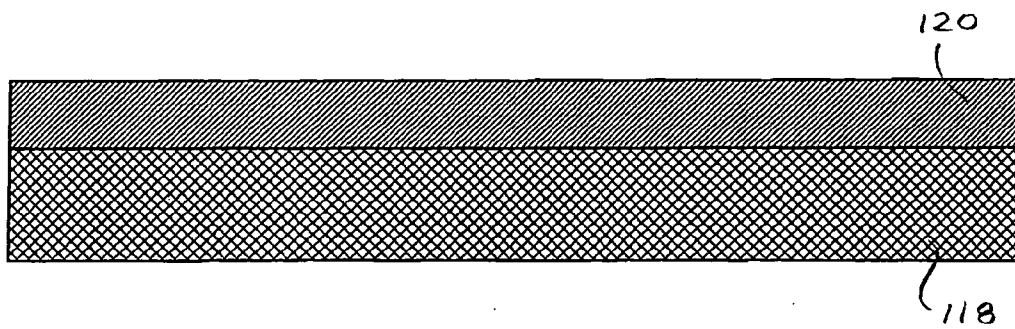


Figure. 4B

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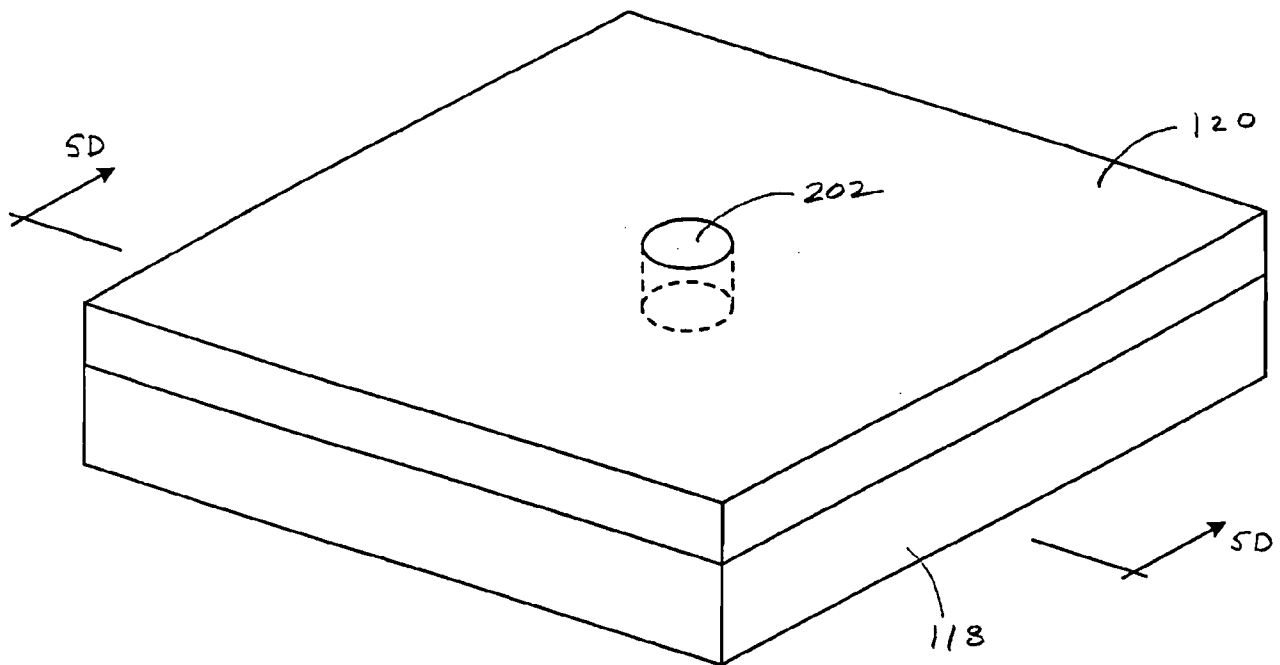


Figure 4C

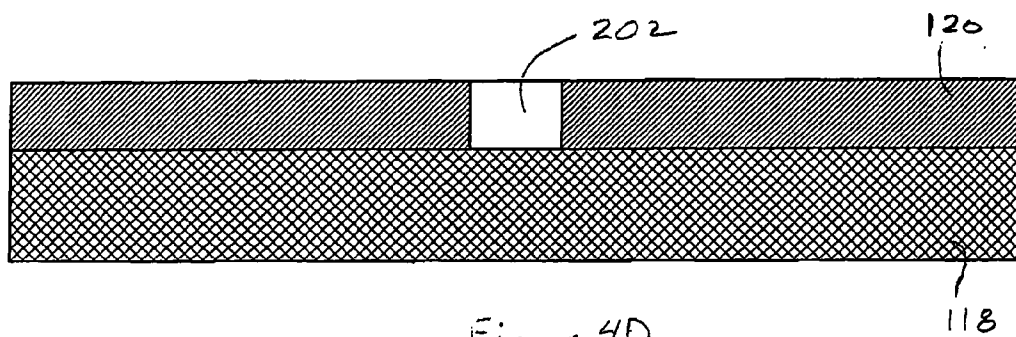


Figure 4D

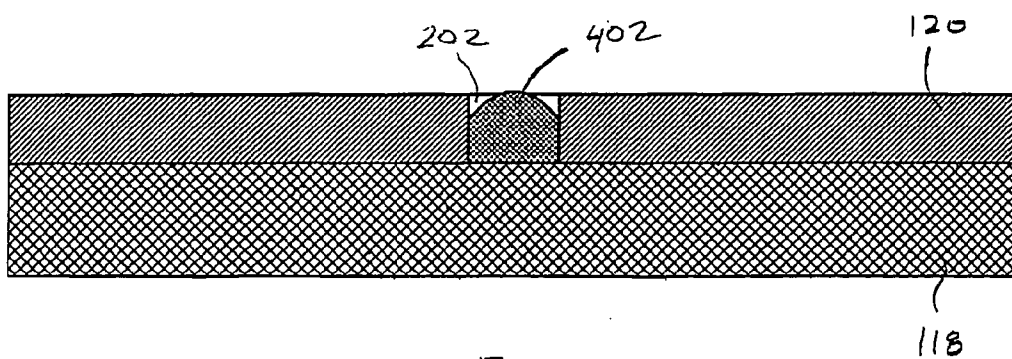
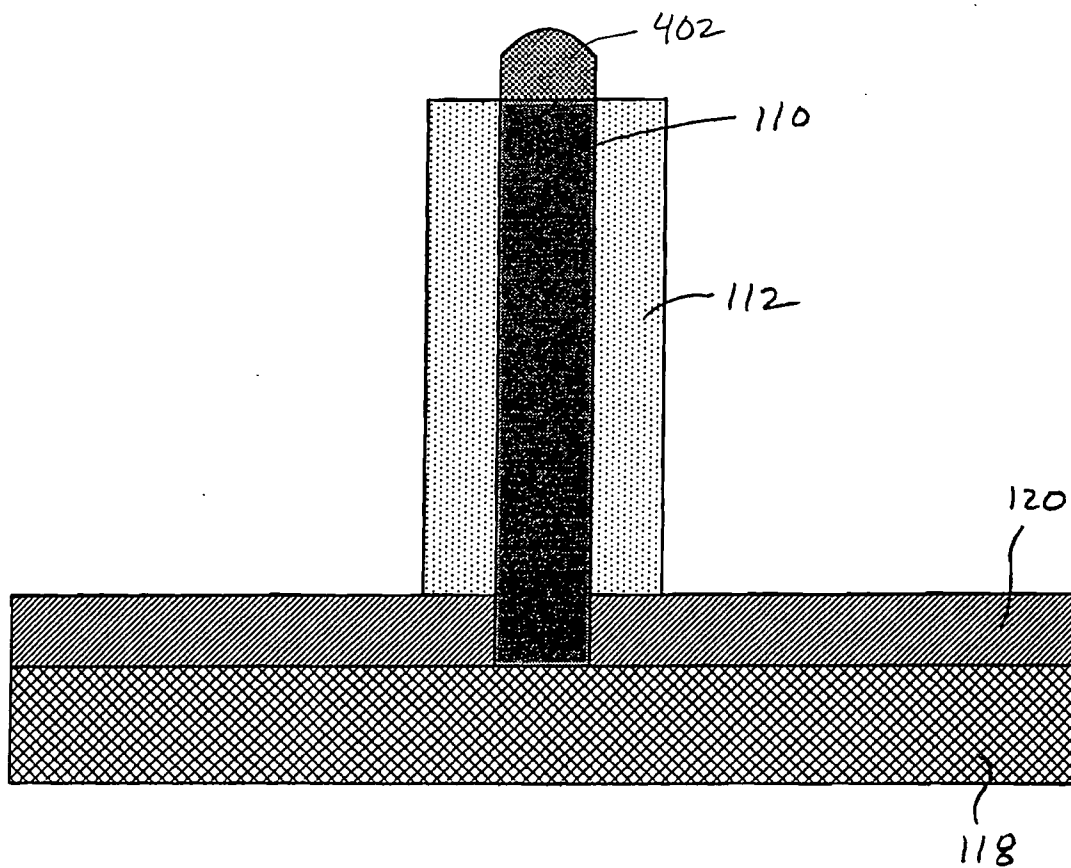
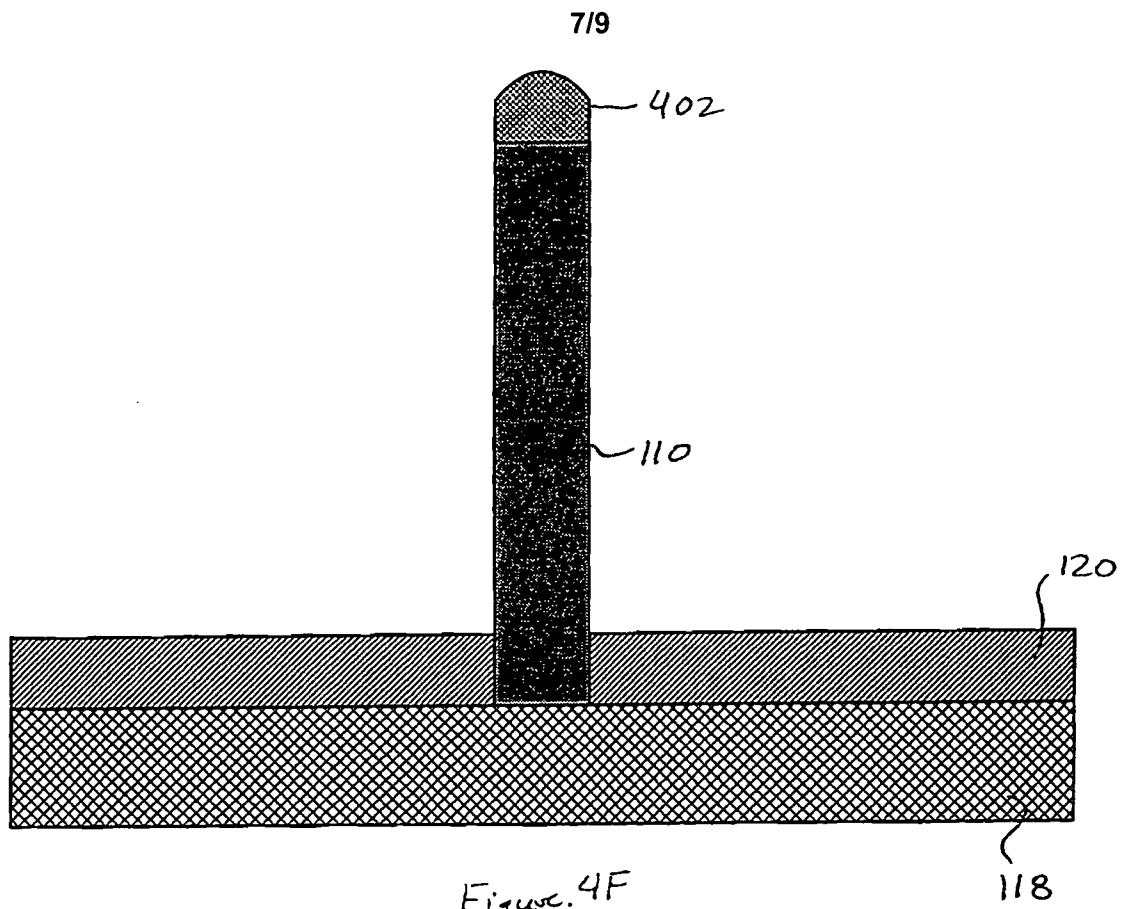


Figure 4E



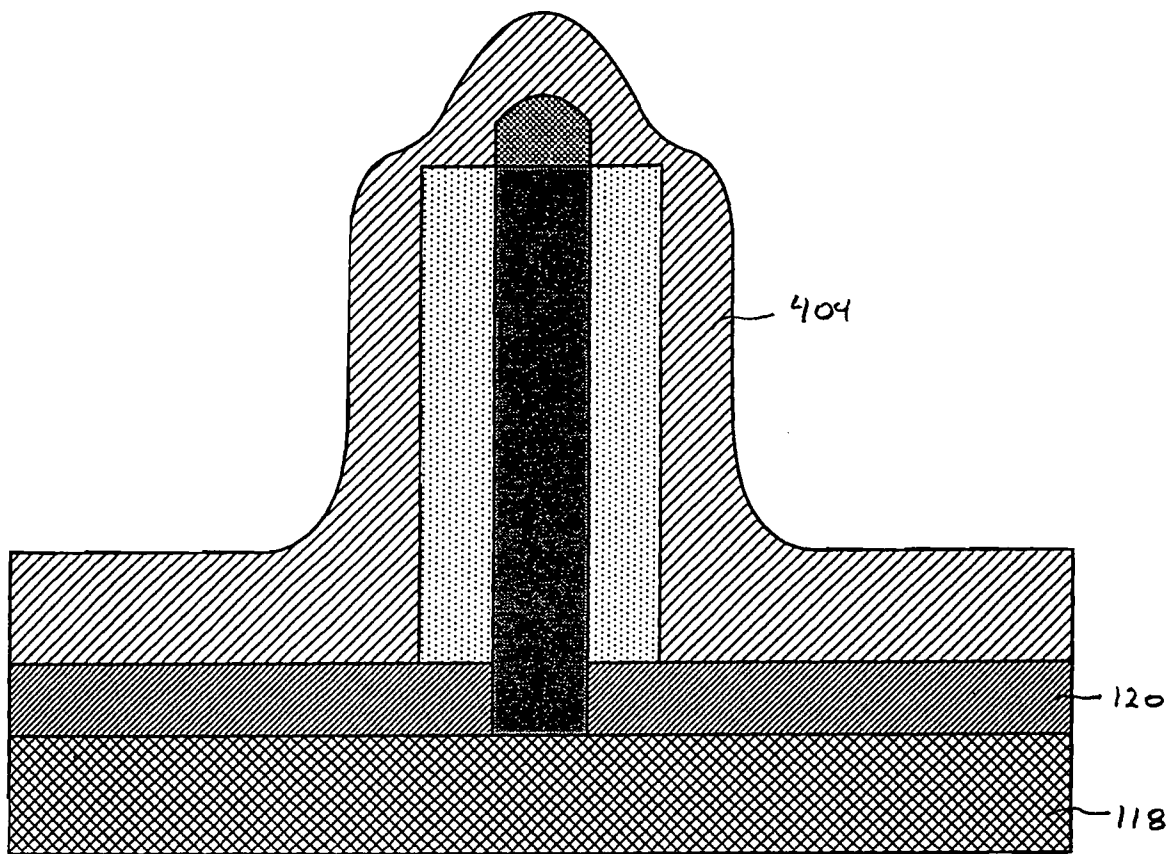


Figure 4H

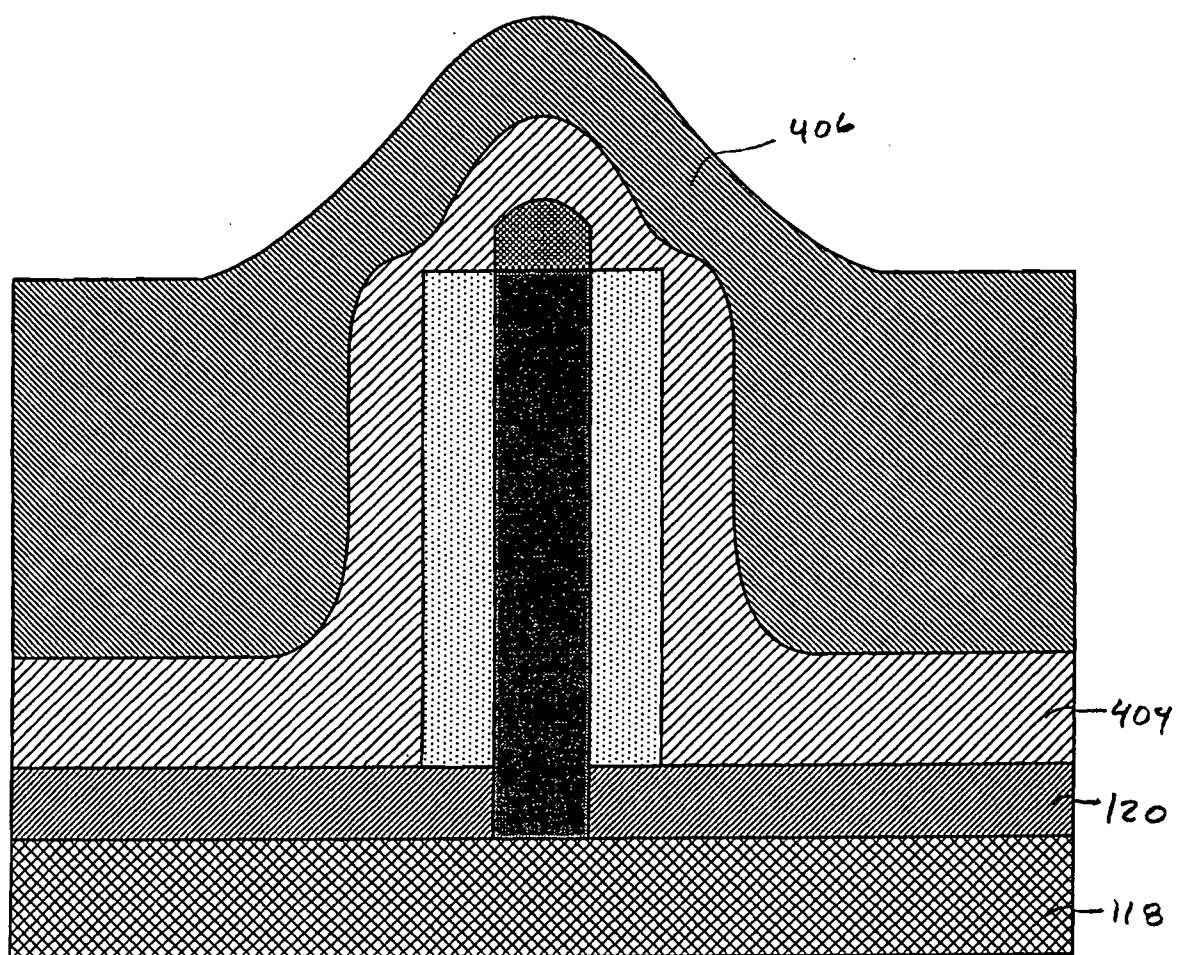


Figure 4I

A. CLASSIFICATION OF SUBJECT MATTER**G01N 21/27(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 G01N, G02B, G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) "metal", "layer", "conduct", "eimt", "voltage"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7,177,515 B2 (ESTES et al.) 13 February 2007 See Abstract, Fig. 1-2	1-7
A	US 6,034,809 A (ANEMOGIANNIS) 7 March 2000 See Abstract, Fig. 2-3	1-7
A	US 6,521,916 B2 (ROBERTS et al.) 18 February 2003 See Abstract, Fig. 3	1-7
A	US 7,244,932 B2 (NAKASUJI et al.) 17 July 2007 See Abstract, Fig. 19-20	1-7
A	JELENA VUCKOVIC et al., 'Surface Plasmon Enhanced Light-Emitting Diode', IEEE Journal of Quantum Electronics Vol.36, No.10, October 2000 See Introduction, Fig. 1	1-7
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Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 DECEMBER 2008 (26.12.2008)

Date of mailing of the international search report

26 DECEMBER 2008 (26.12.2008)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2008/008716**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 8-10
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
because they are dependant claims but are cited the claim No's which doesn't make sense'

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/008716

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