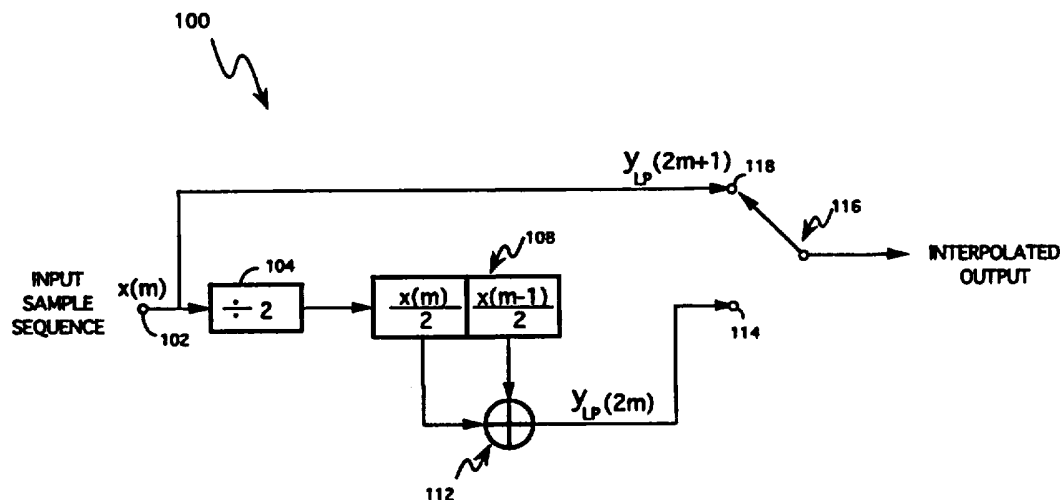




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(54) Title: ARCHITECTURE FOR EFFICIENT INTERPOLATOR



(57) Abstract

An efficient architecture for an interpolator (100) disposed to process oversampled data is disclosed herein. The interpolator (100) includes an input divider circuit (104) configured to receive an input data word over an input data line. A register (108) is provided for latching the divided input data word from the divider (104). The divided input data word is added within a summer (112) to a latched divided data word from the register, thereby forming a summed data word. A multiplexer (116) produces an interpolated output by multiplexing the summed data word with an input data word. In a preferred implementation, the register (108) is latched at a first clock rate, and the multiplexer (116) is clocked at twice the first clock rate. The efficient filter architecture allows interpolation to be performed in the absence of multipliers, and in a manner using filter coefficients equivalent to powers of two. This enables the interpolator (100) to be realized inexpensively, and renders the filter particularly suitable for implementation within integrated circuits.

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ARCHITECTURE FOR EFFICIENT INTERPOLATOR

Field of the Invention

5 This invention relates generally to the field of digital filters used for digital signal processing and communications. In particular, it pertains to a digital architecture for performing high-speed interpolation of oversampled signals without relying upon multipliers, and by using filter coefficients that are powers of two.

Background of the Invention

10 In general, the purpose of a communication system is to transmit information-bearing message signals from a source to a user destination. A communication system generally consists of three basic components: transmitter, channel, and receiver. The transmitter has the function of processing the message signal into a form suitable for transmission over the channel. This processing of the message signal is referred to as modulation.

15 In any communication system, the "channel bandwidth" defines the range of frequencies that the channel can handle for the transmission of signals with satisfactory fidelity. Channel bandwidth is important because, for a prescribed band of frequencies characterizing a message signal, the channel bandwidth determines the number of such message signals that can be multiplexed over the channel. In other words, for a prescribed
20 number of independent message signals that have to share a common channel, the channel bandwidth determines the band of frequencies that may be allotted to the transmission of each message signal without discernible distortion.

 Analog and digital transmission methods are used to transmit a message signal over a communication channel. The use of digital methods offers several operational advantages
25 over analog methods, including but not limited to: increased immunity to channel noise and interference, flexible operation of the system, and a common format for the transmission of different kinds of message signals.

 In high-speed digital transmitters, the task of creating wideband communication channels often involves producing a frequency-division multiplexed (FDM) wideband signal

from input narrowband baseband signals. For example, the input signals may comprise many voice channels with bandwidths of only a few kilohertz, which prior to transmission are combined into a wideband signal spanning many megahertz. In order to prevent aliasing of the information included within the wideband signal, it will generally be necessary that the sample rate of the voice channels be significantly increased during conversion of the narrowband signal to a wideband signal.

The process of increasing the sample rate is typically performed by "interpolating" the sampled information in one or more stages. At each stage of interpolation, a higher sample rate is achieved by effectively inserting one or more zero samples between each incoming sample of the incident lower-rate data stream. Following this zero-padding operation, the data stream is filtered in order to suppress spurious signal energy created by the zero-padding. This filtering has often been performed using finite impulse response (FIR) digital filters.

The conventional hardware implementation of an FIR digital filter utilizes delay units, multipliers, and adders. Among these filter components, multipliers often occupy a relatively large circuit area, which tends to increase the cost of the filter. Moreover, cost is often not the only significant factor of interest, and operational speed may often be of even greater significance at the high sample rates required during the later stages of interpolation. In the conventional FIR digital filter, the maximum sample rate is often determined by the speed of the multipliers. Accordingly, to improve operational speed and reduce cost, it is desirable to eliminate multipliers from FIR filters.

One such "multiplierless" FIR digital filter is described by Benvenuto et al., *Dynamic Programming Methods for Designing FIR Filters Using Coefficients -1, 0 and +1*; IEEE Transactions on Acoustics, Speech and Signal Processing, Volume ASSP-34, Number 4, August 1986. These filters are comprised of a transversal filter with tap coefficients restricted to a coefficient space of -1, 0 and +1, and cascaded with simple recursive sections. This type of filter is well-suited to high-speed (i.e., high sample rate) filtering applications since the integral tap coefficients are easily implemented in digital hardware. However, improved performance can be achieved, while maintaining ease of implementation, through a multiplierless filter characterized by a coefficient space of 2^{-n} .

Objects of the Invention

Accordingly, it is an object of the present invention to provide an efficient architecture for interpolating oversampled data.

Summary of the Invention

In summary, the present invention comprises an efficient architecture for
5 interpolating oversampled data, such as a stream of digitized voice data. The efficient interpolator includes an input divider circuit, which receives an input data word over an input data line. A register is provided for latching the divided input data word from the divider. The divided input data word is added within a summer to the previously latched data word from the register, thereby forming a summed data word. A multiplexer produces
10 an interpolated output by multiplexing the summed data word with the input data word. In a preferred implementation the register is latched at a first clock rate, and the multiplexer is clocked at twice the first clock rate.

The efficient interpolator architecture allows interpolation to be performed in the absence of multipliers, and simultaneously allows filtering to be achieved using coefficients
15 equivalent to powers of two. This enables the interpolator to be realized inexpensively, and renders the interpolator particularly suitable for implementation within integrated circuits.

Brief Description of the Drawings

Additional objects and features of the invention will be more readily apparent from
20 the following detailed description and appended claims when taken in conjunction with the drawings, in which:

FIG. 1 shows a simplified block diagrammatic representation of the architecture of an interpolator using a conventional 3-tap filter.

FIG. 2 shows a block diagram of the architecture of an interpolator of the present
25 invention.

FIG. 3 depicts a specific hardware realization of an interpolator of the present invention.

FIG. 4 is a block diagram of an interpolator network designed to interpolate by a factor of thirty two.

30 FIG. 5 is a block diagram of a specific hardware implementation of an interpolating filter which does not require an output multiplexer.

Detailed Description of the Preferred Embodiment

In order to provide appropriate context for a description of the present invention, an overview is initially provided of a conventional manner in which the sample rate of a digital sequence is increased by a factor of 2 through a zero-padding and filtering
 5 process. In particular, consider an infinite sample sequence $x(k)$, where $x(k) = \dots, x(-2), x(-1), x(0), x(1), x(2), x(3), \dots$, which may be represented in the digital frequency domain as $X(w)$, where

$$10 \quad X(w) = \sum_{k=-\infty}^{\infty} x(k)e^{-jwk}$$

Assuming the samples $x(k)$ to be of a sample rate f_s , increasing the sample rate to $2f_s$ by zero padding yields the sample sequence $y(k)$, where $y(k) = \dots, x(-2), 0, x(-1), 0, x(0), 0, x(1), 0, x(2), \dots$. That is,

$$15 \quad \begin{aligned} y(k) &= x(k/2), \text{ k even} \\ y(k) &= 0, \text{ k odd.} \end{aligned}$$

In the digital frequency domain,

$$20 \quad Y(w) = \sum_{k=-\infty}^{\infty} y(k)e^{-jwk} = \sum_{\substack{k=-\infty \\ \text{k, even}}}^{\infty} y(k)e^{-jwk}$$

$$25 \quad \begin{aligned} &= \sum_{k=-\infty}^{\infty} y(2k)e^{-j2wk} \\ &= X(2w) \end{aligned}$$

30 It is observed that $X(w)$ is periodic with a period of 2π radians, and that $Y(w)$ is periodic with a period of π radians. This results in an image of the input frequency domain response appearing within the frequency domain representation of the zero-padded output, i.e., within $Y(w)$ centered at a frequency equivalent to the sample rate of the input sequence $x(k)$. In order to eliminate the unwanted high-frequency "image" arising within $Y(w)$ due to
 35 zero padding, the sequence $y(k)$ will typically be passed through a low-pass filter having

an impulse response represented by $h(k)$. The resultant filtered sequence, $y_{LP}(k)$, may be expressed as:

$$y_{LP}(k) = \sum_{i=-\infty}^{\infty} y(i)h(k-i) = \sum_{\substack{i=-\infty \\ i \text{ even}}}^{\infty} y(i)h(k-i) = \sum_{j=-\infty}^{\infty} y(2j)h(k-2j)$$

$$y_{LP}(k) = \sum_{j=-\infty}^{\infty} x(j)h(k-2j)$$

The low-pass filter employed to obtain $y_{LP}(k)$ is typically realized using two distinct filters. A first filter, characterized by impulse response $h_e(k)$ is applied to the samples of the sequence $x(k)$; and a second filter, having an impulse response $h_o(k)$, is also utilized to filter the samples of $x(k)$. Specifically, if

$$h_e(k) = h(2k)$$

$$h_o(k) = h(2k+1),$$

then the even samples in the low-pass filtered sequence may be represented by:

$$y_{LP}(2p) = \sum_{j=-\infty}^{\infty} x(j)h(2p-2j)$$

$$= \sum_{j=-\infty}^{\infty} x(j)h(2(p-j))$$

and the odd samples in the low-pass filtered output sequence may be expressed as:

$$y_{LP}(2p+1) = \sum_{j=-\infty}^{\infty} x(j)h(2p+1-2j)$$

$$= \sum_{j=-\infty}^{\infty} x(j)h(2(p-j)+1),$$

Accordingly,

$$y_{LP}(2p) = \sum_{j=-\infty}^{\infty} x(j)h_e(p-j),$$

where $y_{LP}(2p)$ corresponds to the sequence $x(k)$ filtered by $h_e(k)$. Similarly,

$$y_{LP}(2p+1) = \sum_{j=-\infty}^{\infty} x(j)h_o(p-j),$$

which corresponds to the sequence $x(k)$ filtered by $h_o(k)$.

Turning now to FIG. 1, a simplified block diagrammatic representation is provided of the architecture of a 3-tap interpolating filter 10 designed to effect the zero padding and low-pass filtering operations described above. The interpolating filter 10 includes a switch 14, which alternately couples the even, i.e., $y_{LP}(2p)$, and odd, i.e., $y_{LP}(2p+1)$, low-pass filtered samples to the filter output. As is indicated by FIG. 1, the input sample sequence is provided to an input shift register 18, which stores consecutive input samples $x(p)$ and $x(p-1)$. Input register 18 provides the sample $x(p)$ to first and second multipliers 20 and 22, and provides the sample $x(p-1)$ to a third multiplier 24. The "even" filter coefficients $h_e(0)$ and $h_e(1)$ are stored within a first filter register 28, and are respectively provided to the multipliers 20 and 24. The "odd" filter coefficient, $h_o(0)$, is stored within a second filter register 32 connected to multiplier 22.

The scaled sample values $x(p)$ and $x(p-1)$ produced by multipliers 20 and 24 are summed within adder 36, which produces the "even" low-pass filtered output samples $y_{LP}(2p)$. The "odd" low-pass filtered output samples, $y_{LP}(2p+1)$, are produced by multiplier 22. The complete low-pass filtered output sequence is obtained by toggling the switch 14 between the outputs of adder 36 and multiplier 22.

Unfortunately, implementation of the filter architecture of FIG. 1 at a high sample rate is relatively expensive, as it is necessary to realize digital multipliers. Moreover, the large wafer area, or "real-estate" generally required by digital multipliers renders the architecture of FIG. 1 particularly disadvantageous for integrated circuit implementations.

Referring to FIG. 2, a block diagram is provided of the architecture of the interpolating filter 100 of the present invention. The interpolating filter 100 is seen to not include any digital multipliers, thereby enabling cost-effective integrated circuit

implementation. As is indicated by FIG. 2, the input sample sequence $x(m)$ impressed upon input terminal 102 is received by a divide-by-two circuit 104. The divided samples of the input sequence are sequentially latched, at the clock rate of the input sequence $x(m)$, by a register 108. Each consecutive pair of divided samples, i.e., $x(m)/2$ and $x(m-1)/2$, are combined within adder 112. The output of adder 112 forms the "even" terms of the interpolated output sequence applied to a first input terminal 114 of the multiplexing output switch 116. The sequence of even terms is denoted as $y_{LP}(2m)$, and the sequence of odd terms as $y_{LP}(2m+1)$, where $m = \dots -2, -1, 0, 1, 2, \dots$. The output multiplexing switch 116 operates to multiplex, at twice the input clock rate, the sequences of even and odd terms applied to the switch terminals 114 and 118.

The output sequence $y_{LP}(n)$ may be viewed as comprising an interpolated (by a factor of two) version of the input sequence $x(n)$. Specifically, the filtering of the sequence $y(n)$ during the interpolation process is performed in accordance with the impulse response function $h(n)$, wherein:

$$h(n) = \begin{cases} 1/2, & n = 0 \\ 1, & n = 1 \\ 1/2, & n = 2 \\ 0, & \text{else} \end{cases}$$

Alternately, $h(n)$ may be expressed as:

$$h(n) = \begin{cases} h_e(n/2), & \text{for even values of } n, \\ h_o([n-1]/2), & \text{for odd values of } n, \end{cases}$$

where even and odd samples of the input sequence $x(n)$ are processed by a filter having an impulse response specified by $h_e(n)$ and $h_o(n)$, respectively. Recall $h_e(n) = h(2n)$ and $h_o(n) = h(2n+1)$, so:

$$h_e(n) = \begin{cases} 1/2, & n = 0 \\ 1/2, & n = 1 \\ 0, & \text{else,} \end{cases}$$

and,

$$h_o(n) = \begin{cases} 1, & n = 0 \\ 0, & \text{else} \end{cases}$$

The filtering of $x(n)$ in accordance with the impulse response $h_e(n)$, yields a filtered output sequence $y_{LP}(2m)$:

$$\begin{aligned}
 y_{LP}(2m) &= \sum_{j=-\infty}^{\infty} x(j)h_e(m-j) = x(m)h_e(0) + x(m-1)h_e(1) \\
 &= [1/2] \cdot x(m) + [1/2] \cdot x(m-1) \\
 &= [1/2] \cdot [x(m) + x(m-1)]
 \end{aligned}$$

5

wherein "•" denotes multiplication. Similarly, the output samples of the output sequence $y_{LP}(2m+1)$ may be expressed as:

$$\begin{aligned}
 y_{LP}(2m+1) &= \sum_{j=-\infty}^{\infty} x(j)h_o(m-j) = x(m)h_o(0) = x(m)1 \\
 &= x(m)
 \end{aligned}$$

10

That is, the "odd" samples within the output sequence $y_{LP}(m)$, i.e., $y_{LP}(2m+1)$, correspond to the input sequence. This correspondence is seen to be manifested within the filter architecture of FIG. 2, since the switch terminal 118 is directly connected to the input terminal 102. Similarly, direct correspondence is also seen to exist between this expression for $y_{LP}(2m)$ and the architecture of the filter 100. Namely, the divide-by-two circuit 104 introduces the factor of (1/2) and the register 108 is used to provide the samples $[1/2] \cdot x(m)$ and $[1/2] \cdot x(m-1)$, the adder 112 performs the required addition operation.

15

Turning now to FIG. 3, there is shown a specific hardware realization of an interpolating filter 200 of the present invention. In the embodiment of FIG. 3, the filter 200 processes the 14-bit samples comprising the input sequence $x(n)$. The thirteen most significant bits (MSBs) of each 14-bit input sample are simultaneously clocked, at the input sample rate f_s , into a 13-bit register 204. Since each 14-bit input sample corresponds to a binary number, the extraction of the thirteen MSBs from each sample effectively results in division by two. The 13-bit register 204 will generally be comprised of a set of thirteen D-type flip-flops, each of which latches one of the thirteen MSBs of each input sample. The thirteen MSBs of each pair of consecutive samples are added within 13-bit adder 208, and the 14-bit result provided to an output multiplexer 212. The multiplexer 212 operates to produce the output sequence $y_{LP}(m)$ by multiplexing, at the output sample rate of twice f_s , the sequence of 14-bit values from the adder 208 with the 14-bit input sequence $x(n)$. In a preferred implementation, the "even" output sample component associated with a given input sample is output by the filter 200 before the corresponding "odd" sample component.

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The filter 200 is seen to be capable of being realized very efficiently, in that it requires only a register comprised of 13 flip-flops, a 14-bit adder, and a multiplexer. Using terminology familiar to those skilled in the art, the filter 200 may be described as functioning as a 3-tap finite impulse response (FIR) half-band filter having coefficients
5 of $1/2$, 1 , $1/2$.

Turning now to FIG. 4, there is shown an interpolating filter network 300 designed to interpolate by a factor of thirty-two. The filter network 300 is comprised of a set of five serially-connected interpolation-by-two filters of the present invention (see, e.g., FIG. 3). The filter network 300 may be included within, for example, a digital transmitter
10 disposed to convert multiple low data rate, oversampled, narrowband input sequences into a high data rate, wideband output sequence. For example, in a specific embodiment input data having a baseband bandwidth of approximately 14 kHz is applied at a rate of 960 Ksps to the network 300. The oversampled characteristic of the input data (i.e., high sampling rate relative to the Nyquist rate) allows each interpolation-by-two stage to be
15 realized using the half-band architecture of FIG. 3. In this exemplary application each interpolation-by-two stage provides a low-pass filtering function characterized by a -3 dB frequency of approximately 14 kHz, passband ripple of less than approximately 0.25 dB, and image rejection on the order of 67dB.

Referring to FIG. 5, a block diagram is provided of an alternate realization of an
20 interpolating filter 400 of the present invention. In the embodiment of FIG. 5, the filter 400 processes the 14-bit samples comprising the input sequence $x(n)$ of sample rate f_s . The bits of each 14-bit input sample are simultaneously clocked, at a rate of $2f_s$, into a 14-bit register 404. The 14-bit register 404 will generally be comprised of a set of fourteen D-type flip-flops, each of which latches one of the bits of each input sample. The fourteen
25 bits of each pair of consecutive samples are added within 14-bit adder 408, and the 14 MSBs from the result of each addition comprise the output of the filter 400. In particular, the output of the filter 400 may be represented as:

$$\dots x(n), 1/2[x(n) + x(n-1)], x(n-1), 1/2[x(n-1) + x(n-2)], x(n-2), \dots$$

The filter 400 may be described as functioning as a 3-tap finite impulse response (FIR)
30 half-band filter having coefficients of $1/2$, 1 , $1/2$, which is disposed to operate upon a zero-padded sample sequence (i.e., one "padding" zero per sample).

While the present invention has been described with reference to a few specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. An interpolator comprising:
 - means for receiving an input data word, and for dividing said input data word by
 - 5 removing one or more bits from said input data word;
 - a register for latching said divided input data word;
 - a summer for summing said divided input data word with a latched data word from said register to thereby form a summed data word; and
 - a multiplexer for producing an interpolated output by multiplexing said input data
 - 10 word with said summed data word.
2. The interpolator of claim 1 wherein said input data word includes N data bits, said divided input data word being comprised of N-1 most significant bits of said input data word.
- 15 3. The interpolator of claim 2 wherein said register comprises an N-1 bit parallel data register.
4. The interpolator of claim 1 wherein said register is latched at a first clock rate and
- 20 said multiplexer is clocked at twice said first clock rate.
5. An interpolator comprising:
 - a divider for dividing each data word within a sequence of input data words;
 - a register for latching each of said divided input data words received from said
 - 25 divider;
 - a summer having first and second input data ports respectively connected to an output of said divider and to an output of said register, said summer producing a sequence of summed data words; and
 - a multiplexer for multiplexing each of said input data words with one of said
 - 30 summed data words.

6. The interpolator of claim 5 wherein said register is latched at a first clock rate and said multiplexer is clocked at a second clock rate approximately twice said first clock rate, said multiplexer producing an interpolated output at twice said first clock rate.
- 5 7. The interpolator of claim 5 wherein each of said input data words includes N bits, said divider forming each of said divided data words by extracting the N-1 least significant bits from a corresponding one of said input data words.
8. A method for interpolating a sequence of input data words comprising the steps of:
- 10 dividing each of said input data words;
 delaying each of said divided input data words;
 summing each of said divided input data words with a delayed one of said divided input data words to thereby produce a sequence of summed data words; and
 multiplexing each of said input data words with one of said summed data words.
- 15 9. The method of claim 8 wherein said step of delaying each of said input data words includes the step of latching each of said input data words at a first clock rate.
10. The method of claim 9 wherein said step of multiplexing is performed at a second
- 20 clock rate equal to twice said first clock rate.
11. The interpolator of claim 2 wherein said register comprises an N-1 bit parallel register and said summer comprises an N-bit adder with input sign extension.
- 25 12. An interpolator comprising:
- an N-bit input data line upon which is impressed an N-bit input data word;
 an N-1 bit register connected to most significant N-1 bit lines of said input data line;
- a summer having a first input port connected to said N-1 bit lines of said input data
- 30 line and having a second input port connected to an N-1 bit output data line of said N-1 bit register, said summer producing an N-bit result; and

a multiplexer having an input connected to said N-bit input data line and an input for receiving said N-bit result from said summer, said multiplexer impressing an N-bit output data word upon an N-bit output line.

- 5 13. The interpolator of claim 12 wherein said N-1 bit register is latched at a first clock rate and said multiplexer is clocked at a second clock rate twice said first clock rate.

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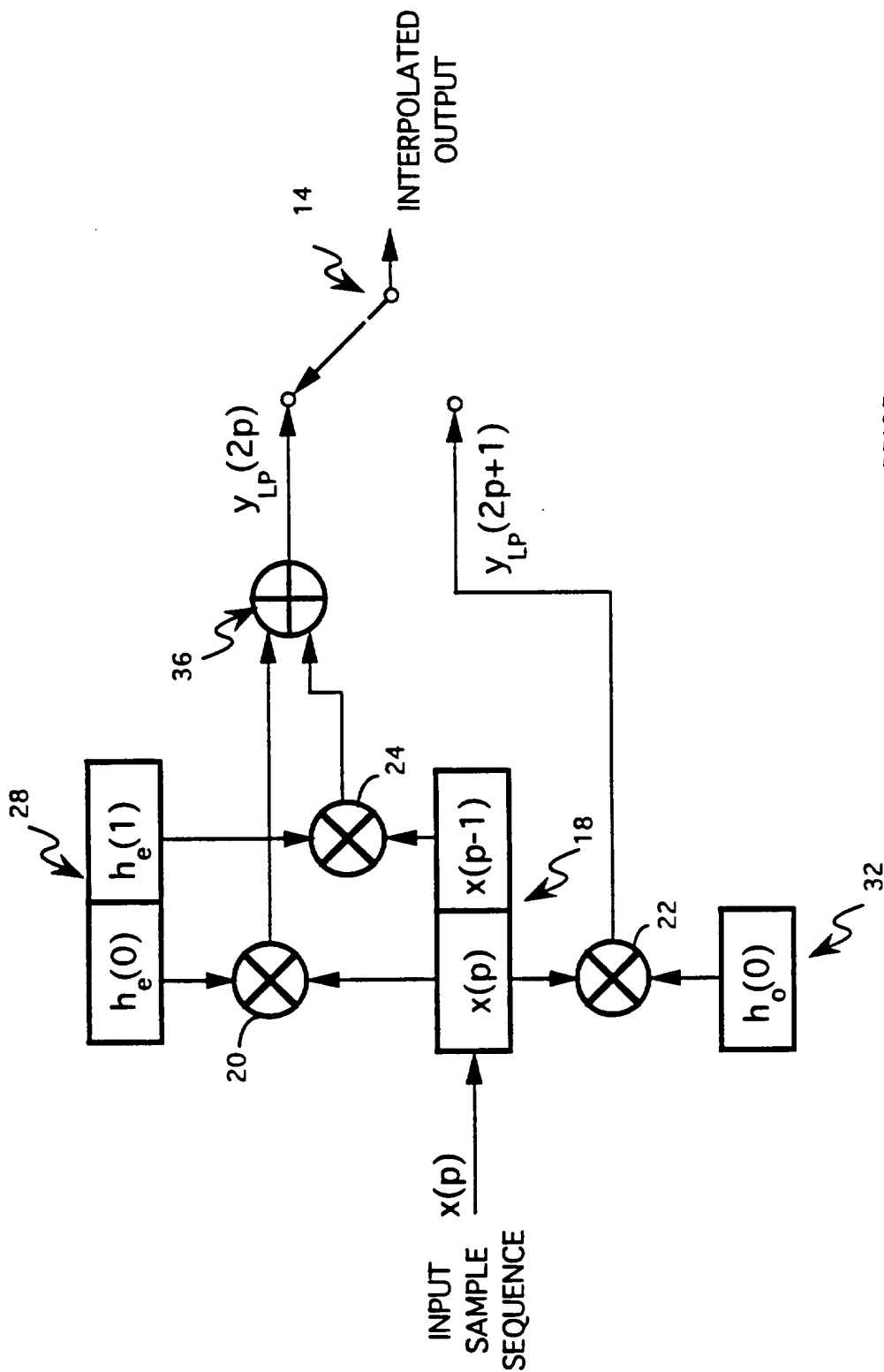


FIG. 1

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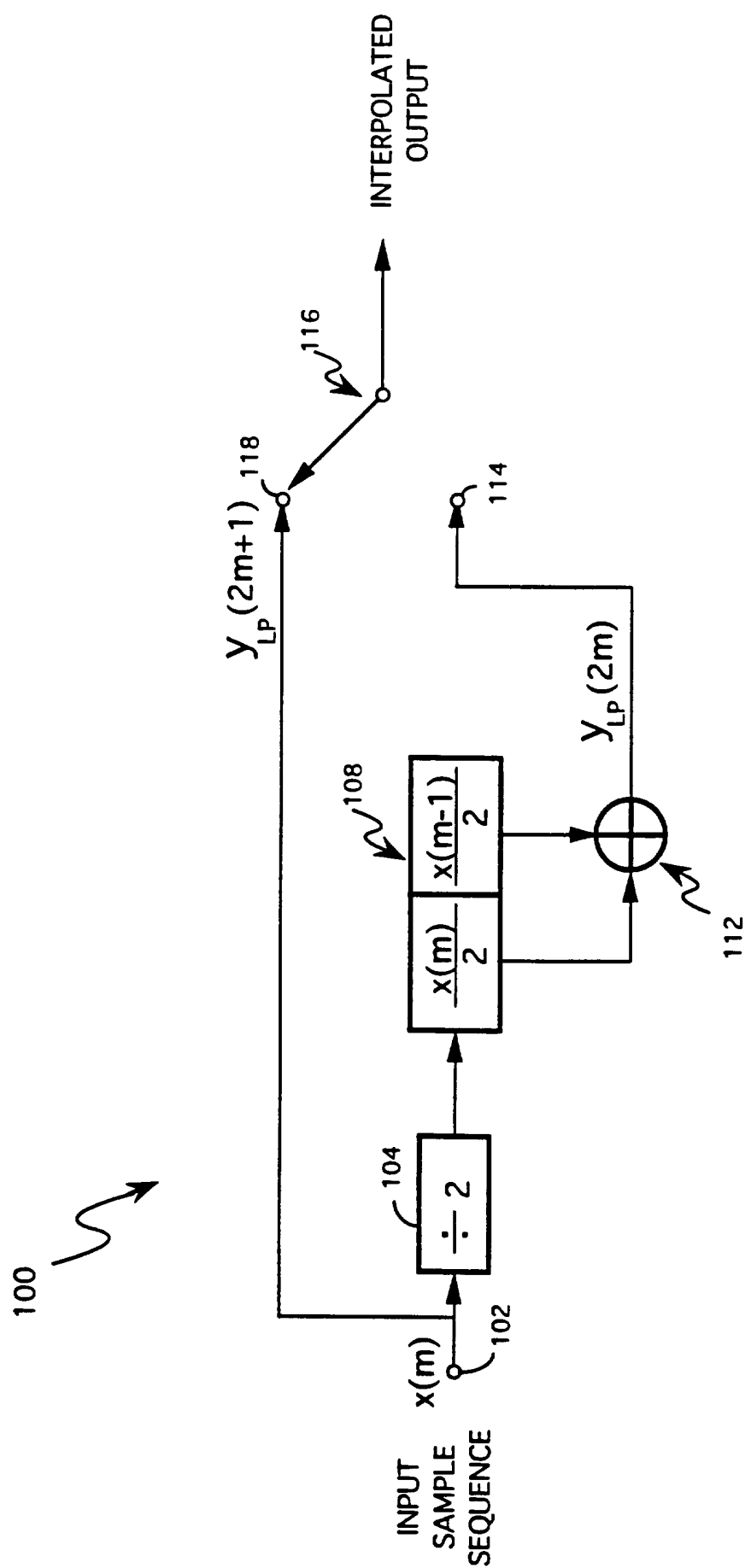


FIG. 2

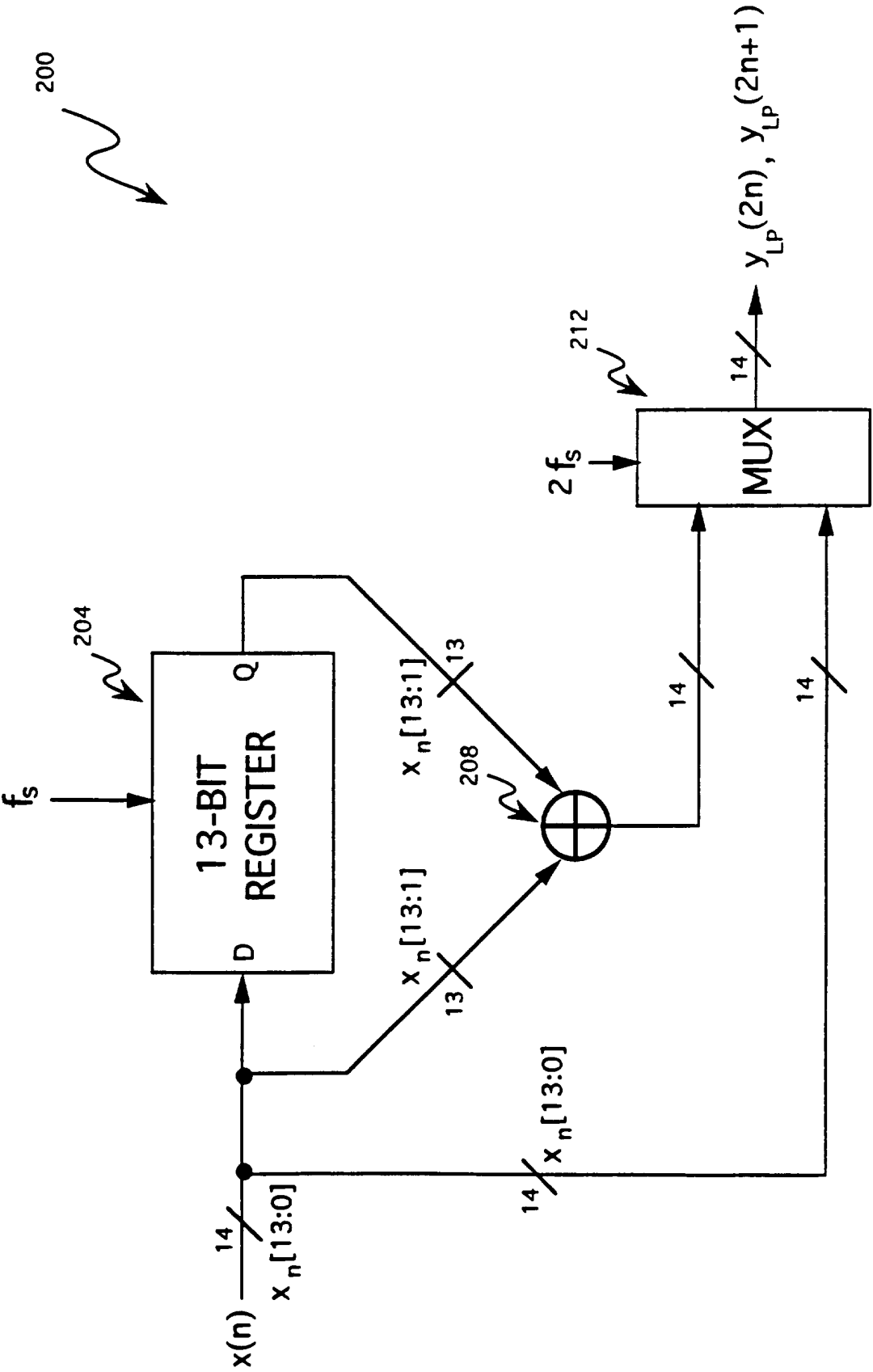
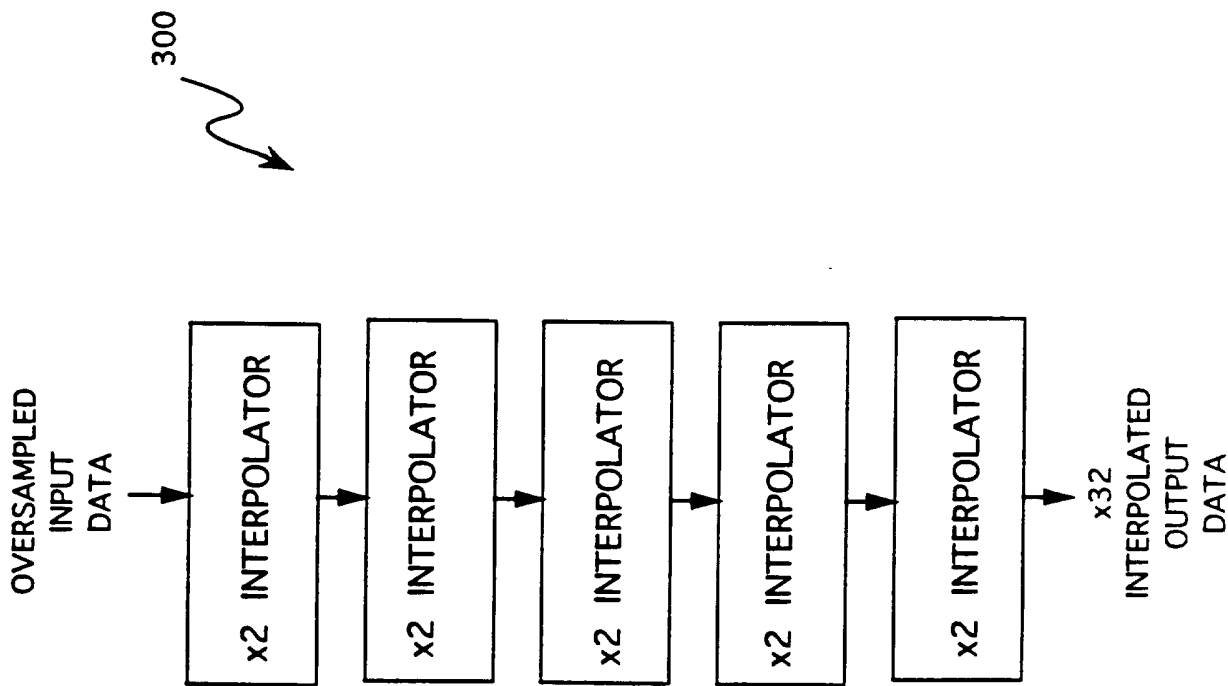


FIG. 3

FIG. 4



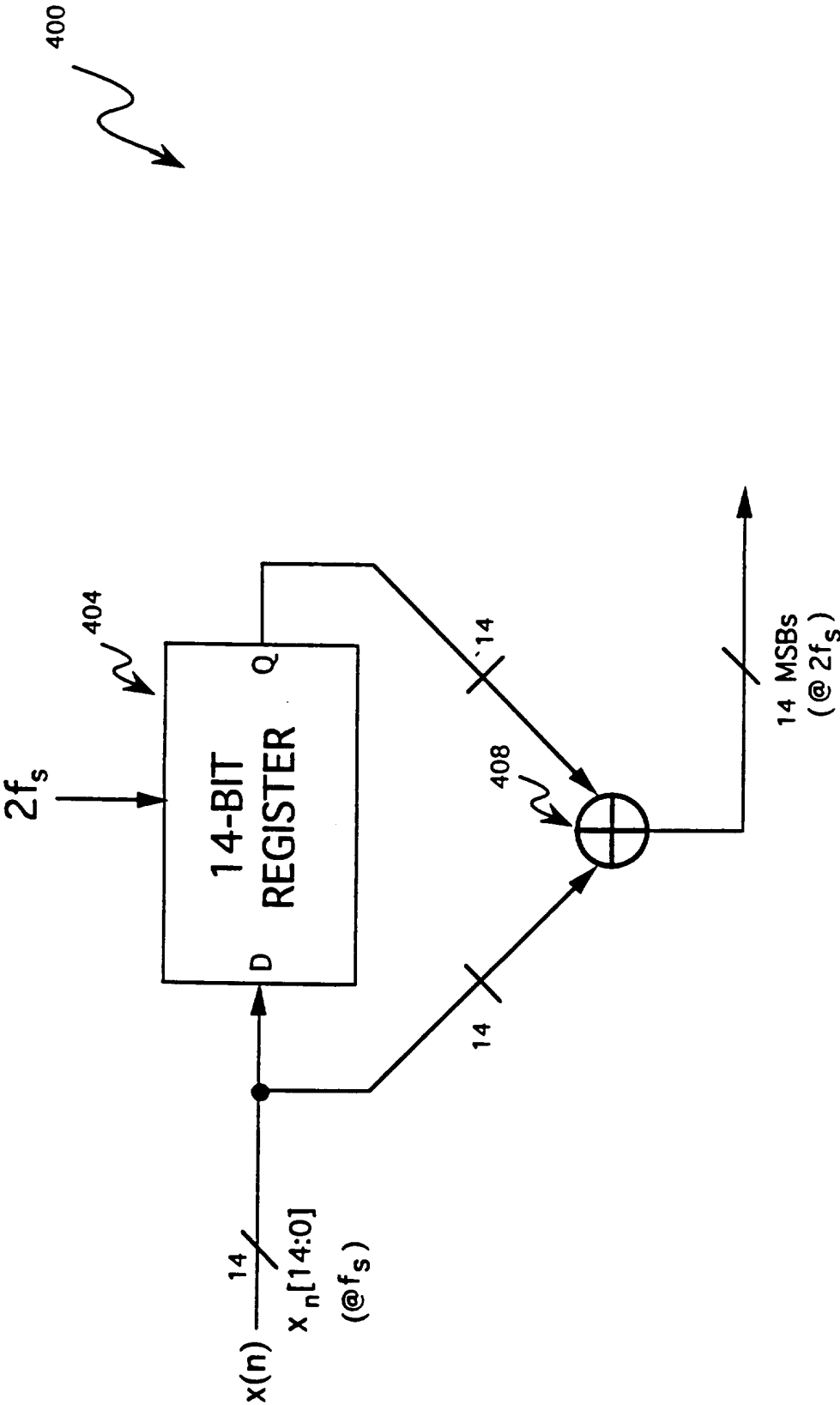


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US96/00747

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G06F 17/17

US CL : 364/724.1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 364/723, 724.1, 724.13, 724.16, 724.17, 724.19, 724.2; 348/441, 443

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS (sum? or add?) and (multiplex? or select? or switch?) and divid? and interpolat?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,473,381 (Lee) 05 December 1995, Fig. 2 and column 6, lines 7-30.	1-13
Y,P	US, A, 5,390,674 (Robinson et al.) 21 February 1995, Fig. 4 and column 3, lines 54-61.	1-13
A	US, A, 5,369,606 (Hessel) 29 November 1994, column 6, lines 1-13.	4, 6, 10, 13
A	US, A, 4,101,964 (Betts) 18 July 1978, column 1, line 68 - column 2, line 15.	1-13



Further documents are listed in the continuation of Box C.



See patent family annex.

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