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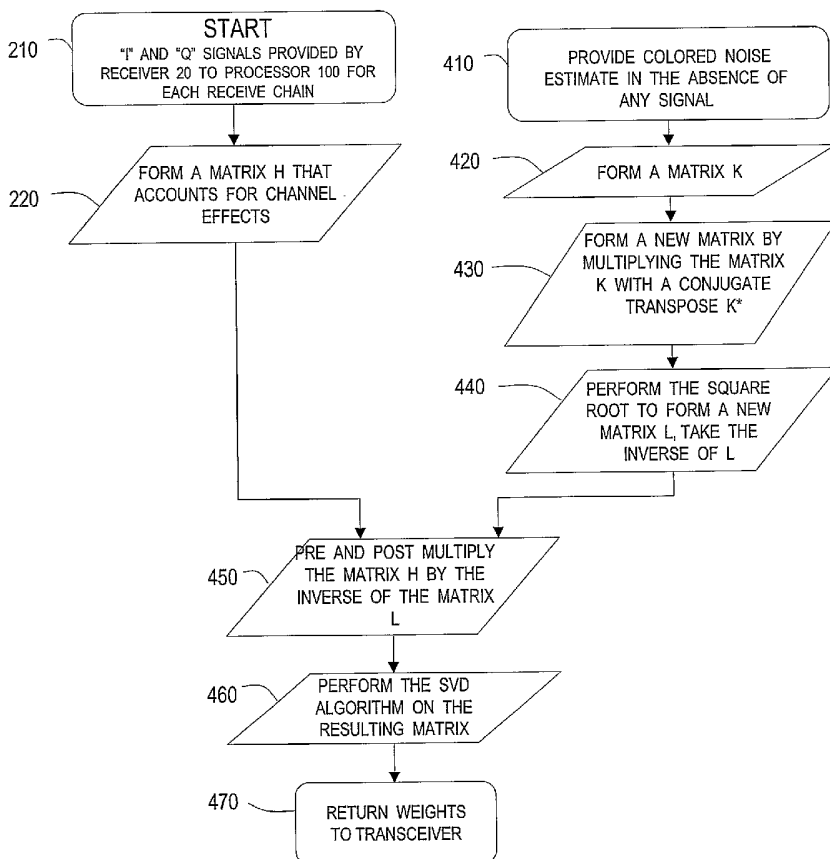
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- (71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).
- (72) Inventors: **HO, Minnie**; 405 Becker Lane, Los Altos, CA 94022 (US). **SANDU, Sumeet**; 25 Rio Robles East, #408, San Jose, CA 95134 (US).
- (74) Agents: **MALLIE, Michael, J.** et al.; Blakely Sokoloff Taylor & Zafman LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).
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[Continued on next page]

(54) Title: BEAM-FORMER AND COMBINER FOR A MULTIPLE-ANTENNA SYSTEM



(57) Abstract: A compensating correction value for adjusting analog signals received from multiple antenna elements takes into account the effects of colored noise, co-channel interference, and inter-sample interference. The method of generating the compensating correction value for analog combining architectures considers the total channel impulse response over a block of time.

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ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

BEAM-FORMER AND COMBINER FOR A MULTIPLE-ANTENNA SYSTEM

Some wireless systems use a single antenna for transmission and reception while some products incorporate multiple antennas, but use the multiple antennas in a very simple way. For instance, some smart-antenna systems incorporate selection diversity, where a switch chooses one of two antennas based on which antenna has a higher received signal power.

For smart-antenna systems there is a continuing need for better ways to control multiple antenna.

10

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

20 FIG. 1 illustrates features of the present invention for controlling the gain and phase of signals in a receive chain that may be incorporated into a wireless communications device;

FIG. 2 illustrates a flow diagram for an embodiment that generates a channel matrix H in accordance with the present invention;

25 FIG. 3 illustrates a flow diagram for an embodiment that includes an averaging step after the formation of the channel matrix H in accordance with the present invention;

FIG. 4 illustrates a flow diagram for an embodiment that accounts for colored noise in accordance with the present invention;

30 FIG. 5 illustrates a flow diagram for an embodiment that reduces co-channel interference in accordance with the present invention; and

FIG. 6 illustrates a flow diagram for an embodiment using Spatial Division Multiple Access (SDMA) that incorporates analog combining in accordance with the present invention.

5 It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate
10 corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set
15 forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

20 In the following description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each
25 other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

FIG. 1 illustrates features of the present invention that may be
30 incorporated into a wireless communications device 10. The transceiver receives and transmits modulated signals from multiple antenna. In a receiver

12, a first receiver chain includes a Low Noise Amplifier (LNA) and Variable Gain Amplifier (VGA) 16 to amplify the received signal from antenna 14 followed by a phase shifter 18. A Digital-To-Analog Converter (DAC) 20 is connected to LNA 16 and phase shifter 18 to adjust the gain and the phase of the received modulated signal. A mixer circuit 32 receives the modulated signals in the first receiver chain and translates the carrier frequency of the modulated signal, down-converting the frequency of the modulated signal in the receiver. The down-converted signal may be filtered through a filter 34 and converted to a digital representation by an Analog-To-Digital Converter (ADC) 36.

Receiver 12 may further include a second receiver chain to receive a signal from antenna 24 that includes a LNA and VGA 26, followed by a phase shifter 28. A DAC 30 is connected to LNA 26 and phase shifter 28 to adjust the gain and the phase of the modulated signal received in the second receiver chain. A mixer circuit 32 receives the modulated signals in the second receiver chain and down-converts the frequency of the modulated signal. The down-converted signal may be filtered through a filter 38 and converted to a digital representation by an ADC 40.

A baseband and application processor 68 is connected to ADCs 36 and 40 to provide, in general, the digital processing of the received data within communications device 10. Note that wireless communications device 10 may operate in a variety of channel conditions where the signals received at the antenna may be corrupted by multiple propagation paths. For instance, pedestrian or vehicular motion induces Doppler frequency shifts on multi-path components, resulting in a time variation of the faded multi-path channel. Thus, a wireless receiver may see multiple signals arriving at the same time, where the signals have been reflected off surfaces and not received in a direct path from the transmitter.

Processor 68 may process the digitized quadrature signals, i.e., the in-phase "I" signal and the quadrature "Q" signal from the first receiver chain, to provide the control signals to DAC 20 to mitigate the effects of channel multi-

path in accordance with features of the present invention. Likewise, the digitized quadrature signals from the second receiver chain are processed to provide the control signals to DAC 30 to mitigate the effects of channel multi-path in that channel.

5 Note that cellular communications systems may also receive signals having interference between adjacent pulses of a transmitted code. The distortion may be manifested in the temporal spreading and consequent overlap of individual pulses causing the receiver difficulty in reliably distinguishing between individual signal elements. Processor 68 may process
10 the digitized quadrature signals from the first and second receiver chains to mitigate the effects of Inter-Symbol Interference (ISI) in accordance with features of the present invention.

The transceiver also includes a transmitter 72 where digital data received from processor 68 may be converted to an analog signal by a Digital-
15 to-Analog Converter (DAC) 64. In a first transmitter path, the analog signal may be modulated by a frequency upconverter 60, with the phase and gain of the modulated signal adjusted by a phase shifter 44 and Variable Gain – Power Amplifier (VGA-PA) 42. A DAC 48 uses control signals from processor
20 68 to set a phase and signal strength that are appropriate for the modulated signal transmitted from antenna 14. In a second transmitter path, the analog signal may be modulated by a frequency upconverter 62, with the phase and gain of the modulated signal adjusted by a phase shifter 54 and VGA-PA 52. Likewise, a DAC 58 uses control signals from processor 68 to set a phase
25 and signal strength that are appropriate for the modulated signal transmitted from antenna 24.

Receiver 12 and transmitter 72 may be embedded with processor 68 as a mixed-mode integrated circuit, or alternatively, the transceiver may be a stand-alone Radio Frequency (RF) integrated circuit. Accordingly, embodiments of the present invention may be used in a variety of
30 applications, with the claimed subject matter incorporated into microcontrollers, general-purpose microprocessors, Digital Signal Processors

(DSPs), Reduced Instruction-Set Computing (RISC), Complex Instruction-Set Computing (CISC), among other electronic components. In particular, the present invention may be used in smart phones, communicators and Personal Digital Assistants (PDAs), medical or biotech equipment, automotive safety and protective equipment, and automotive infotainment products. However, it should be understood that the scope of the present invention is not limited to these examples.

Further, the principles of the present invention may be practiced in wireless devices that are connected in a Code Division Multiple Access (CDMA) cellular network and distributed within an area for providing cell coverage for wireless communication. Additionally, the principles of the present invention may be practiced in Wireless Local Area Network (WLAN), Wide Area Network (WAN), Personal Area Network (PAN) and Local Area Network (LAN), among others.

A memory device 70 may be connected to processor 68 to store data and/or instructions. In some embodiments, memory device 70 may be volatile memories such as, for example, a Static Random Access Memory (SRAM), a Dynamic Random Access Memory (DRAM) or a Synchronous Dynamic Random Access Memory (SDRAM), although the scope of the claimed subject matter is not limited in this respect. In alternate embodiments, the memory devices may be nonvolatile memories such as, for example, an Electrically Programmable Read-Only Memory (EPROM), an Electrically Erasable and Programmable Read Only Memory (EEPROM), a flash memory (NAND or NOR type, including multiple bits per cell), a Ferroelectric Random Access Memory (FRAM), a Polymer Ferroelectric Random Access Memory (PFRAM), a Magnetic Random Access Memory (MRAM), an Ovonic Unified Memory (OUM), a disk memory such as, for example, an electromechanical hard disk, an optical disk, a magnetic disk, or any other device capable of storing instructions and/or data. However, it should be understood that the scope of the present invention is not limited to these examples.

FIGs. 2-6 illustrate flow diagrams for different methods used in computing weights for a multiple-antenna system in accordance with the present invention. The weights may also be referred to as antenna weights and affect the signal gain and signal phase in the receiver chains connected to the various antenna. The weights may be digitally computed by processor 68 for the linear combiner in receiver 12 and the beam-former in transmitter 72. These weights take into account the time-domain signal and the entire channel impulse response and are used by wireless communications device 10 to improve the ratio of average signal power to average noise power. Accordingly, phase shifting and gain amplification may be performed on the multiple receive signals prior to combining, with the weights for the linear combiner supplied to DACs 20 and 30. Additionally, phase shifting and gain amplification may be performed on the multiple transmit signals prior to transmission, with the weights for the beam-former supplied to DACs 48 and 58. Note that the weight precision may be controlled by the number of DAC bits.

Channel estimation may be performed in wireless communications device 10 by averaging over a series of known training or preamble sequences. Known symbols may be sent to receiver 12 to derive a compensating correction value that may be applied to the receiver chain that corresponds to each antenna element. Note that the channel impulse response may be estimated either in the time-domain or in the frequency-domain, where the choice of domain depends on the wireless system being enhanced. By taking into account time-domain transmit or receive signals when computing the weights, these weights may be applied to time-domain, analog signals. In this way, these operations may be performed with analog components and reduce the silicon hardware costs.

Referring specifically to FIG. 2, the effects of the channel on the signals received by antenna 14 and 24 may be estimated, with the digitized quadrature signals supplied to processor 68 for each receive chain (Process 210). The channel matrix is then formed (Process 220), where the rows of

the channel matrix H are simply the channel estimates. The length of the channel estimates may be chosen to be the same for all antenna elements, although this is not a limitation of the present invention. Once the channel matrix has been formed, a new matrix H may be computed (Process 230) by
5 multiplying the matrix H with its conjugate transpose H^* , this mathematical operation being denoted as $H = HH^*$. The Singular Value Decomposition (SVD) algorithm may then be performed on this matrix (Process 240), and the eigenvector corresponding to the maximum singular vector may be computed (Process 250). These weights may be shown to be optimal in terms of
10 maximizing the signal-to-noise power ratio for multiple analog signals. These weights computed by processor 68 may be transferred to receiver 12 and used to control DACs 20 and 30 (Process 260).

The transmit beam-former weights used in transmitter 72 may be computed in the same fashion. In fact, the channel matrix may be the same
15 in both the transmit and receive directions, and in this case, the same weights may be applied at both transmitter 72 and receiver 12. These weights may be used to control DACs 48 and 58 in transmitter 72 to improve the signal-to-noise power ratio at the receiver.

Referring to FIG. 3, the channel associated with each of the multiple-
20 antenna may be estimated and a compensating correction value derived. The digitized quadrature signals for each receive chain may be supplied by receiver 12 to processor 68 (Process 310). The weights may be computed in an average sense by adding an averaging step after the formation of the matrix H (Process 320). In this embodiment, the matrix H may be averaged over a
25 number of channels to obtain a new average matrix " H_a " (Process 330). This channel covariance matrix H_a may then used for SVD computation (Process 340) and weight extraction (Process 350). These weights computed by processor 68 may be transferred to receiver 12 and used to control DACs 20 and 30 (Process 360). This scheme may be used when the exact channel is
30 not known but the channel covariance is known.

Referring to FIG. 4, the weights to compensate for the channel may be computed in the presence of colored noise by adding a chain of steps, where the colored noise is estimated in the absence of any signal (Process 410). A noise matrix K may be formed (Process 420), and a new matrix may be
5 computed by multiplying the matrix K with a conjugate transpose K^* (Process 430). The square root of the new matrix may then be computed and denoted by the matrix L , with the inverse of matrix L then computed (Process 440). In the original sequence of steps (Process 210, 220), a step may be added after the formation of the matrix H , where the matrix H is pre and post-
10 multiplied by the inverse of the matrix L (Process 450). The weights may then be computed using the SVD algorithm (Process 460), just as in the non-colored noise case. These weights computed by processor 68 may be transferred to receiver 12 and used to control DACs 20 and 30 (Process 470).

15 Referring to FIG. 5, the weights used to control DACs 20 and 30 may be computed to reduce the presence of *co-channel interference and/or co-channel users*. The interference plus noise is estimated in the absence of any signal (Process 510) and a noise plus interference matrix O is formed that accounts for the noise and interference (Process 520). Many similarities exist
20 between FIGs. 4 and 5. However, this matrix reduces to a special case of colored noise where the interference plus noise is treated as colored noise. Note that the SVD algorithm is not needed and that sub-optimal iterative algorithms, such as the iterative power method that only compute the optimal eigenvector may be used to reduce digital complexity and computation time
25 (Process 560). Note that the SVD algorithm may be replaced using matrix inverses. These weights computed by processor 68 may be transferred to receiver 12 and used to control DACs 20 and 30 (Process 570).

FIG. 6 illustrates a flow diagram for an embodiment using Spatial
30 Division Multiple Access (SDMA) that incorporates analog combining in accordance with the present invention. SDMA is a communications mode that optimizes the use of radio spectrum and uses directional properties of

antennas. In SDMA, also known as Spatial-Division Multiplex (SDM), highly directional antennas transmit signals, allowing duplicate frequencies to be used.

The weights or the compensating correction value used to control
5 DACs 20 and 30 (FIG. 1) may be computed to reduce the presence of user interference in a SDMA network. The user interference as measured in the quadrature signals (Process 510) is used to form a matrix T (Process 620). A new matrix is formed by multiplying the matrix T with the conjugate transpose T^* (Process 630). The square root is taken and the matrix U is
10 formed, then the inverse of the matrix U is taken (Process 640). Process 650 defines a pre and post multiplying of the matrix H by the inverse of the matrix U . These weights computed by processor 68 may be transferred to receiver 12 and transmitter 72 to control DACs 20 and 30 (Process 670).

In general, all of these embodiments described in FIGs. 2-6 that
15 generate receiver weights may also apply to the computation of the transmitter weights. Note that the weights that control the gain and phase of each receive chain may be a function of time and may be adaptively updated with each new channel estimate. Alternatively, for systems where the channel may vary slowly with time, weights for each new channel matrix do
20 not have to be computed from scratch. Rather, the previous weight may be adjusted using an adaptive filter. By way of example, a Recursive Least Squares (RLS) filter (not shown) may simplify the digital SVD algorithm and reduce the length of computing time that is necessary to update the weights. Further, the compensating correction value may be based on the Minimum
25 Mean-Squared Error (MMSE) algorithm (process 660).

It should be noted that the antenna weights may be complex, purely real, or purely imaginary. The weights are complex numbers as computed by processor 68 in the digital baseband domain. The complex weights take into account the entire impulse response of the channel, and thereby, combine and
30 compensate for channel multi-path. In order to reduce implementation complexity and cost, purely real weights may be used with some loss in

performance (the optimal real weights are the real part of the optimal complex weights). The weights may be implemented as tapped-delay line filters, where the number of taps on each antenna may be one or more. The complex weights on all taps and antennas may be controlled digitally. The number of taps on each antenna may be increased to allow better equalization of the temporal signal in the presence of Intersymbol Interference (ISI).

By now it should be clear that the present invention provides weights that take into account the effects of colored noise, co-channel interference, and inter-sample interference. The described method of weight computation for analog combining architectures considers the total channel impulse response over a block of time. Furthermore, these weights may also be computed to take into consideration co-channel interference or co-channel users in the same frequency band. By incorporating multiple antenna, variable-gain amplifiers, phase-shifters and an RF combiner at the receiver, the present invention provides significant gains in performance. The present invention also provides a low cost solution and reduced power consumption when compared to fully digital systems with multiple antenna.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

What is claimed is:

1. A method, comprising:
computing weights for analog signals from multiple antenna elements
5 of a receiver that combine multi-path signals and inter-sample interference.
2. The method of claim 1 wherein computing weights includes:
using quadrature signals derived from the analog signals to form a first
matrix H;
10 forming a second matrix H^* by multiplying the first matrix H with a
conjugate transpose of the first matrix H; and
performing a Singular Value Decomposition (SVD) algorithm on the
matrix HH^* .
- 15 3. The method of claim 1 wherein computing weights includes:
using quadrature signals derived from the analog signals to form a first
matrix H;
averaging the first matrix H to generate a second matrix H_a ; and
performing the Singular Value Decomposition (SVD) algorithm on the
20 second matrix H_a .
4. The method of claim 1 wherein computing weights includes:
using quadrature signals derived from the analog signals to form a first
matrix H;
25 forming a matrix N based on colored noise estimates;
forming a new matrix by multiplying the matrix N with a conjugate
transpose N^* ;
computing the square root of NN^* ;
pre and post multiplying the first matrix H by an inverse of a square
30 root of NN^* to provide a resulting matrix; and

performing a Singular Value Decomposition (SVD) algorithm on the resulting matrix.

5 5. The method of claim 1 wherein computing weights includes:
using quadrature signals to estimate interference and noise in channels
in the absence of the analog signals to form a matrix N; and
using an iterative algorithm on the matrix N.

10 6. The method of claim 1 further comprising:
controlling a gain of a Low Noise Amplifier in a receive chain with the
computed weights.

15 7. The method of claim 1 further comprising:
controlling a phase of a phase shifter in a receive chain with the
computed weights.

20 8. The method of claim 1 further comprising:
controlling a phase of a phase shifter and a gain of a power amplifier in
a transmitter with the computed weights.

25 9. A method, comprising:
sending known symbols to a receiver having multiple antenna to derive
a compensating correction value that may be applied to a receiver chain that
corresponds to each antenna.

30 10. The method of claim 9 further including:
computing weights for beam-forming analog signals through the
multiple antenna at the receiver that combines multi-path signals and inter-
sample interference.

11. The method of claim 9 further including:
estimating a channel impulse response in a time-domain to provide the
compensating correction value as an analog value.

12. The method of claim 9 further including:
controlling signal amplification provided by a Low Noise Amplifier and
phase through a phase shifter in a receive chain with the compensating
5 correction value.

13. The method of claim 9 further comprising:
controlling a phase of a phase shifter and a gain of a power amplifier in
a transmitter with the compensating correction value.
10

14. A system comprising:
a Static Random Access Memory (SRAM);
a communication processor coupled via an external bus to the SRAM,
where the communication processor receives modulated signals at multiple
15 antenna and computes a compensating correction value for analog signals
from multiple antenna elements that combine multi-path signals and inter-
sample interference; and
amplifier circuits in a receiver to receive the modulated signals and
further receiving the compensating correction value.
20

15. The system of claim 14, further including:
phase shifters in the receiver that are coupled to the amplifier circuits,
wherein the phase shifters receive the compensating correction value.

25 16. The system of claim 14, further including:
power amplifiers in a transmitter to receive the compensating
correction value, wherein the power amplifiers provide gain to signals
transmitted from the multiple antenna elements.

17. A method of computing a compensating correction value for analog signals from multiple antenna elements, comprising:
using quadrature signals derived from the analog signals to estimate
5 interference and noise in channels; and
using the quadrature signals to form a matrix H.

18. The method of claim 17, further comprising:
forming a matrix K based on colored noise estimates;
10 forming a new matrix KK^* by multiplying the matrix K with a conjugate
transpose K^* ; and
computing a square root of the new matrix KK^* .

19. The method of claim 18, further comprising:
15 pre and post multiplying the matrix H by an inverse of the square root
of KK^* to provide a resulting matrix.

20. The method of claim 19, further comprising:
performing a Singular Value Decomposition (SVD) algorithm on the
20 resulting matrix to generate the compensating correction value.

21. The method of claim 17, further comprising:
forming a matrix K based on colored noise estimates; and
generating the compensating correction value based on the Minimum
25 Mean-Squared Error (MMSE) algorithm.

22. The method of claim 17, further comprising:
forming a matrix O based on interference and noise in the channels in
the absence of any signal;
30 forming a new matrix OO^* by multiplying the matrix O with a
conjugate transpose O^* ; and

computing a square root of the new matrix OO^* .

23. The method of claim 22, further comprising:
pre and post multiplying the matrix H by an inverse of the square root
5 of OO^* to provide a resulting matrix.

24. The method of claim 23, further comprising:
performing a Singular Value Decomposition (SVD) algorithm on the
resulting matrix to generate the compensating correction value.
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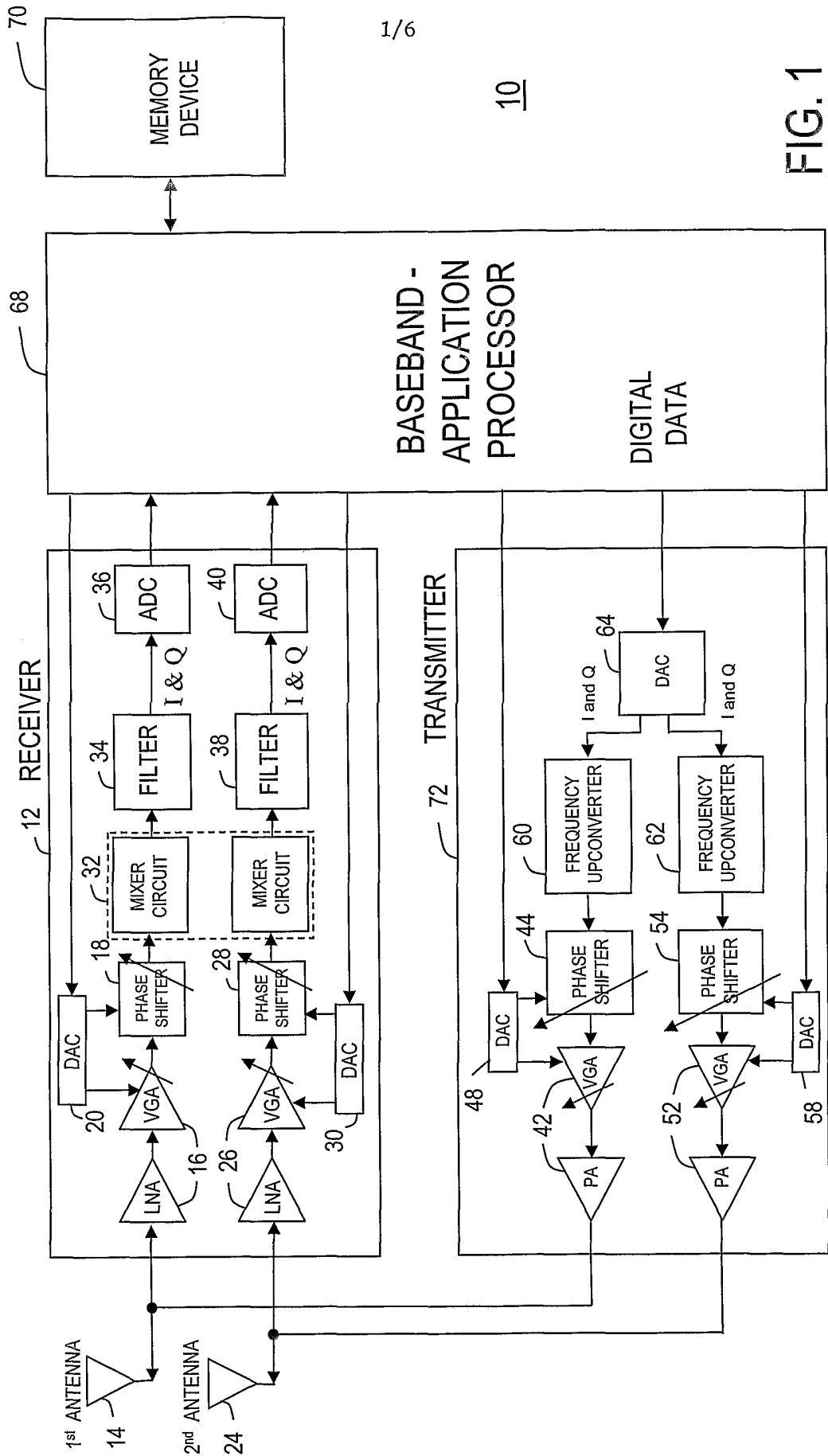
25. The method of claim 17, further comprising:
forming a matrix O based on interference and noise in the channels in
the absence of any signal; and
computing the compensating correction value based on the Minimum
15 Mean-Squared Error (MMSE) algorithm.

26. The method of claim 17, further comprising:
forming a matrix T based on user interference in a Spatial Division
Multiple Access (SDMA) communications network;
20 forming a new matrix TT^* by multiplying the matrix T with a conjugate
transpose T^* ; and
computing a square root of the new matrix TT^* .

27. The method of claim 26, further comprising:
25 pre and post multiplying the matrix H by an inverse of the square root
of TT^* to provide a resulting matrix.

28. The method of claim 27, further comprising:
performing a Singular Value Decomposition (SVD) algorithm on the
30 resulting matrix to generate the compensating correction value.

29. The method of claim 17, further comprising:
forming a matrix T based on user interference in a Spatial Division
Multiple Access (SDMA) communications network; and
computing the compensating correction value based on the Minimum
5 Mean-Squared Error (MMSE) algorithm.



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FIG. 1

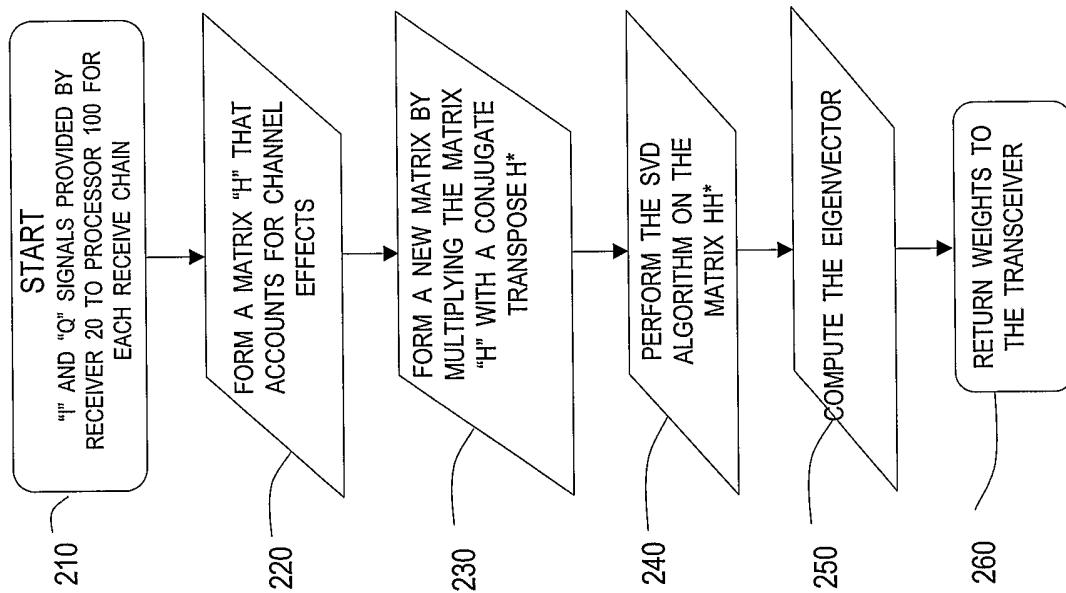


FIG. 2

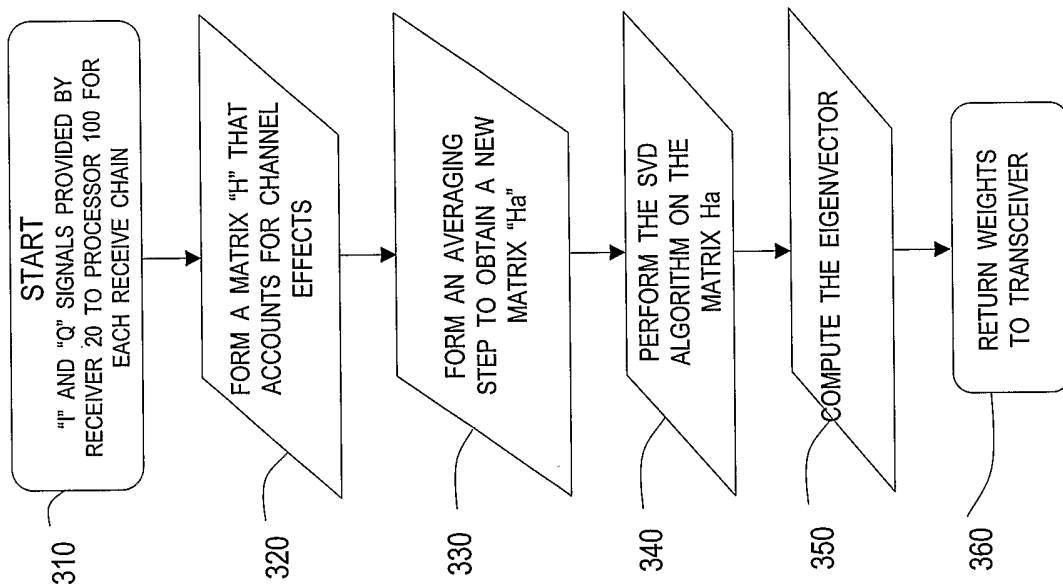


FIG. 3

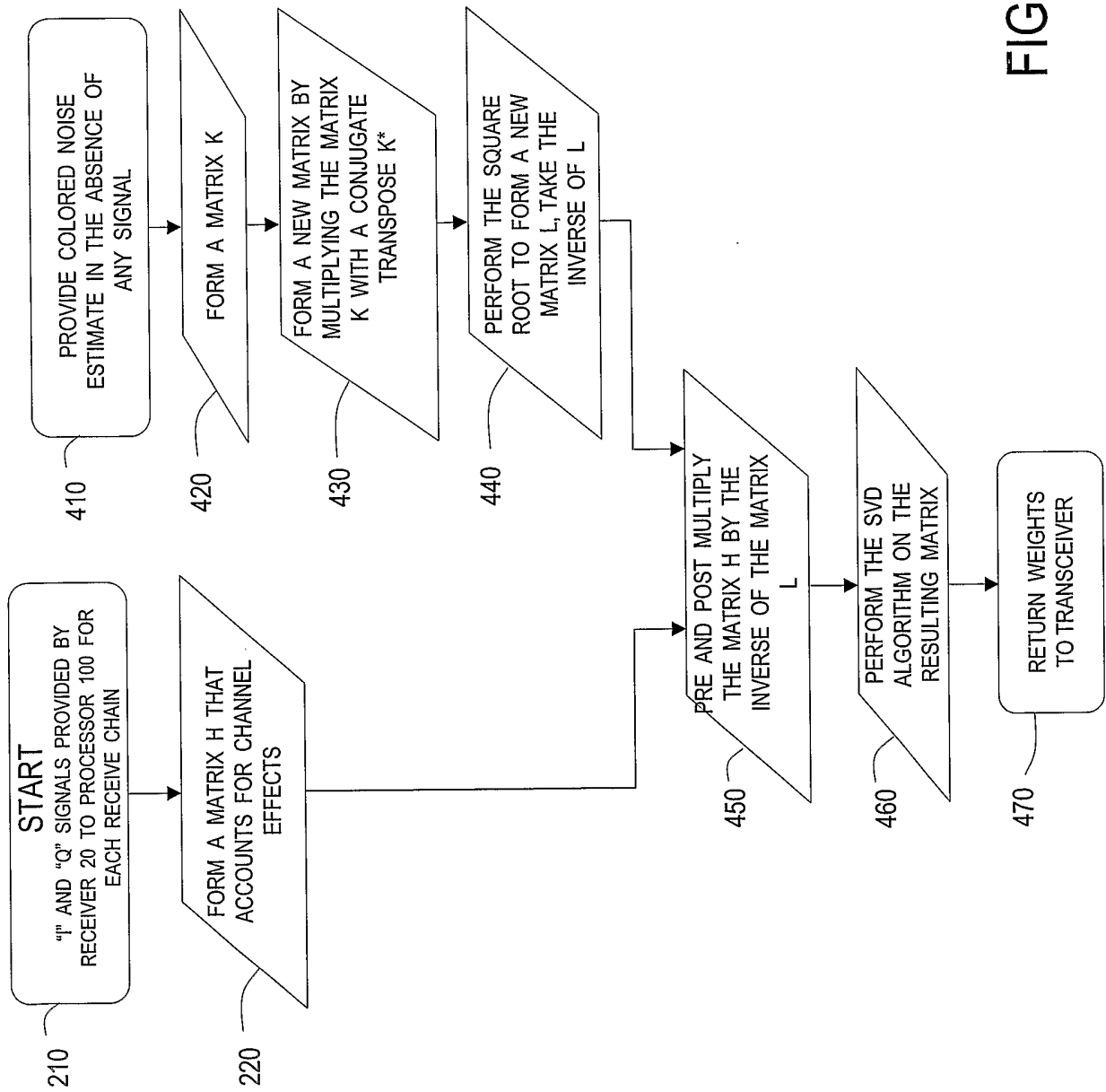


FIG. 4

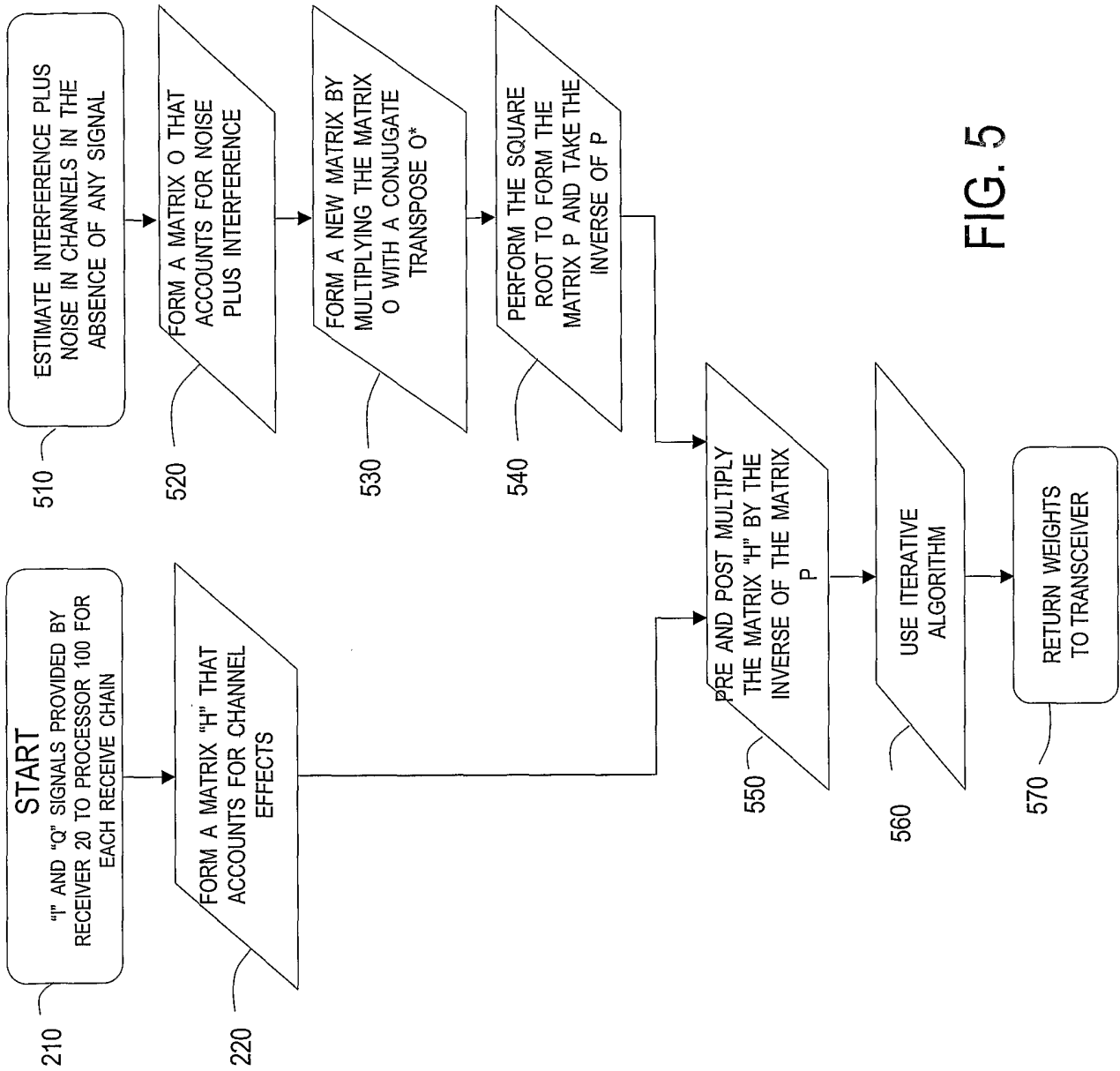


FIG. 5

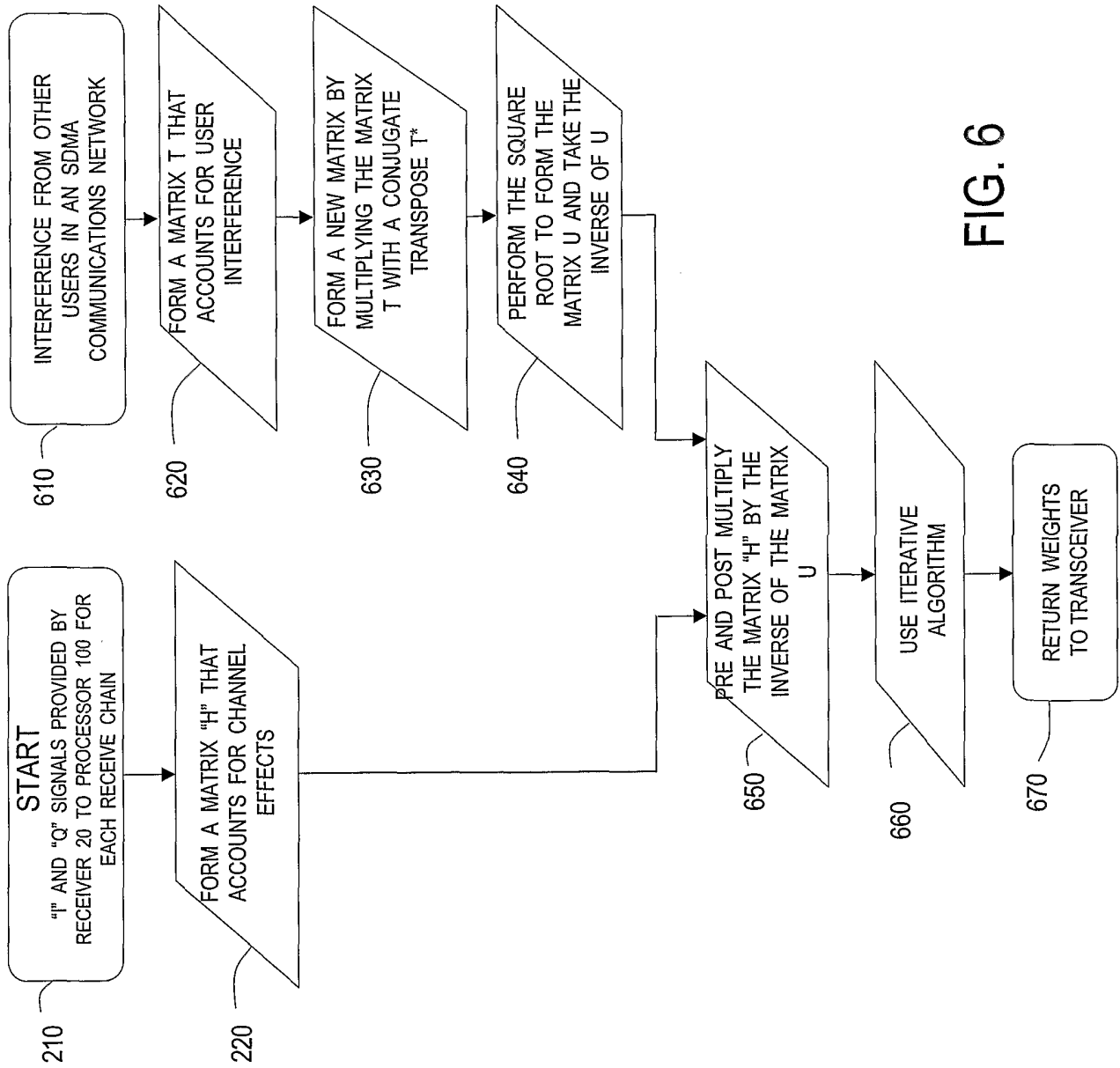


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US2004/011419

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B7/08

PCT

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/013164 A1 (BOROS TIBOR ET AL) 31 January 2002 (2002-01-31) paragraph '0036! paragraph '0043! paragraph '0068! - paragraph '0069! paragraph '0071! - paragraph '0072! paragraph '0083! - paragraph '0084! paragraph '0105! - paragraph '0106! paragraph '0199! abstract; figure 2	1-29
X	US 2003/048861 A1 (KUNG SUN YUAN ET AL) 13 March 2003 (2003-03-13) abstract; figures 3,5	1-8
X	EP 0 892 504 A (CSELT CENTRO STUDI LAB TELECOM) 20 January 1999 (1999-01-20) abstract; figure 2 page 3, line 15 - page 5, line 44	9-13

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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