

DESCRIPTION

SEMICONDUCTOR DEVICE

5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a driving method thereof. Further, the present invention relates to an electronic device provided therewith.

10 [0002]

In this specification and the like, the term "semiconductor device" means all devices that can operate by utilizing semiconductor characteristics. For example, a power device, a display device including the power device, an integrated circuit including the power device, and the like are included in the category of the
15 semiconductor device.

BACKGROUND ART

[0003]

As a semiconductor device used for a power device, a power device
20 manufactured with the use of a silicon material is widely prevalent. The power device including silicon has a narrow band gap; therefore, the operation range is limited at high temperature. Thus, in recent years, a power device including SiC or GaN, which has a wide band gap, has been developed (see Patent Document 1, for example).

[Reference]

25 [Patent Document]

[0004]

[Patent Document 1] Japanese Published Patent Application No. 2009-010142

DISCLOSURE OF INVENTION

30 [0005]

As an example of a power device including GaN, a heterojunction field-effect transistor (HFET) can be given. In the HFET, an AlN layer, a GaN layer, and an

AlGaN layer, which are buffer layers, are stacked over a SiC substrate, and a source electrode, a gate electrode, and a drain electrode are formed over the AlGaN layer. Further, because of a difference between a band gap of the GaN layer and a band gap of the AlGaN layer, a high concentration two dimensional electron gas layer is formed at the interface between the GaN layer and the AlGaN layer. Since the energy level is lower than the Fermi level in a conduction band of the two dimensional electron gas layer, the two dimensional electron gas layer serves as a channel in the HFET and the HFET is in a normally-on state in which current flows even when voltage is not applied to a gate, causing a problem in that a circuit configuration of a driver circuit or a protective circuit is complicated. When an electron concentration is simply reduced in order to obtain a normally-off power device, resistance of an element is increased. Therefore, it is extremely difficult to achieve both a normally-off state of a power device and a low resistance of the power device at the same time. Further, an attempt has been made to realize a normally-off device with an innovative structure; however, a device structure becomes complicated and manufacturing cost is increased, which is a problem.

[0006]

Therefore, it is an object of one embodiment of the present invention to provide a semiconductor which can realize an off state device without increase in power consumption.

[0007]

One embodiment of the present invention is a semiconductor device including a power element which is in an on state when voltage is not applied to a gate, a switching field-effect transistor for applying first voltage to the gate of the power element, and a switching field-effect transistor for applying voltage lower than the first voltage to the gate of the power element. The switching field-effect transistors have small off-state current. Further, each of the switching field-effect transistors is a semiconductor device in which a channel region is formed using an i-type or substantially i-type oxide semiconductor layer. With the switching field-effect transistors, the power element is turned on or off by application of a high potential or a low potential to the gate of the power element.

[0008]

One embodiment of the present invention is a semiconductor device including a power MOSFET in which a first gate and a second gate are included and a channel region is formed using an n-type oxide semiconductor layer, a switching field-effect transistor for applying positive voltage to the first gate and the second gate of the power MOSFET, and a switching field-effect transistor for applying negative voltage to the first gate and the second gate of the power MOSFET. A node of the first gate and the second gate of the power MOSFET is connected to the switching field-effect transistors, and a channel region of each of the switching field-effect transistors is formed using an i-type or substantially i-type oxide semiconductor layer. With the switching field-effect transistors, a high potential or a low potential is applied to the first gate and the second gate of the power MOSFET so that the power MOSFET is turned on or off.

[0009]

One embodiment of the present invention is a semiconductor device including a first field-effect transistor connected to a high voltage generation source, a second field-effect transistor connected to the first field-effect transistor, a third field-effect transistor connected to the second field-effect transistor and a low voltage generation source, a capacitor connected to the second field-effect transistor and the third field-effect transistor, and a power MOSFET connected to the first field-effect transistor and the second field-effect transistor. The power MOSFET includes a first gate, a second gate, a first insulating layer in contact with the first gate, a second insulating layer in contact with the second gate, an oxide semiconductor layer formed between the first insulating layer and the second insulating layer, and a first terminal and a second terminal which are in contact with the oxide semiconductor layer and serve as a source region and a drain region. A node of the first gate and the second gate is connected to the first field-effect transistor and the second field-effect transistor. A channel formation region of each of the first to third field-effect transistors is formed using an i-type oxide semiconductor layer. The oxide semiconductor layer of the power MOSFET is n-type.

[0010]

The carrier concentration of the oxide semiconductor layer in the power MOSFET is higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and lower than or equal to 1×10^{20}

cm^{-3} , preferably higher than or equal to $1 \times 10^{17} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$.

[0011]

The carrier concentration of the oxide semiconductor layer in each of the
5 switching field-effect transistors and each of the first to third field-effect transistors is
lower than $5 \times 10^{14} / \text{cm}^3$.

[0012]

The first gate or the second gate of the power MOSFET overlaps with one of
the first terminal and the second terminal but does not necessarily overlap with the other
10 of the first terminal and the second terminal.

[0013]

According to one embodiment of the present invention, a power device which
can realize an off state and a semiconductor device including the power device can be
provided without increase in power consumption.

15

BRIEF DESCRIPTION OF DRAWINGS

[0014]

In the accompanying drawings:

FIG. 1 is an equivalent circuit diagram illustrating a semiconductor device of
20 one embodiment of the present invention;

FIGS. 2A to 2C are each an equivalent circuit diagram illustrating a
semiconductor device of one embodiment of the present invention;

FIGS. 3A to 3C are each an equivalent circuit diagram illustrating a
semiconductor device of one embodiment of the present invention;

25 FIGS. 4A and 4B are each an equivalent circuit diagram illustrating a
semiconductor device of one embodiment of the present invention;

FIGS. 5A and 5B are a cross-sectional view and a top view illustrating a
semiconductor device of one embodiment of the present invention;

30 FIGS. 6A and 6B are each a cross-sectional view illustrating a semiconductor
device of one embodiment of the present invention;

FIGS. 7A to 7D are cross-sectional views illustrating manufacturing steps of a

semiconductor device of one embodiment of the present invention;

FIG. 8 is a cross-sectional view illustrating a semiconductor device of one embodiment of the present invention;

FIGS. 9A and 9B are a cross-sectional view and a top view illustrating a semiconductor device of one embodiment of the present invention;

FIG. 10 is a cross-sectional view illustrating a semiconductor device of one embodiment of the present invention;

FIGS. 11A to 11D are cross-sectional views illustrating manufacturing steps of a semiconductor device of one embodiment of the present invention;

FIG. 12 is an equivalent circuit diagram illustrating a semiconductor device of one embodiment of the present invention;

FIG. 13 is an equivalent circuit diagram illustrating a semiconductor device of one embodiment of the present invention;

FIG. 14 is an equivalent circuit diagram illustrating a semiconductor device of one embodiment of the present invention;

FIG. 15 is an equivalent circuit diagram illustrating a semiconductor device of one embodiment of the present invention;

FIG. 16 is an equivalent circuit diagram illustrating a semiconductor device of one embodiment of the present invention;

FIG. 17 is an equivalent circuit diagram illustrating a semiconductor device of one embodiment of the present invention; and

FIGS. 18A to 18C illustrate electronic devices.

BEST MODE FOR CARRYING OUT THE INVENTION

[0015]

Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings. Note that the present invention can be carried out in many different modes, and it is easily understood by those skilled in the art that modes and details of the present invention can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be interpreted as being limited to the description of the embodiments. Note that in structures of the present invention described below,

reference numerals denoting the same portions are used in common in different drawings.

[0016]

Note that the size, the thickness of a layer, and a region of each structure
5 illustrated in the drawings and the like in the embodiments are exaggerated for
simplicity in some cases. Therefore, embodiments of the present invention are not
limited to such scales.

[0017]

Note that terms such as first, second, third, and N th (N is a natural number)
10 employed in this specification are used in order to avoid confusion between components
and do not set a limitation on number.

[0018]

Note that voltage refers to a potential difference between a given potential and
a reference potential (e.g., a ground potential) in many cases. Accordingly, voltage,
15 potential, and a potential difference can be referred to as potential, voltage, and a
voltage difference, respectively.

[0019]

Note that when it is explicitly described that "A and B are connected", the case
where A and B are electrically connected, the case where A and B are functionally
20 connected, and the case where A and B are directly connected are included therein.
Here, each of A and B corresponds to an object (e.g., a device, an element, a circuit, a
wiring, an electrode, a terminal, a conductive layer, or a layer). Accordingly, a
connection relation other than that shown in drawings and texts is also included without
limitation to a predetermined connection relation, for example, the connection relation
25 shown in the drawings and the texts.

[0020]

(Embodiment 1)

In this embodiment, a circuit structure of a semiconductor device, which is a
power device, and operation thereof will be described.

30 [0021]

A semiconductor device illustrated in FIG. 1 includes a power element 110 and
a control circuit 100. The control circuit 100 includes a field-effect transistor 102 (also

referred to as a first transistor), a field-effect transistor 103 (also referred to as a second transistor), a field-effect transistor 104 (also referred to as a third transistor), a capacitor 105, an overvoltage detection circuit 106, a refresh control circuit 107, a high voltage generation source 108, and a low voltage generation source 109.

5 [0022]

The control circuit 100 switches between high voltage generated by the high voltage generation source 108 and low voltage generated by the low voltage generation source 109, which is voltage applied to the power element 110. Moreover, the control circuit 100 controls the amount of current flowing through the power element 110 when
10 overvoltage is applied between an input terminal IN and an output terminal OUT.

[0023]

As for the field-effect transistor 102, a gate is connected to the overvoltage detection circuit 106, a first terminal is connected to the high voltage generation source 108, and a second terminal is connected to the power element 110. The field-effect
15 transistor 102 controls application of a high potential to the power element 110 connected to the second terminal.

[0024]

As for the field-effect transistor 103, a gate is connected to the overvoltage detection circuit 106, a first terminal is connected to the capacitor 105 and a second
20 terminal of the field-effect transistor 104, and a second terminal is connected to the power element 110.

[0025]

The field-effect transistor 103 controls application of a low potential stored in the capacitor 105 from the low voltage generation source 109, to the power element 110
25 connected to the second terminal.

[0026]

Note that off-state current in this specification refers to current flowing between a source and a drain, that is, between a first terminal and a second terminal of a field-effect transistor when the field-effect transistor is not conducting.

30 [0027]

As for the field-effect transistor 104, a gate is connected to the refresh control circuit 107, a first terminal is connected to the low voltage generation source 109, and

the second terminal is connected to the capacitor 105 and the first terminal of the field-effect transistor 103. The field-effect transistor 104 controls charging of the capacitor 105 connected to the second terminal with a low potential.

[0028]

5 A channel region of each of the field-effect transistors 102 to 104 is formed using an i-type or substantially i-type oxide semiconductor layer. The carrier density of the i-type or substantially i-type oxide semiconductor layer is lower than 5×10^{14} /cm³, preferably lower than 1×10^{12} /cm³, more preferably lower than or equal to 1×10^{11} /cm³. Moreover, it is preferable that hydrogen or oxygen deficiency serving as a
10 donor be little and the hydrogen concentration be lower than or equal to 1×10^{16} /cm³. Note that the carrier density can be obtained by the Hall effect measurement. Lower carrier density can be obtained with the use of measurement results of capacitance-voltage (CV) measurement. The hydrogen concentration of the oxide semiconductor layer can be measured by secondary ion mass spectrometry (SIMS).

15 [0029]

The field-effect transistor 102 including the i-type or substantially i-type oxide semiconductor in a channel region can have an off-state current of 1×10^{-16} A/ μ m or smaller, and further can have an off-state current of 1×10^{-19} A/ μ m or smaller. An i-type or substantially i-type oxide semiconductor has a wide band gap and requires a
20 large amount of thermal energy for excitation of electrons; therefore, direct recombination and indirect recombination are less likely to occur. In a state where a negative potential is applied to a gate electrode (an off state), holes which are minority carriers are substantially zero; accordingly, direct recombination and indirect recombination are less likely to occur and the amount of current is as small as possible.
25 As a result, in a state where the field-effect transistor is in a non-conducting (also referred to as OFF) state, a circuit can be designed with the oxide semiconductor layer that can be considered as an insulator. On the other hand, when the field-effect transistor is in a conducting state, the current supply capability of the i-type or substantially i-type oxide semiconductor layer is expected to be higher than the current
30 supply capability of a semiconductor layer formed of amorphous silicon. The field-effect transistors 102 to 104 are enhancement type transistors and normally-off

transistors with extremely small leakage current in an off state, and thus have excellent switching characteristics.

[0030]

5 The capacitor 105 is an element for holding a low potential to be applied to the power element 110 when the field-effect transistor 104 is intermittently conducting (also referred to as ON). The capacitor 105 may have a structure in which an insulating layer is sandwiched between conductors.

[0031]

10 The overvoltage detection circuit 106 is a circuit for controlling conduction and non-conduction of the field-effect transistor 102 and the field-effect transistor 103 in accordance with voltage between the input terminal IN and the output terminal OUT. Specifically, when overvoltage is applied between the input terminal IN and the output terminal OUT, the field-effect transistor 102 is made to be conducting, the field-effect transistor 103 is made to be non-conducting, and application of high voltage from the high voltage generation source 108 to the power element 110 is controlled. When
15 overvoltage is not applied between the input terminal IN and the output terminal OUT, the field-effect transistor 102 is made to be non-conducting, the field-effect transistor 103 is made to be conducting, and application of a low potential stored in the capacitor 105 from the low voltage generation source 109, to the power element 110 is controlled.

20 [0032]

The refresh control circuit 107 is a circuit for controlling conduction and non-conduction of the field-effect transistor 104 in order to control charging of the capacitor 105 with a low potential from the low voltage generation source 109. Specifically, the refresh control circuit 107 is a circuit for intermittently making the
25 field-effect transistor 104 conducting in order to charge the capacitor 105 with a low potential before releasing a low potential to the power element 110, which is held because of charging of the capacitor 105 from the low voltage generation source 109.

[0033]

30 A power element which is turned on without application of voltage to its gate is used as the power element 110. As the power element 110, a bipolar transistor, a field-effect transistor (FET), a gate turnoff thyristor, an insulated gate bipolar transistor (IGBT), or the like, which includes Si, SiC, GaN, or an oxide semiconductor, can be

used as appropriate. Further, as the field-effect transistor, a power metal oxide semiconductor FET (power MOSFET), an HFET, a junction field-effect transistor (JFET), or the like can be used as appropriate. An equivalent circuit including a power element 121 having three terminals is illustrated in FIG. 2A. A gate of the power element 121 is connected to the field-effect transistor 102 and the field-effect transistor 103. Further, one of a source terminal and a drain terminal of the power element 121 is referred to as a first terminal and the other of the source terminal and the drain terminal of the power element 121 is referred to as a second terminal. The first terminal is connected to the input terminal IN and the second terminal is connected to the output terminal OUT.

[0034]

In this embodiment, hereinafter, as a typical example of the power element 110, description is given with the use of a power MOSFET 101 having four terminals as illustrated in FIG. 2B.

[0035]

The power MOSFET 101 includes four terminals, which are typically a first gate terminal (also referred to as a first gate), a second gate terminal (also referred to as a second gate), a drain terminal (also referred to as a drain), and a source terminal (also referred to as a source). In the power MOSFET 101, the first gate and the second gate are provided above and below a channel region, and a signal for controlling switching of the power MOSFET 101 is supplied to the first gate and the second gate.

[0036]

FIG. 2C is a circuit symbol of the power MOSFET 101 in which a first gate 201 and a second gate 206 are provided above and below a channel region. As illustrated in FIG. 2C, the power MOSFET 101 includes the first gate 201, the second gate 206, a first terminal 204A, and a second terminal 204B. In the power MOSFET 101, a signal (a signal G in FIG. 2C) output from the high voltage generation source 108 or the low voltage generation source 109 is input to the first gate 201 and the second gate 206. By the signal output from the high voltage generation source 108 or the low voltage generation source 109, switching of conduction and non-conduction between the first terminal 204A and the second terminal 204B of the power MOSFET 101 is controlled.

[0037]

The channel region of the power MOSFET 101 may be formed using an n-type oxide semiconductor layer. The n-type oxide semiconductor layer has a carrier density of higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$,
5 preferably higher than or equal to $1 \times 10^{17} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$. Since hydrogen and oxygen deficiency serve as donors in an oxide semiconductor, it is preferable that the hydrogen concentration be higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$.

[0038]

10 Since the power MOSFET 101 includes an n-type oxide semiconductor layer in the channel region, on-resistance can be reduced and a large amount of current can flow as compared to a power MOSFET including an i-type oxide semiconductor layer in a channel region. However, since the power MOSFET including an n-type oxide semiconductor layer in a channel region is a depletion type transistor, the transistor is a
15 normally-on transistor in which current flows even in a state where voltage is not applied to its gate. The power MOSFET described in this embodiment includes the second gate 206 in addition to the first gate 201. When negative voltage is applied to the first gate 201 and the second gate 206, the power MOSFET can be turned off. Therefore, the power MOSFET in which on-resistance is low and a large amount of
20 current can flow can be turned off. On the other hand, when positive voltage is applied to the first gate 201 and the second gate 206, the power MOSFET can be turned on. Further, since the power MOSFET 101 includes the first gate 201 and the second gate 206, the threshold voltage can be made further negative by making the channel region thicker and on current can be increased as compared to a power MOSFET having a
25 single gate.

[0039]

Next, operation of the semiconductor device illustrated in FIG. 2B will be described with reference to FIGS. 3A to 3C and FIGS. 4A and 4B. In FIGS. 3A to 3C and FIGS. 4A and 4B, dotted arrows are shown to facilitate understanding of flow of
30 signals in accordance with conduction and non-conduction of the power MOSFET 101 and the field-effect transistors. The channel region of the power MOSFET 101

included in a semiconductor device is formed using an n-type oxide semiconductor layer, and the power MOSFET 101 is made to be conducting by the high potential from the high voltage generation source 108 and is made to be non-conducting by the low potential from the low voltage generation source 109. Note that as for operation of the semiconductor device illustrated in FIG. 2A, the power MOSFET 101 in the equivalent circuits illustrated in FIGS. 3A to 3C and FIGS. 4A and 4B may be replaced with the power element 121.

[0040]

Operation in the case where the power MOSFET 101 is conducting will be described with reference to FIG. 3A. The field-effect transistor 102 is made to be conducting by control of the overvoltage detection circuit 106, the field-effect transistor 103 is made to be non-conducting by control of the overvoltage detection circuit 106, and the field-effect transistor 104 is made to be non-conducting by control of the refresh control circuit 107. The field-effect transistor 102 is made to be conducting, so that a high potential is applied to the first gate and the second gate of the power MOSFET 101 from the high voltage generation source 108 and thus the power MOSFET 101 is conducting.

[0041]

Operation in the case where the power MOSFET 101 is non-conducting will be described with reference to FIG. 3B. The field-effect transistor 102 is made to be non-conducting by control of the overvoltage detection circuit 106, the field-effect transistor 103 is made to be conducting by control of the overvoltage detection circuit 106, and the field-effect transistor 104 is made to be non-conducting by control of the refresh control circuit 107. As illustrated in FIG. 3B, the field-effect transistor 103 is conducting, so that a low potential which is stored in the capacitor 105 from the low voltage generation source 109 is applied to the first gate and the second gate of the power MOSFET 101 and thus the power MOSFET 101 is non-conducting.

[0042]

Operation in the case where the capacitor 105 is charged with a low potential described with reference to FIG. 3B will be described with reference to FIG. 3C. The field-effect transistor 102 is made to be non-conducting by control of the overvoltage detection circuit 106, the field-effect transistor 103 is made to be conducting by control

of the overvoltage detection circuit 106, and the field-effect transistor 104 is made to be conducting by control of the refresh control circuit 107. A low potential is stored in the capacitor 105 from the low voltage generation source 109.

[0043]

5 Note that charge of the capacitor 105 with a low potential, which is described with reference to FIG. 3C, is performed at regular intervals controlled by the refresh control circuit 107. Specifically, the semiconductor device keeps the state illustrated in FIG. 3B while a low potential making the power MOSFET 101 non-conducting, with which the capacitor 105 is charged by the low voltage generation source 109, is held in
10 the capacitor 105. Then, the semiconductor device is made to be in a state illustrated in FIG. 3C in an intermittent manner; thus, the field-effect transistor 104 is made to be conducting and a low potential is stored in the capacitor 105. For example, the operation illustrated in FIG. 3C may be performed once a minute, with enough time taken for charging.

15 [0044]

In the structure of this embodiment as described above, the state in FIG. 3A or FIG. 3B and the state in FIG. 3C are repeated, but a period in which the state in FIG. 3B is held is longer.

[0045]

20 Here, an effect of this embodiment will be described in detail with reference to FIG. 4A. In FIG. 4A, a node connected to the first gate and the second gate of the power MOSFET 101, the field-effect transistor 103, and one of the terminals of the capacitor 105, which are in a state illustrated in FIG. 3B, are illustrated with solid lines and other connections are illustrated by dotted lines.

25 [0046]

The field-effect transistor 102 and the field-effect transistor 104 become non-conducting, whereby the node connected to the first gate and the second gate of the power MOSFET 101 is electrically in a floating state. As described above, each of the field-effect transistor 102 and the field-effect transistor 104 includes an i-type or
30 substantially i-type oxide semiconductor layer in the channel region, so that off-state current is extremely small. Therefore, the node connected to the first gate and the second gate of the power MOSFET 101 can hold a low potential stored in the capacitor

105 from the low voltage generation source 109 for a long time. A low potential may be applied to the capacitor not constantly but intermittently. Further, when a low potential is applied to the first gate and the second gate of the power MOSFET 101, the power MOSFET 101 is in an off state. Therefore, the semiconductor device of this
5 embodiment can realize an off state of the power MOSFET 101 without increase in power consumption.

[0047]

Further, in the semiconductor device illustrated in FIG. 2C, in order to increase a holding property of a potential of the node connected to the first gate and the second
10 gate of the power MOSFET 101, a capacitor 401 may be additionally provided to the node connected to the first gate and the second gate as illustrated in FIG. 4B. Note that in the semiconductor devices illustrated in FIGS. 2A and 2B, the capacitor 401 may be provided to the gate of the power MOSFET 101 or the gate of the power element 121.

[0048]

15 Note that in this embodiment, what is illustrated in the drawing can be freely combined with or replaced with what is described in another embodiment as appropriate.

[0049]

(Embodiment 2)

20 In this embodiment, a structure of the power MOSFET 101 described in Embodiment 1 and a manufacturing method thereof will be described with reference to FIGS. 5A and 5B, FIGS. 6A and 6B, and FIGS. 7A to 7D.

[0050]

FIG. 5A illustrates one embodiment of a cross-sectional structure of the power
25 MOSFET 101 described in Embodiment 1 and FIG. 5B illustrates a top view of the power MOSFET 101. A cross-sectional view taken along line A-B in FIG. 5B corresponds to FIG. 5A.

[0051]

30 In the power MOSFET 101 illustrated in FIG. 5A, the first gate 201 formed of a conductive layer is provided over a substrate 200, a gate insulating layer 202 is provided over the first gate 201, an n-type oxide semiconductor layer 203 is provided over the gate insulating layer 202, the first terminal 204A and the second terminal 204B formed

of a conductive layer are provided so as to cover part of the oxide semiconductor layer 203, an insulating layer 205 is provided so as to cover the oxide semiconductor layer 203, the first terminal 204A, and the second terminal 204B, and the second gate 206 formed of a conductive layer is provided over the insulating layer 205 so as to overlap
5 with part of the first terminal 204A and part of the second terminal 204B.

[0052]

It is necessary that the substrate 200 have at least heat resistance high enough to withstand heat treatment performed later. When a glass substrate is used as the substrate 200, a glass substrate having a strain point of higher than or equal to 730 °C is
10 preferably used. As the glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Note that a glass substrate containing BaO and B₂O₃ so that the amount of BaO is larger than that of B₂O₃ is preferably used.

[0053]

15 Instead of the glass substrate, a substrate formed of an insulator, such as a ceramic substrate, a quartz substrate, or a sapphire substrate can be used. Alternatively, crystallized glass or the like may be used. Further alternatively, a substrate obtained by forming an insulating layer over a surface of a semiconductor substrate such as a silicon wafer or a surface of a conductive substrate formed of a metal material can be
20 used.

[0054]

Although not illustrated in FIG. 5A, when an insulating layer having high thermal conductivity is formed between the substrate 200 and the first gate 201, the power MOSFET 101 having high heat resistance can be manufactured. Examples of
25 the insulating layer having high thermal conductivity include an aluminum nitride layer, an aluminum nitride oxide layer, a silicon nitride layer, and the like.

[0055]

The first gate 201 is formed using a metal element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing
30 any of these metal elements as a component; an alloy containing these metal elements in combination; or the like. Further, one or more metal elements selected from manganese, magnesium, zirconium, and beryllium may be used. In addition, the first

gate 201 may have a single-layer structure or a stacked structure having two or more layers. For example, a single-layer structure of an aluminum layer containing silicon, a two-layer structure in which a titanium layer is stacked over an aluminum layer, a two-layer structure in which a titanium layer is stacked over a titanium nitride layer, a two-layer structure in which a tungsten layer is stacked over a titanium nitride layer, a two-layer structure in which a tungsten layer is stacked over a tantalum nitride layer, a three-layer structure in which a titanium layer, an aluminum layer, and a titanium layer are stacked in this order, and the like can be given. Alternatively, a layer, an alloy layer, or a nitride layer, which contains aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium, thereof may be used.

[0056]

The first gate 201 can be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible to have a stacked-layer structure formed using the above light-transmitting conductive material and the above metal element.

[0057]

The gate insulating layer 202 can be formed in a single layer or a stacked layer using a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer. A portion of the gate insulating layer 202 which is in contact with the oxide semiconductor layer 203 preferably contains oxygen, and in particular, the portion of the gate insulating layer 202 is preferably formed using a silicon oxide layer. By using a silicon oxide layer, oxygen can be supplied to the oxide semiconductor layer 203 and favorable characteristics can be obtained.

[0058]

The gate insulating layer 202 is formed using a high-*k* material such as hafnium silicate (HfSiO_x), hafnium silicate to which nitrogen is added ($\text{HfSi}_x\text{O}_y\text{N}_z$), hafnium aluminate to which nitrogen is added ($\text{HfAl}_x\text{O}_y\text{N}_z$), hafnium oxide, or yttrium oxide, so that gate leakage current can be reduced. Further, a stacked structure can be used in

which a high-*k* material and one or more of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, and an aluminum oxide layer are stacked. The thickness of the gate insulating layer 202 can be greater than or equal to 100 nm and less than or equal to 300 nm.

5 [0059]

As the n-type oxide semiconductor layer 203, a four-component metal oxide such as an In-Sn-Ga-Zn-O-based metal oxide, a three-component metal oxide such as an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, or a
10 Sn-Al-Zn-O-based metal oxide, a two-component metal oxide such as an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, or an In-Mg-O-based metal oxide can be used. Here, an *n*-component metal oxide includes *n* kinds of metal
15 element other than the metal oxide of main component at 1 %, preferably at 0.1 %.

[0060]

The n-type oxide semiconductor layer 203 is formed of a three-component metal oxide, and may be formed of a metal oxide expressed by $\text{In}M_X\text{Zn}_Y\text{O}_Z$ ($Y = 0.5$ to
5). Here, *M* represents one or a plurality of elements selected from Group 13, such as
20 gallium (Ga), aluminum (Al), or boron (B). Note that the contents of In, *M*, Zn, and O can be set freely, and the case where the *M* content is zero (that is, $X = 0$) is included. On the other hand, the contents of In and Zn are not zero. In other words, the above
expression may represent an In-Ga-Zn-O-based metal oxide, an In-Zn-O-based metal
oxide semiconductor, and the like.

25 [0061]

Further, it is preferable that the energy gap of the metal oxide forming the n-type oxide semiconductor layer 203 be 2 eV or more, preferably 2.5 eV or more, more preferably 3 eV or more.

[0062]

30 As the n-type oxide semiconductor layer 203, an oxide semiconductor having an amorphous structure, a microcrystalline structure, a polycrystalline structure, or a

single crystal structure can be used as appropriate. Further, an oxide semiconductor having a crystal in which the c-axis is approximately parallel to a direction perpendicular to a surface can be used.

[0063]

5 The n-type oxide semiconductor layer 203 has a carrier density of higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$, preferably higher than or equal to $1 \times 10^{17} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$. Since hydrogen and oxygen deficiency serve as donors in an oxide semiconductor, it is preferable that the hydrogen concentration be higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and
10 lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$.

[0064]

The thickness of the n-type oxide semiconductor layer 203 is set so that a depletion layer spreads in a channel region and the power MOSFET 101 is turned off when negative voltage is applied to the first gate and the second gate. In the case
15 where the carrier density is higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$, the dielectric constant is 15, the band gap is 3.15, the effective density of states in the conduction band is $N_c = 2.8 \times 10^{19} \text{ cm}^{-3}$, the effective density of states in the valence band is $N_v = 1.04 \times 10^{19} \text{ cm}^{-3}$, and a gate is provided on one surface side of the oxide semiconductor layer, the maximum width of the depletion layer is
20 greater than or equal to 7 nm and less than or equal to 677 nm. Since the power MOSFET illustrated in FIG. 5A includes the first gate 201 and the second gate 206, the thickness of the n-type oxide semiconductor layer 203 can be set to greater than or equal to 14 nm and less than or equal to 1354 nm. Further, in the case where the carrier density is higher than or equal to $1 \times 10^{17} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$,
25 the maximum width of the depletion layer is greater than or equal to 7 nm and less than or equal to 218 nm. In this case, the thickness of the n-type oxide semiconductor layer 203 can be set to greater than or equal to 14 nm and less than or equal to 436 nm.

[0065]

The first terminal 204A and the second terminal 204B are formed using a metal
30 element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of these metal elements as a component; an alloy

containing these metal elements in combination; or the like. Further, one or more metal elements selected from manganese, magnesium, zirconium, and beryllium may be used. In addition, the first terminal 204A and the second terminal 204B may have a single-layer structure or a stacked structure having two or more layers. For example, a
5 single-layer structure of an aluminum layer containing silicon, a two-layer structure in which a titanium layer is stacked over an aluminum layer, a two-layer structure in which a titanium layer is stacked over a titanium nitride layer, a two-layer structure in which a tungsten layer is stacked over a titanium nitride layer, a two-layer structure in which a tungsten layer is stacked over a tantalum nitride layer, a three-layer structure in which a
10 titanium layer, an aluminum layer, and a titanium layer are stacked in this order, and the like can be given. Alternatively, a layer, an alloy layer, or a nitride layer, which contains aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

[0066]

15 The first terminal 204A and the second terminal 204B can be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible to have a
20 stacked-layer structure formed using the above light-transmitting conductive material and the above metal element.

[0067]

The insulating layer 205 can be formed using the material of the gate insulating layer 202 as appropriate.

25 [0068]

The second gate 206 can be formed using the material of the first gate 201 as appropriate.

[0069]

30 Since the power MOSFET 101 illustrated in FIGS. 5A and 5B includes an n-type oxide semiconductor layer in the channel region, on-resistance can be reduced and a large amount of current can flow. However, since the power MOSFET including an n-type oxide semiconductor layer in a channel region is a depletion type transistor,

the transistor is a normally-on transistor in which current flows even in a state where voltage is not applied to its gate. The power MOSFET described in this embodiment includes the second gate 206 in addition to the first gate 201. When negative voltage is applied to the first gate 201 and the second gate 206, the power MOSFET can be
5 turned off. Therefore, the power MOSFET in which on-resistance is low and a large amount of current can flow can be turned off. On the other hand, when positive voltage is applied to the first gate 201 and the second gate 206, the power MOSFET can be turned on. Further, since the power MOSFET 101 includes the first gate 201 and the second gate 206, the channel region can be made thicker and on current can be
10 increased as compared to a power MOSFET having a single gate.

[0070]

As illustrated in FIG. 5B, the power MOSFETs 101 are connected in parallel, so that the channel width W can be made wide. Accordingly, a power device through which a large amount of current can flow can be manufactured.

15 [0071]

Next, cross-sectional structures of a power MOSFET, which are different from the structure in FIGS. 5A and 5B, are illustrated in FIGS. 6A and 6B. In a power MOSFET 101A illustrated in FIG. 6A, a second gate 206A overlaps with one of the first terminal 204A and the second terminal 204B and does not overlap with the other.

20 [0072]

In the power MOSFET 101A illustrated in FIG. 6A, the first gate 201 formed of a conductive layer is provided over the substrate 200, the gate insulating layer 202 is provided over the first gate 201, the n-type oxide semiconductor layer 203 is provided over the gate insulating layer 202, the first terminal 204A and the second terminal 204B
25 formed of a conductive layer are provided so as to cover part of the oxide semiconductor layer 203, and the insulating layer 205 is provided so as to cover the oxide semiconductor layer 203, the first terminal 204A, and the second terminal 204B. Further, the second gate 206A formed of a conductive layer is provided over the insulating layer 205 so as to overlap with one of the first terminal 204A and the second
30 terminal 204B and so as not to overlap with the other. That is, a region 208 is provided so that the oxide semiconductor layer 203 is overlapped with none of the second gate 206A, the first terminal 204A, and the second terminal 204B in the region

208.

[0073]

The second gate 206A can be formed using the material and the method similar to those of the second gate 206 illustrated in FIGS. 5A and 5B.

5 [0074]

In a power MOSFET 101B illustrated in FIG. 6B, a first gate 201A formed of a conductive layer is provided over the substrate 200, the gate insulating layer 202 is provided over the first gate 201A, the n-type oxide semiconductor layer 203 is provided over the gate insulating layer 202, the first terminal 204A and the second terminal 204B
10 formed of a conductive layer are provided so as to cover part of the oxide semiconductor layer 203, and the insulating layer 205 is provided so as to cover the oxide semiconductor layer 203, the first terminal 204A, and the second terminal 204B. Further, the second gate 206A formed of a conductive layer is provided over the insulating layer 205 so as to overlap with one of the first terminal 204A and the second
15 terminal 204B and so as not to overlap with the other. That is, an offset region 209 is provided so that the oxide semiconductor layer 203 is overlapped with none of the first gate 201A, the second gate 206A, the first terminal 204A, and the second terminal 204B in the offset region 209.

[0075]

20 The first gate 201A can be formed using the material and the method similar to those of the first gate 201 illustrated in FIGS. 5A and 5B.

[0076]

Since the power MOSFET 101A and the power MOSFET 101B illustrated in FIGS. 6A and 6B each includes the n-type oxide semiconductor layer 203 in the channel
25 region, on-resistance can be reduced and a large amount of current can flow. However, since the power MOSFET including an n-type oxide semiconductor layer in a channel region is a depletion transistor, the transistor is a normally-on transistor in which current flows even in a state where voltage is not applied to its gate. The power MOSFET described in this embodiment includes the second gate 206A in addition to the first gate
30 201 or the first gate 201A. When negative voltage is applied to either the first gate 201 or the first gate 201A and the second gate 206A, the power MOSFET can be turned off. Therefore, the power MOSFET in which on-resistance is low and a large amount

of current can flow can be turned off. On the other hand, when positive voltage is applied to either the first gate 201 or the first gate 201A and the second gate 206A, the power MOSFET can be turned on. Further, since the power MOSFET includes either the first gate 201 or the first gate 201A and the second gate 206A, the channel region
5 can be made thicker and a large amount of current can flow as compared to a power MOSFET having a single gate. Furthermore, in the power MOSFET 101B illustrated in FIG. 6B, the n-type oxide semiconductor has the offset region 209 which is not covered with the first gate 201A, the second gate 206A, the first terminal 204A, and the second terminal 204B, so that the drain breakdown voltage can be increased as
10 compared to the power MOSFET 101 illustrated in FIG. 5A, and high voltage can be applied to the first terminal 204A or the second terminal 204B.

[0077]

Here, a method for manufacturing the power MOSFET 101 illustrated in FIGS. 5A and 5B will be described with reference to FIGS. 7A to 7D.

15 [0078]

As illustrated in FIG. 7A, the first gate 201 is formed over the substrate 200. Next, the gate insulating layer 202 is formed over the first gate 201.

[0079]

When the first gate 201 is formed by a printing method, an inkjet method, or
20 the like, the number of steps can be reduced. Alternatively, the first gate 201 can be formed in such a manner that a conductive layer is formed by a sputtering method, a CVD method, an evaporation method, or the like, and then the conductive layer is etched with the use of a resist formed in a photolithography step as a mask. Note that it is preferable that an end portion of the first gate 201 be tapered because coverage with
25 an insulating layer, a semiconductor layer, and a conductive layer which are to be formed later can be improved. Further, an insulating layer having high thermal conductivity is preferably formed between the substrate 200 and the first gate 201 by a sputtering method, a CVD method, a coating method, a printing method, or the like.

[0080]

30 The gate insulating layer 202 can be formed by a sputtering method, a CVD method, a printing method, a coating method, or the like. Alternatively, the dense and high-quality gate insulating layer 202 having high withstand voltage can be formed by

high-density plasma CVD using a microwave (e.g., a frequency of 2.45 GHz), for example. When an oxide semiconductor layer and a high-quality gate insulating layer are in close contact with each other, the interface state density can be reduced and favorable interface characteristics can be obtained. In addition, since the gate insulating layer 202 formed by the high-density plasma CVD can have a uniform thickness, the gate insulating layer 202 has excellent step coverage. Further, the thickness of the gate insulating layer 202 formed by the high-density plasma CVD can be controlled precisely.

[0081]

10 Next, as illustrated in FIG. 7B, the n-type oxide semiconductor layer 203 is formed over the gate insulating layer 202. When the n-type oxide semiconductor layer 203 is formed by a printing method, an inkjet method, or the like, the number of steps can be reduced. Alternatively, the n-type oxide semiconductor layer 203 having an island shape can be formed in such a manner that an n-type oxide semiconductor layer is formed over the gate insulating layer 202 by a sputtering method, a CVD method, a coating method, a pulsed laser deposition method, or the like, and then the oxide semiconductor layer is etched with the use of a resist formed in a photolithography step as a mask.

[0082]

20 The carrier density of an oxide semiconductor layer depends on a deposition condition such as the hydrogen concentration and the oxygen concentration of a source gas and a target, a material for deposition, or composition of the material. When the hydrogen concentration of the oxide semiconductor layer is increased, or the oxygen concentration of the oxide semiconductor layer is reduced and oxygen deficiency is included, hydrogen or oxygen deficiency serving as a donor can be included in the oxide semiconductor layer and thus an n-type oxide semiconductor layer can be formed.

[0083]

Note that after formation of the oxide semiconductor layer 203, heat treatment may be performed so that the oxide semiconductor layer has a microcrystalline structure, a polycrystalline structure, or a single crystal structure. Further, an oxide semiconductor having a crystal structure with a crystal in which the c-axis is approximately parallel to a direction perpendicular to a surface can be used.

[0084]

Next, as illustrated in FIG. 7C, the first terminal 204A and the second terminal 204B serving as a source electrode and a drain electrode are formed. When the first terminal 204A and the second terminal 204B are formed by a printing method, an inkjet method, or the like, the number of steps can be reduced. Alternatively, the first terminal 204A and the second terminal 204B can be formed in such a manner that a conductive layer is formed over the gate insulating layer 202 and the oxide semiconductor layer 203 by a sputtering method, a CVD method, an evaporation method, or the like, and then the conductive layer is etched with the use of a resist formed in a photolithography method as a mask.

[0085]

Next, as illustrated in FIG. 7D, the insulating layer 205 is formed over the gate insulating layer 202, the oxide semiconductor layer 203, the first terminal 204A, and the second terminal 204B. The insulating layer 205 can be formed in a manner similar to that of the gate insulating layer 202. Next, the second gate 206 is formed over the insulating layer 205. The second gate 206 can be formed in a manner similar to that of the first gate.

[0086]

Through the above steps, the depletion type power MOSFET 101 including an n-type oxide semiconductor layer in the channel region can be manufactured. Note that in the above manufacturing steps, a layout of the second gate is changed, so that the power MOSFET 101A illustrated in FIG. 6A or the power MOSFET 101B illustrated in FIG. 6B can be manufactured.

[0087]

25 (Embodiment 3)

In this embodiment, a structure of a power MOSFET which can be used instead of the power MOSFET 101 described in Embodiment 1 and Embodiment 2 will be described with reference to FIG. 8 and FIGS. 9A and 9B.

[0088]

30 Power MOSFETs illustrated in FIG. 8 and FIGS. 9A and 9B are different from the power MOSFETs illustrated in FIGS. 6A and 6B in that a gate is not provided between the substrate 200 and an oxide semiconductor layer 213.

[0089]

In a power MOSFET 111A illustrated in FIG. 8, the n-type oxide semiconductor layer 213 is provided over the substrate 200, the first terminal 204A and the second terminal 204B formed of a conductive layer is provided so as to cover part of
5 the oxide semiconductor layer 213, a gate insulating layer 212 is provided so as to cover the oxide semiconductor layer 213, the first terminal 204A, and the second terminal 204B, and a gate 211 formed of a conductive layer is provided over the gate insulating layer 212 so as to overlap with part of one of the first terminal 204A and the second terminal 204B. That is, a region 208 is provided so that the oxide semiconductor layer
10 213 is overlapped with none of the gate 211, the first terminal 204A, and the second terminal 204B in the region 208.

[0090]

Note that as in the power MOSFET 101 described in Embodiment 2, when an insulating layer having high thermal conductivity is formed between the substrate 200
15 and the oxide semiconductor layer 213, the power MOSFET 111A having high heat resistance can be manufactured. Further, the first terminal 204A and the second terminal 204B may be provided between the substrate 200 and the oxide semiconductor layer 213. Furthermore, the region 208 may not be provided and the gate 211 may be provided so as to overlap with part of the first terminal 204A and part of the second
20 terminal 204B as in FIG. 5A.

[0091]

In a power MOSFET 111B illustrated in FIG. 9A, the first terminal 204A formed of a conductive layer is provided over the substrate 200, the n-type oxide semiconductor layer 213 is provided so as to cover the first terminal 204A formed of the
25 conductive layer, the second terminal 204B formed of a conductive layer is provided so as to cover part of the oxide semiconductor layer 213, the gate insulating layer 212 is provided so as to cover the oxide semiconductor layer 213 and the second terminal 204B, and the gate 211 formed of a conductive layer, a wiring 214 connected to the first terminal 204A, and a wiring 215 connected to the second terminal 204B are provided
30 over the gate insulating layer 212.

[0092]

FIG. 9B is a top view of the power MOSFET 111B illustrated in FIG. 9A. A

cross-sectional view taken along line A-B in FIG. 9B corresponds to FIG. 9A. As illustrated in FIG. 9B, the gate 211 is provided in the periphery of the second terminal 204B and the wiring 215 connected to the second terminal 204B. Further, the first terminal 204A and the wiring 214 connected to the first terminal 204A are provided in the periphery of the gate 211.

[0093]

That is, the first terminal 204A and the second terminal 204B do not overlap with each other. The gate 211 is provided over a region including a region which overlaps with neither the first terminal 204A nor the second terminal 204B. Further, part (an end portion) of the gate 211 may overlap with one or both of the first terminal 204A and the second terminal 204B.

[0094]

Note that as in the power MOSFET 101 described in Embodiment 2, when an insulating layer having high thermal conductivity is formed between the substrate 200, and the first terminal 204A and the oxide semiconductor layer 213, the power MOSFET 111B having high heat resistance can be manufactured.

[0095]

The oxide semiconductor layer 213 illustrated in FIG. 8 and FIGS. 9A and 9B can be formed using a material similar to the oxide semiconductor layer 203 described in Embodiment 2. Note that in the power MOSFET 111A illustrated in FIG. 8 and the power MOSFET 111B illustrated in FIGS. 9A and 9B, the gate 211 is formed on only one surface side of the oxide semiconductor layer 213. Therefore, the thickness of the oxide semiconductor layer 213 is set so that a depletion layer spreads in the channel region and the power MOSFET 111B can be turned off when negative voltage is applied to the gate 211. Since the number of gates in this embodiment is half of the number of gates of the power MOSFET 101 described in Embodiment 2, the maximum width of the depletion layer is greater than or equal to 7 nm and less than or equal to 677 nm in the case where the carrier density is higher than or equal to $1 \times 10^{16} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$. Therefore, the thickness of the n-type oxide semiconductor layer 213 can be set to greater than or equal to 7 nm and less than or equal to 677 nm. Further, the maximum width of the depletion layer is greater than or equal to 7 nm and

less than or equal to 218 nm in the case where the carrier density is higher than or equal to $1 \times 10^{17} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{20} \text{ cm}^{-3}$. In that case, the thickness of the n-type oxide semiconductor layer 213 can be set to greater than or equal to 7 nm and less than or equal to 218 nm.

5 [0096]

Note that as methods for manufacturing the power MOSFETs illustrated in FIG. 8 and FIGS. 9A and 9B, the methods for manufacturing the power MOSFETs described in Embodiment 2 can be used as appropriate in accordance with the structures illustrated in FIG. 8 and FIGS. 9A and 9B.

10 [0097]

Since each of the power MOSFETs illustrated in FIG. 8 and FIGS. 9A and 9B includes an n-type oxide semiconductor layer in the channel region, on-resistance can be reduced and a large amount of current can flow. However, since the power MOSFET including an n-type oxide semiconductor layer in a channel region is a depletion type transistor, the transistor is a normally-on transistor in which current flows
15 even in a state where voltage is not applied to its gate. The power MOSFETs described in this embodiment can be turned off when negative voltage is applied to the gate 211 and can be turned on when positive voltage is applied to the gate 211. Therefore, the power MOSFET in which on-resistance is low and a large amount of
20 current can flow can be turned off.

[0098]

(Embodiment 4)

In this embodiment, a method for manufacturing the field-effect transistors 102 to 104 described in Embodiment 1 will be described with reference to FIG. 10 and FIGS.
25 11A to 11D. Since all the field-effect transistors 102 to 104 can have the same structure, here, a description is given on the field-effect transistor 102 as an example.

[0099]

In the field-effect transistor 102 illustrated in FIG. 10, a gate 251 formed of a conductive layer is provided over a substrate 250, a gate insulating layer 252 is provided
30 over the gate 251, an i-type or substantially i-type oxide semiconductor layer 253 is provided over the gate insulating layer 252, a first terminal 254A and a second terminal 254B formed of a conductive layer are provided so as to cover part of the oxide

semiconductor layer 253, and an insulating layer 255 is provided so as to cover the oxide semiconductor layer 253, the first terminal 254A, and the second terminal 254B.

[0100]

As the substrate 250, the substrate 200 described in Embodiment 2 can be used
5 as appropriate.

[0101]

The gate 251 can be formed using any of the materials for the first gate 201 described in Embodiment 2 as appropriate.

[0102]

10 The gate insulating layer 252 can be formed using any of the materials for the gate insulating layer 202 described in Embodiment 2 as appropriate. The thickness of the gate insulating layer 252 can be greater than or equal to 50 nm and less than or equal to 500 nm. When the thickness of the gate insulating layer 252 is large, gate leakage current can be reduced.

15 [0103]

The oxide semiconductor layer 253 can be formed using the metal oxide described as the material for the oxide semiconductor layer 203 in Embodiment 2. Further, an oxide semiconductor having an amorphous structure, a polycrystalline structure, or a single crystal structure can be employed as appropriate. Furthermore, an
20 oxide semiconductor having a crystal structure with a crystal in which the c-axis is approximately parallel to a direction perpendicular to a surface can be used. Note that since the oxide semiconductor layer 253 is i-type or substantially i-type, the carrier density is lower than $5 \times 10^{14} / \text{cm}^3$, preferably lower than $1 \times 10^{12} / \text{cm}^3$, more preferably lower than or equal to $1 \times 10^{11} / \text{cm}^3$. Moreover, it is preferably that hydrogen and
25 oxygen deficiency serving as a donor be little, and the hydrogen concentration be lower than or equal to $1 \times 10^{16} / \text{cm}^3$.

[0104]

The field-effect transistor 102 which includes an i-type or substantially i-type oxide semiconductor layer in a channel region, which is purified by drastically
30 removing hydrogen and in which oxygen deficiency is reduced to satisfy the stoichiometric composition ratio, whereby the off-state current can be smaller than or

equal to 1×10^{-16} A. In other words, a circuit can be designed with the oxide semiconductor layer that can be regarded as an insulator when a field-effect transistor is in a non-conducting state. On the other hand, when the field-effect transistor is in a conducting state, the current supply capability of the oxide semiconductor layer 253 is
5 expected to be higher than the current supply capability of a semiconductor layer formed of amorphous silicon. Therefore, the field-effect transistor 102 is an enhancement type transistor, which is normally off with an extremely small leakage current in an off state; thus, the field-effect transistor 102 has excellent switching characteristics.

10 [0105]

The first terminal 254A and the second terminal 254B can be formed using the material for the first terminal 204A and the second terminal 204B in Embodiment 2 as appropriate.

[0106]

15 The insulating layer 255 is preferably formed using an oxide insulating layer. As a typical example of the oxide insulating layer, a silicon oxide layer, a silicon oxynitride layer, or an aluminum oxide layer can be given. Note that the insulating layer 205 may have a stacked structure of an oxide insulating layer and a nitride insulating layer. As a typical example of the nitride insulating layer, a silicon nitride
20 layer, a silicon nitride oxide layer, or an aluminum nitride layer can be given. In the insulating layer 255, a region in contact with the oxide semiconductor layer 253 is formed using an oxide insulating layer, whereby oxygen deficiency of the oxide semiconductor layer can be reduced and the stoichiometric composition ratio can be satisfied.

25 [0107]

Note that a structure of the field-effect transistor 102 can employ various modes without being limited to a specific structure. For example, a multi-gate structure with two or more of gates can be employed. Further, a structure where gate electrodes are provided above and below a channel region can be used. Note that
30 when gate electrodes are provided above and below a channel region, it is possible to employ a structure where two field-effect transistors are connected in parallel.

[0108]

Here, the method for manufacturing the field-effect transistor 102 illustrated in FIG. 10 will be described with reference to FIGS. 11A to 11D.

[0109]

As illustrated in FIG. 11A, the gate 251 is formed over the substrate 250.

5 Next, the gate insulating layer 252 is formed over the gate 251.

[0110]

The gate 251 can be formed by the method for manufacturing the first gate 201 described in Embodiment 2 as appropriate. The gate insulating layer 252 can be formed by the method for manufacturing the gate insulating layer 202 described in
10 Embodiment 2 as appropriate. Since an i-type or substantially i-type oxide semiconductor layer is highly sensitive to an interface state and interface charge, the gate insulating layer 252 is formed by high-density plasma CVD with the use of microwaves, so that the interface state density can be reduced and favorable interface characteristics can be obtained.

15 [0111]

Note that the substrate 200 is heated when the gate insulating layer 252 is formed, whereby hydrogen, water, a hydroxyl group, hydride, or the like contained in the gate insulating layer 252 can be reduced.

[0112]

20 In the case where the gate insulating layer 252 is formed by a sputtering method, the gate insulating layer 252 is preferably formed while hydrogen, water, a hydroxyl group, hydride, or the like remaining in a treatment chamber is removed in order that hydrogen, water, a hydroxyl group, hydride, or the like contained in the gate insulating layer 252 is reduced. An entrapment vacuum pump is preferably used for
25 removing hydrogen, water, a hydroxyl group, hydride, or the like remaining in the treatment chamber. As an example of the entrapment vacuum pump, a cryopump, an ion pump, or a titanium sublimation pump can be given. Further, a turbo pump provided with a cold trap can be used for an exhaustion unit.

[0113]

30 When the purity of a sputtering gas used for forming the gate insulating layer 252 is higher than or equal to 6N (99.9999 %), preferably higher than or equal to 7N

(99.99999 %) (that is, the impurity concentration is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm), hydrogen, water, a hydroxyl group, hydride, or the like contained in the gate insulating layer 252 can be reduced.

[0114]

5 Next, as illustrated in FIG. 11B, an oxide semiconductor layer 253A is formed over the gate insulating layer 202. The oxide semiconductor layer 253A can be formed by a printing method, an inkjet method, or the like. Alternatively, the island-shaped oxide semiconductor layer 253A can be formed in such a manner that an oxide semiconductor layer is formed over the gate insulating layer 252 by a sputtering method,
10 a CVD method, a coating method, a pulsed laser deposition method, or the like and the oxide semiconductor layer is etched with the use of a resist formed in a photolithography step as a mask.

[0115]

 The carrier density of an oxide semiconductor layer depends on a deposition
15 condition such as the hydrogen concentration and the oxygen concentration of a source gas and a target, a material for deposition, composition of the material, or a condition of heat treatment. When the hydrogen concentration of the oxide semiconductor layer is made lower, or the oxygen concentration of the oxide semiconductor layer is increased and oxygen deficiency is reduced, the oxide semiconductor layer becomes i-type or
20 substantially i-type. In this embodiment, because treatment in which the oxide semiconductor layer is processed into an i-type or substantially i-type oxide semiconductor layer is performed in a later step, the oxide semiconductor layer 253A may be either i-type or n-type.

[0116]

25 The substrate is heated in the case where the oxide semiconductor layer is formed by a sputtering method, whereby an impurity such as hydrogen, water, a hydroxyl group, or hydride contained in the oxide semiconductor layer can be reduced. Further, crystal growth can be promoted in first heat treatment.

[0117]

30 In the case where the oxide semiconductor layer is formed by a sputtering method, the relative density of the metal oxide in the metal oxide target is higher than or

equal to 80 %, preferably higher than or equal to 95 %, further preferably higher than or equal to 99.9 %, whereby the impurity concentration in the oxide semiconductor layer can be reduced; thus, a transistor having excellent electrical characteristics and high reliability can be obtained.

5 [0118]

Further, when preheat treatment is performed before formation of the oxide semiconductor layer, hydrogen, water, a hydroxyl group, hydride, or the like remaining on an inner wall of the sputtering apparatus, on a surface of the target, or in a target material can be removed, so that an impurity such as hydrogen, water, a hydroxyl group,
10 or hydride contained in the oxide semiconductor layer can be reduced.

[0119]

As in the gate insulating layer 252, before, during, or after formation of the oxide semiconductor layer, it is preferable to use an entrapment vacuum pump for removing hydrogen, water, a hydroxyl group, hydride, or the like remaining in the
15 sputtering apparatus. As a result, hydrogen, water, a hydroxyl group, hydride, or the like is evacuated, and the concentration of hydrogen, water, a hydroxyl group, hydride, or the like contained in the oxide semiconductor layer can be reduced.

[0120]

Next, first heat treatment is performed, so that an impurity such as hydrogen,
20 water, a hydroxyl group, or hydride contained in the oxide semiconductor layer 253A is removed. That is, at least dehydration or dehydrogenation can be performed. Note that oxygen deficiency in the oxide semiconductor layer 253A is also formed in the first heat treatment. In FIG. 11C, the oxide semiconductor layer from which an impurity such as hydrogen, water, a hydroxyl group, or hydride is removed by the first heat
25 treatment is referred to as an oxide semiconductor layer 253B.

[0121]

The temperature of the first heat treatment is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. A heat treatment apparatus used for the first heat
30 treatment is not limited to a particular apparatus, and the apparatus may be provided with a device for heating an object to be processed by heat radiation or heat conduction

from a heating element such as a resistance heating element. For example, an electric furnace, or a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by
5 radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas.

[0122]

10 It is preferable that in the first heat treatment, hydrogen, water, a hydroxyl group, hydride, or the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. Alternatively, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is preferably higher than or equal to
15 6N (99.9999 %), more preferably higher than or equal to 7N (99.99999 %) (that is, the impurity concentration is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm).

[0123]

Further, in the first heat treatment, an atmosphere inside the furnace may be a nitrogen atmosphere at the time of increasing the temperature and the atmosphere may
20 be switched to an oxygen atmosphere at the time of performing cooling. When the atmosphere is switched to an oxygen atmosphere after dehydration or dehydrogenation in a nitrogen atmosphere, oxygen can be supplied into the oxide semiconductor layer, the hydrogen concentration can be reduced, and oxygen can be supplied to oxygen deficiency in the oxide semiconductor layer, whereby an i-type or substantially i-type
25 oxide semiconductor layer can be formed.

[0124]

Further, depending on the conditions of the first heat treatment or the material of the oxide semiconductor layer, the oxide semiconductor layer 253A might be crystallized to be an oxide semiconductor layer including crystals. For example, an
30 oxide semiconductor layer including crystals with a crystallinity of 90 % or higher, or 80 % or higher, is formed in some cases.

[0125]

Depending on the conditions of the first heat treatment or the materials of the oxide semiconductor layer, the oxide semiconductor layer has a crystal structure with a crystal in which the c-axis is approximately parallel to a direction perpendicular to a surface is formed over a surface portion of an amorphous oxide semiconductor layer in some cases.

[0126]

Note that the first heat treatment may be performed after the first terminal and the second terminal are formed over the oxide semiconductor layer.

[0127]

Here, the substrate is introduced into an electric furnace and the heat treatment is performed in an inert gas atmosphere such as nitrogen or a rare gas at 450 °C for one hour.

[0128]

Next, as illustrated in FIG. 11C, the first terminal 254A and the second terminal 254B which serve as a source electrode and a drain electrode are formed.

[0129]

The first terminal 254A and the second terminal 254B can be formed in a manner similar to that of the first terminal 204A and the second terminal 204B described in Embodiment 2.

[0130]

Next, as illustrated in FIG. 11D, the insulating layer 255 is formed over the gate insulating layer 252, the oxide semiconductor layer 253B, the first terminal 254A, and the second terminal 254B. The insulating layer 255 can be formed by a sputtering method, a CVD method, a printing method, a coating method, or the like. Note that when a silicon oxide layer is formed by a sputtering method as the insulating layer 255, oxygen can be supplied from the silicon oxide layer to the oxygen deficiency which is generated in the first heat treatment and included in the oxide semiconductor layer 253A; thus, oxygen deficiency serving as a donor can be reduced and a structure satisfying the stoichiometric composition ratio can be obtained. As a result, the i-type or substantially i-type oxide semiconductor layer 253 can be formed.

[0131]

Next, second heat treatment (preferably, at higher than or equal to 200 °C and lower than or equal to 400 °C, for example, at higher than or equal to 250 °C and lower than or equal to 350 °C) is performed in an inert gas atmosphere or in an oxygen gas atmosphere. The second heat treatment may be performed after a protective insulating layer or a planarization insulating layer is formed over the insulating layer 255. By this heat treatment, oxygen can be supplied from the insulating layer 255 formed using an oxide insulating layer to the oxygen deficiency which is generated in the first heat treatment and included in the oxide semiconductor layer; thus, oxygen deficiency serving as a donor can be reduced and a structure satisfying the stoichiometric composition ratio can be obtained. As a result, the more i-type or substantially i-type oxide semiconductor layer 253 can be formed.

[0132]

In this embodiment, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour.

15 [0133]

Further, heat treatment may be performed in air at higher than or equal to 100 °C and lower than or equal to 200 °C for longer than or equal to 1 hour and shorter than or equal to 30 hours. Reliability of a field-effect transistor can be increased by the heat treatment.

20 [0134]

Through the above steps, the enhancement type field-effect transistor 102 can be manufactured which includes an i-type or substantially i-type oxide semiconductor layer in a channel region and has extremely small off-state current.

[0135]

25 (Embodiment 5)

FIG. 12 is one embodiment of a semiconductor device in which the power element described in any of Embodiments 1 to 3 is used for a protective element. The protective element functions so that current flows through the power element which is a protective element and overcurrent does not flow through a circuit to be protected when overvoltage is input to a power source terminal. The circuit to be protected includes any circuit with low withstand voltage which is broken by application of overvoltage.

30

In this embodiment, as an example of a power element, description will be given with the use of the power MOSFET having four terminals described in Embodiments 1 and 2.

[0136]

5 FIG. 12 is a semiconductor device including a power MOSFET 501, a control circuit 502, a circuit 503 to be protected, an input terminal 504, and an output terminal 505. The control circuit 502 controls operation of the power MOSFET 501 serving as a protective element by detecting overvoltage applied to the input terminal 504 or the output terminal 505.

10 [0137]

FIG. 13 is a detailed diagram of the control circuit 502. The control circuit 502 includes an overvoltage detection circuit 511, an inverter 512, a positive power source 513, switch transistors 514, 515, and 516, a capacitor 517, a negative voltage generation circuit 518, an oscillator circuit 519, a divider circuit 520, a delay circuit 521, and an AND circuit 522. The positive power source 513 corresponds to the high voltage generation source 108 in Embodiment 1. The switch transistors 514, 515, and 516 correspond to the field-effect transistors 102, 103, and 104 in Embodiment 1, respectively. The capacitor 517 corresponds to the capacitor 105 in Embodiment 1. The negative voltage generation circuit 518 corresponds to the low voltage generation source 109 in Embodiment 1. The oscillator circuit 519, the divider circuit 520, the delay circuit 521, and the AND circuit 522 correspond to the refresh control circuit 107 in Embodiment 1. Note that the structure of the control circuit 502 is not limited to this structure.

[0138]

25 Next, operation of the control circuit 502 and the power MOSFET 501 in FIG. 13 will be described. The overvoltage detection circuit 511 is a circuit which operates in the case where overvoltage which exceeds normal power supply voltage is input to the input terminal 504. In this embodiment, the overvoltage detection circuit 511 has a function of outputting a pulse having a high potential in the case where overvoltage is input.

30

[0139]

An output terminal of the overvoltage detection circuit 511 is connected to a

gate terminal of the switch transistor 514 and an input terminal of the inverter 512. An output terminal of the inverter 512 is connected to a gate terminal of the switch transistor 515. Thus, when overvoltage is input, the switch transistor 514 is turned on, a gate terminal of the power MOSFET 501 is connected to the positive power source 513, and the power MOSFET 501 is turned on. Accordingly, current flows from the input terminal 504 to the output terminal 505, and overvoltage is prevented from flowing through the circuit 503 to be protected in FIG. 12.

[0140]

When overvoltage is not applied, output from the overvoltage detection circuit 511 is low; therefore, the switch transistor 514 is off state and the switch transistor 515 is on state. The negative voltage generation circuit 518 includes a charge pump circuit in FIG. 17 and the like to generate negative voltage.

[0141]

Since the protective circuit does not frequently operate, it is not appropriate to constantly feed a large amount of current in terms of power consumption. Accordingly, it is effective in terms of reduction in power consumption that the capacitor 517 is charged with the use of a small electric capacity. Therefore, power consumption can be reduced in such a manner that the capacitor 517 is intermittently charged by the negative voltage generation circuit 518 through the switch transistor 516.

[0142]

A signal in which an oscillation signal generated in the oscillator circuit 519 is divided by the divider circuit 520, and the divided signal is supplied to a gate terminal of the switch transistor 516. That is, one of output terminals of the divider circuit 520 is connected to a first input terminal of the AND circuit 522. The other of the output terminals of the divider circuit 520 is connected to a second input terminal of the AND circuit 522 through the delay circuit 521. Thus, a pulse which has a pulse width equivalent to delayed time of the delay circuit 521 and a cycle similar to output of the divider circuit 520 can be obtained. With the use of the pulse, the gate terminal of the switch transistor 516 can be controlled.

[0143]

As the oscillator circuit 519, a general oscillator circuit such as a ring oscillator can be used, but it is not limited thereto. Further, a flip-flop can be used for the divider

circuit 520. As the delay circuit 521, a circuit using an inverter, a circuit using a CR delay circuit, or the like can be used, but it is not particularly limited thereto. Furthermore, a pulse can be generated by other methods.

[0144]

5 Thus, negative voltage is held in the capacitor 517, and when overvoltage is not applied, the negative voltage is applied to the power MOSFET 501 through the switch transistor 515. The power MOSFET 501 is in an off state during the negative voltage is applied to the gate terminal of the power MOSFET 501; accordingly, current does not flow.

10 [0145]

FIG. 14 is a semiconductor device in which a power MOSFET and a circuit to be protected are connected in series. Unlike FIG. 12, a power MOSFET 601 is turned off and application of overvoltage to a circuit 603 to be protected is prevented when overvoltage is applied to an input terminal.

15 [0146]

The semiconductor device shown in FIG. 14 includes a power MOSFET 601, a control circuit 602, a circuit 603 to be protected, an input terminal 604, and an output terminal 605. The control circuit 602 controls the power MOSFET 601 serving as a protective element by detecting overvoltage applied to the input terminal 604 or the

20

output terminal 605.

[0147]

FIG. 15 is a detailed diagram of the control circuit 602. The control circuit 602 includes an overvoltage detection circuit 611, an inverter 612, a positive power source 613, switch transistors 614, 615, and 616, a capacitor 617, a negative voltage generation circuit 618, an oscillator circuit 619, a divider circuit 620, a delay circuit 621, and an AND circuit 622. The positive power source 613 corresponds to the high voltage generation source 108 in Embodiment 1. The switch transistors 614, 615, and 616 correspond to the field-effect transistors 103, 102, and 104 in Embodiment 1, respectively. The capacitor 617 corresponds to the capacitor 105 in Embodiment 1.

25

30 The negative voltage generation circuit 618 corresponds to the low voltage generation source 109 in Embodiment 1. The oscillator circuit 619, the divider circuit 620, the delay circuit 621, and the AND circuit 622 correspond to the refresh control circuit 107

in Embodiment 1. Note that the structure of the control circuit 602 is not limited to this structure.

[0148]

Next, operation of the control circuit 602 and the power MOSFET 601 in FIG. 5 15 will be described. The overvoltage detection circuit 611 is a circuit which operates in the case where overvoltage which exceeds normal power supply voltage is input to the input terminal 604. In this embodiment, the overvoltage detection circuit 611 has a function of outputting a pulse having a high potential in the case where overvoltage is input in this embodiment.

10 [0149]

An output terminal of the overvoltage detection circuit 611 is connected to a gate terminal of the switch transistor 615 and the inverter 612. An output terminal of the inverter 612 is connected to a gate terminal of the switch transistor 614. Thus, when overvoltage is input to the input terminal 604, the switch transistor 615 is turned on, a gate terminal of the power MOSFET 601 is connected to the negative voltage generation circuit 618, and the power MOSFET 601 is turned off. Accordingly, the input terminal 604 and the circuit 603 to be protected are disconnected, and overvoltage is prevented from flowing through the circuit 603 to be protected. The negative voltage generation circuit 618 includes a charge pump circuit in FIG. 17 and the like to generate negative voltage.

20

[0150]

When overvoltage is not applied, output of the overvoltage detection circuit 611 is low; therefore, the switch transistor 615 is off, the switch transistor 614 is on, and the gate terminal of the power MOSFET 601 is connected to the capacitor 617. Since positive voltage from a positive power source is held in the capacitor 617 to be described later, the power MOSFET 601 is in on state.

25

[0151]

Since the protective circuit does not frequently operate, it is not appropriate to constantly feed a large amount of current in terms of power consumption. Accordingly, it is effective in terms of reduction in power consumption that the capacitor 617 is charged with a small electric capacity. Therefore, power consumption can be reduced in such a manner that the capacitor 617 is intermittently charged by the positive power

30

source 613 through the switch transistor 616.

[0152]

A signal in which an oscillation signal generated in the oscillator circuit 619 is divided by the divider circuit 620, and the divided signal is supplied to a gate terminal of the switch transistor 616. That is, one of output terminals of the divider circuit 620 is connected to a first input terminal of the AND circuit 622. The other of the output terminals of the divider circuit 620 is connected to a second input terminal of the AND circuit 622 through the delay circuit 621. Thus, a pulse which has a pulse width equivalent to delayed time of the delay circuit 621 and a cycle similar to output of the divider circuit 620 can be obtained. With the use of the pulse, the gate terminal of the switch transistor 616 can be controlled.

[0153]

As the oscillator circuit 619, a general oscillator circuit such as a ring oscillator can be used, but it is not limited thereto. Further, a flip-flop can be used for the divider circuit 620. As the delay circuit 621, a circuit using an inverter, a circuit using a CR delay circuit, or the like can be used, but it is not particularly limited thereto. Furthermore, a pulse can be generated by other methods.

[0154]

Thus, positive voltage is held in the capacitor 617, and when overvoltage is not applied, the positive voltage is applied to the power MOSFET 601 through the switch transistor 614. The power MOSFET 601 is in an on state during the positive voltage is applied to the gate terminal of the power MOSFET 601; accordingly, the input terminal 604 and the circuit 603 to be protected in FIG. 14 are connected to each other.

[0155]

FIG. 16 is an example of structures of the overvoltage detection circuits 511 and 611. In FIG. 16, a diode chain in which transistors 701 to 705 are diode-connected, a transistor 707, a resistor 706, and an inverter 708 are included. When the diode chain includes n transistors connected in series and the threshold voltage of a transistor is V_{th} , n is set so that normal operation voltage $< nV_{th}$ is satisfied. The transistors 701 to 705 are turned on when overvoltage is applied, and thus current flows through the diode chain. When the transistor 705 is turned on, the transistor 707 is also turned on and a high potential is output from an output of the inverter 708.

[0156]

In this embodiment, a normally-on power MOSFET which includes an oxide semiconductor layer with a wide band gap in a channel region is used as a protective element; thus, destruction of a semiconductor device due to application of overvoltage
5 can be prevented.

[0157]

(Embodiment 6)

In this embodiment, applications of the power device described in the above embodiments will be described. The semiconductor device which is the power device
10 described in the above embodiments can be used, for example, for a protective circuit of a battery in an electronic device such as a computer display that can display images; and a protective circuit of a battery provided for an electromagnetic cooker or a vehicle (e.g., a bicycle) that is driven with power from a fixed power source.

[0158]

15 Application examples of a semiconductor device which is a power device functioning as a protective circuit will be described with reference to FIGS. 18A to 18C.

[0159]

FIG. 18A illustrates an electromagnetic cooker 1000 as an application example of a semiconductor device serving as a protective circuit. The electromagnetic cooker
20 1000 heats cookware and the like by using electromagnetic induction generated by current flowing through a coil unit 1001. The electromagnetic cooker 1000 includes a battery 1002 for supplying current that is to flow through the coil unit 1001, a semiconductor device 1003 serving as a protective circuit, and a solar battery 1004 for charging the battery 1002. Although the solar battery 1004 is illustrated as a means to
25 charge the battery 1002 in FIG. 18A, the battery 1002 may be charged by another means. The semiconductor device 1003 serving as a protective circuit can reduce application of overvoltage to the battery 1002 and thus, it is possible to reduce power consumption when the protective circuit is not operated.

[0160]

30 FIG. 18B illustrates an electric bicycle 1010 as an application example of a semiconductor device serving as a protective circuit. The electric bicycle 1010 obtains power when current flows through a motor unit 1011. The electric bicycle 1010

includes a battery 1012 for supplying current that is to flow through the motor unit 1011 and a semiconductor device 1013 serving as a protective circuit. Although a means to charge the battery 1012 is not particularly illustrated in FIG. 18B, the battery 1012 may be charged by an electric generator or the like that is additionally provided. The semiconductor device 1013 serving as a protective circuit can reduce application of overvoltage to the battery 1012 in charging and thus, it is possible to reduce power consumption when the protective circuit is not operated. Note that although a pedal is illustrated in FIG. 18B, the pedal is not necessarily provided.

[0161]

10 FIG. 18C illustrates an electric car 1020 as an application example of a semiconductor device serving as a protective circuit. The electric car 1020 obtains power when current flows through a motor unit 1021. Moreover, the electric car 1020 includes a battery 1022 for supplying current that is to flow through the motor unit 1021 and a semiconductor device 1023 serving as a protective circuit. Although a means to charge the battery 1022 is not particularly illustrated in FIG. 18C, the battery 1022 may be charged by an electric generator or the like that is additionally provided. The semiconductor device 1023 serving as a protective circuit can reduce application of overvoltage to the battery 1022 in charging and thus, it is possible to reduce power consumption when the protective circuit is not operated.

20 [0162]

Note that in this embodiment, what is described in this embodiment with reference to the drawings can be freely combined with or replaced with what is described in other embodiments as appropriate.

25 This application is based on Japanese Patent Application serial no. 2010-012627 filed with Japan Patent Office on January 22, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a first voltage generation source;

5 a first transistor comprising a first gate, a first terminal connected to the first voltage generation source, and a second terminal;

a second transistor comprising a second gate, a third terminal connected to the second terminal, and a fourth terminal;

10 a power element comprising a third transistor comprising a third gate connected to the second terminal and the third terminal, a fifth terminal, and a sixth terminal;

a fourth transistor comprising a fourth gate, a seventh terminal connected to the fourth terminal, and a eighth terminal; and

a second voltage generation source connected to the eighth terminal;

15 a capacitor connected to the fourth terminal and the seventh terminal,

wherein the power element is provided so that current flows between the fifth terminal and the sixth terminal when voltage is not applied to the third gate.

2. The semiconductor device according to claim 1, wherein the third transistor
20 further comprises a fifth gate connected to the second terminal, the third terminal, and the third gate.

3. The semiconductor device according to claim 1,

25 wherein the first voltage generation source is a positive voltage generation source, and

wherein the second voltage generation source is a negative voltage generation source.

4. The semiconductor device according to claim 1,

30 wherein the first voltage generation source is a negative voltage generation circuit, and

wherein the second voltage generation source is a positive voltage generation

circuit.

5 5. The semiconductor device according to claim 1, wherein current does not flow in each of the first transistor, the second transistor, and the fourth transistor when voltage is not applied to each of the first gate, the second gate, and the fourth gate, respectively.

6. The semiconductor device according to claim 1, wherein the third transistor comprises:

10 the third gate;
a first insulating layer over the third gate;
an oxide semiconductor layer over the first insulating layer; and
the fifth terminal and the sixth terminal over the oxide semiconductor layer.

15 7. The semiconductor device according to claim 6, wherein the third transistor further comprises:

a second insulating layer over the fifth terminal and the sixth terminal, and
a fifth gate over the third gate with the second insulating layer interposed therebetween.

20 8. The semiconductor device according to claims 7, wherein the fifth gate partly overlaps the fifth terminal and does not overlap the sixth terminal.

25 9. The semiconductor device according to claim 7, wherein the fifth gate does not overlap the fifth terminal and the sixth terminal.

10. The semiconductor device according to claim 1, wherein the third transistor comprises:

30 the fifth terminal;
an oxide semiconductor layer over the fifth terminal;
the sixth terminal over the oxide semiconductor layer;
an insulating layer over the sixth terminal; and

the third gate over the insulating layer,
wherein the third gate is provided in a region between the fifth terminal and the sixth terminal.

5 11. A semiconductor device comprising:
a first voltage generation source;
a first transistor comprising a first gate, a first terminal connected to the first
voltage generation source, and a second terminal;
a second transistor comprising a second gate, a third terminal connected to the
10 second terminal, and a fourth terminal;
a power element comprising a third transistor comprising a third gate
connected to the second terminal and the third terminal, a fifth terminal, and a sixth
terminal; and
a second voltage generation source connected to the fourth terminal;
15 an overvoltage detection circuit connected to the first gate and the second gate,
wherein the power element is provided so that current flows between the fifth
terminal and the sixth terminal when voltage is not applied to the third gate.

20 12. The semiconductor device according to claim 11, wherein the third
transistor further comprises a fourth gate connected to the second terminal, the third
terminal, and the third gate.

25 13. The semiconductor device according to claim 11, further comprising:
a fourth transistor comprising a fourth gate, a seventh terminal, and a eighth
terminal; and
a capacitor,
wherein the seventh terminal is connected to the fourth terminal and the
capacitor,
wherein the eighth terminal is connected to the second voltage generation
30 source, and
wherein the fourth terminal is connected to the second voltage generation
source through the fourth transistor.

14. The semiconductor device according to claim 11,
wherein the first voltage generation source is a positive voltage generation
source, and

5 wherein the second voltage generation source is a negative voltage generation
source.

15. The semiconductor device according to claim 11,
wherein the first voltage generation source is a negative voltage generation
10 circuit, and

 wherein the second voltage generation source is a positive voltage generation
circuit.

16. The semiconductor device according to claim 11, further comprising an
15 inverter,

 wherein the second gate is connected to the overvoltage detection circuit
through the inverter.

17. The semiconductor device according to claim 11, wherein current does not
20 flow in each of the first transistor and the second transistor when voltage is not applied
to each of the first gate and the second gate, respectively.

18. The semiconductor device according to claim 11, wherein the third
transistor comprises:

25 the third gate;
 a first insulating layer over the third gate;
 an oxide semiconductor layer over the first insulating layer; and
 the fifth terminal and the sixth terminal over the oxide semiconductor layer.

19. The semiconductor device according to claim 18, wherein the third
30 transistor further comprises:

 a second insulating layer over the fifth terminal and the sixth terminal, and

a fifth gate over the third gate with the second insulating layer interposed therebetween.

20. The semiconductor device according to claims 19, wherein the fifth gate
5 partly overlaps the fifth terminal and does not overlap the sixth terminal.

21. The semiconductor device according to claim 19, wherein the fifth gate does not overlap the fifth terminal and the sixth terminal.

10 22. The semiconductor device according to claim 11, wherein the third transistor comprises:

the fifth terminal;

an oxide semiconductor layer over the fifth terminal;

the sixth terminal over the oxide semiconductor layer;

15 an insulating layer over the sixth terminal; and

the third gate over the insulating layer,

wherein the third gate is provided in a region between the fifth terminal and the sixth terminal.

20 23. A semiconductor device comprising:

a first voltage generation source;

a first transistor comprising a first gate, a first terminal connected to the first voltage generation source, and a second terminal;

25 a second transistor comprising a second gate, a third terminal connected to the second terminal, and a fourth terminal;

a power element comprising a third transistor comprising a third gate connected to the second terminal and the third terminal, a fifth terminal, and a sixth terminal;

30 a fourth transistor comprising a fourth gate, a seventh terminal connected to the fourth terminal, and an eighth terminal;

a capacitor connected to the fourth terminal and the seventh terminal;

a second voltage generation source connected to the eighth terminal;

an overvoltage detection circuit connected to the first gate and the second gate;
and

a refresh control circuit connected to the fourth gate,

wherein the power element is provided so that current flows between the fifth
5 terminal and the sixth terminal when voltage is not applied to the third gate.

24. The semiconductor device according to claim 23, wherein the third
transistor further comprises a fifth gate connected to the second terminal, the third
terminal, and the third gate.

10

25. The semiconductor device according to claim 23,

wherein the first voltage generation source is a positive voltage generation
source, and

wherein the second voltage generation source is a negative voltage generation
15 source.

26. The semiconductor device according to claim 23,

wherein the first voltage generation source is a negative voltage generation
circuit, and

20 wherein the second voltage generation source is a positive voltage generation
circuit.

27. The semiconductor device according to claim 23, further comprising an
inverter,

25 wherein the second gate is connected to the overvoltage detection circuit
through the inverter.

28. The semiconductor device according to claim 23, wherein current does not
flow in each of the first transistor, the second transistor, and the fourth transistor when
30 voltage is not applied to each of the first gate, the second gate, and the fourth gate,
respectively.

29. The semiconductor device according to claim 23, wherein the refresh control circuit comprises:

an oscillator circuit;

a divider circuit connected to the oscillator circuit;

5 a delay circuit connected to the divider circuit; and

an AND circuit comprising a first input terminal, a second input terminal, and an output terminal,

wherein the first input terminal is connected to the divider circuit,

wherein the second input terminal is connected to the delay circuit, and

10 wherein the output terminal is connected to the fourth gate.

30. The semiconductor device according to claim 23, wherein the third transistor comprises:

the third gate;

15 a first insulating layer over the third gate;

an oxide semiconductor layer over the first insulating layer; and

the fifth terminal and the sixth terminal over the oxide semiconductor layer.

31. The semiconductor device according to claim 30, wherein the third transistor further comprises:

20 a second insulating layer over the fifth terminal and the sixth terminal; and

a fifth gate over the third gate with the second insulating layer interposed therebetween.

32. The semiconductor device according to claims 31, wherein the fifth gate partly overlaps the fifth terminal and does not overlap the sixth terminal.

33. The semiconductor device according to claim 31, wherein the fifth gate does not overlap the fifth terminal and the sixth terminal.

30

34. The semiconductor device according to claim 1, wherein the third transistor comprises:

the fifth terminal;
an oxide semiconductor layer over the fifth terminal;
the sixth terminal over the oxide semiconductor layer;
an insulating layer over the sixth terminal; and
5 the third gate over the insulating layer,
wherein the third gate is provided in a region between the fifth terminal and the
sixth terminal.

FIG. 1

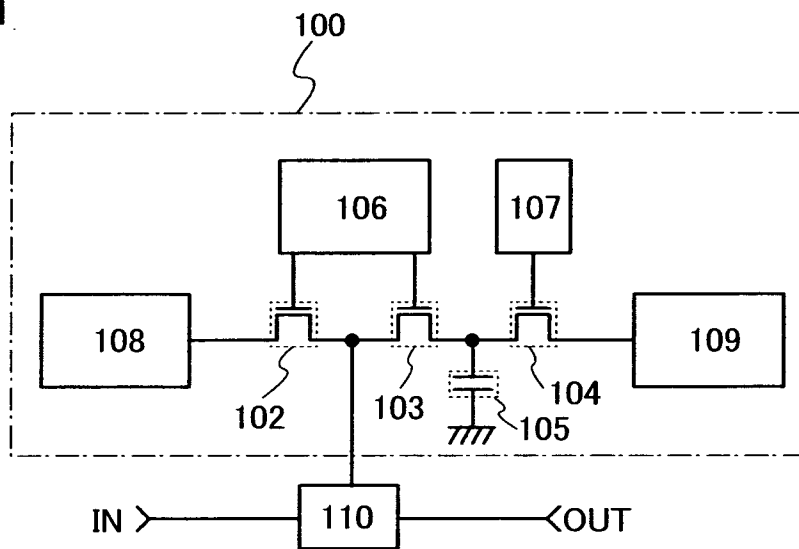


FIG. 2A

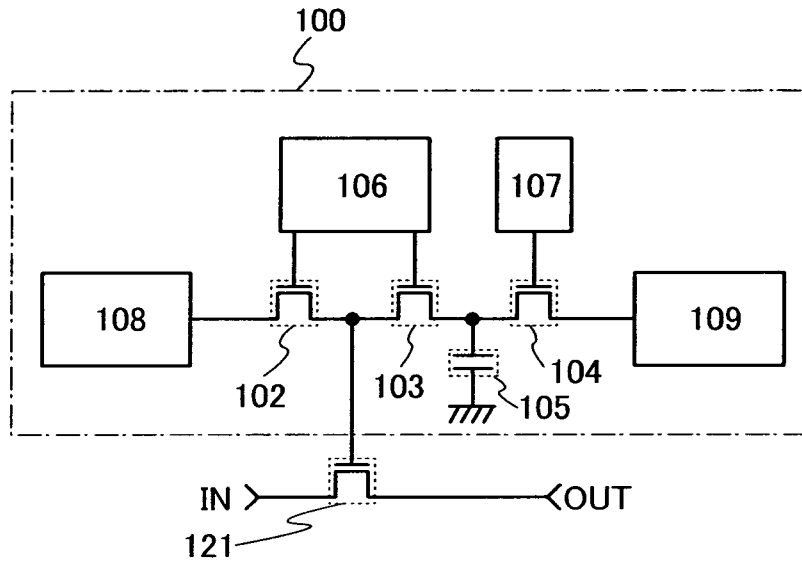


FIG. 2B

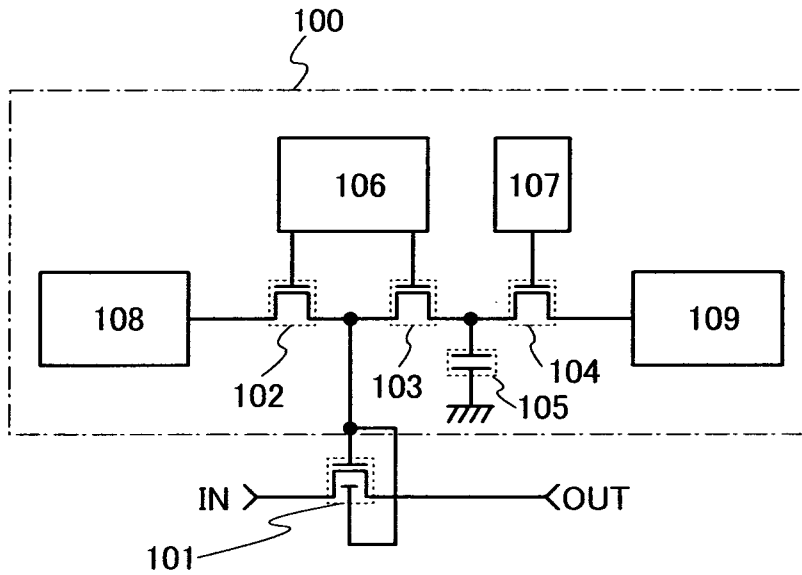


FIG. 2C

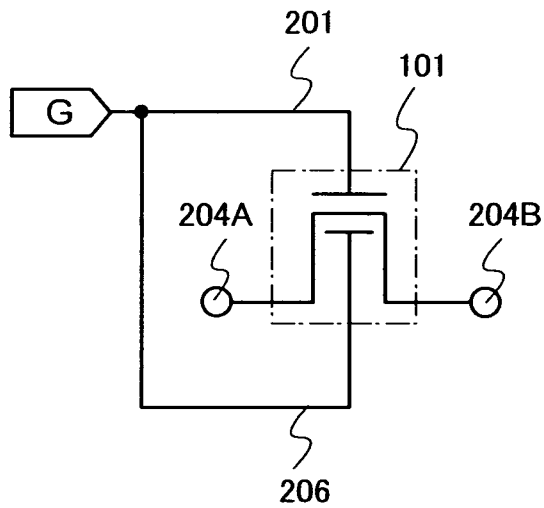


FIG. 3A

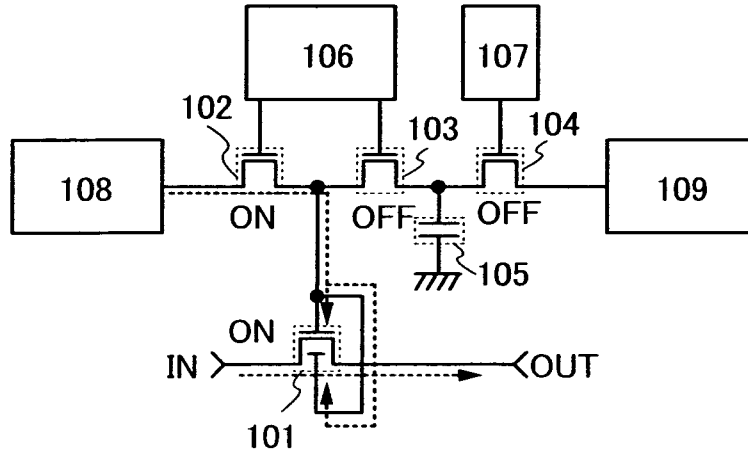


FIG. 3B

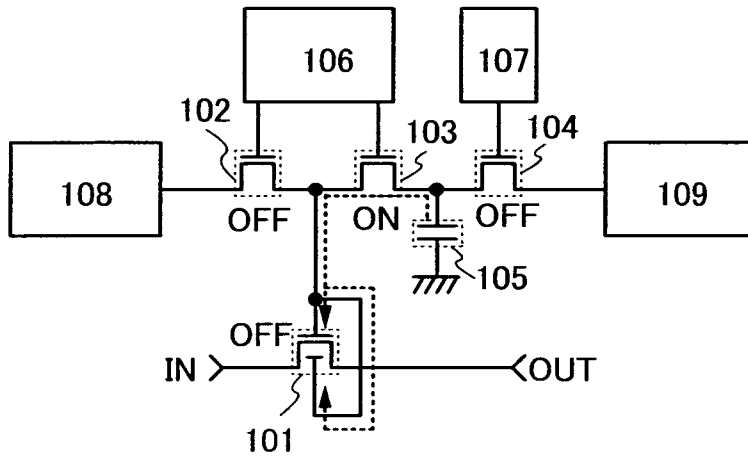


FIG. 3C

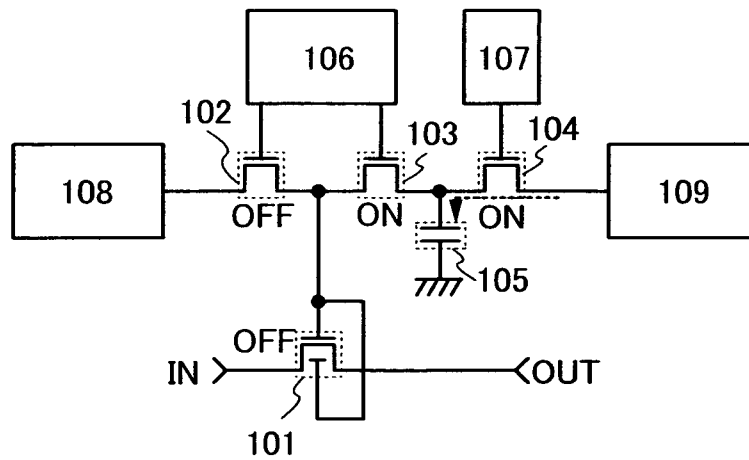


FIG. 4A

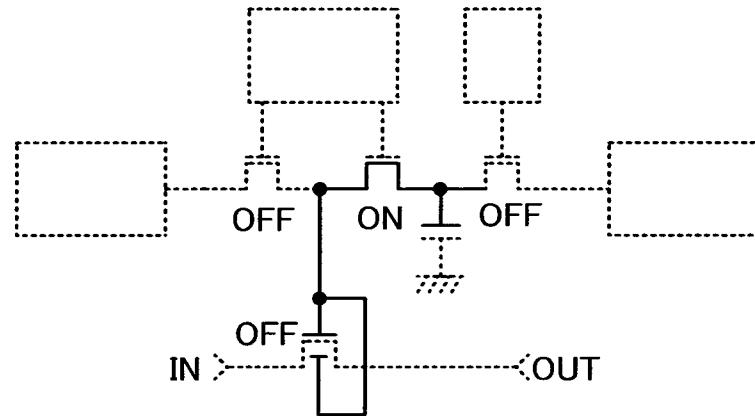


FIG. 4B

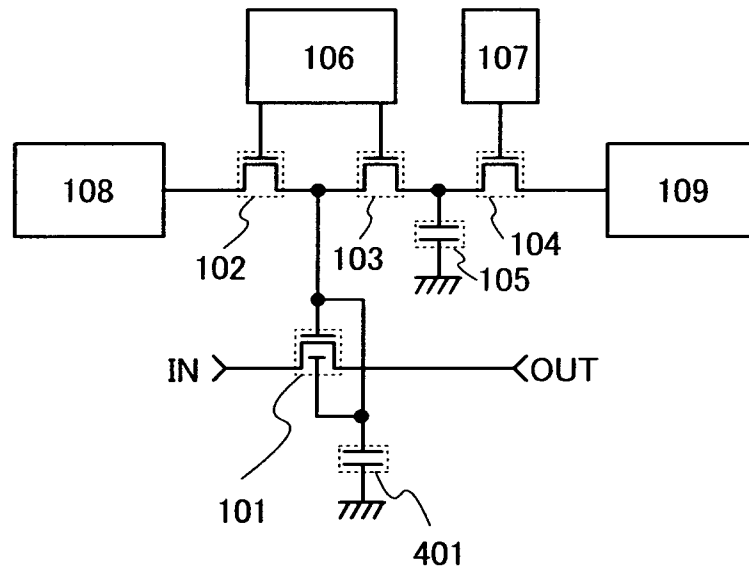


FIG. 5A

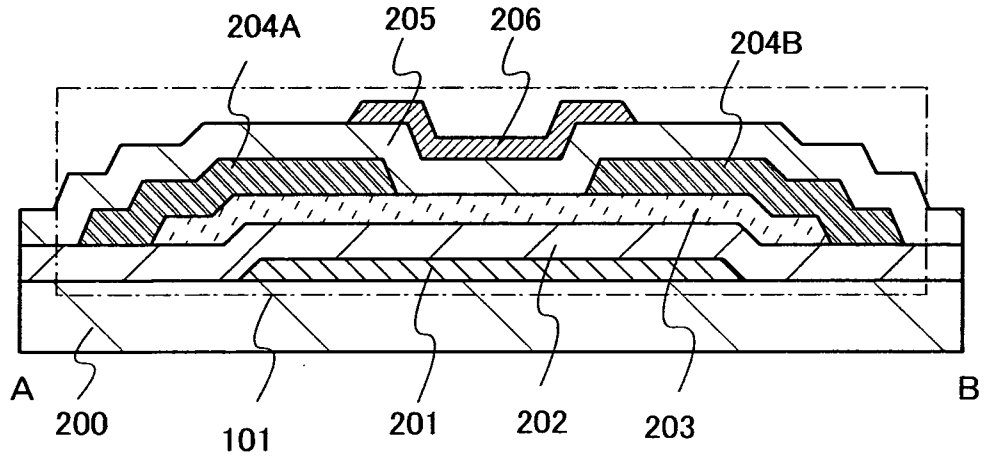


FIG. 5B

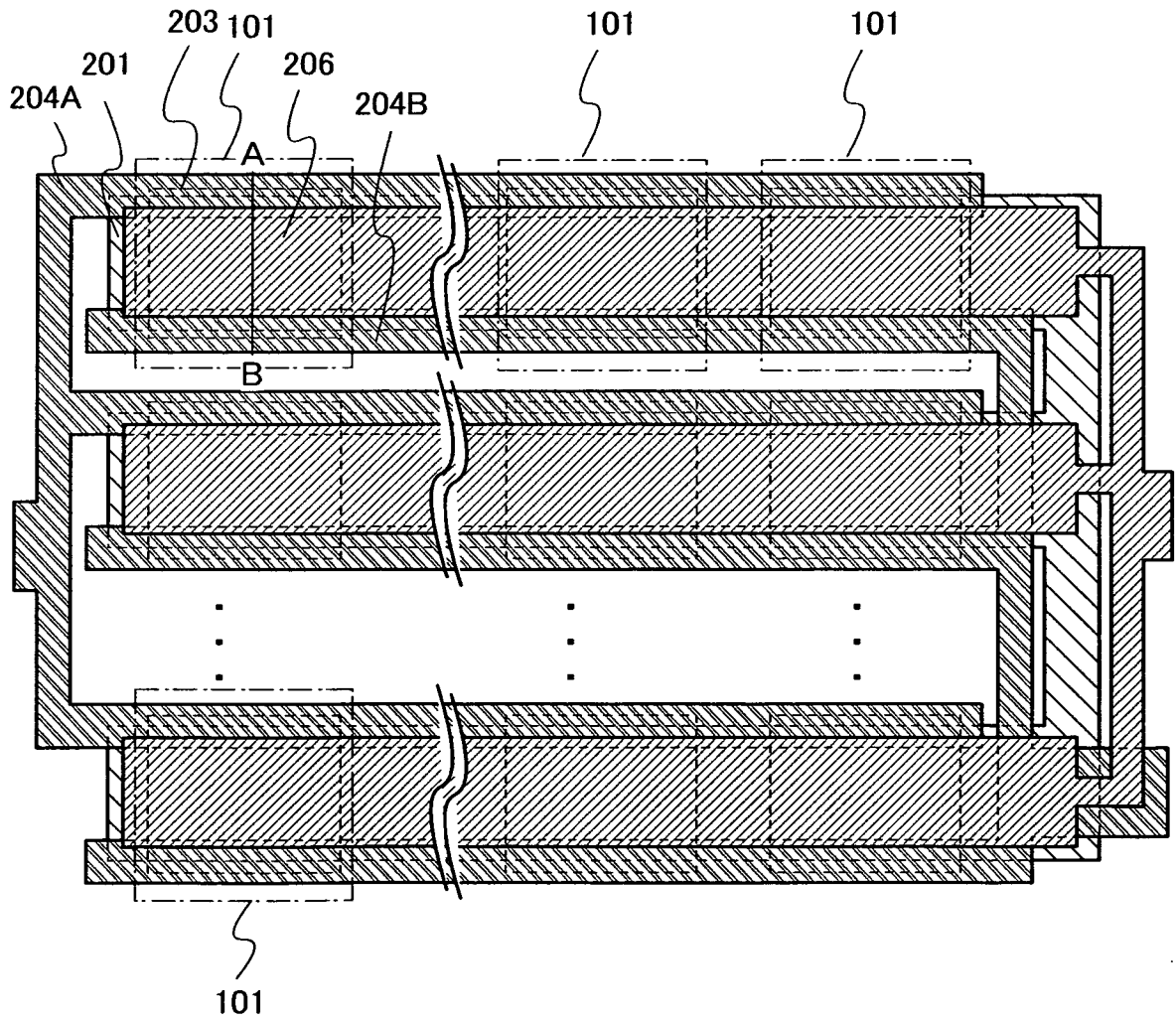


FIG. 6A

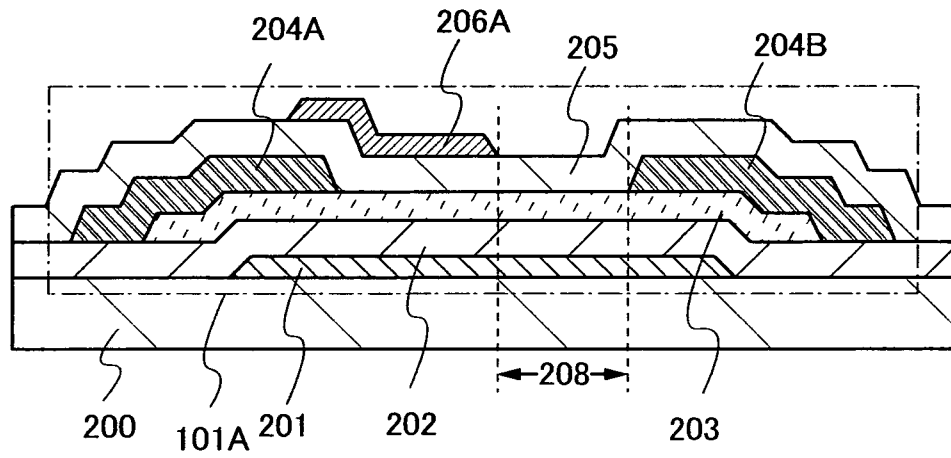


FIG. 6B

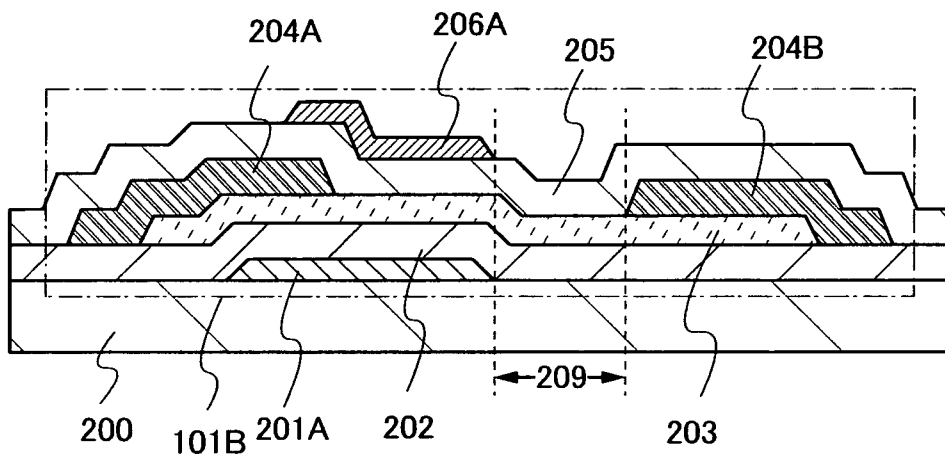


FIG. 7A

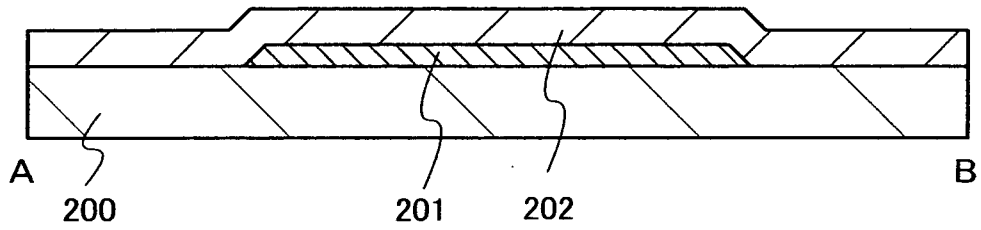


FIG. 7B

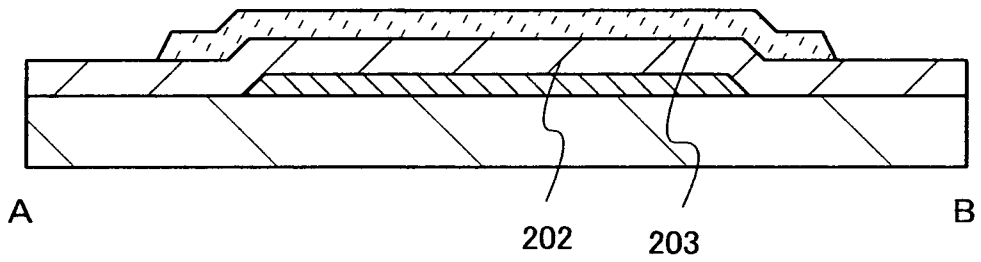


FIG. 7C

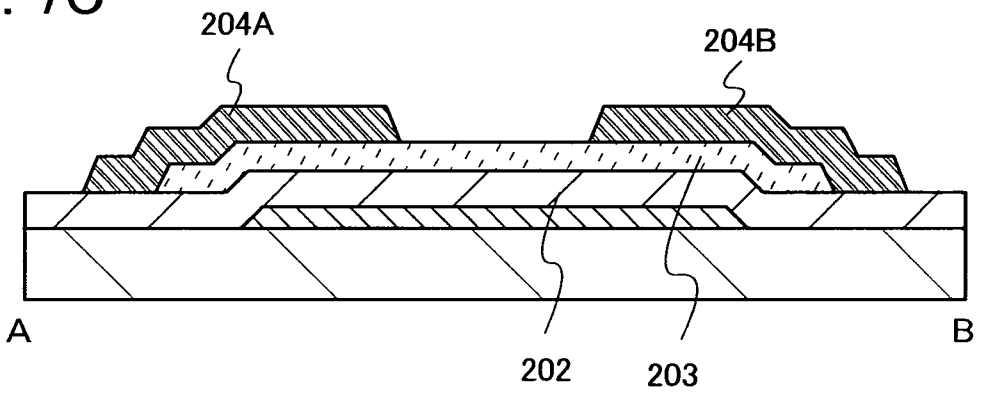


FIG. 7D

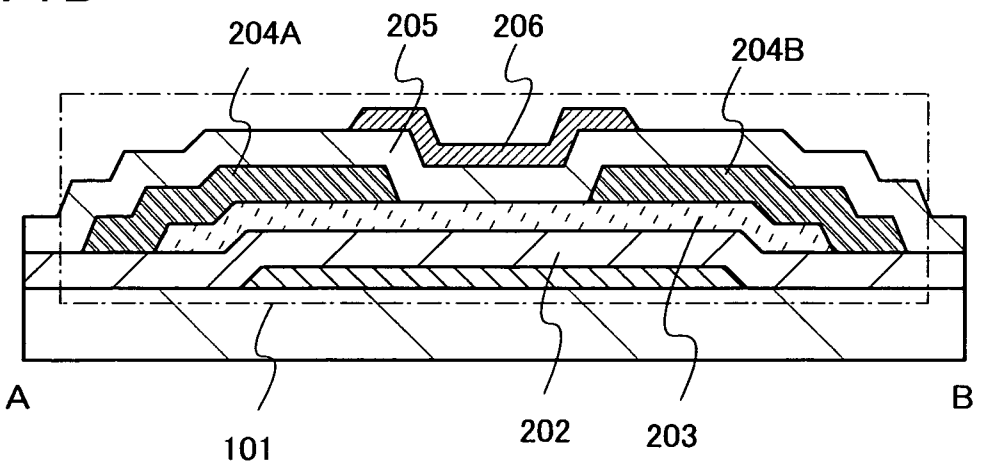


FIG. 8

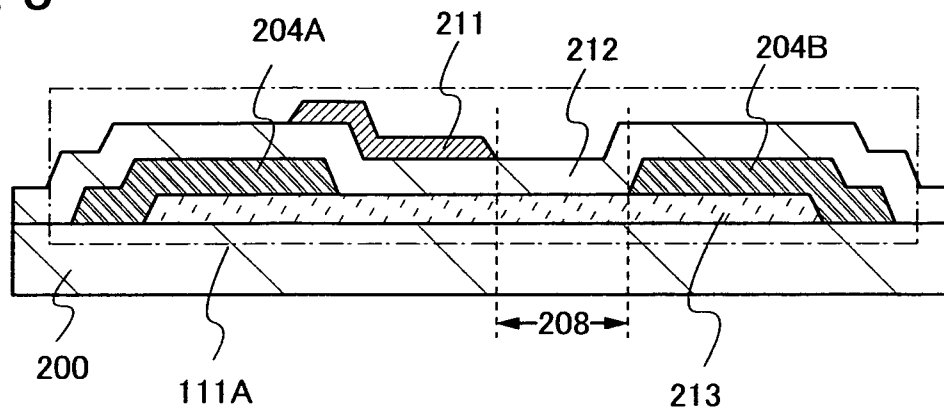


FIG. 9A

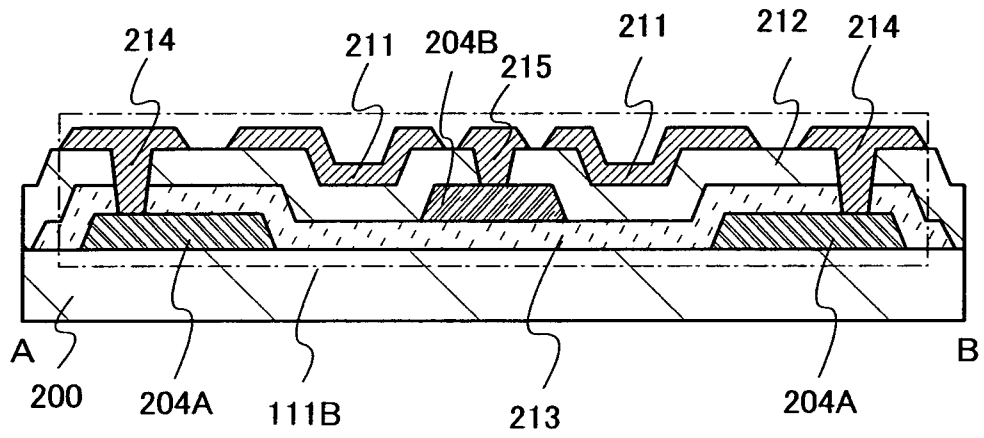


FIG. 9B

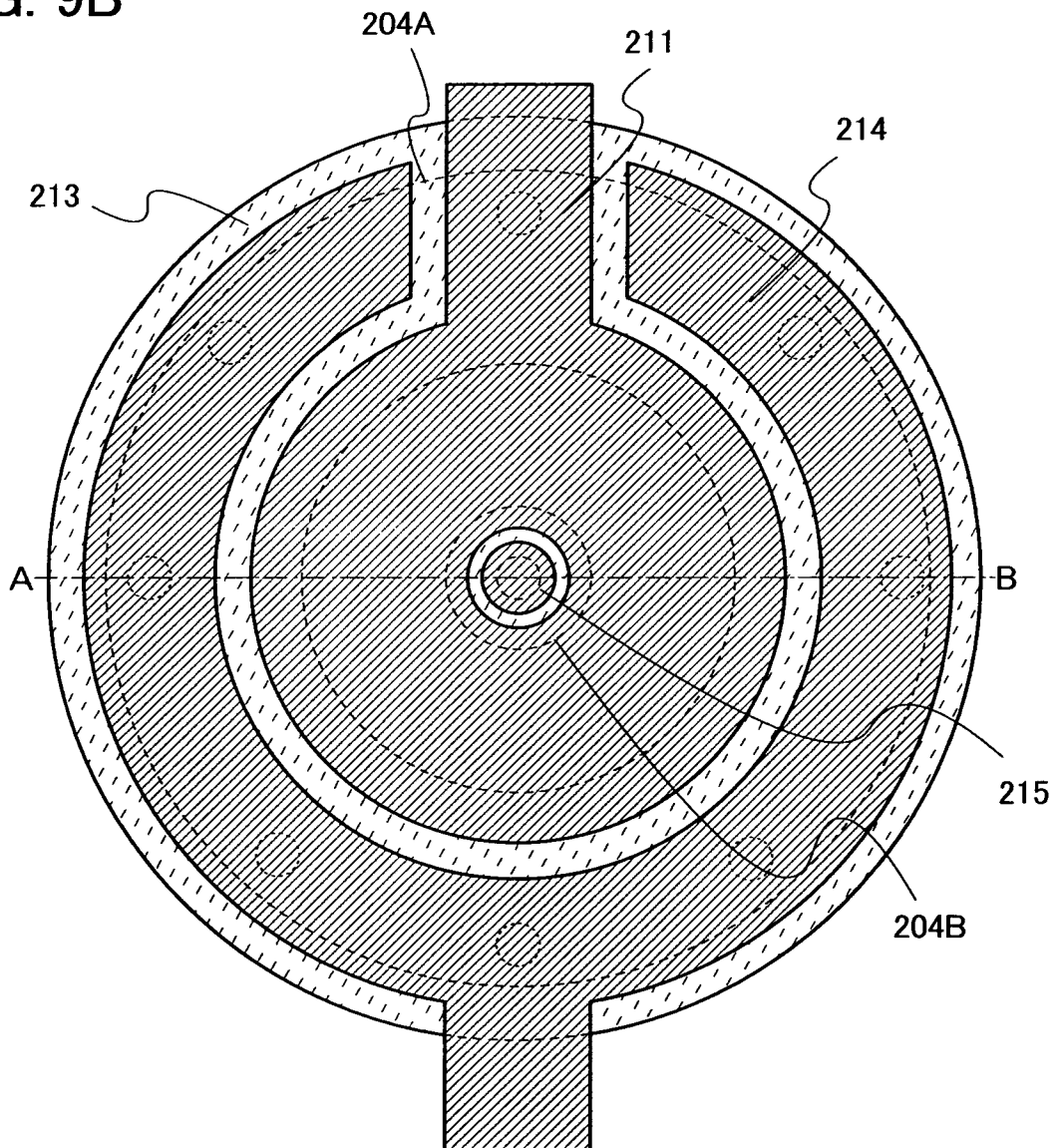


FIG. 10

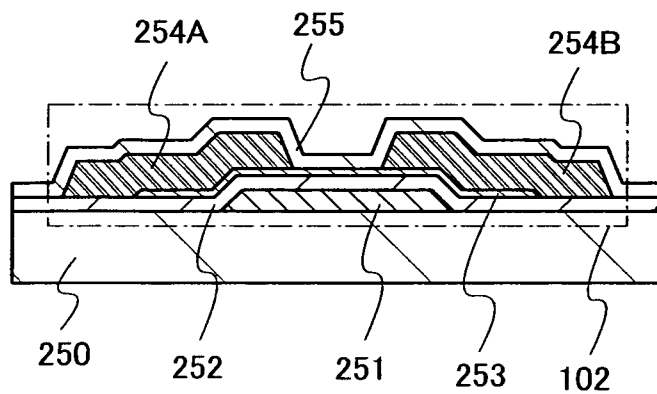


FIG. 11A

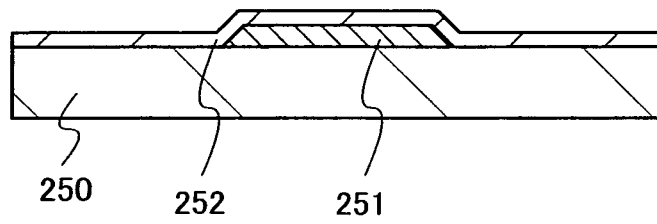


FIG. 11B

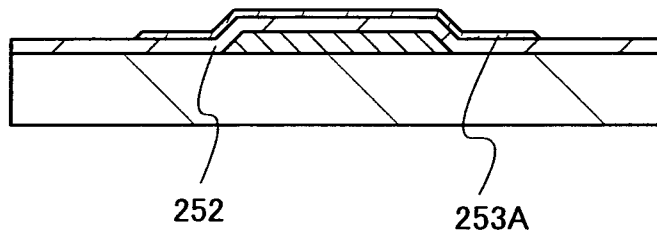


FIG. 11C

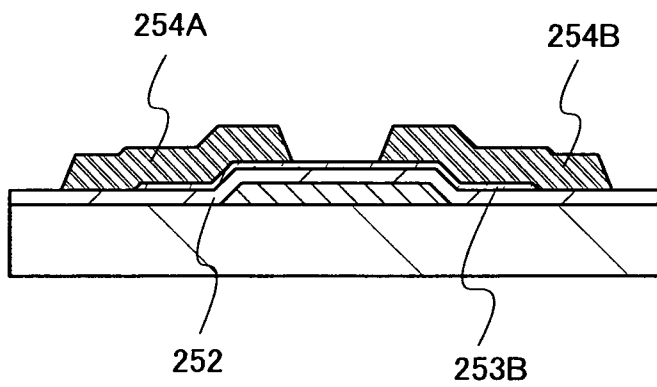


FIG. 11D

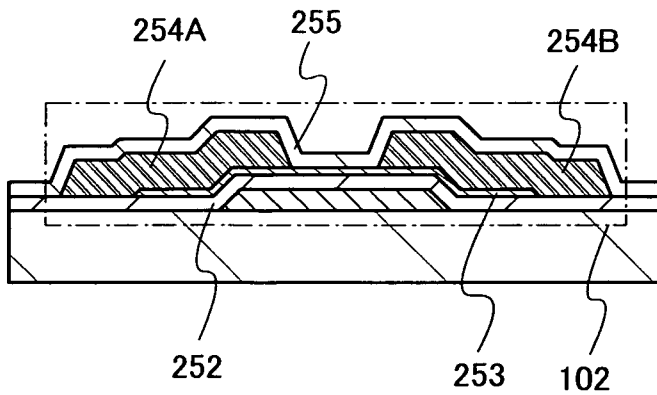
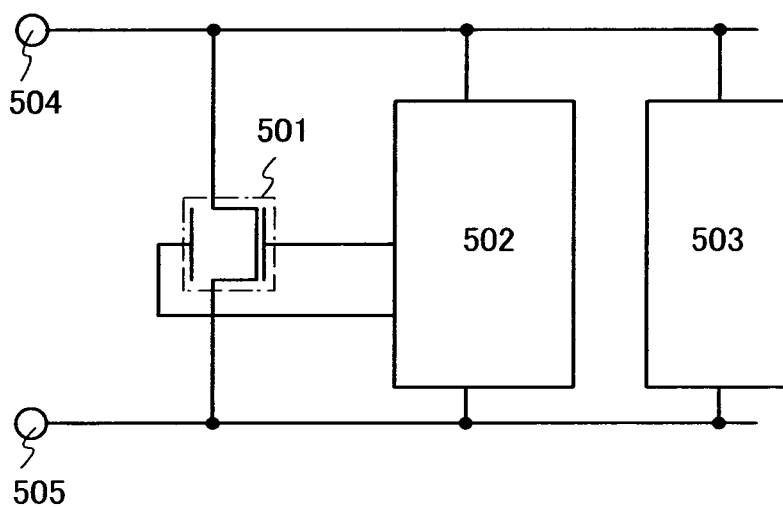


FIG. 12



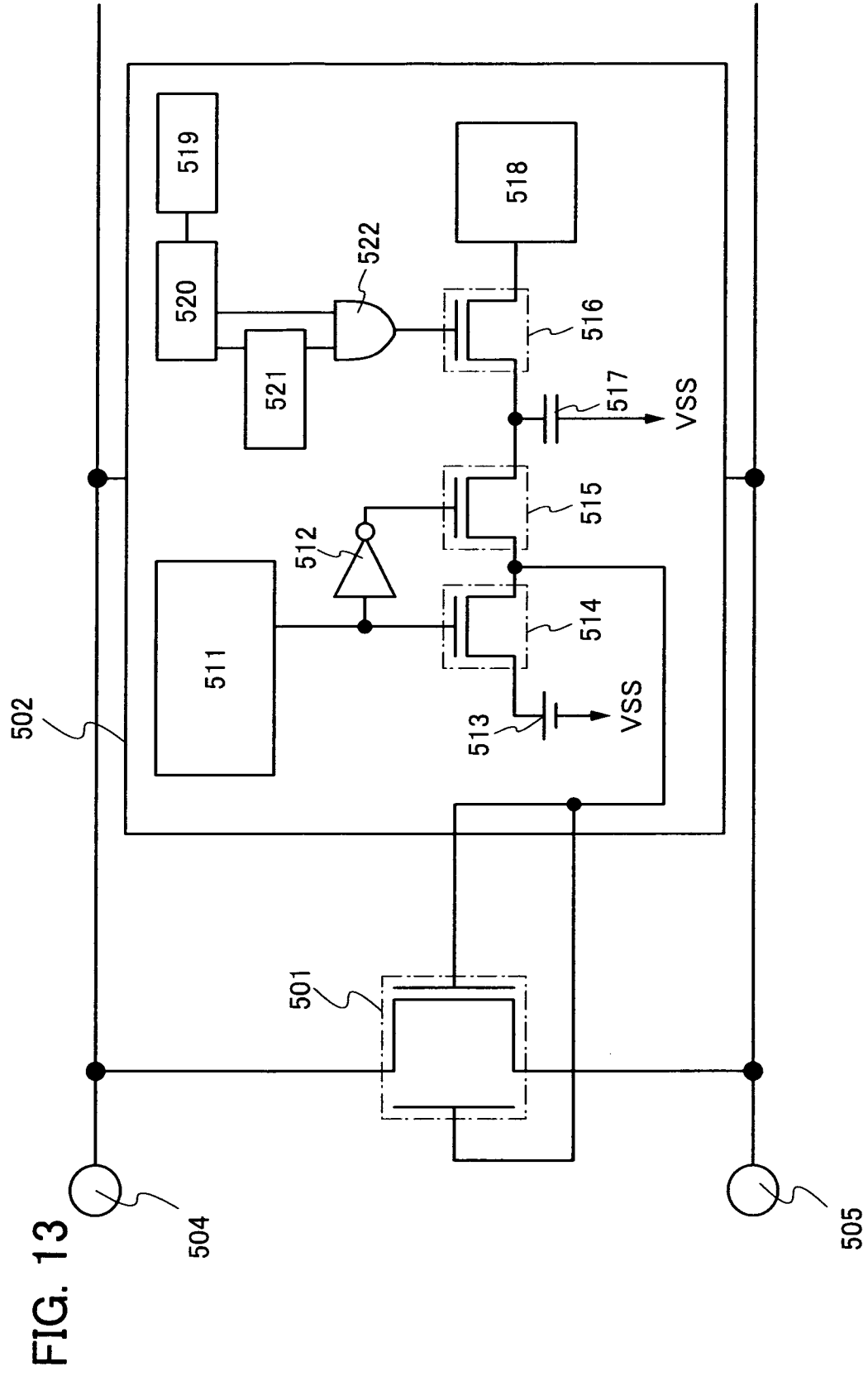
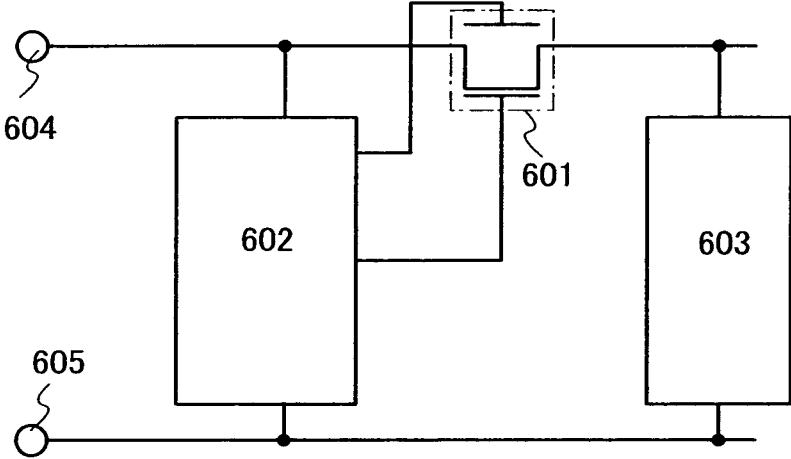


FIG. 13

504

505

FIG. 14



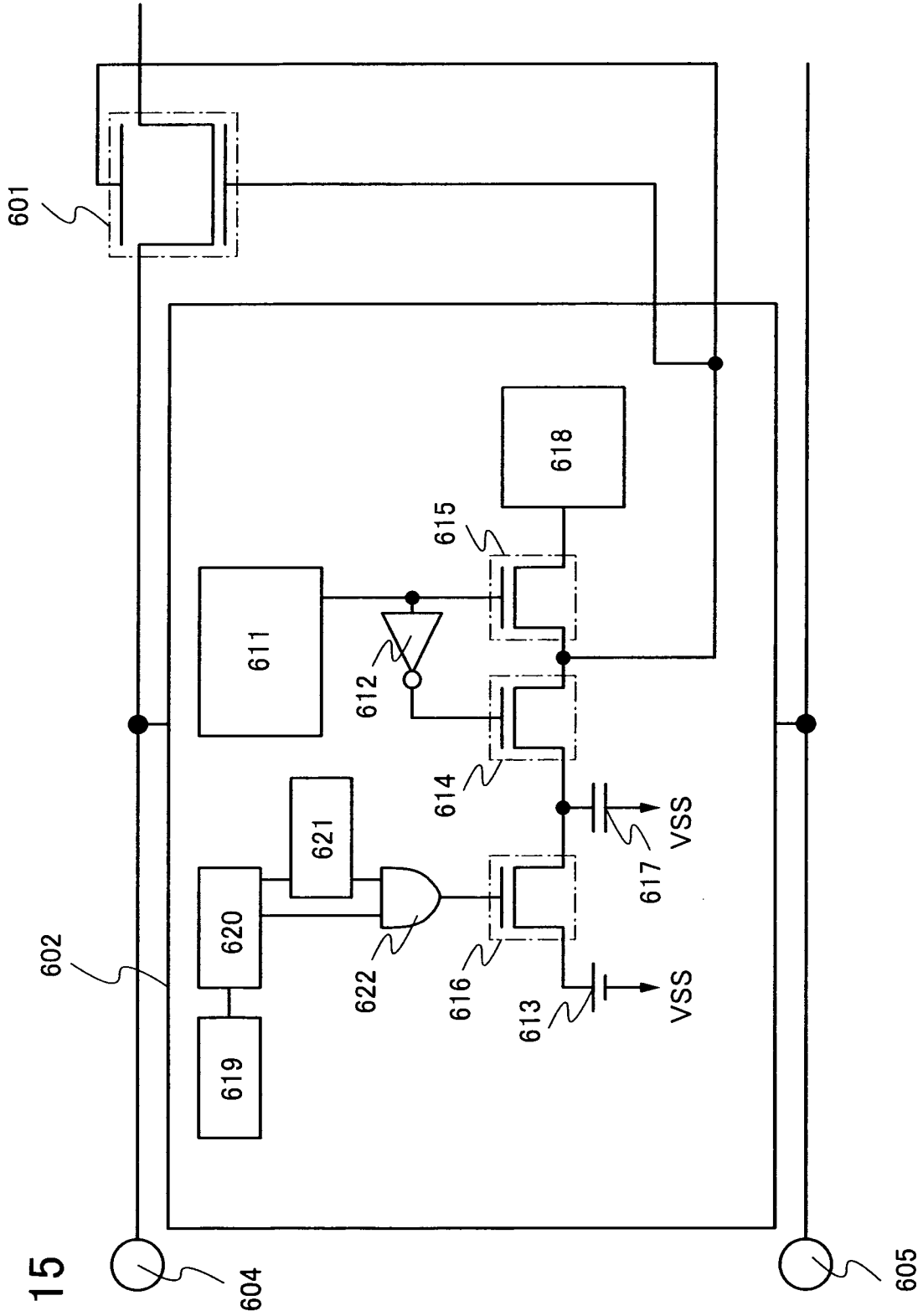


FIG. 15

FIG. 16

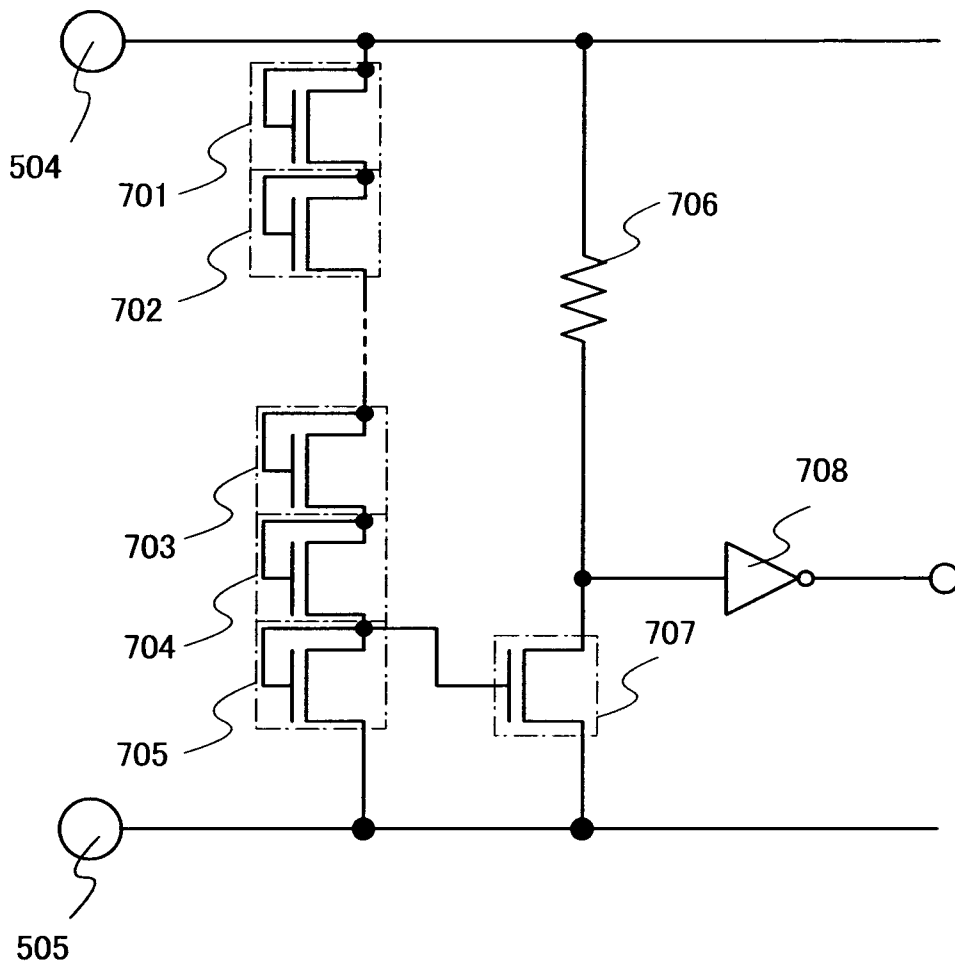


FIG. 17

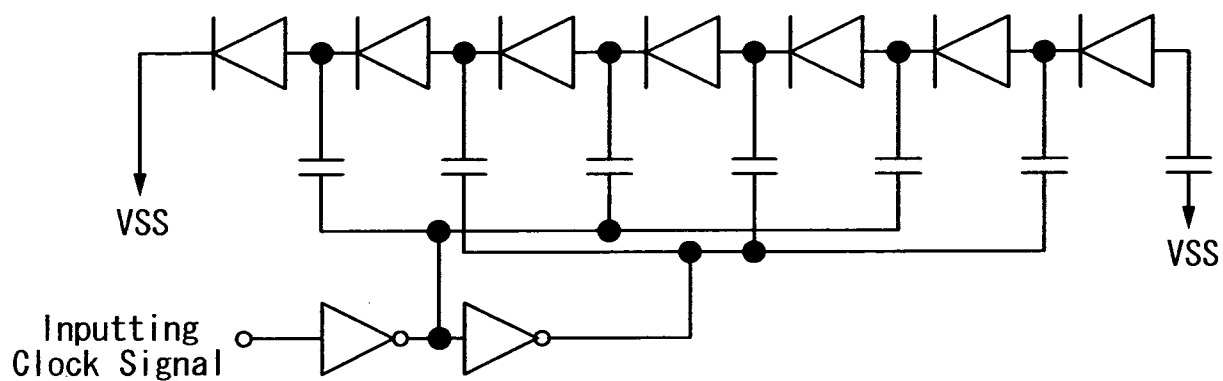


FIG. 18A

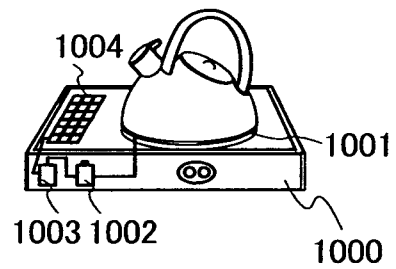


FIG. 18B

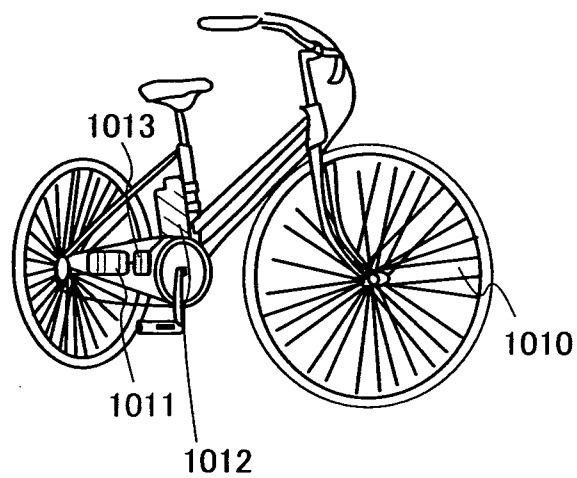
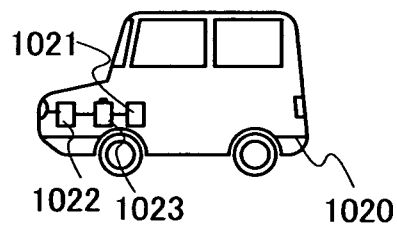


FIG. 18C



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EXPLANATION OF REFERENCE

100: control circuit, 101: power MOSFET, 101A: power MOSFET, 101B: power MOSFET, 102: field-effect transistor, 103: field-effect transistor, 104: field-effect transistor, 105: capacitor, 106: overvoltage detection circuit, 107: refresh control circuit, 108: high voltage generation source, 109: low voltage generation source, 110: power element, 111A: power MOSFET, 111B: power MOSFET, 121: power element, 200: substrate, 201: gate, 201A: gate, 202: gate insulating layer, 203: oxide semiconductor layer, 204A: terminal, 204B: terminal, 205: insulating layer, 206: gate, 206A: gate, 208: region, 209: off-set region, 211: gate, 212: gate insulating layer, 213: oxide semiconductor layer, 214: wiring, 215: wiring, 250: substrate, 251: gate, 252: gate insulating layer, 253: oxide semiconductor layer, 253A: oxide semiconductor layer, 253B: oxide semiconductor layer, 254A: terminal, 254B: terminal, 255: insulating layer, 401: capacitor, 501: power MOSFET, 502: control circuit, 503: circuit, 504: input terminal, 505: output terminal, 511: overvoltage detection circuit, 512: inverter, 513: positive power source, 514: switch transistor, 515: switch transistor, 516: switch transistor, 517: capacitor, 518: negative voltage generation circuit, 519: oscillator circuit, 520: divider circuit, 521: delay circuit, 522: AND circuit, 601: power MOSFET, 602: control circuit, 603: circuit, 604: input terminal, 605: output terminal, 611: overvoltage detection circuit, 612: inverter, 613: positive power source, 614: switch transistor, 615: switch transistor, 616: switch transistor, 617: capacitor, 618: negative voltage generation circuit,

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619: oscillator circuit, 620: divider circuit, 621: delay circuit, 622: AND circuit, 701: transistor, 702: transistor, 703: transistor, 704: transistor, 705: transistor, 706: resistor, 707: transistor, 708: inverter, 1000: electromagnetic cooker, 1001: coil unit, 1002: battery, 1003: semiconductor device, 1004: solar battery, 1010: electric bicycle, 1011: motor unit, 1012: battery, 1013: semiconductor device, 1020: electric car, 1021: motor unit, 1022: battery, 1023: semiconductor device.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/073844

A. CLASSIFICATION OF SUBJECT MATTER		
Int.Cl. H03K17/687(2006.01) i, H01L21/336(2006.01) i, H01L29/786(2006.01) i, H02J7/00(2006.01) i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
Int.Cl. H03K17/00-17/70, H01L21/336, H01L29/786, H02J7/00		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2011 Registered utility model specifications of Japan 1996-2011 Published registered utility model applications of Japan 1994-2011		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP 2001-251772 A (TOKIN Corp.) 2001.09.14, [Abstract], [0020]-[0024], figure 1 (No Family)	11-12, 14-17 18-22
Y	JP 2009-4733 A (Canon Inc.) 2009.01.08, [0005]-[0010], [0025]-[0032], figure 3 & WO 2008/143304 A1	18-22
A	JP 9-121470 A (Canon Inc.) 1997.05.06, [0015]-[0019], figures 3-4 & US 5714869 A	1-34
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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Date of the actual completion of the international search		Date of mailing of the international search report
24.01.2011		01.02.2011
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