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(51) INT CL^7
H01L 21/60 // H01L 23/485

(52) UK CL (Edition S)
H1K KPXDB K4C1F K4C1U K4C11 K4C23 K4C3U K4C8 K5BX K5B2 K5B5 K5B9 K5C3X K5E9 K5K K5L

(56) Documents Cited
US 5683942 A
IEMT/IMC Proc."Advanced MCM-Ls for consumer Electronics"1998 Amami et al, pp 249-254

(58) Field of Search
UK CL (Edition S) **H1K KHAE KPX KPXB KPXDB**
INT CL^7 **H01L 21/56 21/58 21/60 21/603 23/29 23/31 23/485 23/522 23/532 23/66 , H05K 1/18 7/02**
ONLINE: EPODOC, JAPIO, WPI

(54) Abstract Title
Flip-chip type semiconductor device with stress absorbing layer made of resin

(57) A flip-chip type semiconductor device, or method of manufacturing such a device, wherein the device comprises; an insulating stress absorbing resin layer 14, 34 made of thermosetting resin film on a semiconductor substrate 11, 31. The thermosetting resin has openings corresponding to pad electrodes 12, 32 formed on the substrate. A plurality of flexible conductive members 16, 38 fills each one of the openings. A plurality of metal bumps 17 are formed on the flexible conductive members. Alternatively, the plurality of metal bumps (39, Figure 14Q) may each be formed on a plurality of conductive members 35, 37. The conductive members may be formed on a second photosensitive insulating stress absorbing resin layer (34', Figure 14Q) which may be formed on a first insulating stress absorbing resin layer (34, Figure 14Q). The thermosetting resin may be for example, epoxy resin, silicone resin, polymide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin and fluorene resin. The flexible conductive members may be made from powdered material including at least one of copper, lead, tin, nickel, gold, silver, and Palladium.

Fig. 2H

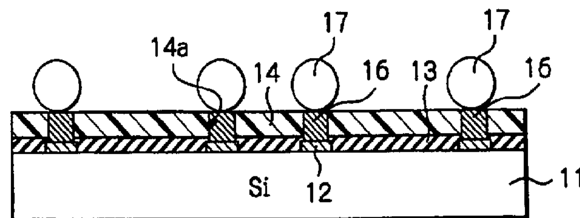

Fig. 6L

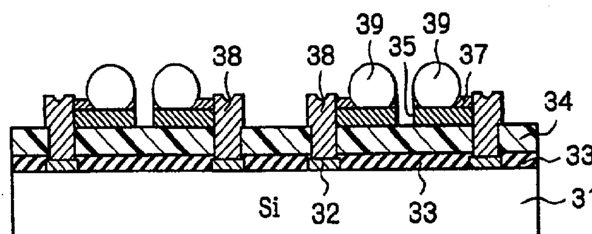

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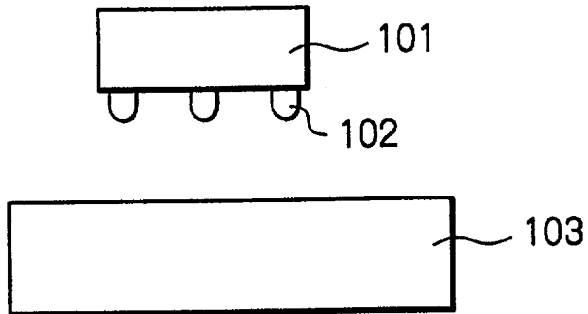
Fig. 1A



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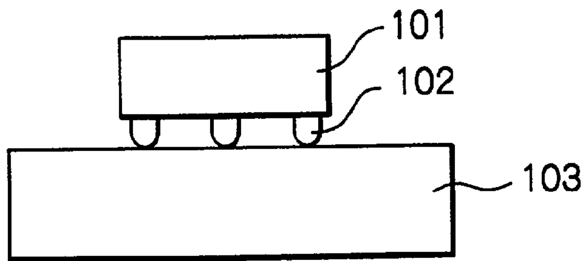
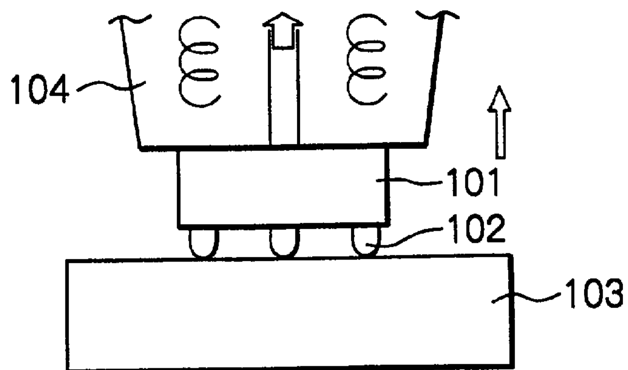


Fig. 1C



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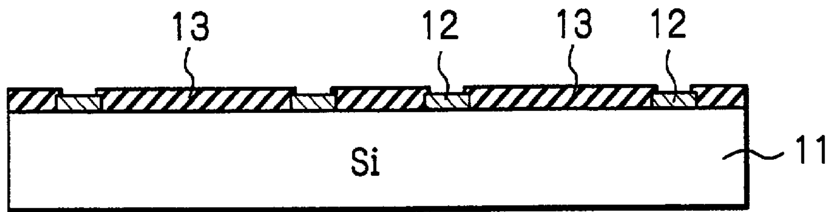

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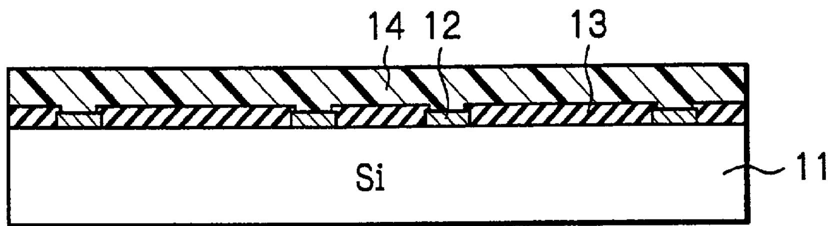

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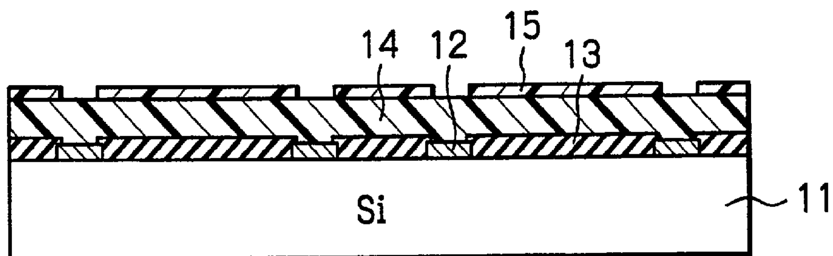

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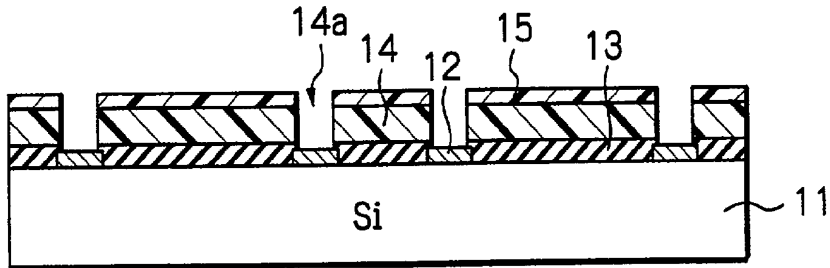

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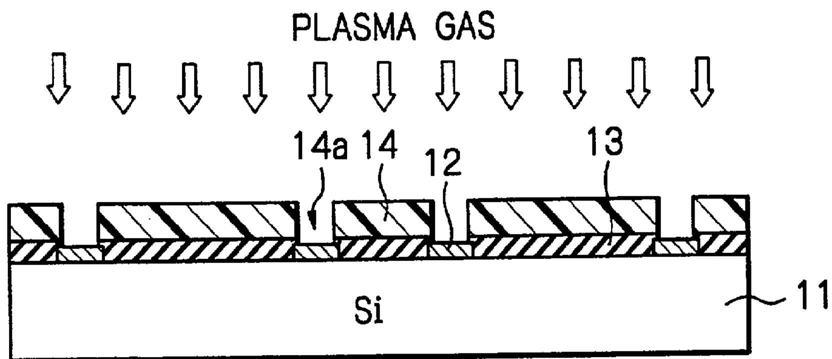

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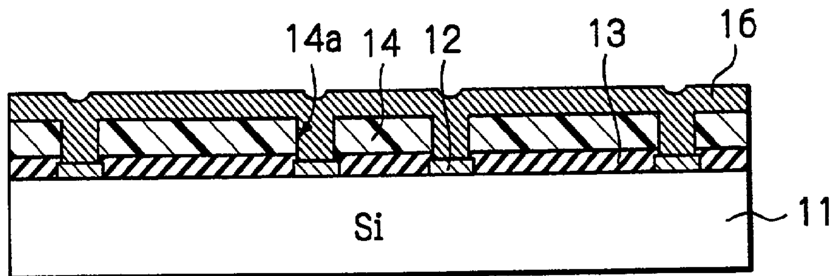

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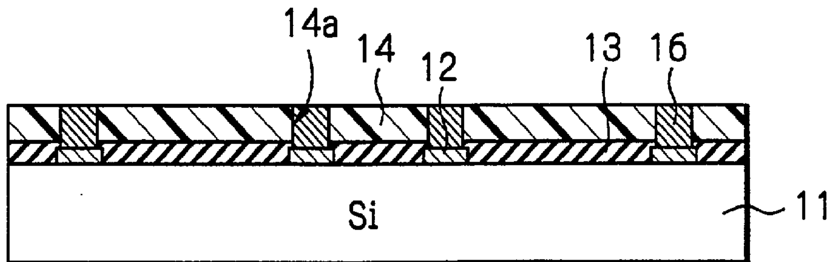

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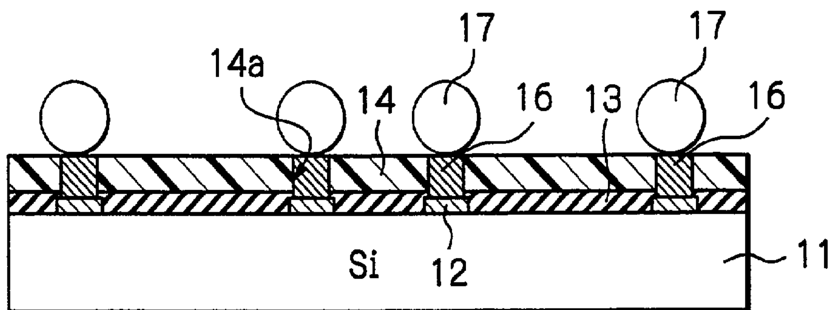

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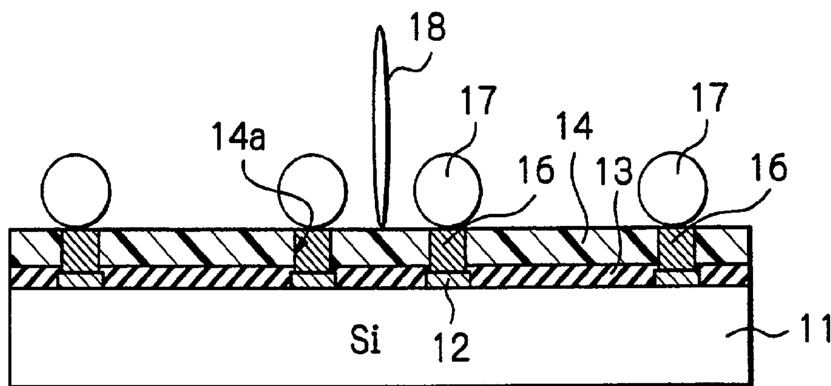

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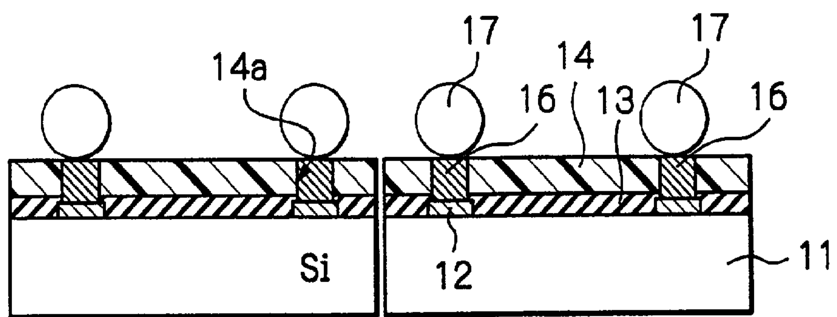

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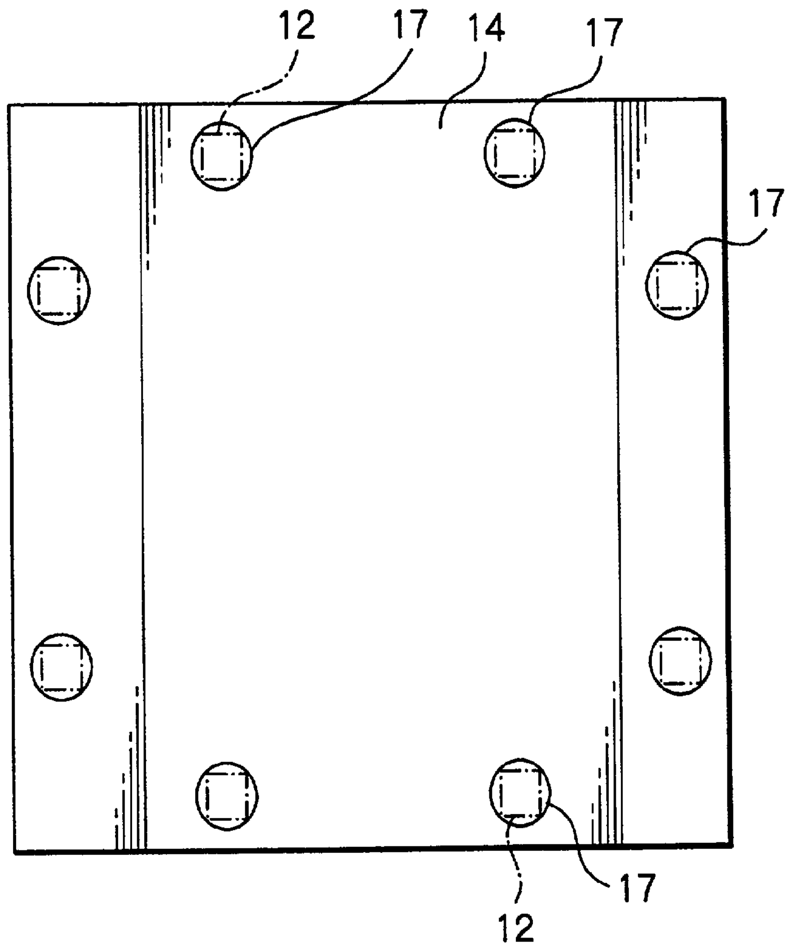

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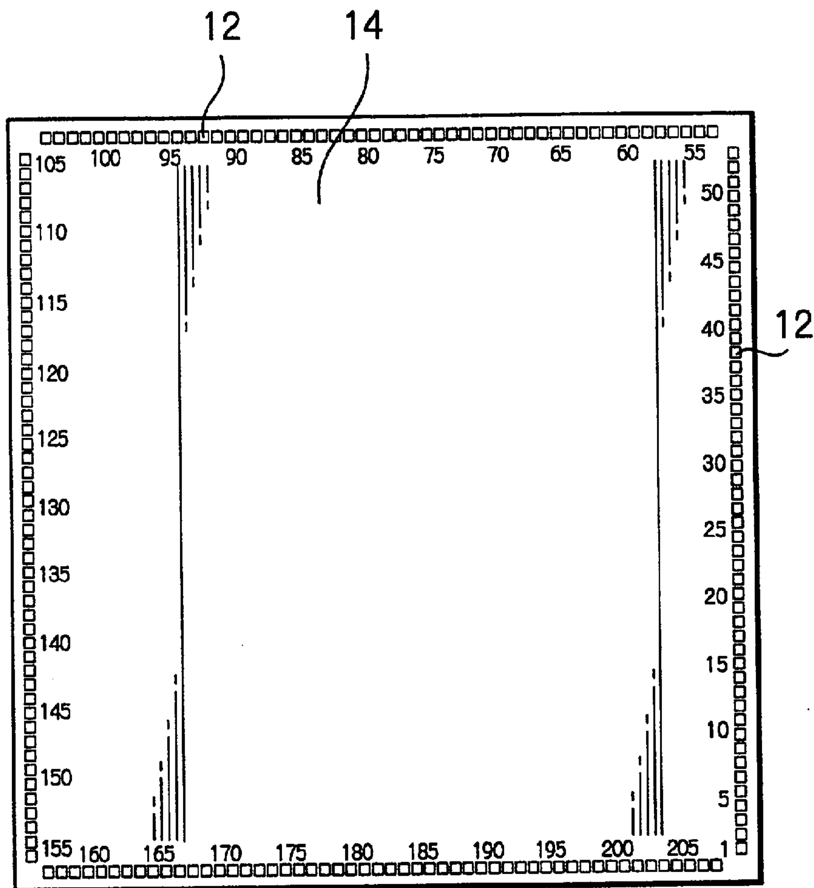

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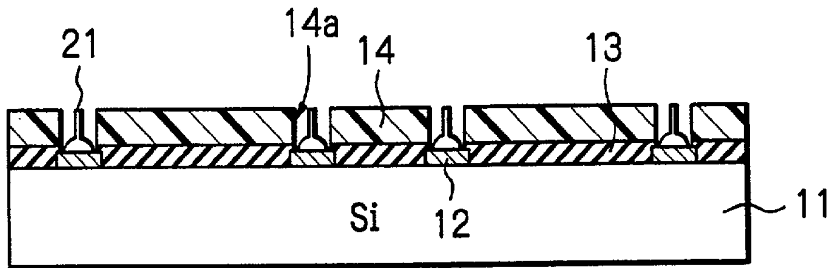

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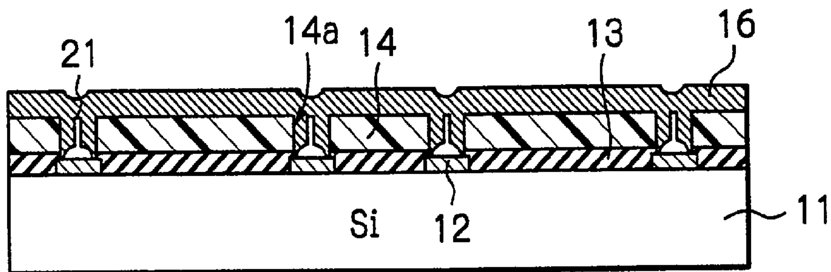

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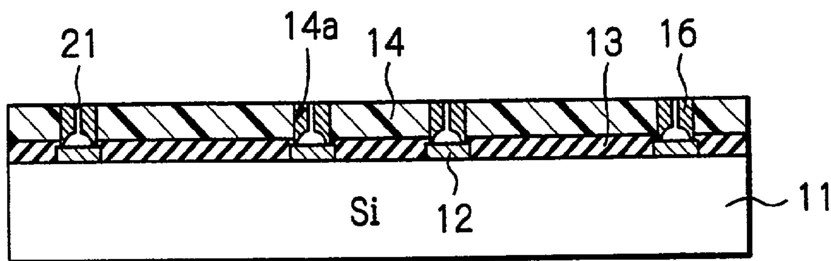

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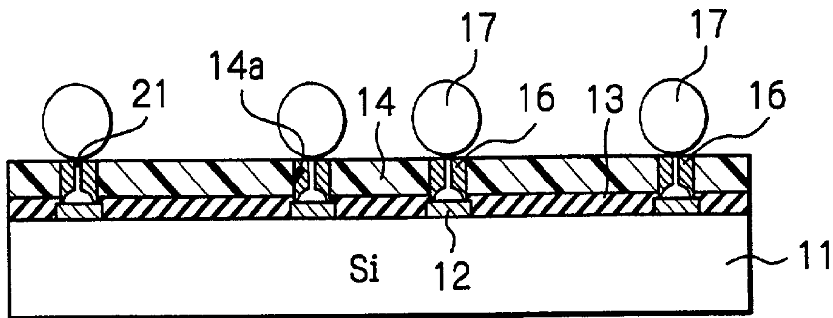

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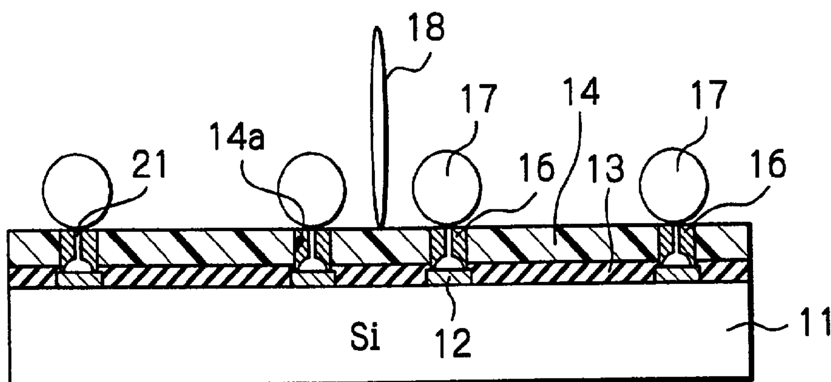

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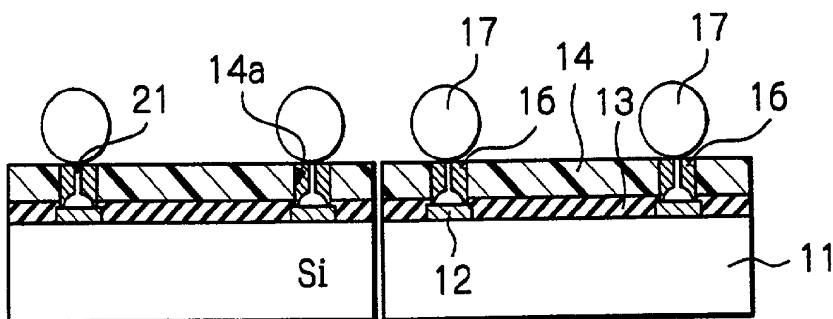

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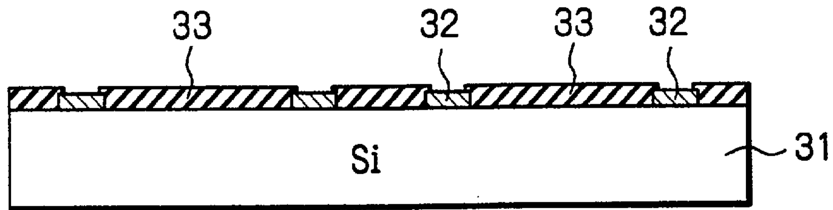

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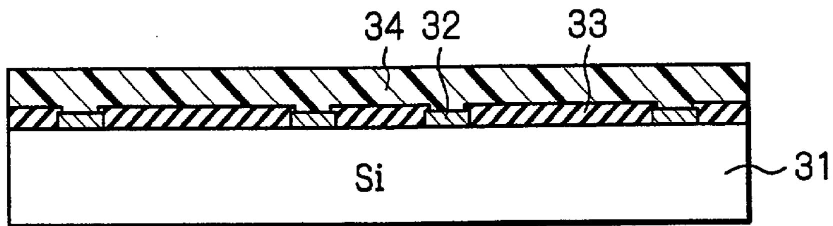

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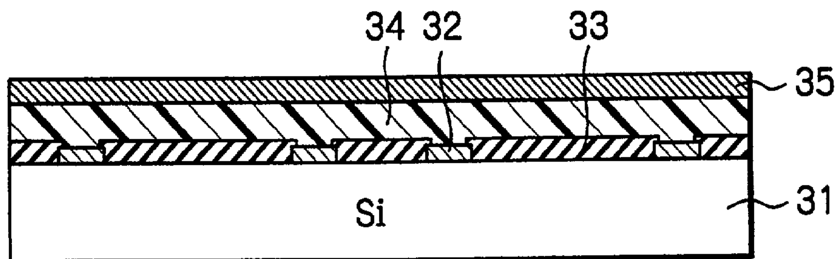

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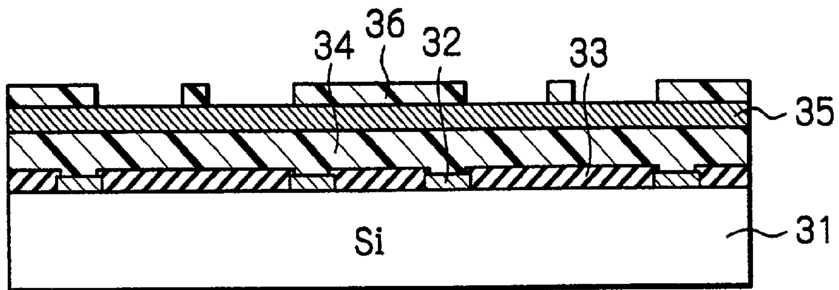

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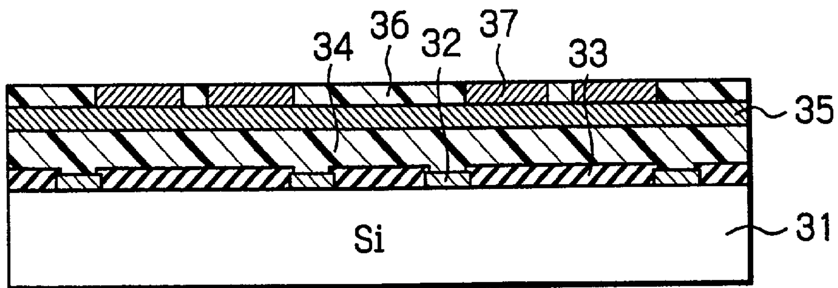

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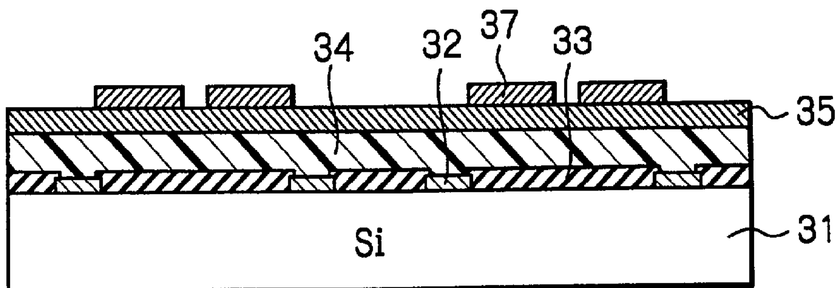

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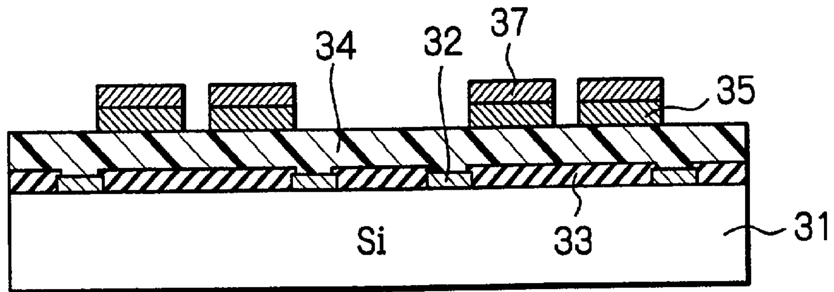

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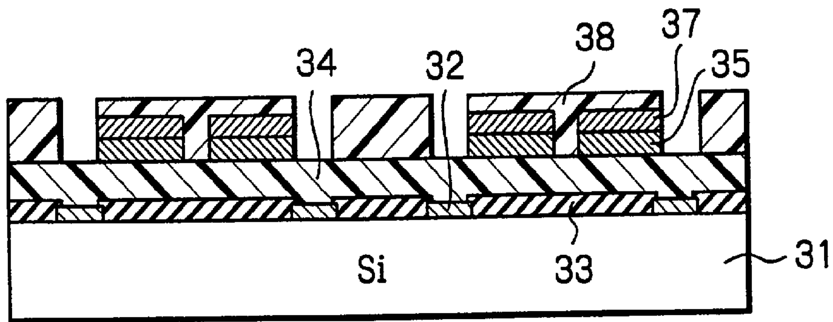

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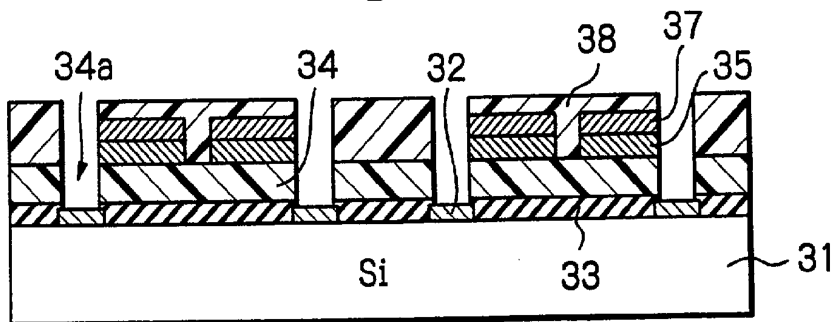

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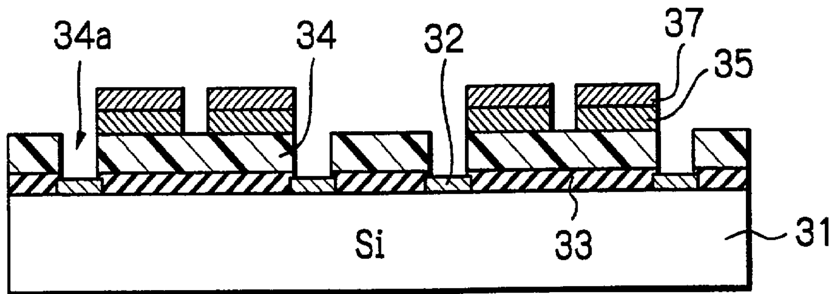

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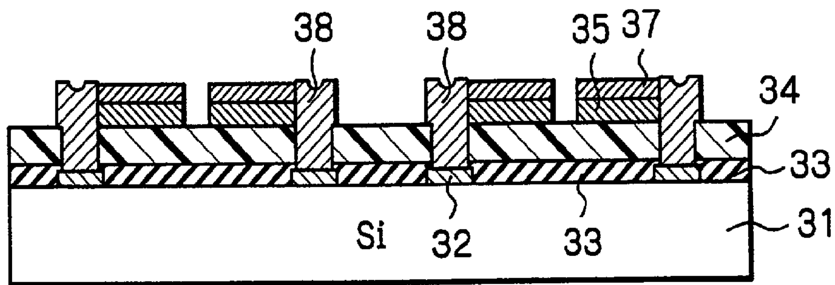

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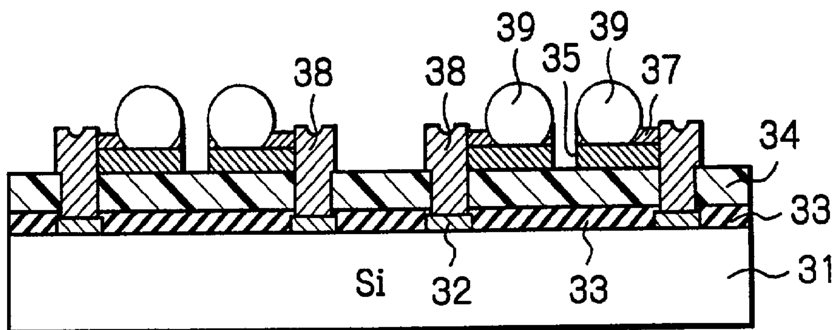


Fig. 6M

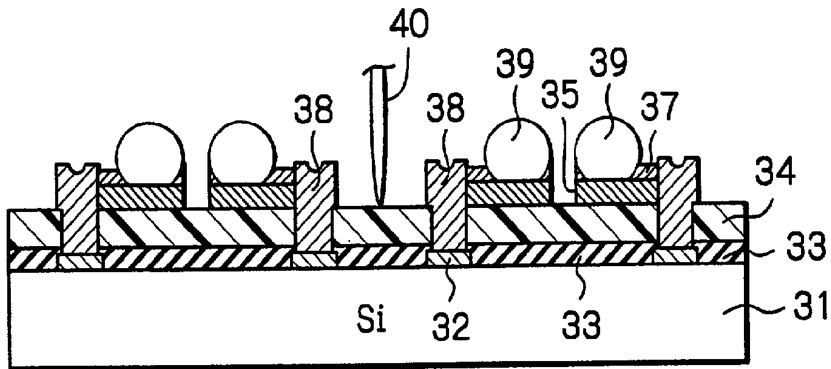


Fig. 6N

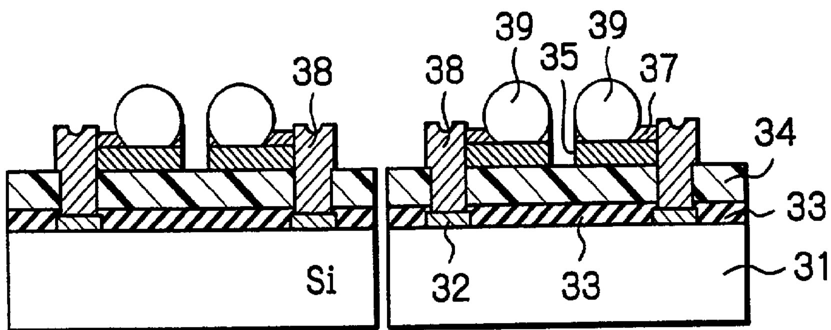


Fig. 7

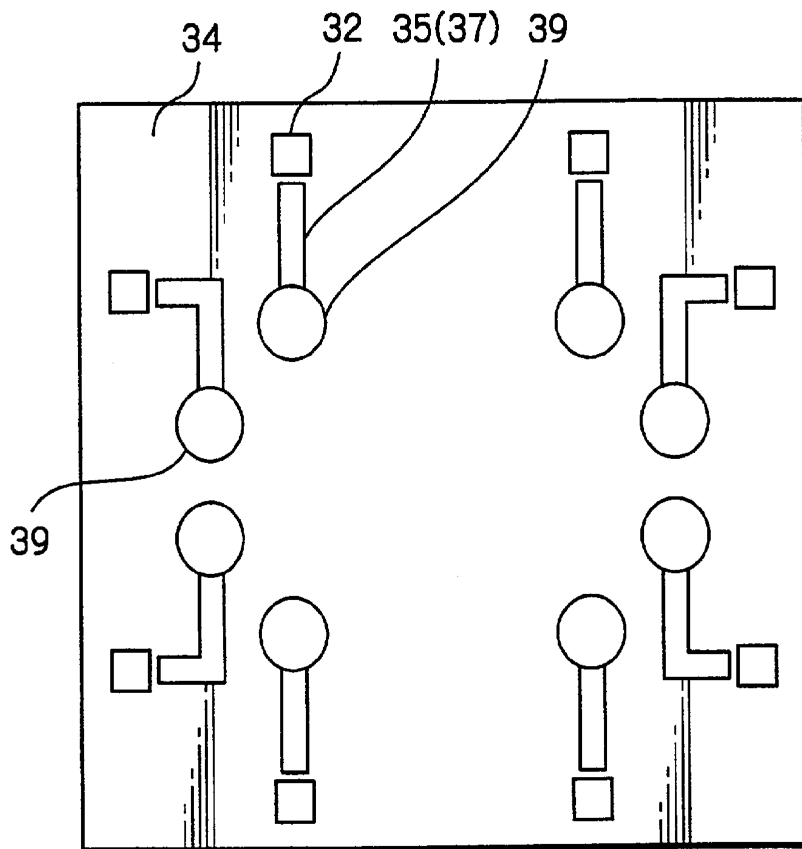
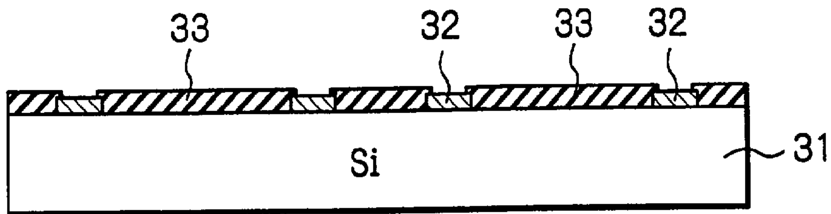


Fig. 8A



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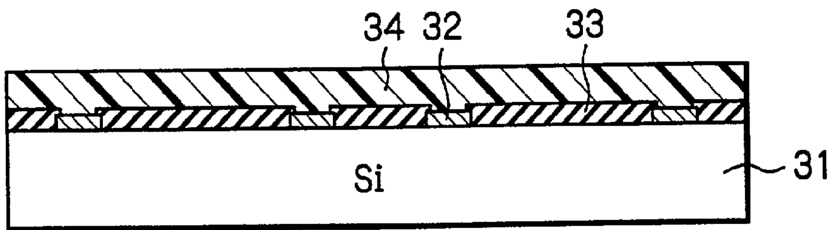


Fig. 8C

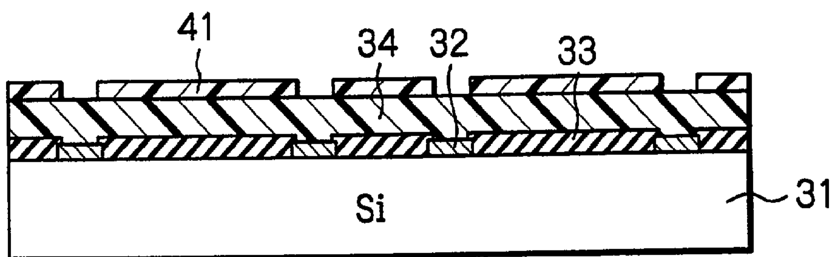
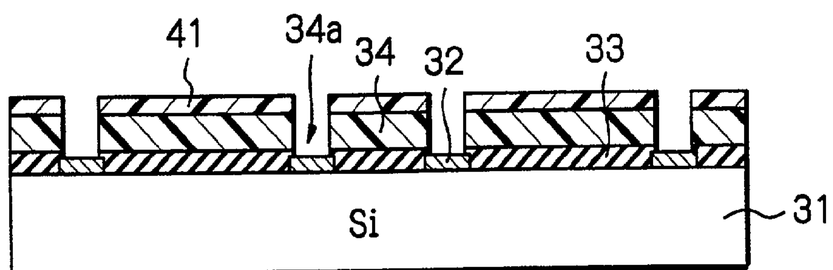


Fig. 8D



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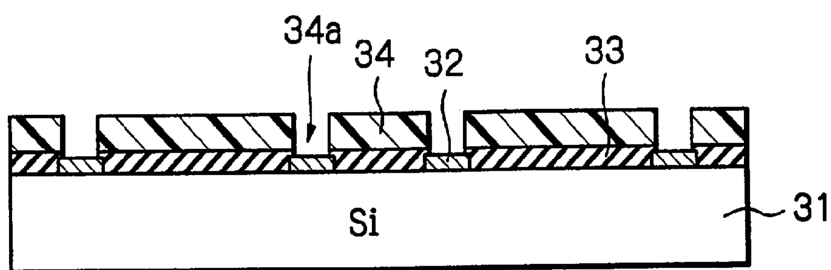

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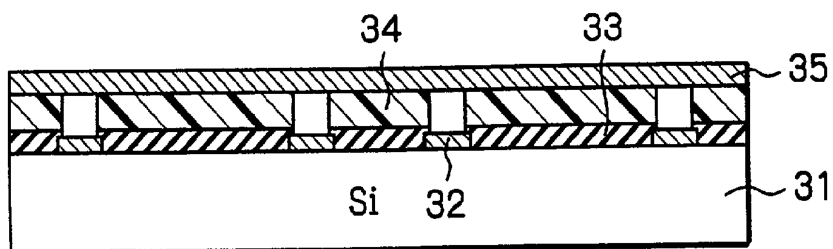

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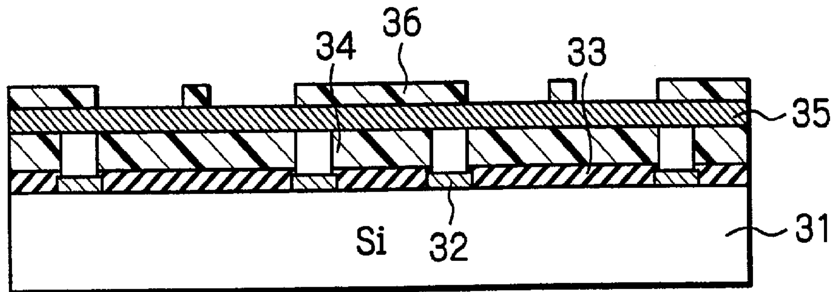

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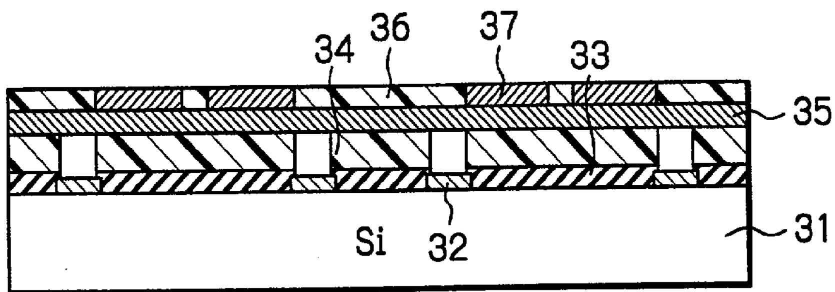

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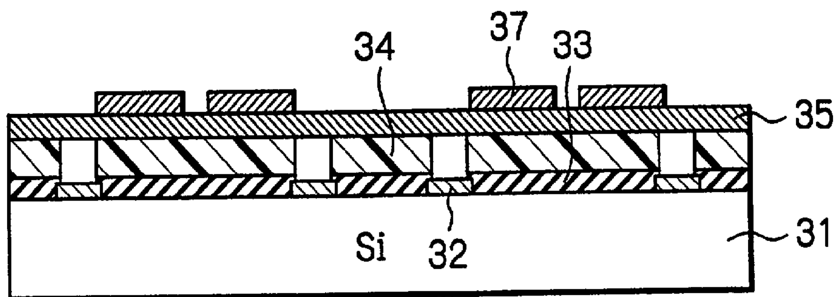

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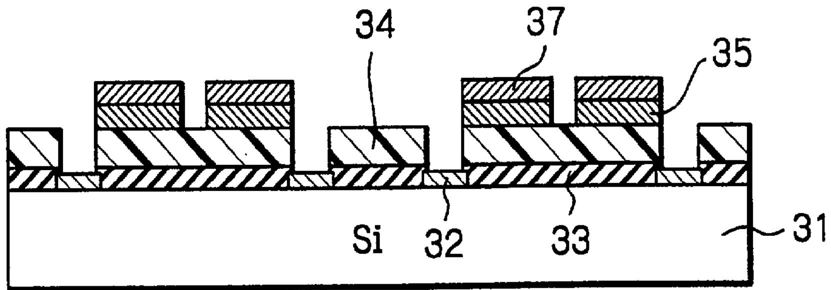

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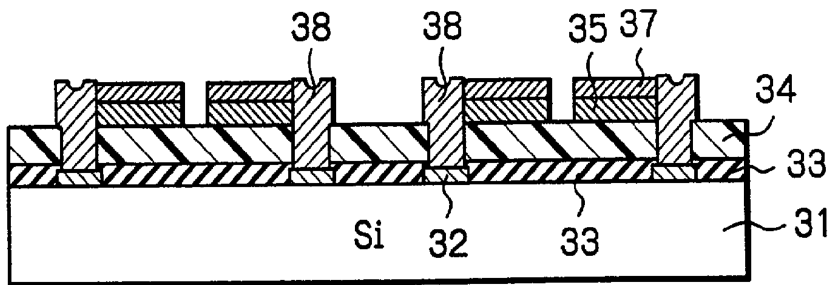

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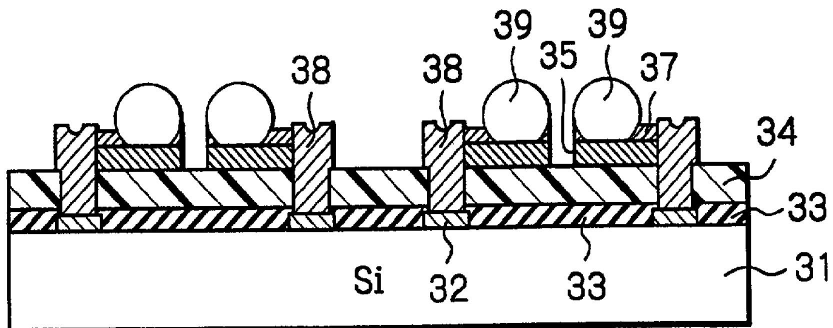

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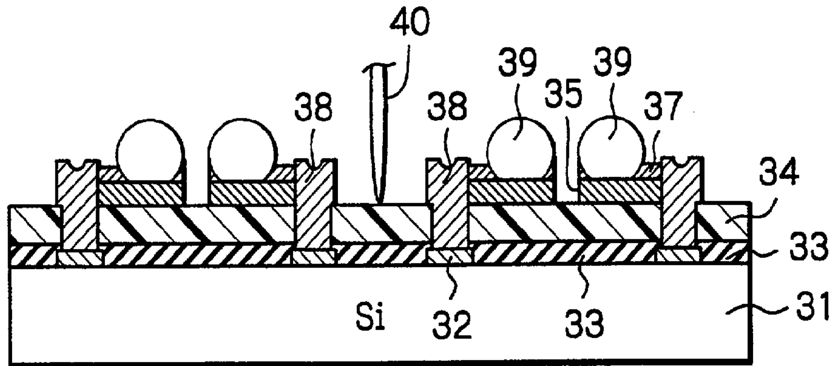

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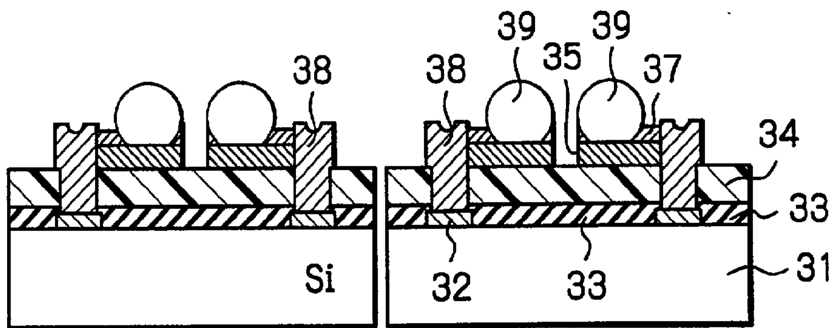

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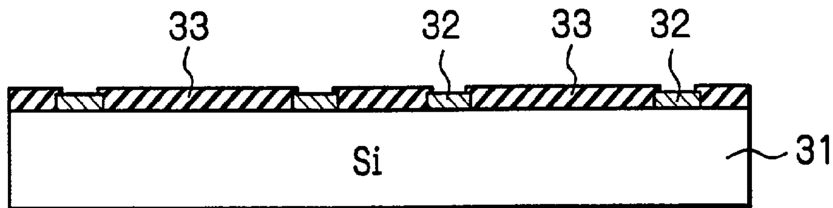
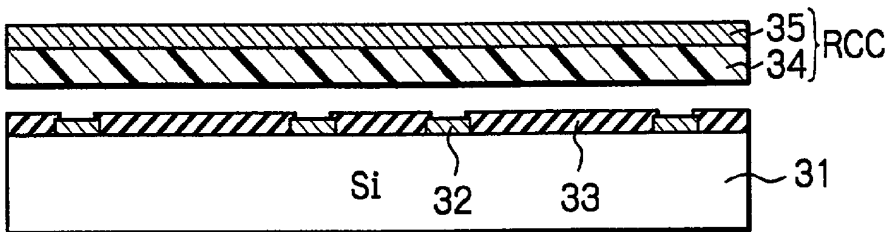


Fig. 9B



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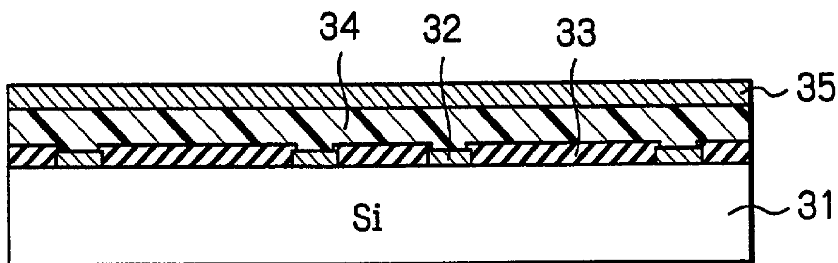

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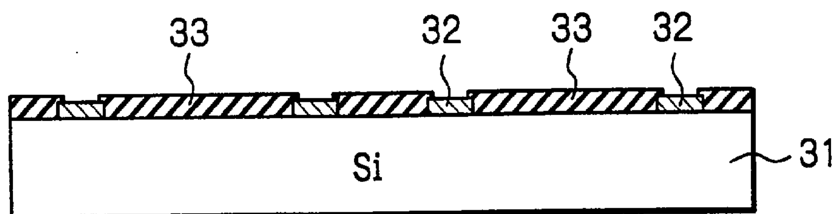

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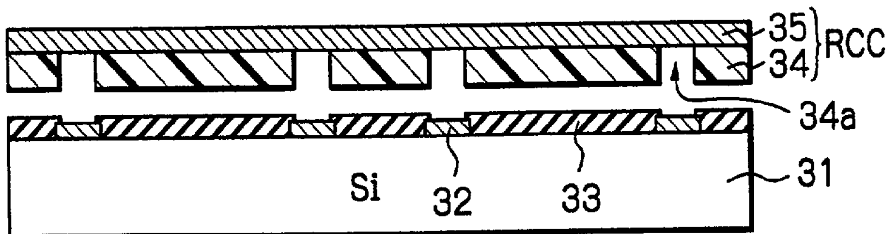

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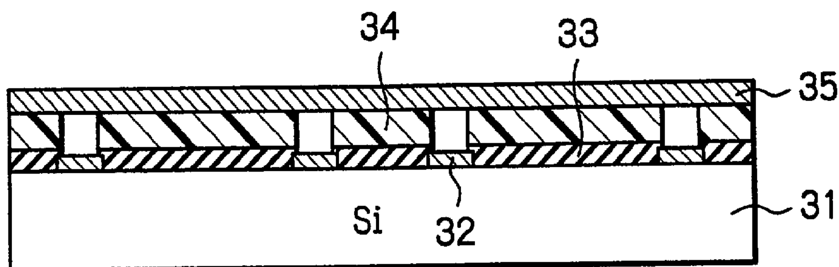

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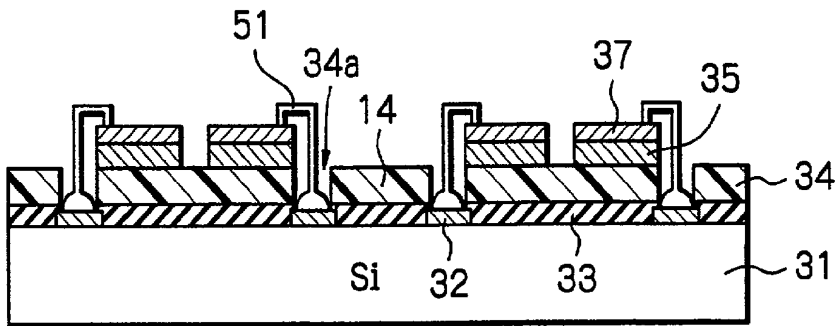

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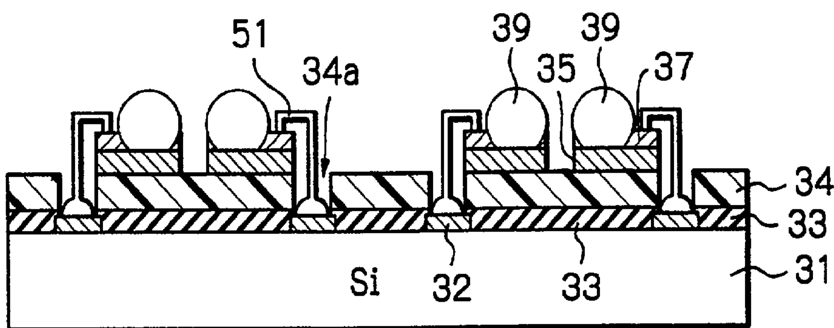

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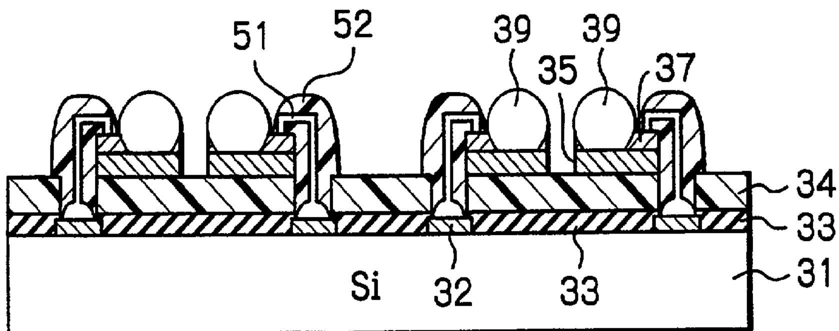


Fig. 11D

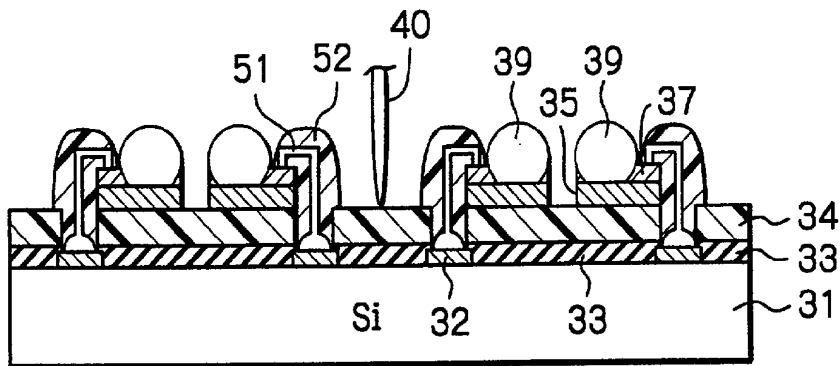
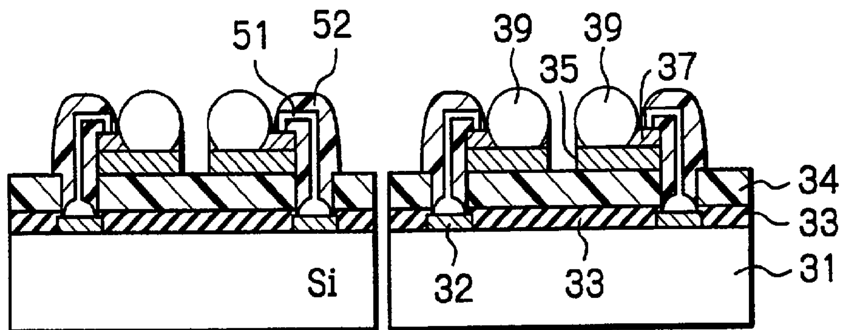


Fig. 11E



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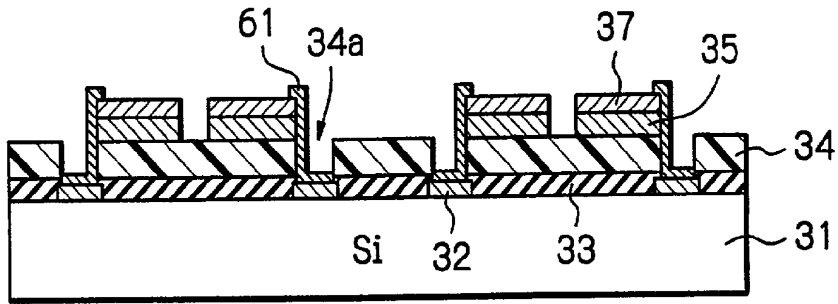

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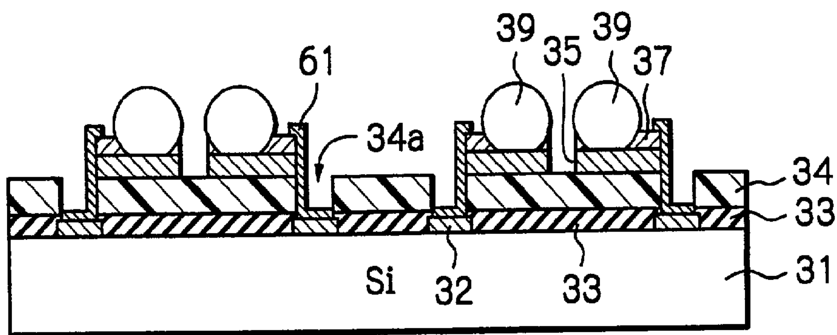


Fig. 12C

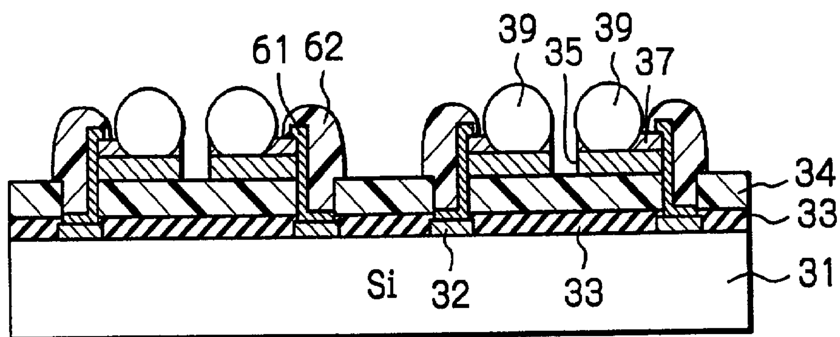


Fig. 12D

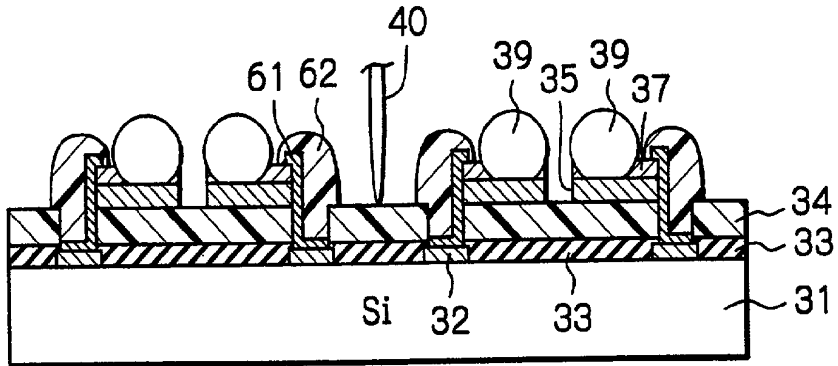


Fig. 12E

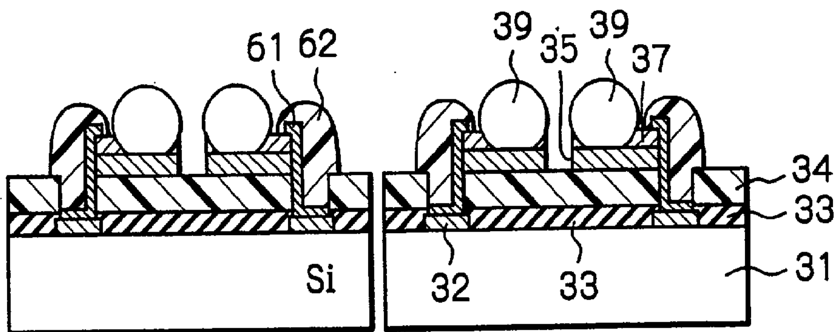


Fig. 13A

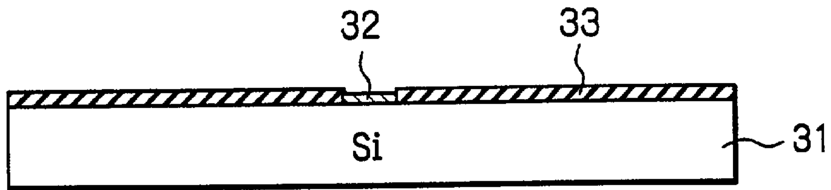


Fig. 13B

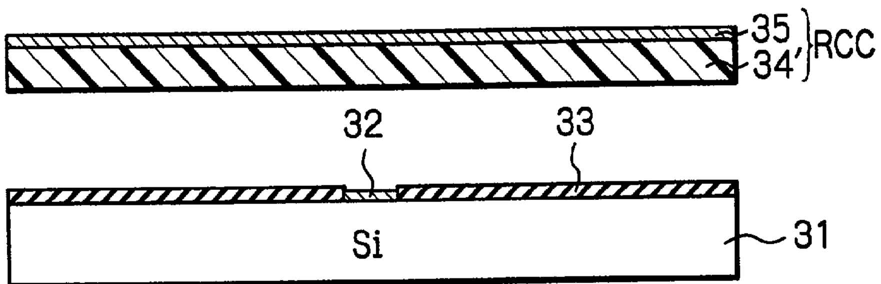


Fig. 13C

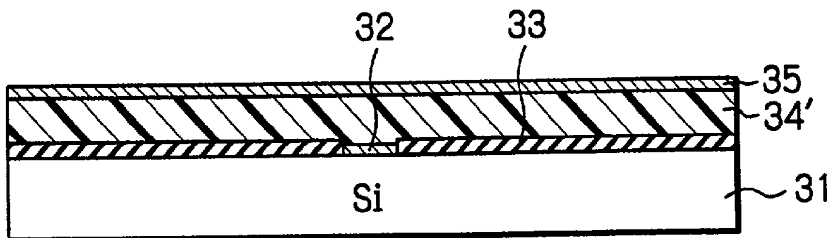


Fig. 13D

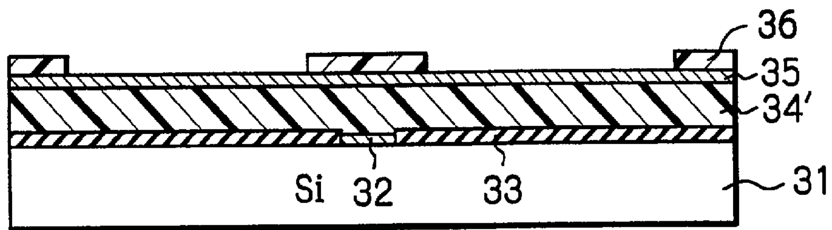


Fig. 13E

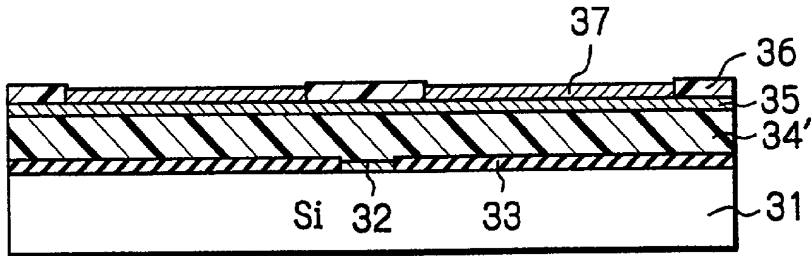


Fig. 13F

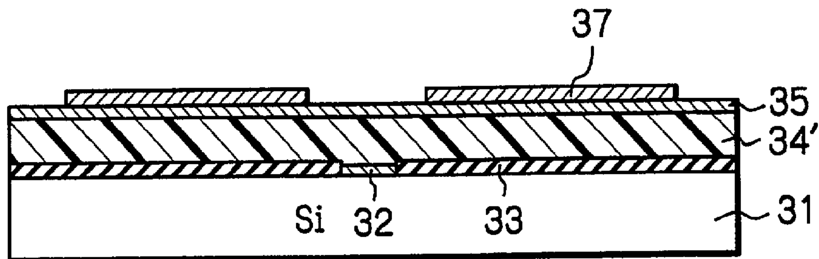


Fig. 13G

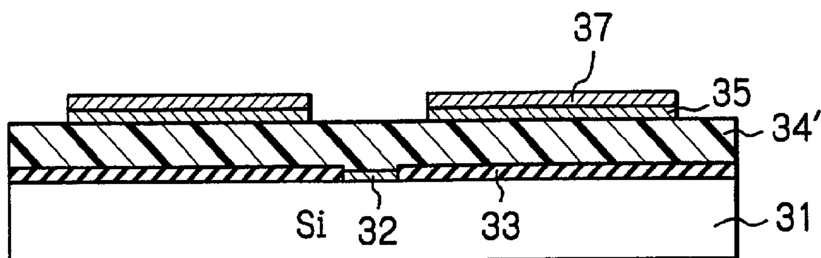


Fig. 13H

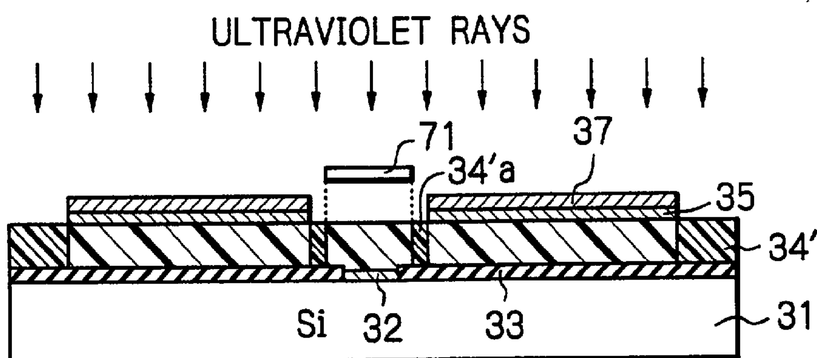


Fig. 13I

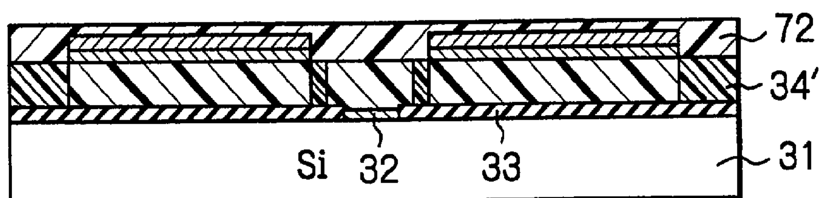


Fig. 13J

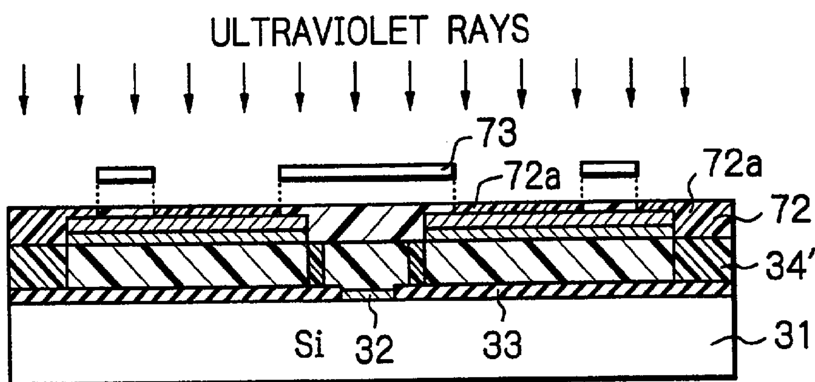


Fig. 13K

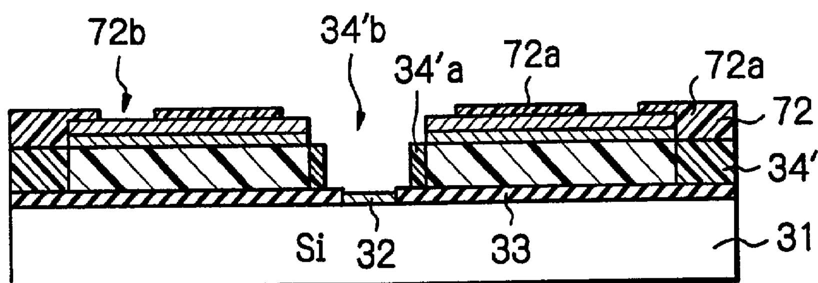


Fig. 13L

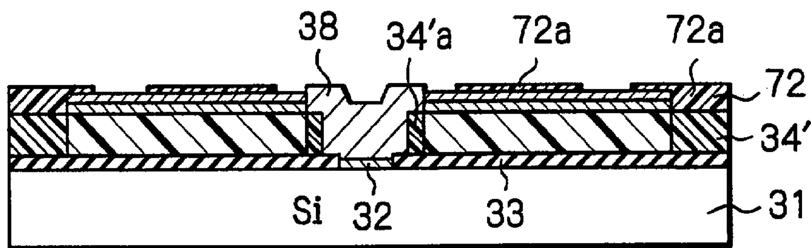


Fig. 13M

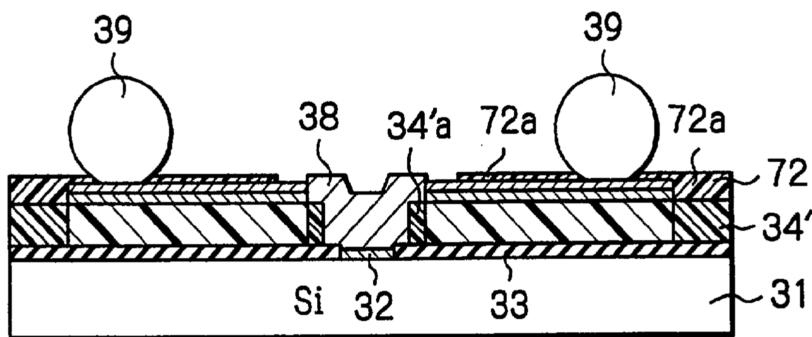


Fig. 14A

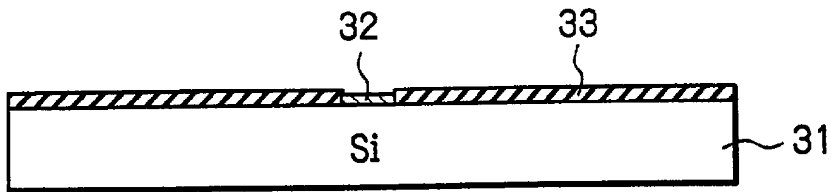


Fig. 14B

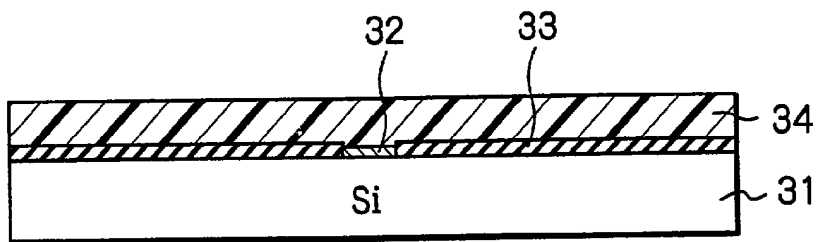


Fig. 14C

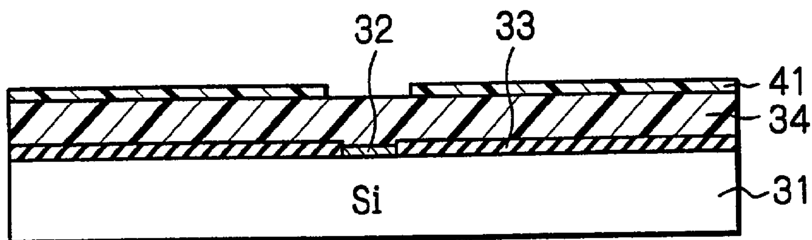


Fig. 14D

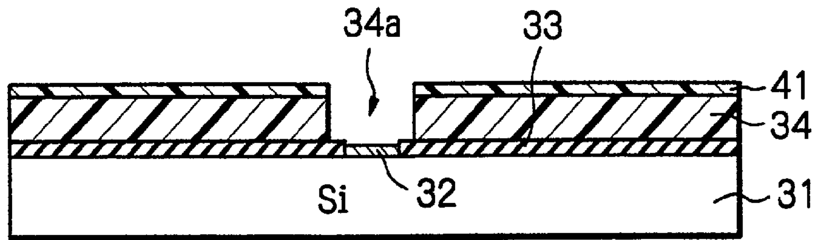


Fig. 14E

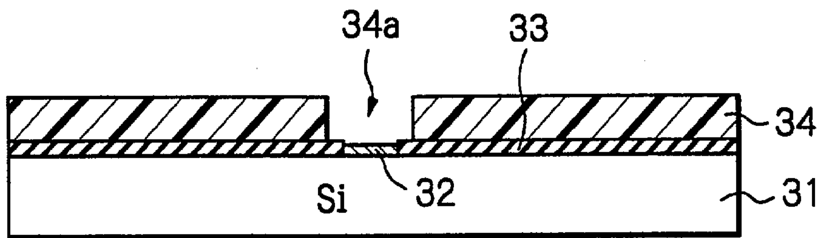


Fig. 14F

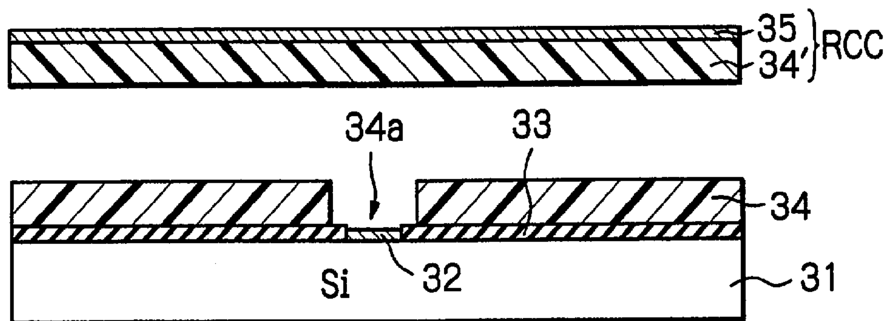


Fig. 14G

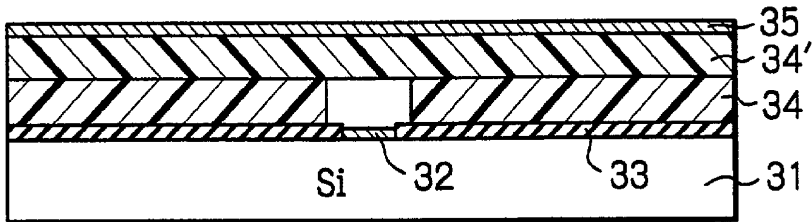


Fig. 14H

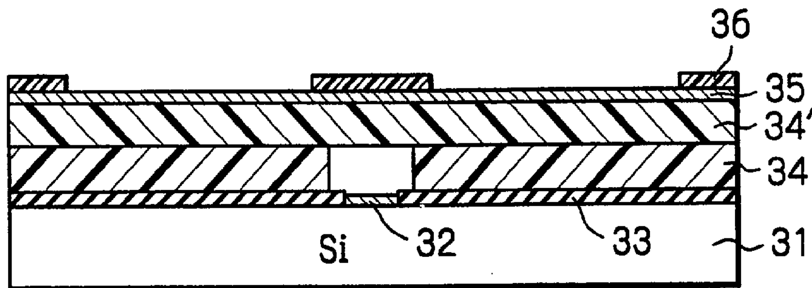


Fig. 14I

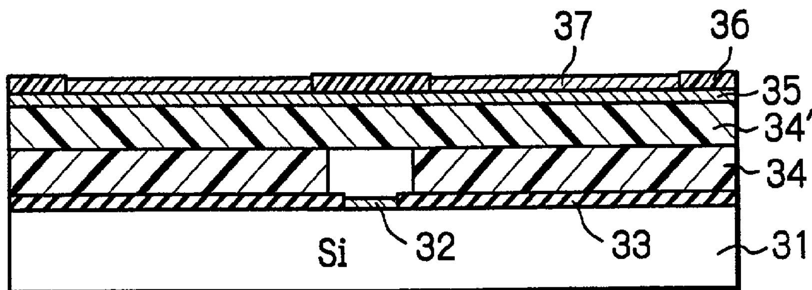


Fig. 14J

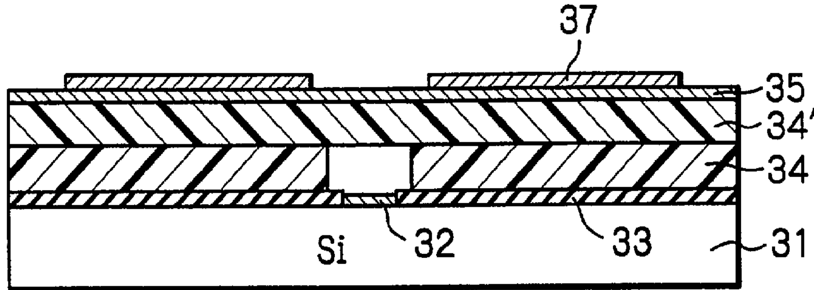


Fig. 14K

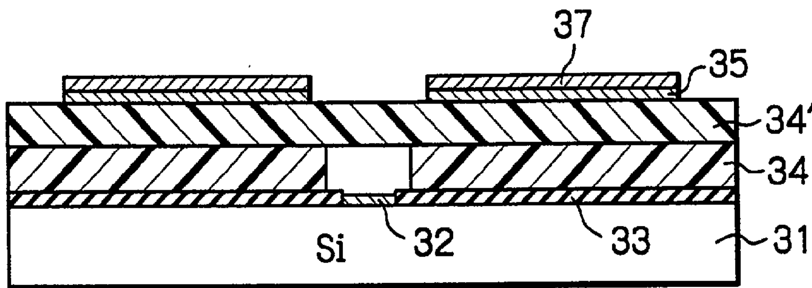


Fig. 14L

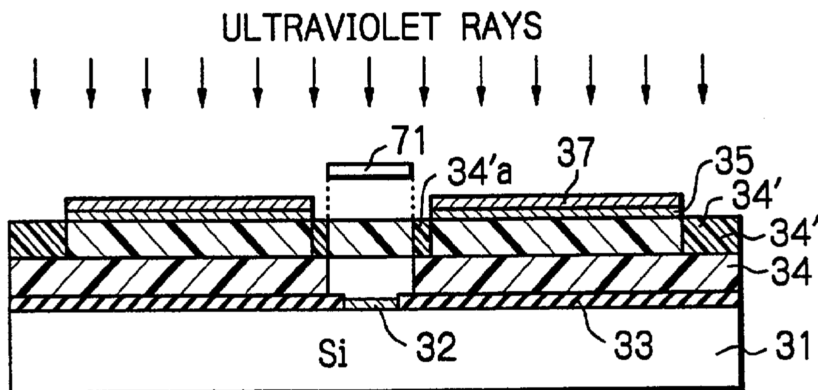


Fig. 14M

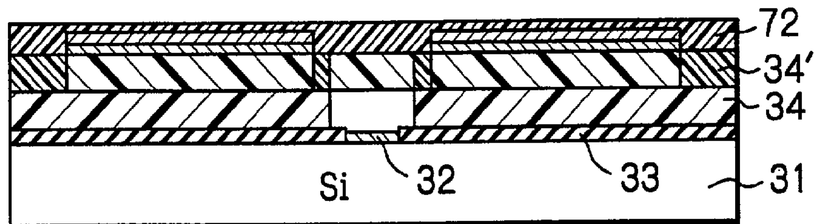


Fig. 14N

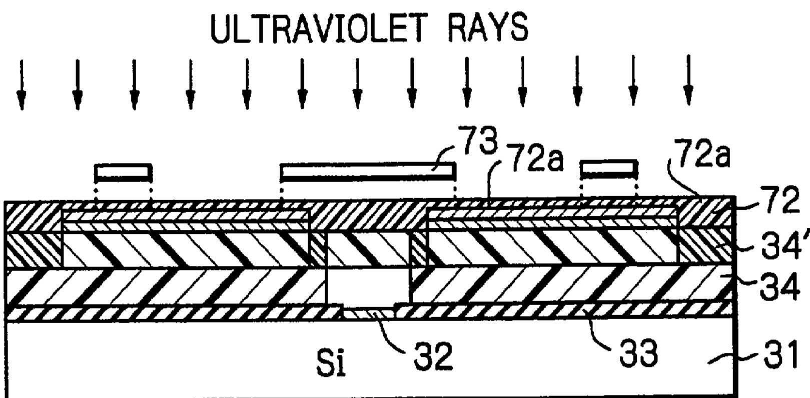


Fig. 14O

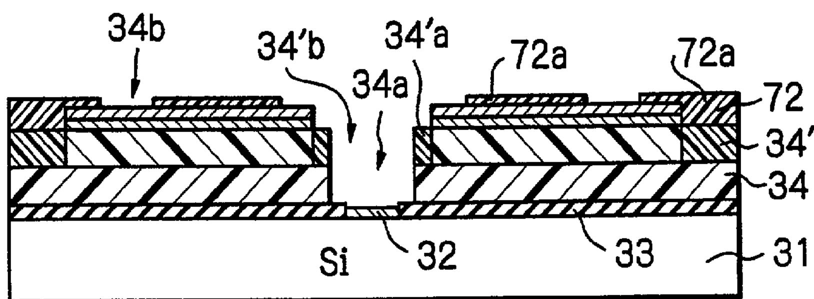


Fig. 14P

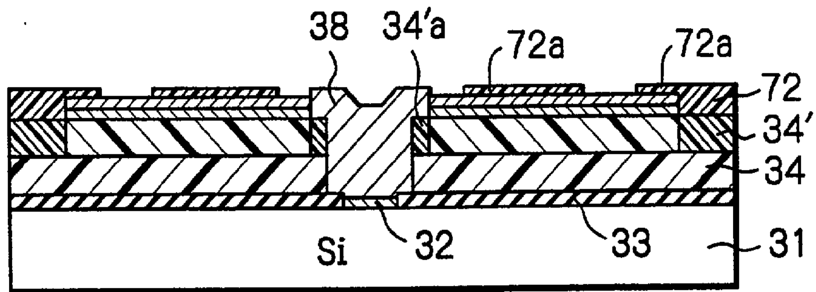
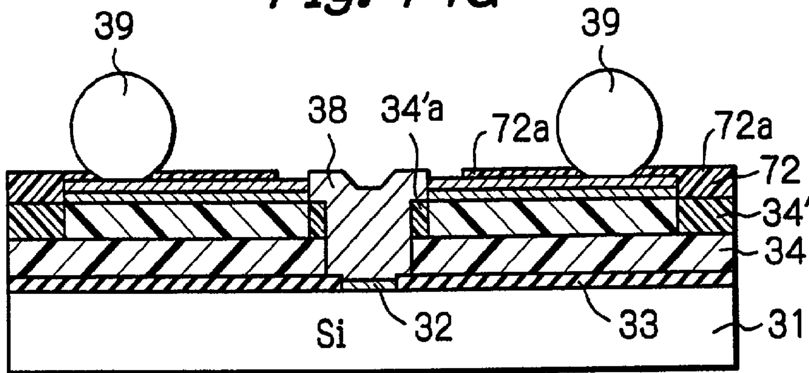


Fig. 14Q



FLIP-CHIP TYPE SEMICONDUCTOR DEVICE WITH STRESS-ABSORBING LAYER MADE OF THERMOSETTING RESIN, AND ITS MANUFACTURING METHOD

5 BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a flip-chip type semiconductor device and its manufacturing method, and more particularly, to the improvement of reducing stress strain
10 within the flip-chip type semiconductor device.

Description of the Related Art

Recently, flip-chip type semiconductor devices have been developed to meet the requirements of higher performance, smaller and lighter size and higher speed for
15 electronic equipment.

Generally, a flip-chip type semiconductor device having metal bumps is directly mounted on a motherboard having electrodes corresponding to the metal bumps. That is, if the metal bumps are solder balls, the solder balls are reflown and
20 soldered on the motherboard. In this case, a stress strain occurs due to the discrepancy in thermal expansion coefficient between the semiconductor device and the motherboard, which will deteriorate the reliability characteristics of the semiconductor device. This will be explained later in detail.

25 In order to minimize the above-mentioned discrepancy in thermal expansion coefficient, the motherboard is made of ceramic material such as aluminum nitride (AlN), mullite or glass ceramics, which has a thermal expansion coefficient close to that of silicon. In this case, however,
30 the motherboard becomes more expensive, and therefore, its application is limited to high-priced equipment such as a super computer and a large-scale computer.

On the other hand, in order to disperse shearing stress occurring at the metal bumps to substantially reduce
35 the above-mentioned stress strain, under-fill resin is inserted between the semiconductor device and the motherboard (see JP-A-9-92685). In this case, however, if voids may be

generated within the under-fill resin or if the adhesive characteristics between the under-fill resin and the semiconductor device (or the motherboard) are deteriorated, the semiconductor device will be separated from the
5 motherboard.

In other approaches to disperse shearing stress occurring at the metal bumps to substantially reduce the above-mentioned stress strain, an elastic layer made of rubber or expandable styrene is provided on the semiconductor device
10 (see JP-A-11-40613, JP-A-11-74309). This also will be explained later in detail.

In the above-mentioned approaches, however, since the elastic layer includes much contamination, the reliability of the semiconductor device will be
15 deteriorated.

SUMMARY OF THE INVENTION

It is an object of the preferred embodiments of the present invention to provide a reliable flip-flop type
20 semiconductor device and its manufacturing method.

According to the present invention, in a flip-chip type semiconductor device, a plurality of pad electrodes are formed on a semiconductor substrate. An insulating stress-absorbing resin layer made of thermosetting resin is formed on
25 the semiconductor substrate and has openings corresponding to the pad electrodes. A plurality of flexible conductive members are filled in the openings. A plurality of metal bumps are formed on the flexible conductive layers.

Since the thermosetting resin has little
30 contamination, the reliability of the flip-chip type semiconductor device is improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred features of the present invention will
35 now be described, by way of example only, with reference to the accompanying drawings, in which:-

Figs. 1A, 1B and 1C are views for explaining a method for mounting a flip-chip type semiconductor device on a motherboard;

Figs. 2A through 2J are cross-sectional views for explaining a first embodiment of the method for manufacturing a flip-chip type semiconductor device;

Fig. 3 is a plan view of one flip-chip type semiconductor device obtained by the method as illustrated in Figs. 2A through 2J;

Fig. 4 is a detailed plan view of the flip-chip type semiconductor device of Fig. 3;

Figs. 5A through 5F are cross-sectional views for explaining a second embodiment of the method for manufacturing a flip-chip type semiconductor device;

Figs. 6A through 6N are cross-sectional views for explaining a third embodiment of the method for manufacturing a flip-chip type semiconductor device;

Fig. 7 is a plan view of one flip-chip type semiconductor device obtained by the method as illustrated in Figs. 6A through 6N;

Figs. 8A through 8N are cross-sectional views for explaining a fourth embodiment of the method for manufacturing a flip-chip type semiconductor device;

Figs. 9A, 9B and 9C are cross-sectional views illustrating a modification of the third embodiment as illustrated in Figs. 6A through 6N;

Figs. 10A, 10B and 10C are cross-sectional views illustrating a modification of the fourth embodiment as illustrated in Figs. 8A through 8N;

Figs. 11A through 11E are cross-sectional views illustrating another modification of the third and fourth embodiments as illustrated in Figs. 6A through 6N and Figs. 8A through 8N;

Figs. 12A through 12E are cross-sectional views illustrating another modification of the third and fourth embodiments as illustrated in Figs. 6A through 6N and Figs. 8A through 8N;

Figs. 13A through 13M are cross-sectional views for explaining a fifth embodiment of the method for manufacturing a flip-chip type semiconductor device; and

Figs. 14A through 14Q are cross-sectional views for
5 explaining a sixth embodiment of the method for manufacturing a flip-chip type semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments,
10 prior art flip-chip type semiconductor devices will be explained with reference to Figs. 1A, 1B and 1C.

Figs. 1A, 1B and 1C are views for explaining a method for mounting a flip-chip type semiconductor device on a motherboard.

15 First referring to Fig. 1A, a flip-chip type semiconductor device 101 having metal bumps 102 and a mother board 103 having electrodes (not shown) corresponding to the metal bumps 102 are prepared. Note that the motherboard 103 is prepared by a user.

20 Next, referring to Fig. 1B, the type semiconductor device 101 is mounted on the motherboard 103. Note that, if the metal bumps 102 are solder balls, the solder balls are reflown at a temperature below a predetermined temperature and soldered on the motherboard 103. In this case, a stress strain
25 occurs due to the discrepancy in thermal expansion coefficient between the semiconductor device 101 and the motherboard 103, which would deteriorate the reliability characteristics of the semiconductor device 101.

In order to minimize the discrepancy in thermal
30 expansion coefficient between the semiconductor device 101 and the motherboard 103, the motherboard 103 may be made of ceramic material such as aluminum nitride (AlN), mullite or glass ceramics, which has a thermal expansion coefficient close to that of silicon. In this case, however, the
35 motherboard 103 becomes more expensive, and therefore, its application is limited to high-priced equipment such as a super computer and a large scale computer.

On the other hand, in order to disperse shearing stress occurring at the metal bumps 102 to substantially reduce the above-mentioned stress strain, under-fill resion is inserted between the semiconductor device 101 and the motherboard 103 (see JP-A-9-92685). In JP-A-9-92685, note that under-fill is inserted between a flip-chip type semiconductor device and an interposer substrate. In this case, however, if voids may be generated within the under-fill resin or if the adhesive characteristics between the under-fill resin and the semiconductor device 101 (or the motherboard 103) are deteriorated, the semiconductor device 101 would be separated from the motherboard 103.

In other approaches to disperse shearing stress occurring at the metal bumps 102 to substantially reduce the above-mentioned stress strain, an elastic layer made of rubber or expandable styrene is provided on the semiconductor device (see JP-A-11-40613, JP-A-11-74309).

In the state as illustrated in Fig. 1B, if an open state or a short-circuit state is generated by a defective soldering process, the semiconductor device 101 is separated and detached by a special heating tool 104 as illustrated in Fig. 1C. In this case, the metal bumps 102 are damaged. Therefore, the metal bumps 102 are repaired, and the semiconductor device 101 can be reused.

However, in a case where under-fill is used, the semiconductor device 101 per se may be damaged, so that it is impossible to reuse the semiconductor device 101. Additionally, the motherboard 103 may also be damaged.

Further, in a case where an elastic layer is made of rubber or expansible styrene, since the elastic layer includes much contamination, the reliability of the semiconductor device 101 would be deteriorated.

A first embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 2A through 2J.

First, referring to Fig. 2A, pad electrodes 12 made

of aluminum (Al) or copper (Cu) are formed on a silicon substrate 11. Then, a passivation layer 13 made of non-organic material such as silicon oxide (SiO_2) or organic material such as polyimide is deposited on the silicon substrate 11 to
5 protect active areas thereof.

Next, referring to Fig. 2B, an insulating stress-absorbing resin layer 14 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin,
10 naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 14 is approximately from 0.01 to 8 GPa.

Next, referring to Fig. 2C, a photoresist layer is
15 coated on the insulating stress-absorbing resin layer 14 and is patterned by a photolithography process to form a photoresist pattern layer 15 which has openings corresponding to the pad electrodes 12.

Next, referring to Fig. 2D, the insulating
20 stress-absorbing resin layer 14 is perforated by a wet etching process, a plasma etching process or a laser process using the photoresist pattern layer 15 as a mask, to form openings 14a, thus exposing the pad electrodes 12. Note that, if the insulating stress-absorbing resin layer 14 is made of material
25 which can be subjected to a chemical etching process, the wet etching process can be used. On the other hand, if the insulating stress-absorbing resin layer 14 is made of material which cannot be subjected to a chemical etching process, the plasma etching process or the laser process can be used.

30 Next, referring to Fig. 2E, the photoresist pattern layer 15 is removed to expose the insulating stress-absorbing resin layer 14. Then, the device is subjected to a plasma surface treatment using inert gas such as Ar gas under a low pressure atmosphere. As a result, the remainder of the
35 insulating stress-absorbing resin layer 14 on the pad electrodes 12 is completely removed, and also metal oxide on the surface of the pad electrodes is removed.

Next, referring to Fig. 2F, a flexible conductive layer 16 is coated on the insulating stress-absorbing resin layer 14 by a screen printing method or the like, so that the flexible conductive layer 16 is filled in the openings 14a, 5 thus preventing the pad electrodes 12 from being oxidized. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent 10 flexibility characteristics.

Next, referring to Fig. 2G, the flexible conductive layer 16 is flattened by a chemical mechanical polishing (CMP) process, so that the flexible conductive layer 16 is filled only in the openings 14a. In this case, a plasma surface 15 treatment may be carried out to remove polishing waste caused by the CMP process.

Next, referring to Fig. 2H, an electroless Cu plating process or an electroless Ni plating process is carried out to form land portions (not shown) on the pad 20 electrodes 12. The land portions can be formed by carrying out an electroless Au plating process after an electrolytic Cu plating process. Then, metal bumps (solder balls) 17 made of Sn and Pb are soldered to the pad electrodes 12 via the land portions. Thus since the land portions improves the 25 wettability of the metal bumps 17, the metal bumps 17 can be securely adhered to the pad electrodes 12.

In Fig. 2H, flux (not shown) instead of the land portions can be coated on the pad electrodes 12, and then, metal bumps 17 are soldered to the pad electrodes 12 and a 30 heating reflowing process is performed thereupon. Even in this case, the metal bumps 17 can be securely adhered to the pad electrodes 12.

Note that the metal bumps 17 can be made of Au or Sn-Ag alloy.

35 Next, referring to Fig. 2I, the device is cut by a dicing blade 18 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 2J.

One of the flip-chip type semiconductor chips obtained by the manufacturing method as illustrated in Figs. 2A through 2J is illustrated in Fig. 3. In Fig. 3, the pad electrodes 12 are arranged at the periphery of the flip-chip type semiconductor chip and are surrounded by the insulating stress-absorbing resin layer 14, and the metal bumps 17 are arranged on the pad electrodes 12. Actually, the number of the pad electrodes 12 is very large as illustrated in Fig. 4.

According to the above-described first embodiment, since the insulating stress-absorbing resin layer 12 and the flexible conductive layer 16 disperse shearing stress occurring at the metal bumps 17, the reliability of the flip-chip type semiconductor device would be improved. Additionally, since the insulating stress-absorbing resin layer 12 is made of thermosetting resin which includes little contamination, the flip-chip type semiconductor device would be further improved.

A second embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 5A through 5F.

After the steps as illustrated in Figs. 2A through 2D of the first embodiment are carried out, referring to Fig. 5A, conductive wire 21 made of Au or Cu is connected to the pad electrodes 12 via conductive adhesives (not shown) by a wire bonding process.

Next, referring to Fig. 5B, in a similar way to those of Fig. 2F, a flexible conductive layer 16 is coated on the insulating stress-absorbing resin layer 14 by a screen printing method or the like, so that the flexible conductive layer 16 is filled in the openings 14a, to completely cover the conductive wire 21. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

Next, referring to Fig. 5C, in the same way in Fig. 2G, the flexible conductive layer 16 is flattened by a CMP process, so that the flexible conductive layer 16 is filled only in the openings 14a. In this case, a plasma surface treatment may be carried out to remove polishing waste caused by the CMP process.

Next, referring to Fig. 5D, in the same way as in Fig. 2H, an electroless Cu plating process or an electroless Ni plating process is carried out to form land portions (not shown) on the pad electrodes 12. The land portions can be formed by carrying out an electroless Au plating process after an electrolytic Cu plating process. Then, metal bumps (solder balls) 17 made of Sn and Pb are soldered to the pad electrodes 12 via the land portions. Thus, since the land portions improves the wettability of the metal bumps 17, the metal bumps 17 can be securely adhered to the pad electrodes 12.

Even in Fig. 5D, in the same way as in Fig. 2H, flux (not shown) instead of the land portions can be coated on the pad electrodes 12, and then, metal bumps 17 are soldered to the pad electrodes 12 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 17 can be securely adhered to the pad electrodes 12.

Note that the metal bumps 17 can be made of Au or Sn-Ag alloy.

Next, referring to Fig. 5E, in the same way as in Fig. 2I, the device is cut by a dicing blade 18 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 5F.

Thus, in the second embodiment, the metal bumps 17 can be more surely electrically-connected to the pad electrodes 12 due to the presence of the conductive wire 21 as compared with the first embodiment.

A third embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 6A through 6N.

First, referring to Fig. 6A, in the same way as in

Fig. 2A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 33 made of non-organic material such as silicon oxide (SiO_2) or organic material such as polyimide is deposited on the
5 silicon substrate 31 to protect active areas thereof.

Next, referring to Fig. 6B, in the same way as in Fig. 2B, an insulating stress-absorbing resin layer 34 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin,
10 phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 34 is approximately from 0.01 to 8 GPa.

Next, referring to Fig. 6C, a Cu layer 35 is
15 deposited on the insulating stress-absorbing resin layer 34.

Note that other metal such as nickel can be used for the layer 37.

Next, referring to Fig. 6D, a photoresist layer is coated on the entire surface, and then, the photoresist layer
20 is patterned by a photolithography process to form a photoresist pattern layer 36.

Next, referring to Fig. 6E, an An plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

25 Note that other metal such as nickel can be used for the layer 37.

Next, referring to Fig. 6F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

30 Next, referring to Fig. 6G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

Next, referring to Fig. 6H, a photoresist pattern layer 38, which has openings corresponding to the pad
35 electrodes 32, is formed by a photolithography process.

Next, referring to Fig. 6I, the insulating stress-absorbing resin layer 34 is etched by using the

photoresist pattern layer 38 as a mask, to form openings 34a in the insulating stress-absorbing resin layer 34.

Next, referring to Fig. 6J, the photoresist pattern layer 38 is removed.

5 Next, referring to Fig. 6K, a flexible conductive layer 38 is coated by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the openings 34a, thus preventing the pad electrodes 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 10 37 are electrically connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent 15 solder-wettability characteristics as well as excellent flexibility characteristics.

Note that a solder-resist layer or a resin layer can be coated on the portions of the Au layer 37 where metal bumps will be formed. Thus, the Au layer 37 can be protected by the 20 solder-resist layer or the resin layer to improve the waterproof characteristics thereof.

Referring to Fig. 6L, metal bumps 39 are soldered to the Au layer 37 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be 25 securely adhered to the Au layer 37.

Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

Next, referring to Fig. 6M, the device is cut by a dicing blade 40 to separate flip-chip type semiconductor chips 30 (pellets) from each other, as illustrated in Fig. 2N.

One of the flip-chip type semiconductor chips obtained by the manufacturing method as illustrated in Figs. 6A through 6N is illustrated in Fig. 7. In Fig. 7, although the pad electrodes 32 are arranged at the periphery of the 35 flip-chip type semiconductor chip and then surrounded by the insulating stress-absorbing resin layer 34 in the same way as in the first embodiment, the metal bumps 39 are arranged in

an inner area of the flip-chip type semiconductor chip as compared with the metal bumps 25 of Fig. 3, which would prevent the metal bumps 39 from being short-circuited.

A fourth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 8A through 8N.

First, referring to Fig. 8A, in the same way as in Fig. 6A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 32 made of non-organic material such as silicon oxide (SiO_2) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

Next, referring to Fig. 8B, in the same way as in Fig. 6B, an insulating stress-absorbing resin layer 34 made of thermosetting resin such as epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 34 is approximately from 0.01 to 8 GPa.

Next, referring to Fig. 8C, a photoresist pattern layer 41, which has openings corresponding to the pad electrodes 32, is formed by a photolithography process.

Next, referring to Fig. 8D, the insulating stress-absorbing resin layer 34 is etched by using the photoresist pattern layer 41 as a mask. As a result, openings 34 corresponding to the pad electrodes 32 are perforated in the insulating stress-absorbing resin layer 34.

Next, referring to Fig. 8E, the photoresist pattern layer 41 is removed.

Next, referring to Fig. 8F, in a similar way to that of Fig. 6C, a Cu layer 35 is formed on the insulating stress-absorbing resin layer 34 by using a film laminating method or a pressing method.

Note that other metal such as nickel can be used for the layer 37.

Next, referring to Fig. 8G, in the same way as in Fig. 6D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 5 36.

Next, referring to Fig. 8H, in the same way as in Fig. 6E, an An plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

Note that other metal such as nickel can be used for 10 the layer 37.

Next, referring to Fig. 8I, in the same way as in Fig. 6F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

Next, referring to Fig. 8J, in the same way as in 15 Fig. 6G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

Next, referring to Fig. 8K, in the same way as in Fig. 6K, a flexible conductive layer 38 is coated on the 20 insulating stress-absorbing resin layer 34 by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the openings 34a, thus preventing the pad electrodes 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 37 are electrically 25 connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability 30 characteristics as well as excellent flexibility characteristics.

Note that a solder-resist layer or a resin layer can be coated on the portions of the Au layer 37 where metal bumps will be formed. Thus, the Au layer 37 can be protected by the 35 solder-resist layer or the resin layer to improve the waterproof characteristics.

Referring to Fig. 8L, in the same way as in Fig. 6L,

metal bumps 39 are soldered to the pad electrodes 32 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the pad electrodes 32.

5 Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

Next, referring to Fig. 8M, in the same way as in Fig. 6M, the device is cut by a dicing blade 40 to separate flip-chip type semiconductor chips (pellets) from each other,
10 as illustrated in Fig. 8N.

In the fourth embodiment, although the steps as illustrated in Figs. 8C and 8D are added to the third embodiment, the steps as illustrated in Figs. 6H, 6I and 6J of the third embodiment are omitted, which would decrease the
15 manufacturing cost.

A modification of the third embodiment of the present invention will be explained next with reference to Figs. 9A through 9C.

First, referring to Fig. 9A, in the same way as in
20 Fig. 6A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 32 made of non-organic material such as silicon oxide (SiO_2) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

25 Next, referring to Fig. 9B, a resin coated copper (RCC) layer consisting of an insulating stress-absorbing resin layer 34 laminated by a Cu layer 35 is prepared.

Next, referring to Fig. 9C, the RCC layer (34, 35) is adhered to the pad electrodes 32 and the passivation layer
30 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34, 35) has good adhesive characteristics, the RCC layer (34, 35) per se can be easily adhered to the pad electrodes 32 and the passivation layer 33.

After that, the steps as illustrated in Figs. 6D
35 through 6N are carried out to complete a flip-chip type semiconductor chip.

A modification of the fourth embodiment of the

present invention will be explained next with reference to Figs. 9A through 9C.

First, referring to Fig. 10A, in the same way as in Fig. 8A, pad electrodes 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 32 made of non-organic material such as silicon oxide (SiO_2) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

Next, referring to Fig. 10B, an RCC layer consisting of an insulating stress-absorbing resin layer 34 laminated by a Cu layer 35 is prepared. In this case, openings 34a are perforated in the insulating stress-absorbing resin layer 34 in advance by an etching process or the like.

Next, referring to Fig. 10C, the RCC layer (34, 35) is adhered to the pad electrodes 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34, 35) has good adhesive characteristics, the RCC layer (34, 35) per se can be easily adhered to the pad electrodes 32 and the passivation layer 33.

After that, the steps as illustrated in Figs. 8G through 8N are carried out to complete a flip-chip type semiconductor chip.

Another modification of the third and fourth embodiments of the present invention will be explained next with reference to Figs. 11A through 11E. After the steps of Figs. 6A through 6J or the steps of Figs. 8A through 8J are carried out, the steps of Figs. 11A through 11E are carried out.

First, referring to Fig. 11A, conductive wiring 51 made of Au or Cu is formed by using a wire bonding process, to electrically connect the pad electrodes 32 to the Cu layer 35 and the Au layer 37. Note that, the pad electrodes 32 are subjected to a plasma surface treatment before the wire bonding process, to remove etching remainder of the insulating stress-absorbing resin layer 34 on the pad electrodes 32 and oxide thereon, which would improve the wire bonding characteristics.

Next, referring to Fig. 11B, metal bumps 39 are soldered to the pad electrodes 32 and a heating reflowing process is performed thereupon. Even in this case, the metal bumps 39 can be securely adhered to the pad electrodes 32.

5 Next, referring to Fig. 11C, an insulating resin layer 52 is filled in the openings 34a, to mechanically and chemically protect the conductive wiring 51 as well as to enhance the water-vapor proof characteristics.

The insulating resin layer 52 can be made of the same 10 or similar material as that of the insulating stress-absorbing resin layer 34. If the insulating resin layer 52 is liquid, a partial coating process is performed upon the conductive wiring 51 by a potting method. On the other hand, if the insulating resin layer 52 is solid, the conductive wiring 51 15 can be partially sealed by a transfer sealing method using metal molds.

Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

Next, referring to Fig. 11D, the device is cut by 20 a dicing blade 40 to separate flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 11E.

A further modification of the third and fourth embodiments of the present invention will be explained next with reference to Figs. 12A through 12E. After the steps of 25 Figs. 6A through 6J or the steps of Figs. 8A through 8J are carried out, the steps of Figs. 12A through 12E are carried out.

First, referring to Fig. 12A, a conductive layer 61 made of Zn or NiSn is formed by using an electroless plating 30 and etching process, to electrically connect the pad electrodes 32 to Cu layer 35 and the Au layer 37. Note that the conductive layer 61 can be formed by adhering L-shaped conductive members made of Cu, Ni or their alloy by conductive adhesives.

35 Next, referring to Fig. 12B, in the same way as in Fig. 11B metal bumps 39 are soldered to the pad electrodes 32 and a heating reflowing process is performed thereupon. Even

in this case, the metal bumps 39 can be securely adhered to the pad electrodes 32.

Next, referring to Fig. 12C, in the same way as in Fig. 11C, an insulating resin layer 52 is filled in the
5 openings 34a, to mechanically and chemically protect the conductive wiring 51 as well as to enhance the water-vapor proof characteristics.

The insulating resin layer 52 can be made of the same or similar material as that of the insulating stress-absorbing
10 resin layer 34. If the insulating resin layer 52 is liquid, a partial coating process is performed upon the conductive wiring 51 by a potting method. On the other hand, if the insulating resin layer 52 is solid, the conductive wiring 51 can be partially sealed by a transfer sealing method using
15 metal molds.

Note that the metal bumps 39 can be made of Au or Sn-Ag alloy.

Next, referring to Fig. 12D, in the same way as in Fig. 11D, the device is cut by a dicing blade 40 to separate
20 flip-chip type semiconductor chips (pellets) from each other, as illustrated in Fig. 12E.

A fifth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 13A
25 through 13N.

First, referring to Fig. 13A, in the same way as in Fig. 9A, pad electrode 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 33 made of non-organic material such as silicon oxide (SiO_2)
30 or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

Next, referring to Fig. 13B, an (RCC) layer consisting of a photosensitive insulating stress-absorbing resin layer 34' laminated by a Cu layer 35 is prepared. The
35 photosensitive insulating stress-absorbing layer 14' is made of the above-mentioned thermosetting resin added by photosensitive material such as bisazide compound or

thodiazo-naphthoquinone compound.

Next, referring to Fig. 13C, in the same way as in Fig. 9C, the RCC layer (34', 35) is adhered to the pad electrodes 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34', 35) has good adhesive characteristics the RCC layer (34', 35) per se can be easily adhered to the pad electrodes 32 and the passivation layer 33.

Next, referring to Fig. 13D, in the same way as in Fig. 6D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 36.

Next, referring to Fig. 13E, in the same way as in Fig. 6E, an Au plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

Note that other metal such as nickel can be used for the layer 37.

Next, referring to Fig. 13F, in the same way as in Fig. 6F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

Next, referring to Fig. 13G, in the same way as in Fig. 6G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

Next, referring to Fig. 13H, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 71 corresponding to the pad electrode 32. As a result, if the photosensitive insulating stress-absorbing resin layer 34' is negative, the exposed portions 34'a thereof are hardened.

Next, referring to Fig. 13I, a solder resist layer 72 is coated on the entire surface.

Next, referring to Fig. 13J, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 73 corresponding to the pad electrode 32 and a metal bump which will be formed later. As a result, if the solder resist layer 72 is negative, the exposed portions 72a thereof are hardened.

Next, referring to Fig. 13K, the device is subjected to a developing process, i.e., a chemical etching process using tetraethyl ammonium hydroxide (TMAH) solution. As a result, the unexposed portion of the photosensitive
5 insulating stress-absorbing resin layer 34' and the unexposed portion of the solder resist layer 72 are simultaneously removed. Thus, an opening 34'b is perforated in the photosensitive insulating stress-absorbing resin layer 34', and an opening 72b is perforated in the solder resist layer
10 72. Then, a high-temperature curing operation is performed upon the device to react the thermosetting components of the photosensitive insulating stress-absorbing resin layer 34' and the solder resist layer 72.

Next, referring to Fig. 13L, in the same way as in
15 Fig. 6K, a flexible conductive layer 38 is coated by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the openings 34'a, thus preventing the pad electrode 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 37 are electrically
20 connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability
25 characteristics as well as excellent flexibility characteristics.

Referring to Fig. 13N, in the same way as in Fig. 6L, metal bumps 39 are soldered to the Au layer 37 and a heating reflowing process is performed thereupon. Even in this case,
30 the metal bump 39 can be securely adhered to the Au layer 37.

Note that the metal bump 39 can be made of Au or Sn-Ag alloy.

Finally, the device is cut by a dicing blade (not shown) to separate flip-chip type semiconductor chips
35 (pellets) from each other.

In the fifth embodiments as illustrated in Figs. 13A through 13M, since the steps as illustrated in Figs. 6H and

6I are unnecessary, the manufacturing steps can be simplified.

In the fifth embodiment, the steps of Figs. 6B and 6C can be used instead of the steps of Figs. 13B and 13C. Also, the conductive wiring 51 of Figs. 11A through 11E or the
5 conductive layer 61 of Figs. 12A through 12E can be used instead of the conductive layer 38.

A sixth embodiment of the method for manufacturing a flip-chip type semiconductor device according to the present invention will be explained next with reference to Figs. 14A
10 through 14N.

First, referring to Fig. 14A, in the same way as in Fig. 8A, a pad electrode 32 made of aluminum (Al) or copper (Cu) are formed on a silicon substrate 31. Then, a passivation layer 33 made of non-organic material such as silicon oxide
15 (SiO_2) or organic material such as polyimide is deposited on the silicon substrate 31 to protect active areas thereof.

Next, referring to Fig. 14B, in the same way as in Fig. 8B, an insulating stress-absorbing resin layer 34 made of thermosetting resin such as epoxy resin, silicone resin,
20 polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin or fluorene resin is coated on the entire surface by a spin-coating process. Note that the modulus of elasticity of the insulating stress-absorbing resin layer 34 is approximately from 0.01 to 8 GPa.

25 Next, referring to Fig. 14C, in the same way as in Fig. 8C, a photoresist pattern layer 41, which has a opening corresponding to the pad electrode 32, is formed by a photolithography process.

Next, referring to Fig. 14D, in the same way as in
30 Fig. 8D, the insulating stress-absorbing resin layer 34 is etched by using the photoresist pattern layer 41 as a mask. As a result, an opening 34a corresponding to the pad electrode 32 is perforated in the insulating stress-absorbing resin layer 34.

35 Next, referring to Fig. 14E, in the same way as in Fig. 8E, the photoresist pattern layer 41 is removed.

Note that, if the insulating stress-absorbing resin

layer 34 is photosensitive, the steps of Figs. 14C, 14D and 14E are replaced by an ultraviolet exposing and developing process.

Next, referring to Fig. 14F, in the same way as in Fig. 13B, an (RCC) layer consisting of a photosensitive insulating stress-absorbing resin layer 34' laminated by a Cu layer 35 is prepared.

Next, referring to Fig. 14G, in the same way as in Fig. 13C, the RCC layer (34', 35) is adhered to the pad electrode 32 and the passivation layer 33 by a film laminating method or a pressing method. In this case, since the RCC layer (34', 35) has good adhesive characteristics the RCC layer (34', 35) per se can be easily adhered to the pad electrode 32 and the passivation layer 33.

Next, referring to Fig. 14H, in the same way as in Fig. 13D, a photoresist layer is coated on the entire surface, and then, the photoresist layer is patterned by a photolithography process to form a photoresist pattern layer 36.

Next, referring to Fig. 14I, in the same way as in Fig. 13E, an Au plating layer 37 is formed on the Cu layer 35 through the photoresist pattern layer 36.

Note that other metal such as nickel can be used for the layer 37.

Next, referring to Fig. 14J, in the same way as in Fig. 13F, the photoresist pattern layer 36 is removed. The Au layer 37 serves as lands for metal bumps.

Next, referring to Fig. 14K, in the same way as in Fig. 13G, the Cu layer 35 is etched by a wet etching process using ferric chloride or sulfuric acid and the Au layer 37 as a mask.

Next, referring to Fig. 14L, in the same way as in Fig. 13H, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 71 corresponding to the pad electrode 32. As a result, if the photosensitive insulating stress-absorbing resin layer 34' is negative, the exposed portions 34'a thereof are hardened.

Next, referring to Fig. 14M, in the same way as in Fig. 13I, a solder resist layer 72 is coated on the entire surface.

Next, referring to Fig. 14N, in the same way as in Fig. 13I, the device is exposed to ultraviolet rays from a mercury lamp using an exposure mask 73 corresponding to the pad electrode 32 and a metal bump which will be formed layer. As a result, if the solder resist layer 72 is negative, the exposed portions 72a thereof are hardened.

Next, referring to Fig. 14O, in the same way as in Fig. 13J, the device is subjected to a developing process, i.e., a chemical etching process using TMAH solution. As a result, the unexposed portion of the photosensitive insulating stress-absorbing resin layer 34' and the unexposed portion of the solder resist layer 72 are simultaneously removed. Thus, an opening 34'b leading to the opening 34a is perforated in the photosensitive insulating stress-absorbing resin layer 34', and an opening 72b is perforted in the solder resist layer 72. Then, a high-temperature curing operation is performed upon the device to react the thermosetting components of the photosensitive insulating stress-absorbing resin layer 34' and the solder resist layer 72.

Next, referring to Fig. 14P, in the same way as in Fig. 13K, a flexible conductive layer 38 is coated by a screen printing method or a potting method, so that the flexible conductive layer 38 is filled only in the opening 34'b as well as in the opening 34a, thus preventing the pad electrode 32 from being oxidized. As a result, the Cu layer 35 and the Au layer 37 are electrically connected to the corresponding pad electrode 32 via the flexible conductive layer 38. The flexible conductive layer 16 is made of powdered material of at least one of copper (Cu), lead (Pb), tin (Sn), nickel (Ni), palladium (Pd), silver (Ag) or gold (Au), that shows excellent solder-wettability characteristics as well as excellent flexibility characteristics.

Referring to Fig. 14Q, in the same way as in Fig. 13L, metal bumps 39 are soldered to the Au layer 37 and a

heating reflowing process is performed thereupon. Even in this case, the metal bump 39 can be securely adhered to the Au layer 37.

Note that the metal bump 39 can be made of Au or Sn-Ag alloy.

Finally, the device is cut by a dicing blade (not shown) to separate flip-chip type semiconductor chips (pellets) from each other.

In the sixth embodiments as illustrated in Figs. 13A through 13L, since the insulating stress-absorbing resin layer (34, 34′) is much thicker than the insulating stress-absorbing resin layer 34′ in the fifth embodiment, the stress strain due to the discrepancy in thermal expansion coefficient between the device and a motherboard or the like can be remarkably reduced.

As explained hereinabove, according to the present invention, since an elastic layer for reducing the stress strain due to the discrepancy in thermal expansion coefficient is made of thermosetting resin with little contamination, the reliability of flip-chip type semiconductor devices can be improved.

While the present invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation, and that changes may be made to the invention without departing from its scope as defined by the appended claims.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features. Reference numerals appearing in the claims are by way of illustration only and shall be disregarded when interpreting the scope of the claims.

The text of the abstract filed herewith is repeated here as part of the specification.

In a flip-chip type semiconductor device, a plurality of pad electrodes are formed on a semiconductor substrate. An insulating stress-absorbing resin layer made of thermosetting resin is formed on the semiconductor
5 substrate and has openings corresponding to the pad electrodes. A plurality of flexible conductive members are filled in the openings. A plurality of metal bumps are formed on the flexible conductive layers.

CLAIMS

1. A flip-chip type semiconductor device, comprising:
a semiconductor substrate (11, 31);
a plurality of pad electrodes (12, 32) formed on said semiconductor substrate;
an insulating stress-absorbing resin layer (14, 34, 34') made of thermosetting resin, formed on said semiconductor substrate and having openings (14a,34a) corresponding to said pad electrodes;
a plurality of flexible conductive members (16, 21, 36, 38, 51, 61) each filling one of said openings; and,
a plurality of metal bumps (17) each formed on one of said flexible conductive layers.

2. The flip-chip type semiconductor device as set forth in claim 1, wherein said thermosetting resin is one of epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin and fluorene resin.

3. The flip-chip type semiconductor device as set forth in claim 1, wherein said flexible conductive members (16, 36) are made of powered material including at least one of Cu, Pb, Sn, Ni, Pd, Ag and Au.

4. The flip-chip type semiconductor device as set forth in claim 1, further comprising a plurality of conductive wires (21) each included in one of said flexible conductive members.

5. The flip-chip type semiconductor device as set forth in claim 1, further comprising a plurality of conductive members (35, 37) formed between said insulating stress-absorbing resin layer and one of said metal bumps, each of said conductive members being electrically connected to one of said flexible conductive members.

6. The flip-chip type semiconductor device as set forth in claim 1, further comprising a plurality of conductive members (35, 37) formed between said insulating stress-absorbing resin layer and one of said metal bumps,

each of said flexible conductive members comprising a bonding wire (51).

7. The flip-chip type semiconductor device as set forth in claim 1, further comprising a plurality of conductive members (35, 37) formed between said insulating stress-absorbing resin layer and one of said metal bumps,

each of said flexible conductive members comprising an electroless plating layer (61).

8. The flip-chip type semiconductor device as set forth in claim 1, wherein said insulating stress-absorbing resin layer (34') is photosensitive.

9. The flip-chip type semiconductor device as set forth in claim 5, further comprising a photosensitive insulating stress-absorbing resin layer (34') between said insulating stress-absorbing resin layer and said conductive members.

10. A flip-chip type semiconductor device, comprising:

a semiconductor substrate (31);

a plurality of pad electrodes (32) formed on said semiconductor substrate;

a first insulating stress-absorbing resin layer (34) formed on said semiconductor substrate and having first openings (34a) corresponding to said pad electrodes;

a second insulating stress-absorbing resin layer (34') formed on said first insulating stress-absorbing resin layer and having second openings (34'b) corresponding to said first openings, said second insulating stress-absorbing resin layer being photosensitive so that sidewalls of said second insulating stress-absorbing resin layer within said second openings are hardened by light rays;

a plurality of conductive members (35, 37) formed on said second insulating stress-absorbing resin layer;

a plurality of flexible conductive members (38) each filling said first and second openings, and electrically connecting said conductive members to respective ones of said pad electrodes; and,

a plurality of metal bumps (39) each formed on one of said conductive members.

11. The flip-chip type semiconductor device as set forth in claim 10, further comprising a solder resist layer (72a) formed on said conductive members.

12. A method for manufacturing a flip-chip type semiconductor device, comprising the steps of:

forming a plurality of pad electrodes (12, 32) on a semiconductor substrate (11, 31);

forming an insulating stress-absorbing resin layer (14, 34, 34') made of thermosetting resin on said semiconductor substrate, said insulating stress-absorbing resin layer having openings (14a, 34a) corresponding to said pad electrodes;

forming flexible conductive members (16, 21, 36, 38, 51, 61) each filling one of said openings; and

forming a plurality of metal bumps (17) each formed on one of said flexible conductive layers.

13. The method as set forth in claim 12, wherein said thermosetting resin is one of epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin and fluorene resin.

14. The method as set forth in claim 12, wherein said insulating stress-absorbing resin layer forming step comprises the steps of:

coating an insulating stress-absorbing resin layer by a spin-coating process; and

patterning said insulating stress-absorbing resin layer by a photolithography and wet etching process.

15. The method as set forth in claim 12, wherein said flexible conductive members (16, 36) are made of powered material including at least one of Cu, Pb, Sn, Ni, Pd, Ag and Au.

16. The method as set forth in claim 12, further comprising a step of forming a plurality of conductive wire (21) each included in one of said flexible conductive members.

17. The method as set forth in claim 12, further

comprising a step of forming a plurality of conductive members (35, 37) formed between said insulating stress-absorbing resin layer and one of said metal bumps, each of said conductive members being electrically connected to one of said flexible conductive members.

18. The method as set forth in claim 12, further comprising a step of forming a plurality of conductive members (35, 37) formed between said insulating stress-absorbing resin layer and one of said metal bumps,

each of said flexible conductive members comprising a bonding wire (51).

19. The method as set forth in claim 12, further comprising a step of forming a plurality of conductive members (35, 37) formed between said insulating stress-absorbing resin layer and one of said metal bumps,

each of said flexible conductive members comprising a bonding wire (61).

20. The method as set forth in claim 12, where said insulating stress-absorbing resin layer (34') is photosensitive.

21. The method as set forth in claim 17, further comprising a step of forming a photosensitive insulating stress-absorbing resin layer (34') between said insulating stress-absorbing resin layer and said conductive members.

22. A method for manufacturing a flip-chip type semiconductor device, comprising the steps of:

forming a plurality of pad electrodes (32) on a semiconductor substrate (31);

adhering a resin coated conductive layer (34, 35) on said semiconductor substrate, said resin coated conductive layer comprising an insulating stress-absorbing resin layer (34) made of thermosetting resin laminated by a first conductive layer (35);

forming a second conductive layer (37) having a pattern on said first conductive layer;

perforating said first conductive layer by using said second conductive layer as a mask;

etching said insulating stress-absorbing resin layer using said first and second conductive layers as a mask, so that said insulating stress-absorbing resin layer has openings corresponding to said pad electrodes;

5 forming flexible conductive members (21, 36, 38, 51, 61) each filling one of said openings and electrically connecting said first and second conductive layers to respective one of said pad electrodes; and

forming a plurality of metal bumps (39) formed

10 on said second conductive layer.

23. The method as set forth in claim 22, wherein said thermosetting resin is one of epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin and fluorene resin.

15 24. The method as set forth in claim 22, wherein said flexible conductive members (36) are made of powered material including at least one of Cu, Pb, Sn, Ni, Pd, Ag and Au.

25. The method as set forth in claim 22, further comprising a step of forming a plurality of conductive wire

20 (21) each included in one of said flexible conductive members.

26. The method as set forth in claim 22, wherein each of said flexible conductive members comprises a bonding wire (51).

27. The method as set forth in claim 22, where each of

25 said flexible conductive members comprises an electroless plating layer (61).

28. The method as set forth in claim 22, wherein said insulating stress-absorbing resin layer (34') is photosensitive.

30 29. The method as set forth in claim 22, further comprising a step of forming a photosensitive insulating stress-absorbing resin layer (34') between said insulating stress-absorbing resin layer and said first conductive layer.

30. A method for manufacturing a flip-chip type

35 semiconductor device, comprising the steps of:

forming a plurality of pad electrodes (32) on a semiconductor substrate (31);

adhering a resin coated conductive layer (34, 35) on said semiconductor substrate, said resin coated conductive layer comprising an insulating stress-absorbing resin layer (34) made of thermosetting resin laminated by a
5 first conductive layer (35), said insulating stress-absorbing resin layer having openings (34a) corresponding to said pad electrodes;

forming a second conductive layer (37) having a pattern on said first conductive layer;

10 perforating said first conductive layer by using said second conductive layer as a mask, so that said first and second conductive layers have openings corresponding to the openings of said insulating stress-absorbing resin layer;

15 forming flexible conductive members (21, 36, 38, 51, 61) each filling one of said openings and electrically connecting said first and second conductive layers to respective ones of said pad electrodes; and

forming a plurality of metal bumps (39) formed
20 on said second conductive layer.

31. The method as set forth in claim 30, wherein said thermosetting resin is one of epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin and fluorene resin.

25 32. The method as set forth in claim 30, wherein said flexible conductive members (36) are made of powered material including at least one of Cu, Pb, Sn, Ni, Pd, Ag and Au.

33. The method as set forth in claim 30, further comprising a step of forming a plurality of conductive wires
30 (21) each included in one of said flexible conductive members.

34. The method as set forth in claim 30, wherein each of said flexible conductive members comprises a bonding wire (51).

35. The method as set forth in claim 30, wherein each
35 of said flexible conductive members comprises an electroless plating layer (61).

36. The method as set forth in claim 30, wherein said

insulating stress-absorbing resin layer (34') is photosensitive.

37. The method as set forth in claim 30, further comprising a step of forming a photosensitive insulating stress-absorbing resin layer (34') between said insulating stress-absorbing resin layer and said first conductive layer.

38. A method for manufacturing a flip-chip type semiconductor device, comprising the steps of:

forming a plurality of pad electrodes (32) on a semiconductor substrate (31);

adhering a resin coated conductive layer (34', 35) on said semiconductor substrate, said resin coated conductive layer comprising a photosensitive insulating stress-absorbing resin layer (34') made of thermosetting resin laminated by a first conductive layer (35), said insulating stress-absorbing resin layer having openings (34a) corresponding to said pad electrodes;

forming a second conductive layer (37) having a pattern on said first conductive layer;

perforating said first conductive layer by using said second conductive layer as a mask, so that said first and second conductive layers have openings;

irradiating said photosensitive insulating stress-absorbing resin layer with light by using an exposure mask (71) and said patterned first and second conductive layers so that irradiated portions of said photosensitive stress-absorbing resin layer are hardened;

developing said photosensitive insulating stress-absorbing resin layer so that unirradiated portions of said photosensitive insulating stress-absorbing resin layer aare removed, so that said photosensitive insulating stress-absorbing resin layer has openings corresponding to said pad electrodes;

forming flexible conductive members (21, 36, 38, 51, 61) each filling one of said openings and electrically connecting said first and second conductive layers to respective ones of said pad electrodes; and

forming a plurality of metal bumps (39) formed on said second conductive layer.

39. The method as set forth in claim 38, further comprising the steps of:

coating a photosensitive solder resist layer (72) on said second conductive layer after said photosensitive insulating stress-absorbing resin layer is irradiated; and

irradiating said photosensitive solder resist layer with light by using an exposure mask (73),

said developing step developing said photosensitive solder resist layer so that unirradiated portions of said photosensitive solder resist layer are removed, so that said metal bumps are located where said photosensitive solder resist layer is removed.

40. The method as set forth in claim 39, wherein said thermosetting resin is one of epoxy resin, silicone resin, polyimide resin, polyolefin resin, cyanate-ester resin, phenol resin, naphthalene resin and fluorene resin added by photosensitive material.

41. The method as set forth in claim 38, wherein said flexible conductive members (36) are made of powered material including at least one of Cu, Pb, Sn, Ni, Pd, Ag and Au.

42. The method as set forth in claim 38, further comprising a step of forming a plurality of conductive wires (21) each included in one of said flexible conductive members.

43. The method as set forth in claim 38, wherein each of said flexible conductive members comprises a bonding wire (51).

44. The method as set forth in claim 38, wherein each of said flexible conductive members comprises an electroless plating layer (61).

45. The method as set forth in claim 38, further comprising a step of forming an insulating stress-absorbing resin layer (34) on said semiconductor substrate before said resin coated conductive layer is adhered on said semiconductor substrate, said insulating stress-absorbing resin layer having openings corresponding to said pad electrodes.

46. A flip-chip type semiconductor device substantially as herein described with reference to and as shown in Figures 2A to 14Q of the accompanying drawings.

47. A method for manufacturing a flip-chip type semiconductor device, the method being substantially as herein described with reference to and as shown in Figures 2A to 14Q of the accompanying drawings.

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Claims searched: 1-9, 12-21 **Date of search:** 30 August 2001

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K (KHAE, KPXDB, KPX, KPXB)

Int Cl (Ed.7): H01L (21/56, 21/58, 21/60, 21/603, 23/29, 23/485, 23/522,23/532, 23/66, 23/31)
H05K (1/18, 7/02)

Other: ONLINE: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
Y	US 5683942 (NEC CORP) whole document, in particular Figure 5A, and column 8, lines 21 and 22	1-7, 12, 13, 15, 16,
Y	IEMT/IMC Proceedings "Advanced MCM-Ls for Consumer Electronics", 1998, Amami et al, pp 249 - 254	1-7, 12, 13, 15,16

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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