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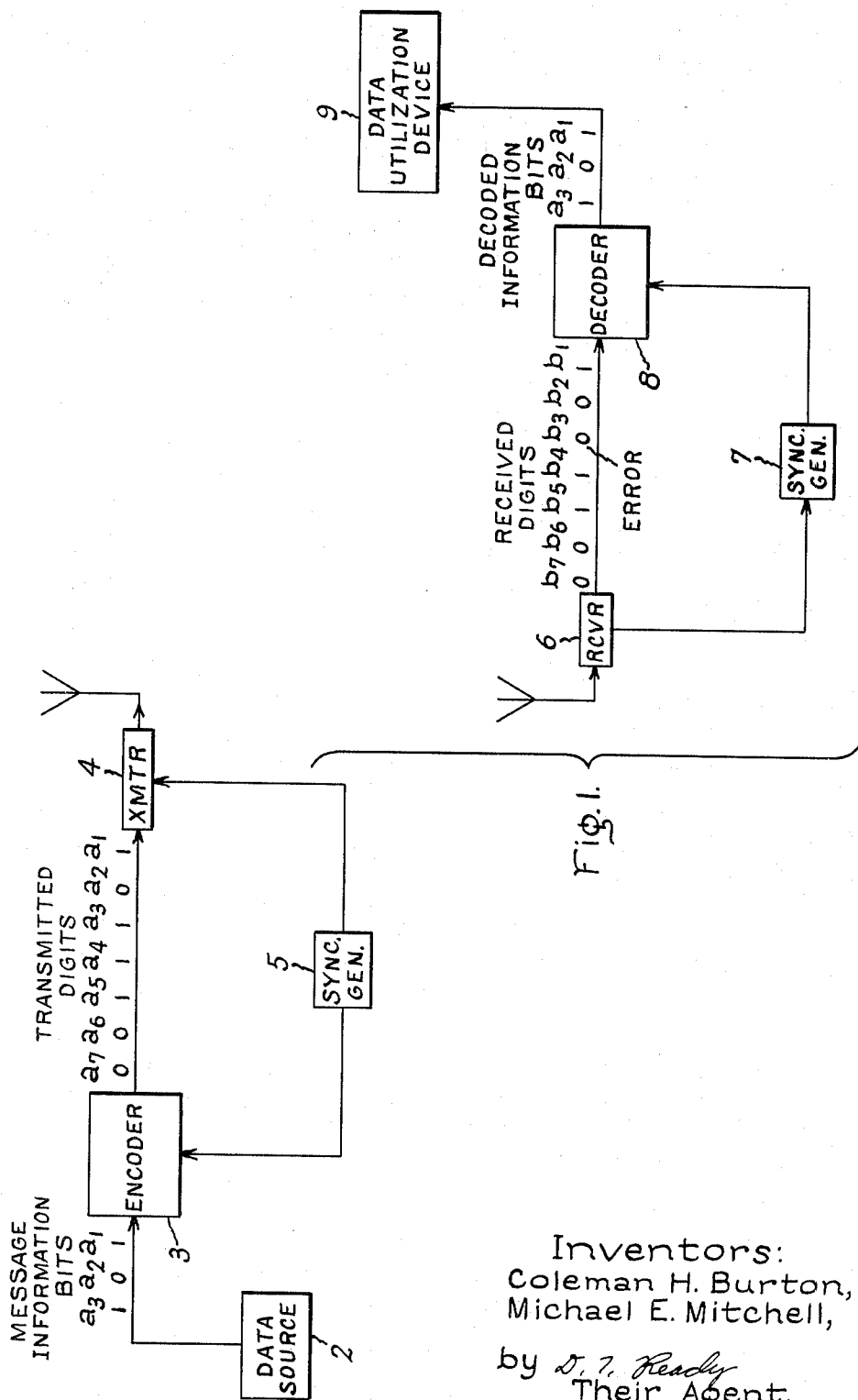
C. H. BURTON ETAL

3,222,644

SIMPLIFIED ERROR-CONTROL DECODER

Filed July 26, 1962

4 Sheets-Sheet 1



Inventors:
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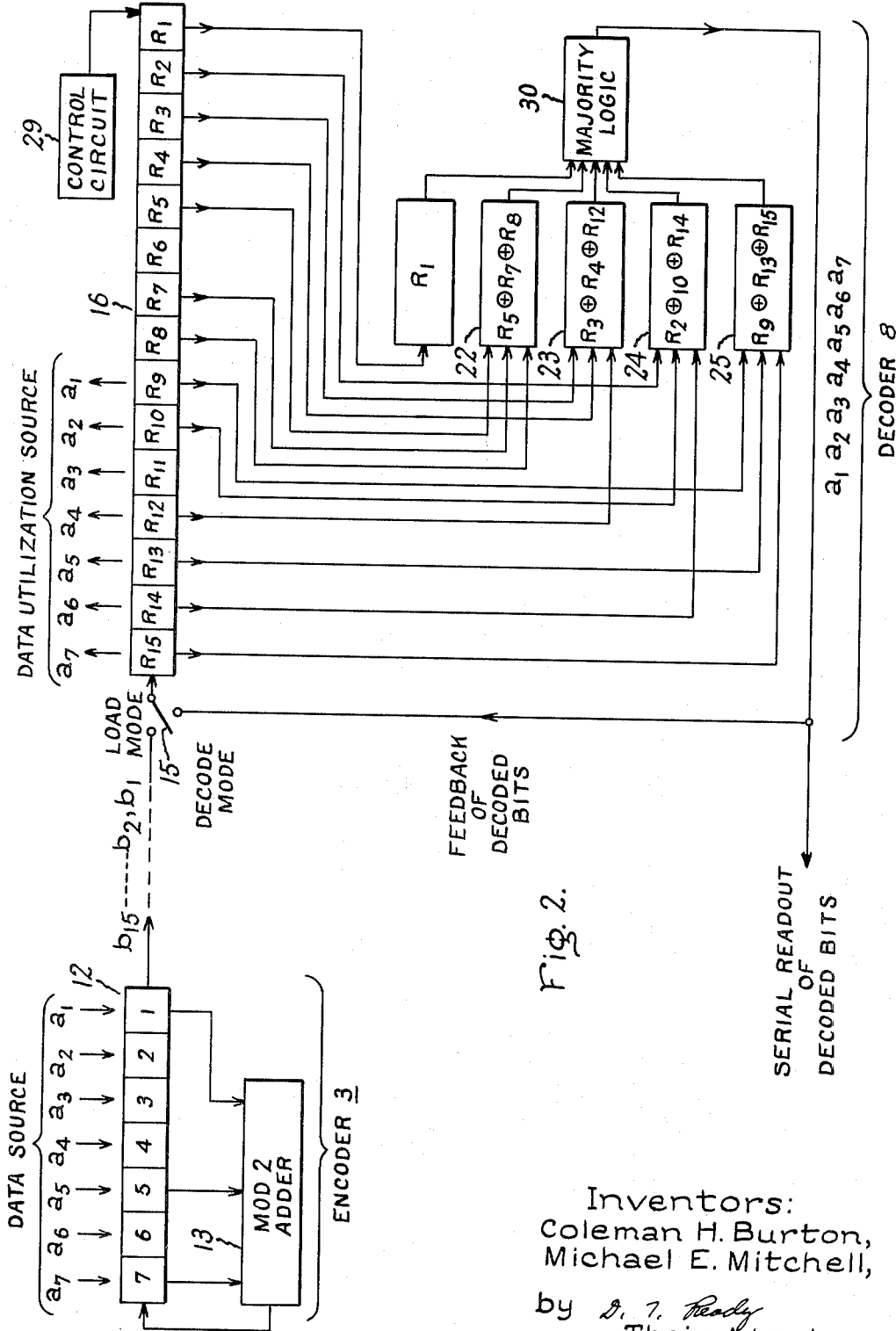
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4 Sheets-Sheet 2



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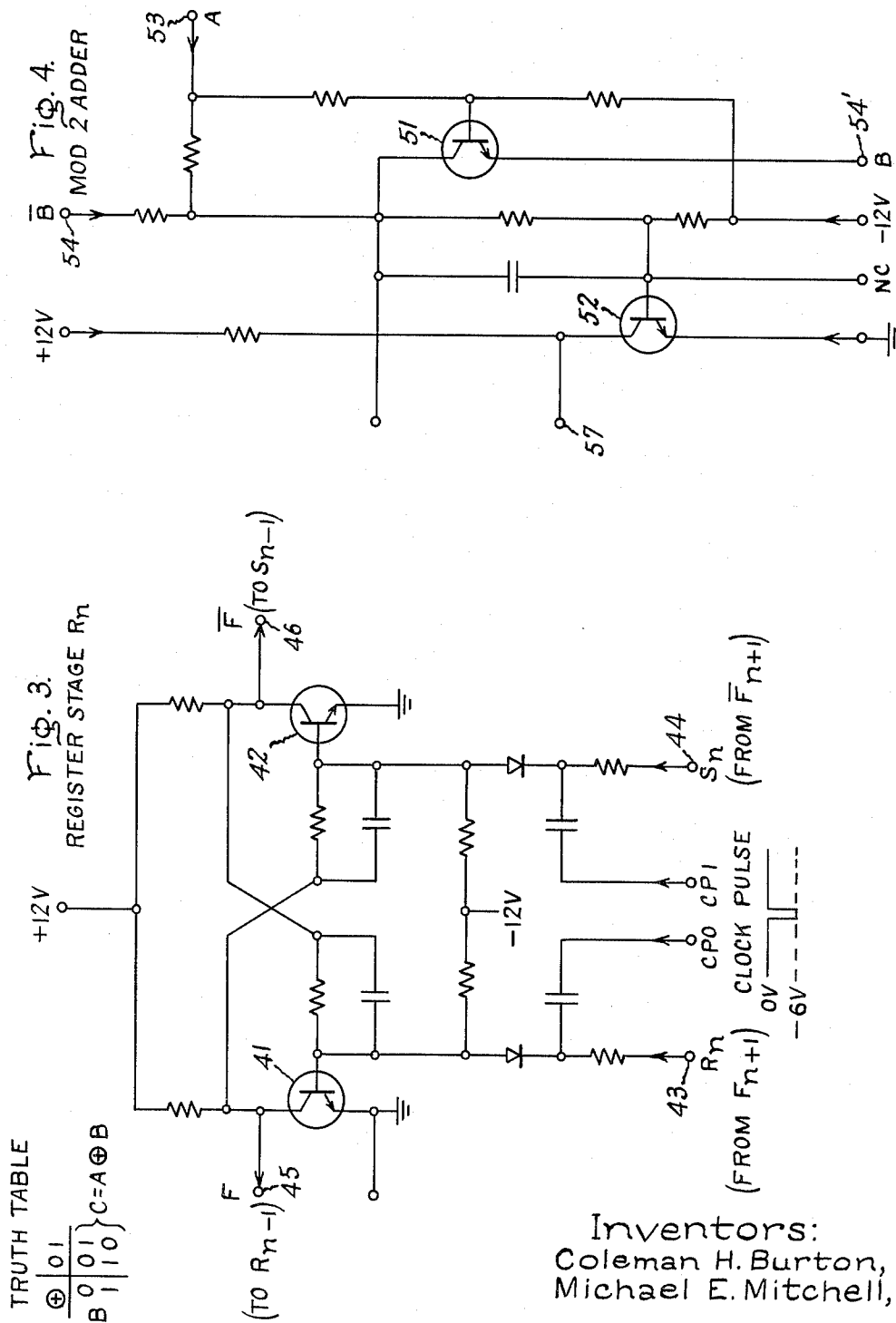
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SIMPLIFIED ERROR-CONTROL DECODER

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4 Sheets-Sheet 3



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SIMPLIFIED ERROR-CONTROL DECODER

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4 Sheets-Sheet 4

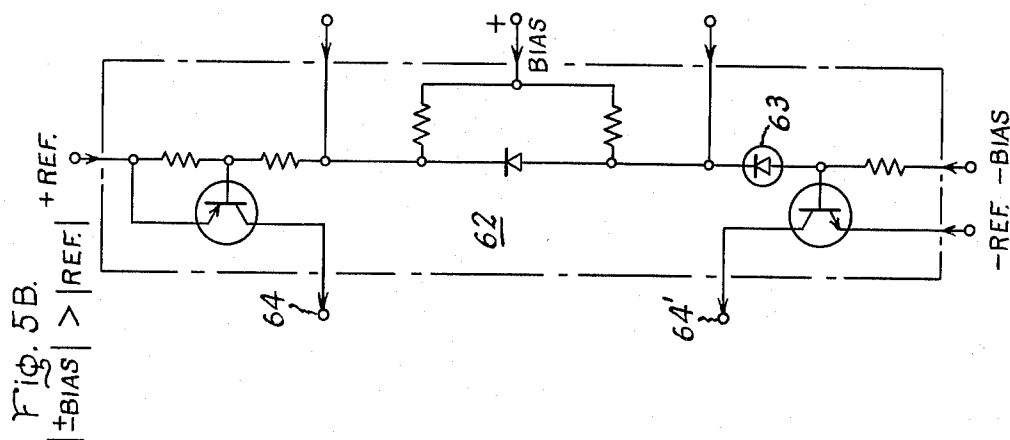
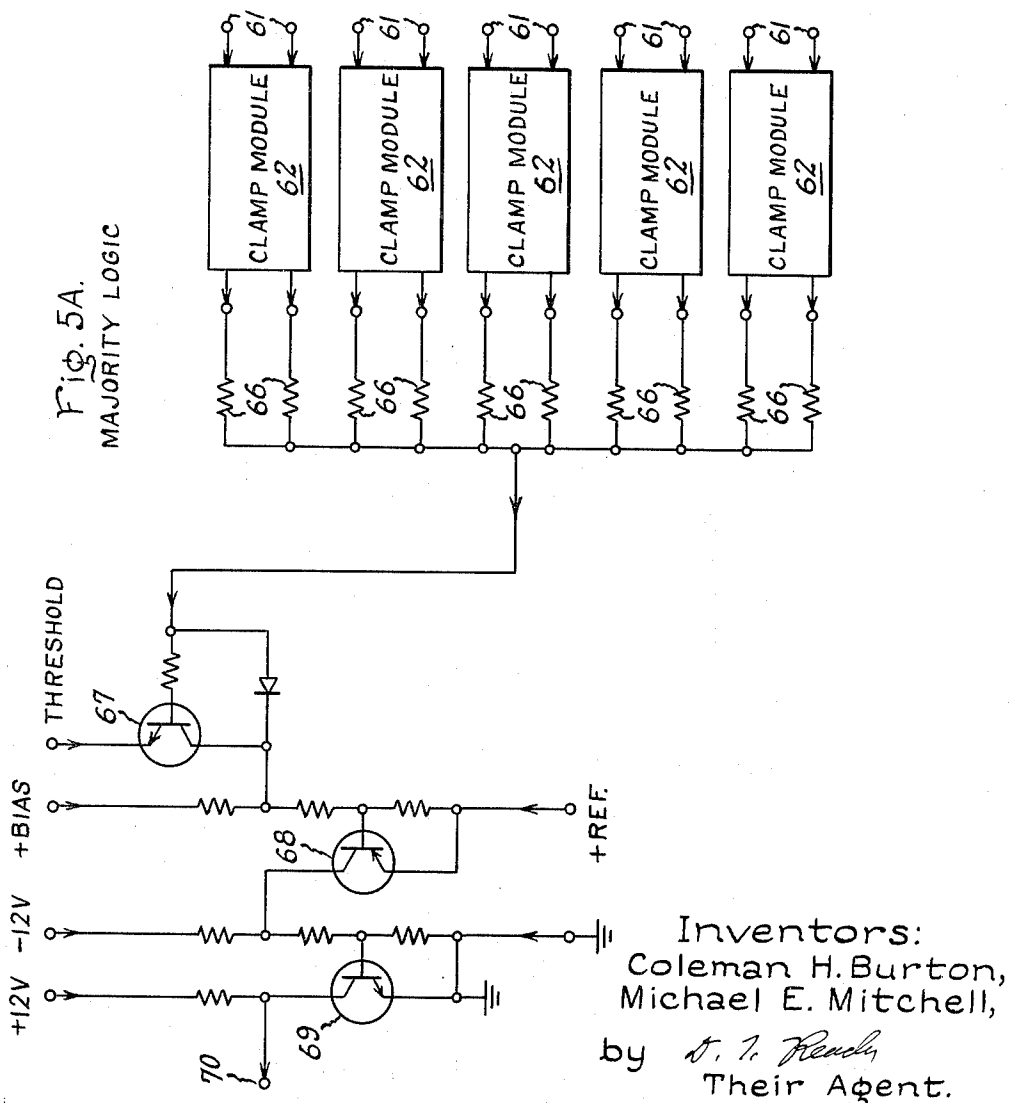


Fig. 5A.
MAJORITY LOGIC



1

2

3,222,644

SIMPLIFIED ERROR-CONTROL DECODER

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Filed July 26, 1962, Ser. No. 212,746

5 Claims. (Cl. 340-146.1)

The invention is directed to error correcting apparatus for digital data processing systems. The apparatus is of the class which operates upon (and generates) code words (or sequences of n digits) which are characterized by consisting of k information digits plus $n-k$ redundant digits whereby errors can be corrected by means of the redundant digits. The apparatus will not correct all possible combinations of errors, but it can correct up to a given number with certainty and some additional errors under special circumstances and perform other related functions such as monitoring the number and rate of error corrections. The invention results in great simplification of apparatus with certain codes.

For many years, a great deal of successful work on the theory of error correcting codes has been carried out. There have also been substantial developments in apparatus for the encoding of many kinds of error correcting codes. However, there has been a distinct lack of success in providing corresponding decoding apparatus of practical simplicity. In fact, prior decoding systems are frequently characterized by marginal increases of overall reliability because the mass of additional decoding apparatus tends to introduce as many errors as it corrects.

In respect to some considerations, the use of error correction codes is that by transmitting information over a longer time period at the same power, more energy is made available and thus greater signal-to-noise ratio is obtainable. However, it is necessary to provide the added signal energy in such a manner that there can be efficient discrimination of the information signal. The relations involved can be approached with various kinds of analysis and a very large body of complex theory exists.

For the purposes of explanation, a representative code will be considered here in the specification. This code is known as the (15, 1) code. It is characterized by consisting of $n=15$ binary characters or bits of which $k=7$ are the information bits and $n-k=8$ bits are redundant bits which provide an error correcting capability of at least 2 errors in each code word.

If one has 7 information bits, there are 2^7 possible binary combinations or words and there are 2^{15} possible combinations for a 15 bit sequence. It is evident that the additional redundant digits can provide a great deal of correction data to determine where errors are. In fact, it has been determined that the seven information bits can be encoded so that all possible correct word combinations will differ from each other in at least five places of their fifteen bit code word. As a result, if a received code word has two errors or less, and it is compared with the 2^7 correct words, the closest code word will be the correct one because all other possible correct code words will differ in at least three places.

Obviously, apparatus which stores 2^7 correct code words is too cumbersome, particularly when the associated equipment for signal distribution and comparison is considered.

As is evident, if codes of increased length are used, the increase in equipment complexity is geometrical. Most prior systems suggested have been characterized by a fourth power rate of increase of complexity as a function of the code length. This increase in complexity necessarily results in corresponding increases in cost, inflexibility, and other problems associated with complexity.

Briefly stated, the invention consists of several related techniques for extracting signal from noise plus signal.

The several techniques are characterized by the fact that the decoding procedure is a bit-by-bit operation in which the following two-step routine is iterated: First, a calculation of the several estimator values for the i th transmitted code digit (or for mod 2 sums of selected code digits) wherein each estimator is based on, or may actually consist of, a mod 2 sum of code digits identically equal to the estimated code digit (or mod 2 sum of code digits) when no errors are present. Second, a combination of the several estimator values for each estimated quantity into a final estimate, wherein the final estimate for the $(i+1)$ th quantity differs from that for the i th only by a unit cyclic permutation of the digits (modulo the code length n) appearing as arguments in the estimators.

Regarding the second step, the combining operation for binary decoding with an odd number of estimators is merely the majority decision operation. Binary decoding with an even number of estimators is accomplished by deciding according to an arbitrary rule in case of a tie (and by majority decision otherwise). If a particular estimator is inherently more reliable for the expected kind of error-producing mechanism, it should obviously be used to break ties. (In most cases, the single-digit estimator is more reliable.) In some cases of equal estimator reliability (or credibility), the best arbitrary rule for breaking ties may be pseudorandom choice, or even a truly random choice.

The most significant feature of the invented decoding techniques is not the variety of detailed differences between specific decoding procedures (and their implementation), but instead consists of the fact that each decoding procedure within the scope of the defined invention employs a decoding function which is independent of the particular quantity being decoded. Thus, the quantity which is decoded according to the above steps always consists of code digits. In spite of the superficial differences, the inherent reason for the simplicity with which the several invented decoding techniques can be implemented is based on the nearly complete exploitation of the cyclic properties of the codes employed.

Accordingly, it is an object of this invention to provide a simplified plural error correction decoder which does not require the complex apparatus for an intermediate series of logic operations on the complete word before the final decoding of any digits in the code word.

It is a further object of the invention to provide a simplified plural error correction decoder which does not require a plurality of storage devices for intermediate logic evaluator operations.

It is another object of this invention to provide a decoder which does not require the decoding of the complete code word to decode the information digits.

These and other objects and features of the present invention will become apparent from the accompanying detailed description and drawings in which:

FIGURE 1 is a block diagram of a one way digital communication system illustrating binary encoding and decoding;

FIGURE 2 is a block diagram of an encoder and decoder for a (15, 7) code;

FIGURE 3 is a schematic diagram of one stage of a shift register suitable for use in the FIGURE 2 encoder or decoder;

FIGURE 4 is a schematic diagram of a two-input modulo 2 adder for the estimator logic circuits in the FIGURE 2 decoder; and

FIGURES 5A and 5B are schematic diagrams of a majority logic circuit for the FIGURE 2 decoder.

Referring now to the drawings, FIGURE 1 is a block diagram of a representative one-way digital communications system. A data source 2 supplies information in the form of digital signals such as code words which it is

desired to transmit to a remote data utilization device 9. The code word illustrated is a three digit message, a_1, a_2, a_3 , shown as 101, which is applied to an encoder in a serial or parallel operation. The output of the encoder is a series of bits ($a_1, a_2, \dots, a_7$) in which the last four are redundant bits generated by the encoder. These redundant bits are generated as predetermined logic functions of the information bits so that the bits are logic functions of both redundant and information bits. The code word is then transmitted by transmitter 4 by sequential bits in accordance with control pulses from a conventional synch generator 5. As illustrated, the message received by receiver 6 has an error in the third place b_3 . When the complete message is received, it has been stored in the decoder 8 under control of synch generator 7 by conventional digital data transmission techniques. The decoder 8 then operates upon the received word, including the erroneous third bit b_3 , and by sensing the redundant bits (together with the information bits), determines the correct values for b_1, b_2, b_3 which are then applied to the utilization device 9.

The apparatus of FIGURE 1 is characterized by the addition of an encoder and a decoder without modification of the original system components. The result is that system performance can be vastly improved without redesign of the system. With the novel decoder disclosed herein, the information is read out of the decoder during k operations following reception of the code word. This is permitted by minimizing the number of the sequential bit decoding operations to the number of information bits in the encoded word.

FIGURE 2 is a block diagram illustrating the major components of the invention arranged for encoding and decoding a (15,7) code. The encoder 3 is of a conventional design. It is comprised of a seven stage shift register 12 which is adapted to receive an information word of seven bits in parallel by suitable gating means. The information word is encoded by simultaneously generating redundant bits and reading out the code word bits during cyclic serial operations. Each clock pulse causes the bit signals in each stage to shift to the right to the next stage. The signals from the last stage are the output bit signals of the encoder 3. During each shift operation, a redundant bit signal is generated by the modulo 2 adder and is entered into the first stage of the shift register 12. The mod 2 adder generates each redundant bit in accordance with the modulo sum of the three bits in the stages where a_1, a_5 and a_7 were originally entered. The mod 2 adder is conveniently a pair of two input mod 2 adders in series in which a_1 and a_5 are applied to the first and the output of the first and a_7 are applied to the second. An appropriate mod 2 adder will be described hereinafter, but it can take any form such as a simplified half adder wherein the sum signal is the output. (The output of each modulo 2 adder in operation is the binary sum casting out all carries.)

The result is that after 15 clock pulses, a code word will be generated in which the first seven bits are the same as the information bits and the eight redundant bits are as follows:

$$\begin{aligned} a_8 &= a_7 \oplus a_5 \oplus a_1 \\ a_9 &= a_8 \oplus a_6 \oplus a_2 \\ &\vdots \\ &\vdots \\ &\vdots \\ a_{15} &= a_{14} \oplus a_{12} \oplus a_8 \end{aligned}$$

Because of their cyclic characteristic, the redundant bits are serially generated as the code word bits are shifted out of the shift register 12.

The decoder 8 in FIGURE 2 includes three major functional units: a 15-stage shift register 16, single-digit cyclic estimator logic circuits 22-25, and a majority logic cir-

cuit 30. A mode switch 15 selects either a load mode or a decode mode by switching the serial input of the shift register 16 either to the incoming code word or to a feedback connection for entering decoded bit signals sequentially. The cyclic estimator logic circuits 22-25 are each connected to three stages of the shift register 16 in accordance with an independent logic equation. Each of these cyclic estimator logic circuits are of the same type as the mod 2 adder 13 in encoder 3. Because of the relations of the redundant bits to the information bits, the information bits can be estimated from the code bits in several ways which rely on independent selections of the code word bits. In the absence of any errors, the outputs of all the cyclic estimator logic circuits are the same. However, in the event of one or two errors, the majority logic circuit 30, since it is arranged to receive the outputs of all cyclic estimator logic circuits, provides an output signal in accordance with the majority of the estimators. In this embodiment, there are four mod 2 estimators and a fifth estimate of a_1 is provided for the majority logic circuit 30 directly, by the last stage of the shift register which contains b_1 . This logic operation is used once for each digit, and will always produce a correct majority logic output if there are two errors or less in the received code word because three of the estimates must be correct.

The sequence of the decoding operations in the decode mode is described as follows. First assume that b_j is the binary quantized received value of the code digit transmitted as a_j , for $j=1, 2, \dots, 15$; and that R_j is the binary value of the contents of the j th stage of the 15-stage shift register where $j=1, 2, \dots, 15$. Then the procedure is:

(1) Compute the estimator logic functions

$$\begin{aligned} F_1 &= R_1 \\ F_2 &= R_5 \oplus R_7 \oplus R_8 \\ F_3 &= R_3 \oplus R_4 \oplus R_{12} \\ F_4 &= R_2 \oplus R_{10} \oplus R_{14} \\ F_5 &= R_9 \oplus R_{13} \oplus R_{15} \end{aligned}$$

where $\oplus$ is the symbol for modulo 2 addition

(2) Compute the majority decision estimate

$$B_1 = \text{Majority } F_1, F_2, F_3, F_4, F_5$$

(3) Feed B_1 (the estimate of the binary content of the terminal stage, R_1) back to the stage of entry, R_{15} , while shifting the contents of all 15 stages to the "right" by one unit.

(4) Repeat steps 1-3 for a total of seven complete cycles, then STOP.

(5) Read out the corrected information bits from stages $R_{15}, R_{14}, \dots, R_9$.

Note that the first time step 1 is executed, the binary digit in the j th stage has the value $R_j = b_j$, where b_j is the binary quantized received value of the digit transmitted as a_j for $j=1, 2, \dots, 15$. However, the second time that step 1 is executed, the binary content of the j th stage is $R_j = b_{j+1}$. The process, of course continues. The important feature here is that the decoding procedure itself is independent of the contents of the shift register. In fact, the process can be allowed to continue indefinitely; and if, at any step, two or fewer errors exist, they will be corrected, and from that point on a completely correct code word will circulate. The invariance of this procedure to the shift-register contents is clearly advantageous from operational and implementation standpoints.

Two alternative information readout modes are possible:

(1) Serial readout of the sequence of estimated information bits $a_0, a_1, \dots, a_6$ in the time sequence with which they are decoded.

(2) Parallel readout of these bits as a single word $a_1 \dots a_7$ from the contents of register stages 9 through 15.

The particular decoding procedure indicated in steps 1 through 4 is described as bit-by-bit single-stage decod-

ing with feedback, which is abbreviated to merely step-by-step single-stage decoding for either of these information readout modes.

Instead of feedback of corrected digits, suppose that the uncorrected digits were merely recirculated. The decoding procedure would be called bit-by-bit as before, but could no longer allow parallel readout (without adding external storage), nor could it be legitimately called "step-by-step." This is because of the prevailing use of the term step-by-step to mean a succession of decoding "steps" toward the correct message. This criterion is indeed satisfied with the type of single-stage decoding procedure having feedback illustrated in FIGURE 2. In this particular example, a "step" is defined as the correction and feedback to the shift register of a digit which was received in error. Each such operation may reduce the Hamming distance between the word stored in the register and the correct word by one unit, which is called a "step."

It is evident that the decoder arrangement of FIGURE 2 is adaptable to various other codes. Examples of such codes are: (21, 11), (73, 45) and $(2^m-1, m)$. The requirements of the codes which are ideally suited for this type of decoder are involved. The practical limitation is the ability to form a set of estimator logic equations which are independent (have no common terms) and are of sufficient number so that the theoretical maximum number of errors can be corrected. In addition, of course, the code must be a cyclic, binary group code so that the recursion relationship enables utilization of the same circuitry for successive bits.

The above codes such as (73, 45) have been known as cyclic binary group codes and from their known properties, their estimator logic equations can be determined. For the (73, 45) code, the equations as formed for a_1 are as follows:

$$\begin{aligned} a_1 &= a_3 \oplus a_{11} \oplus a_{25} \oplus a_{30} \oplus a_{37} \oplus a_{43} \oplus a_{46} \\ a_1 &= a_5 \oplus a_{23} \oplus a_{24} \oplus a_{28} \oplus a_{35} \oplus a_{41} \oplus a_{44} \oplus a_{72} \\ a_1 &= a_{15} \oplus a_{16} \oplus a_{20} \oplus a_{27} \oplus a_{33} \oplus a_{36} \oplus a_{61} \oplus a_{66} \\ a_1 &= a_2 \oplus a_6 \oplus a_{13} \oplus a_{19} \oplus a_{22} \oplus a_{50} \oplus a_{52} \oplus a_{60} \\ a_1 &= a_5 \oplus a_{12} \oplus a_{18} \oplus a_{21} \oplus a_{49} \oplus a_{51} \oplus a_{59} \oplus a_{73} \\ a_1 &= a_8 \oplus a_{14} \oplus a_{17} \oplus a_{45} \oplus a_{47} \oplus a_{55} \oplus a_{69} \oplus a_{70} \\ a_1 &= a_7 \oplus a_{10} \oplus a_{38} \oplus a_{40} \oplus a_{48} \oplus a_{62} \oplus a_{63} \oplus a_{67} \\ a_1 &= a_4 \oplus a_{32} \oplus a_{34} \oplus a_{42} \oplus a_{56} \oplus a_{57} \oplus a_{61} \oplus a_{68} \\ a_1 &= a_{29} \oplus a_{31} \oplus a_{26} \oplus a_{53} \oplus a_{64} \oplus a_{58} \oplus a_{65} \oplus a_{71} \end{aligned}$$

The encoding of these codes are well known by means of sequence generators of the type illustrated in FIGURE 2.

The estimator equations for the above (21, 11) code are as follows:

$$\begin{aligned} a_1 &= a_1 \\ a_1 &= a_2 \oplus a_5 \oplus a_9 \oplus a_{12} \\ a_1 &= a_3 \oplus a_7 \oplus a_{10} \oplus a_{20} \\ a_1 &= a_6 \oplus a_{15} \oplus a_{17} \\ a_1 &= a_4 \oplus a_{14} \oplus a_{16} \oplus a_{21} \\ a_1 &= a_{11} \oplus a_{13} \oplus a_{18} \oplus a_{19} \end{aligned}$$

It is to be understood that there are many variations in the data processing systems incorporating the disclosed decoder. The radio transmission system illustrated in FIGURE 1 is only representative. The data link transmission systems between the encoder and decoder can incorporate different combinations and permutations of parallel and serial data transmissions, from physical movement of punched cards to intricate systems.

The implementation of the FIGURE 2 decoder may be carried out with conventional components. For example, the shift registers 12 and 16 can be implemented by a series of standard flip-flops such as shown in FIGURE 3. Each flip-flop R_n is a single stage in the shift register and is interconnected with the adjoining stages R_{n+1} and R_{n-1} . In the preferred embodiment of the system, a "1" bit signal is in the form of a positive voltage and a "0" bit is in the form of a zero voltage level. Therefore, the n-p-n transistors 41 and 42 are interconnected so that when the flip-flop is "set," the right-hand transistor 42 is conducting and the left-hand transistor 41 is off. Accordingly, a positive voltage appears at the output terminal 45 as F and a zero voltage appears at

the complementary output terminal 46 as $\bar{F}$. When the negative going clock pulse is applied to the base of each transistor, the conducting transistor is cut off. Upon removal of the clock pulse, the flip-flop circuit assumes a "set" or "reset" state in accordance with the last state of the preceding stage. That is, the output signals of stage R_{n+1} are connected to input terminals 43 and 44 so that $S_n = F_{n+1}$ (before the shift) and $R_n = \bar{F}_{n+1}$. It is to be understood that in decoders having an even number of estimators, the "majority" decision would include tie-breaking functions such as selection of the b_j value to be decoded.

A suitable component for the mod 2 adder is shown in FIGURE 4. The illustrated circuit is a two-input mod 2 adder in itself and has its output coupled to one of the inputs of an identical two-input mod 2 adder. The n-p-n transistors 51 and 52 operate to produce a positive voltage at the output terminal 57 in accordance with an "exclusive or" logic function. If either input, A at input terminal 53 or B and $\bar{B}$ at input terminals 54 and 54', is a "1" the output at terminal 57 is a positive voltage and if the inputs are both either "1s" or "0s," the output signal is a zero voltage. This is because the transistor 52 is conducting only if $\bar{B}$ and A provide positive voltages or if B provides a positive voltage while A provides a zero voltage.

FIGURES 5A and 5B illustrate a preferred majority logic circuit. This circuit receives the output of all the estimator logic circuits 22-25 at input terminals 61. Since it combines all of the input signals into an analog signal, it is fundamental that these signals be accurate voltages so that a correct comparison is made. Accordingly, clamping circuits 62 are provided to regulate the comparison voltages. Each clamping circuit includes a zener diode 63 which produces a voltage reference for a standard transistor clamping circuit. Because of the balanced reference and bias sources, the voltage at one of the clamping circuit output terminals 64 and 64' is negative or positive and the other is zero. These carefully referenced signals (negative for "1" estimation and positive for a zero estimation) are then applied to a set of precision summing resistors which sum the signals. The output of the summing network can assume any one of six levels. Accordingly, an output circuit consisting of three transistors 67, 68 and 69 is provided so that the output signal of the majority logic circuit at terminal 70 assumes either a zero value for a "0" bit or a positive signal value for a "1" bit of the decoder circuits. The transistors 68 and 69 therefore produce either a fixed positive voltage or a zero voltage depending upon whether transistor 67 is turned on or off by the majority sum of the estimator signals. The output voltage remains constant regardless of variations in the transistor 67 current.

The construction of the decoder can be carried out with other standard components. For example, binary scaler counters can be used as the modulo 2 adders and other shift registers such as magnetic core shift registers can be employed. The control circuit 29 in the FIGURE 2 system provides the normal data processing control functions. These functions include providing clock pulses to the various components and providing command signals to stop decoding functions after the information bits are decoded and to readout the decoded bits.

While particular embodiments of the invention have been shown and described herein, it is not intended that the invention be limited to such disclosure, but that changes and modifications can be made and incorporated within the scope of the claims.

1. In data processing apparatus that processes code words having n binary digit signals in n respective positions in the word, of which k signals represent information bits, a decoder comprising:

(a) A register adapted to receive the code word signals in such a manner that the bits of the code word sig-

- nals are entered into positions of the register corresponding to their position in the code word;
- (b) cyclic estimation logic circuits which operate as a function of the received bits in said register in a manner to provide the required number of estimate signals by independent value estimations of the correct value of the received bit in a specific position of the register;
- (c) a decision logic circuit responsive to the estimate signals to provide decoded output bit signal in accordance with the majority of the estimate signals; and
- (d) control circuitry to cyclically shift the bit signals in said register for k bit decoding operations, to initiate a bit decoding operation after each shift, and to terminate word decoding operations after k bit decoding operations.
2. In data processing apparatus that processes code words having n binary digit signals in n respective positions in the word, of which k signals represent information bits, a multiple error correction decoder comprising:
- (a) a shift register adapted to receive the code word signals in such a manner that the bits of the code word signals are entered into positions of the shift register corresponding to their position in the code word;
- (b) cyclic estimation logic circuits which operate as a function of the received bits in said shift register to provide estimate signals by independent value estimations of the correct value of the received bit in a specified position of the shift register;
- (c) a majority logic circuit responsive to the estimate signals to provide a decoded output bit signal in accordance with the majority of the estimate signals;
- (d) feedback means to enter the decoded bit signals into said shift register; and
- (e) control circuitry to cyclically shift the bit signals in said registers for k bit decoding operations, to initiate a bit decoding operation after each shift, and to terminate word decoding operations after k bit decoding operations.
3. The multiple error correction decoder of claim 2 for decoding a (15, 7) code wherein:
- (f) said cyclic estimation logic circuits include a plurality of modulo 2 adders which each provide an estimate of a bit being decoded in accordance with the following estimator equations,

$$\begin{aligned} a_1 &= a_1 \\ &= a_1 \oplus a_7 \oplus a_8 \\ &= a_1 \oplus a_4 \oplus a_{12} \\ &= a_1 \oplus a_{16} \oplus a_{14} \\ &= a_1 \oplus a_{13} \oplus a_{15} \end{aligned}$$

4. The multiple error correction decoder of claim 2 for decoding a (73, 45) code wherein:

- (f) said cyclic estimation logic circuits include a plurality of modulo 2 adders which each provide an estimate of a bit being decoded in accordance with the following estimator equations,

$$\begin{aligned} a_1 &= a_3 \oplus a_{11} \oplus a_{25} \oplus a_{26} \oplus a_{30} \oplus a_{37} \oplus a_{43} \oplus a_{46} \\ a_1 &= a_9 \oplus a_{23} \oplus a_{24} \oplus a_{28} \oplus a_{35} \oplus a_{41} \oplus a_{44} \oplus a_{72} \\ a_1 &= a_{15} \oplus a_{16} \oplus a_{20} \oplus a_{27} \oplus a_{33} \oplus a_{38} \oplus a_{64} \oplus a_{68} \\ a_1 &= a_2 \oplus a_6 \oplus a_{13} \oplus a_{19} \oplus a_{22} \oplus a_{30} \oplus a_{52} \oplus a_{60} \\ a_1 &= a_5 \oplus a_{12} \oplus a_{18} \oplus a_{21} \oplus a_{40} \oplus a_{51} \oplus a_{59} \oplus a_{73} \\ a_1 &= a_8 \oplus a_{14} \oplus a_{17} \oplus a_{45} \oplus a_{47} \oplus a_{55} \oplus a_{69} \oplus a_{70} \\ a_1 &= a_7 \oplus a_{10} \oplus a_{36} \oplus a_{40} \oplus a_{48} \oplus a_{62} \oplus a_{63} \oplus a_{67} \\ a_1 &= a_4 \oplus a_{32} \oplus a_{34} \oplus a_{42} \oplus a_{56} \oplus a_{57} \oplus a_{61} \oplus a_{65} \\ a_1 &= a_{29} \oplus a_{31} \oplus a_{29} \oplus a_{53} \oplus a_{54} \oplus a_{55} \oplus a_{65} \oplus a_{71} \end{aligned}$$

5. The multiple error correction decoder of claim 2 for decoding a (21, 11) code wherein:

- (f) said cyclic estimation logic circuits include a plurality of modulo 2 adders which each provide an estimate of a bit being decoded in accordance with the following estimator equations,

$$\begin{aligned} a_1 &= a_1 \\ a_1 &= a_3 \oplus a_5 \oplus a_9 \oplus a_{12} \\ a_1 &= a_5 \oplus a_7 \oplus a_{10} \oplus a_{20} \\ a_1 &= a_2 \oplus a_8 \oplus a_{15} \oplus a_{17} \\ a_1 &= a_4 \oplus a_{14} \oplus a_{16} \oplus a_{21} \\ a_1 &= a_{11} \oplus a_{13} \oplus a_{18} \oplus a_{19} \end{aligned}$$

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ROBERT C. BAILEY, *Primary Examiner*.

MALCOLM A. MORRISON, *Examiner*.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,222,644

December 7, 1965

Coleman H. Burton et al.

It is hereby certified that error appears in the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Column 4, line 36, for " $F_2=R_5 \oplus R_7=R_8$ " read -- $F_2=R_5 \oplus R_7 \oplus R_8$ --; column 5, line 50, for " a_5 " read -- a_1 --; column 7, line 27, after "register" insert -- in a manner to provide the required number of esti- --; line 37, for "registers" read -- register --; line 43, for "incldue" read -- include --; column 8, lines 2 to 5 should appear as shown below instead of as in the patent:

$$\begin{aligned} a_1 &= a_5 \oplus a_7 \oplus a_8 \\ a_1 &= a_3 \oplus a_4 \oplus a_{12} \\ a_1 &= a_2 \oplus a_{10} \oplus a_{14} \\ a_1 &= a_9 \oplus a_{13} \oplus a_{15} \end{aligned}$$

same column 8, line 20, strike out "plural-".

Signed and sealed this 3rd day of January 1967.

(SEAL)

Attest:

ERNEST W. SWIDER
Attesting Officer

EDWARD J. BRENNER
Commissioner of Patents