United States Patent

[11] 3,594,762

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[45] Patented **July 20, 1971**

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[54] **DISPLAY SYSTEM**
32 Claims, 22 Drawing Figs.

[52] **U.S. Cl.** **340/334,** 340/324, 340/337
[51] **Int. Cl.** **G09f 9/34**
[50] **Field of Search** 340/324, 334, 337, 336, 339

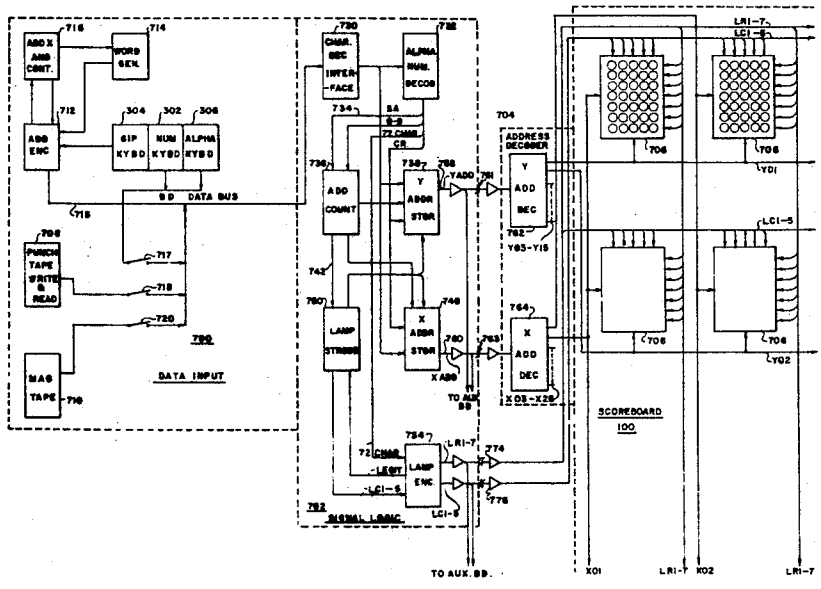
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ABSTRACT: A control system for a data display system such as a scoreboard, message board or the like wherein display indicators having location addresses, on the board are addressed and actuated through a logic system which first receives and stores address data pertaining to a particular indicator, receives display character data, and responsive to the receipt of the character display data automatically reads out the address data to the board for enabling the desired indicator followed by the display character data to actuate it to display the desired character. Indicator circuits are provided for the control of each indicator comprising semiconductor switches which are reset by the addressing of the indicator and actuated to display the desired character responsive to the receipt of the display character data. A memory storage is also provided to cause the display of repeatedly used messages and animated characters.



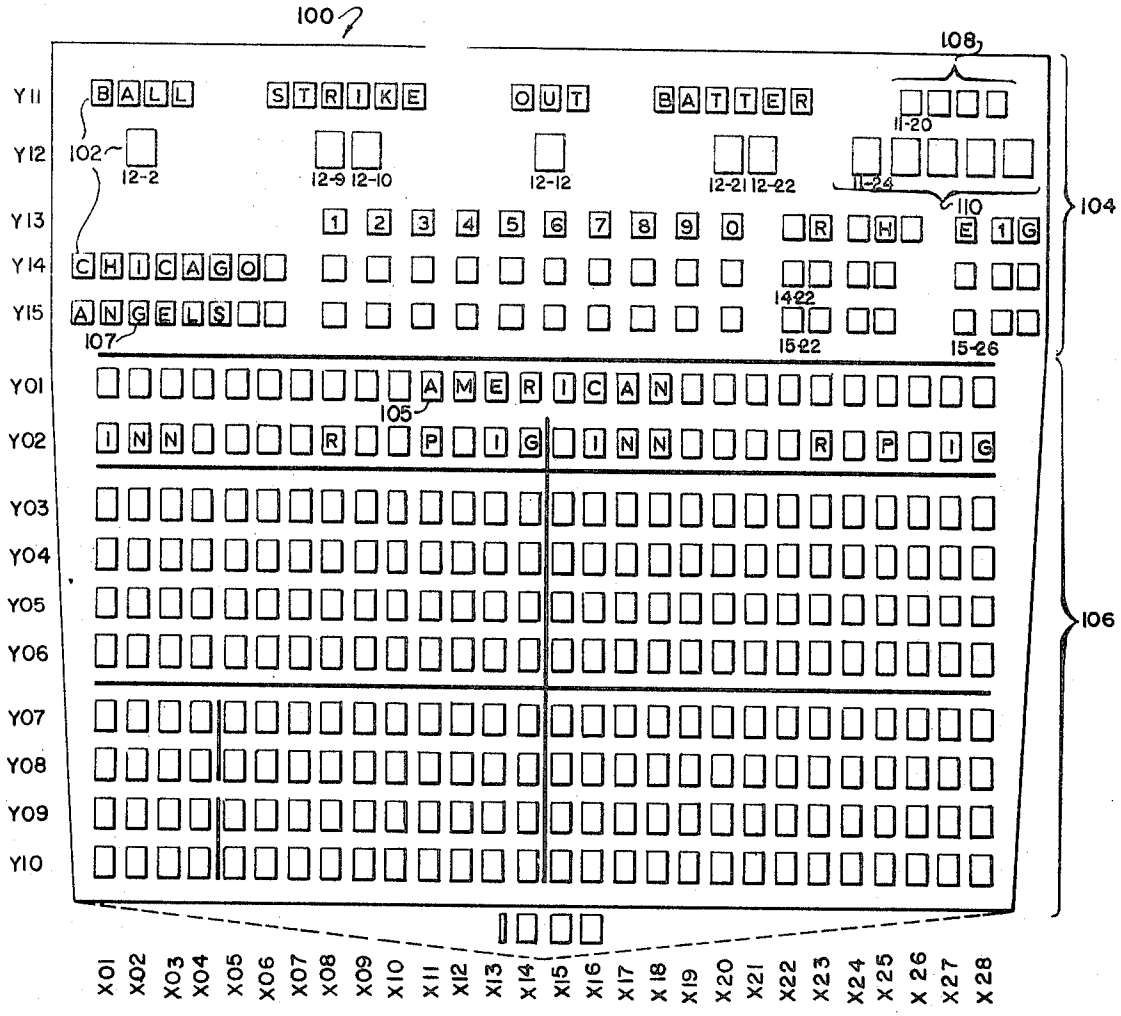


FIG. 1.

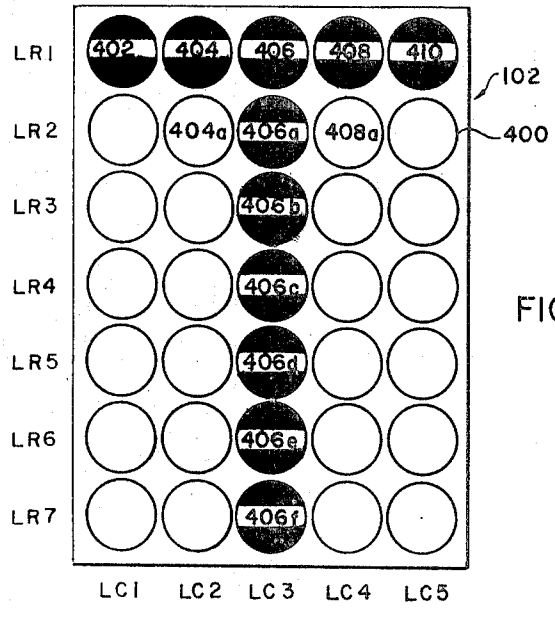


FIG. 4.

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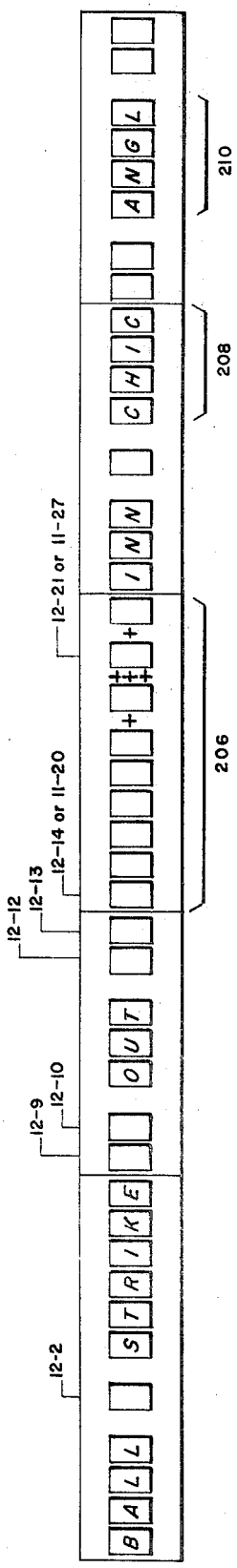


FIG. 2.

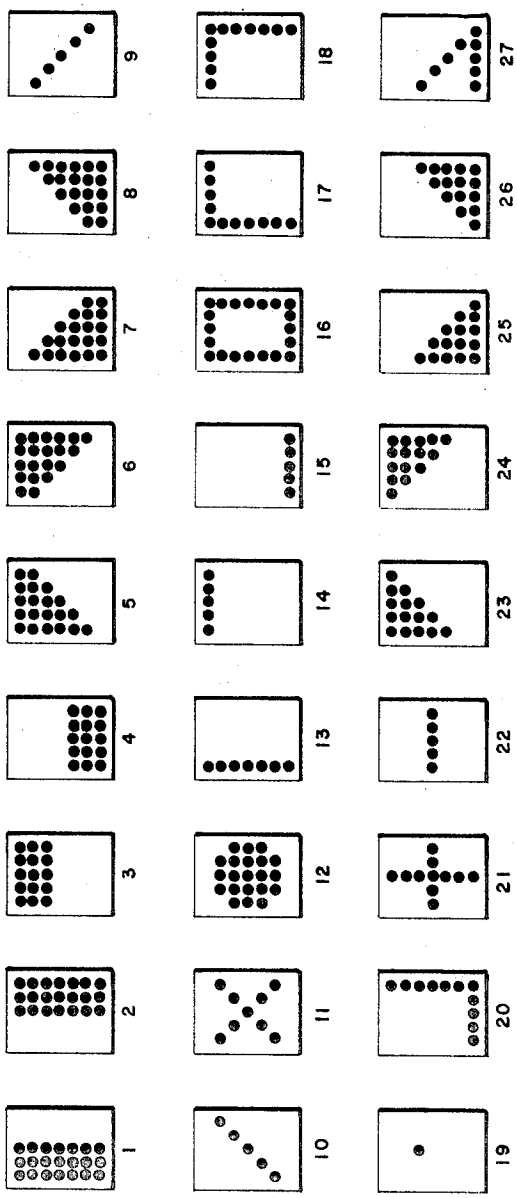


FIG. 5A.

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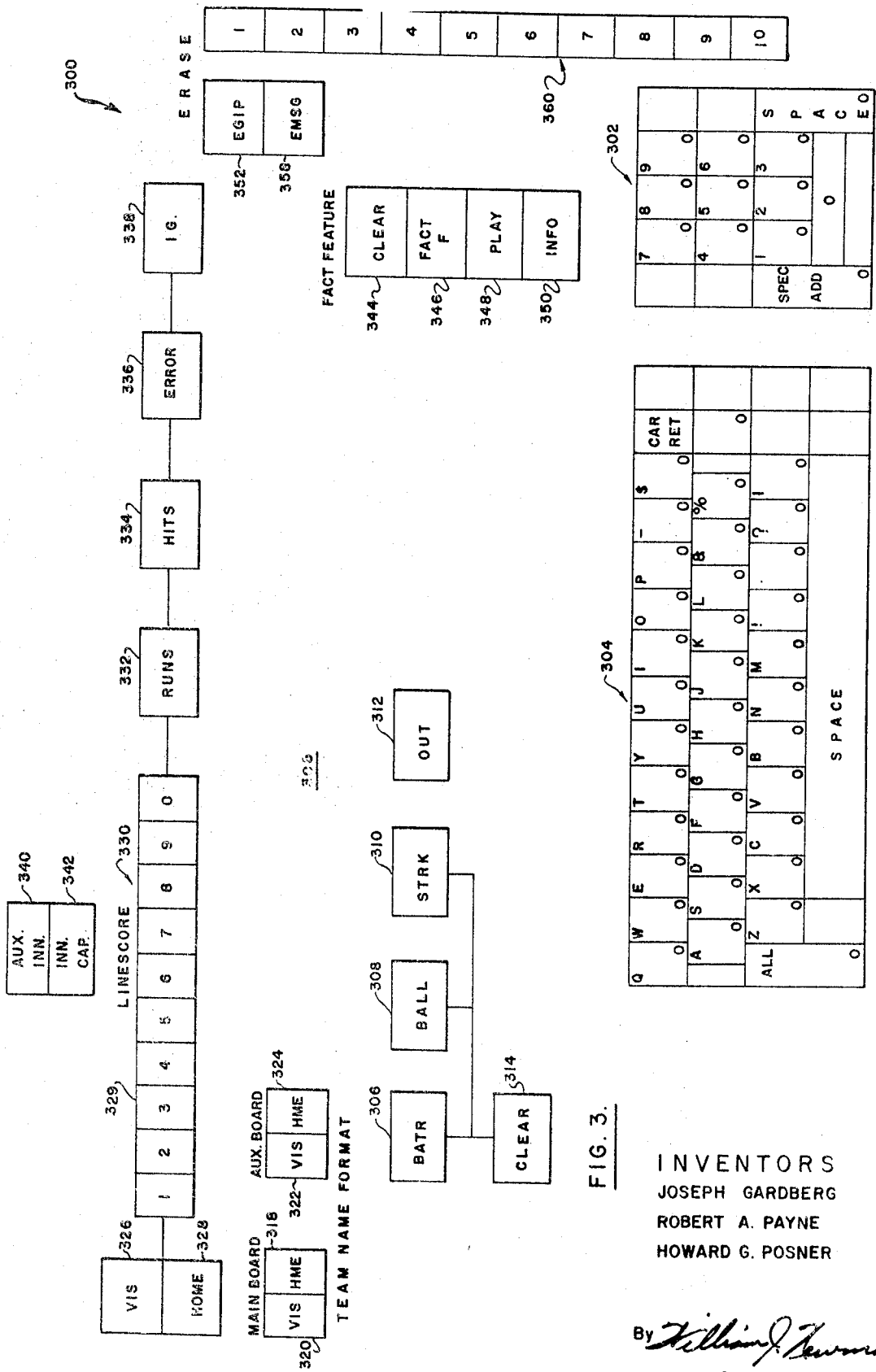


FIG. 3.

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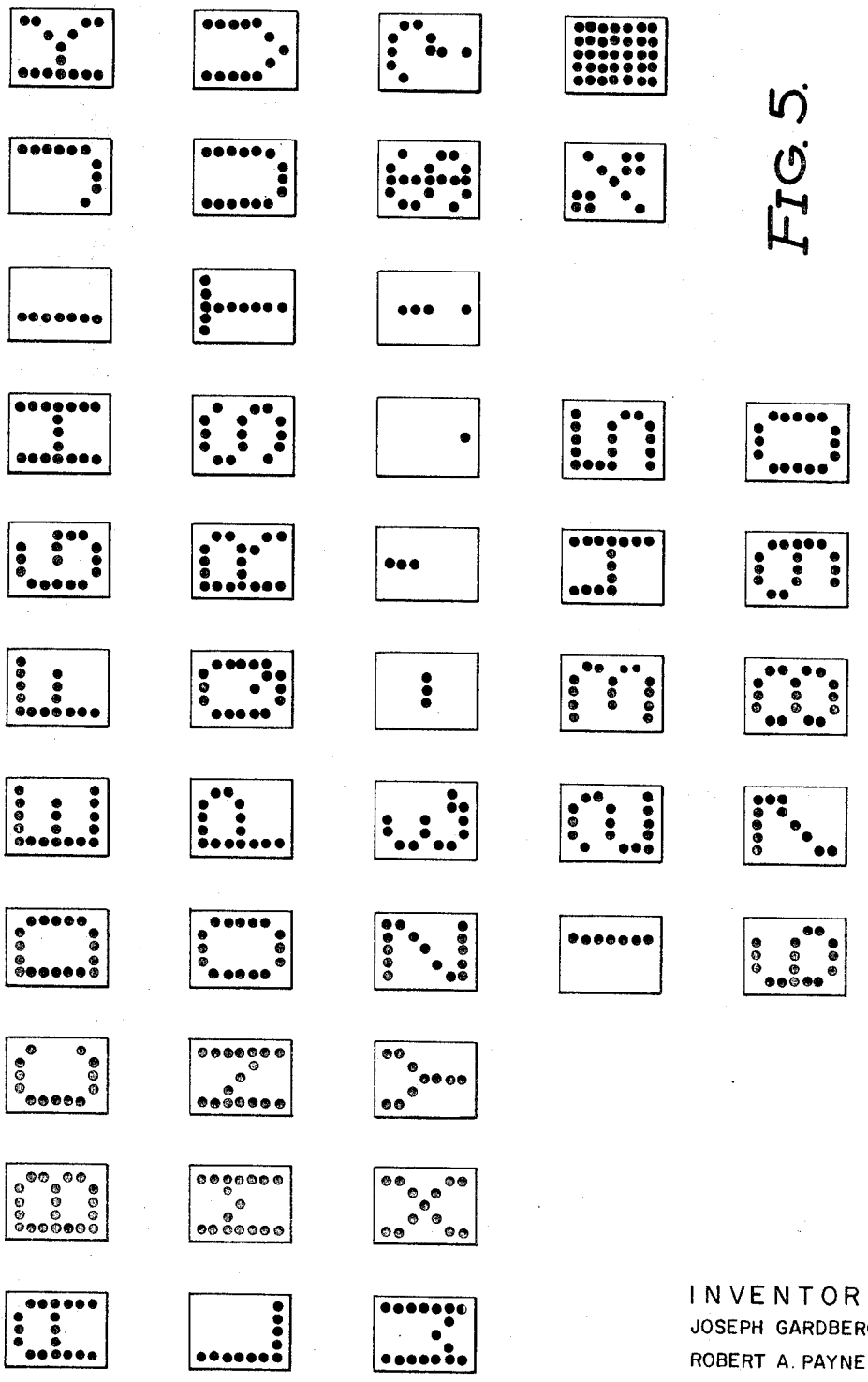


FIG. 5.

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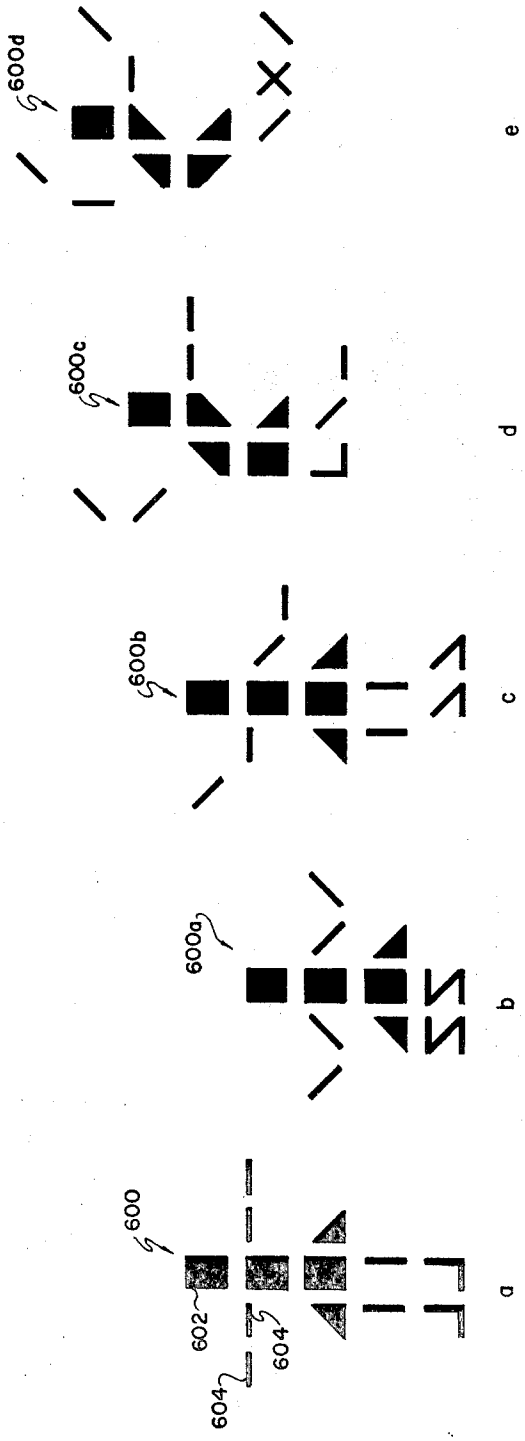


FIG. 6.

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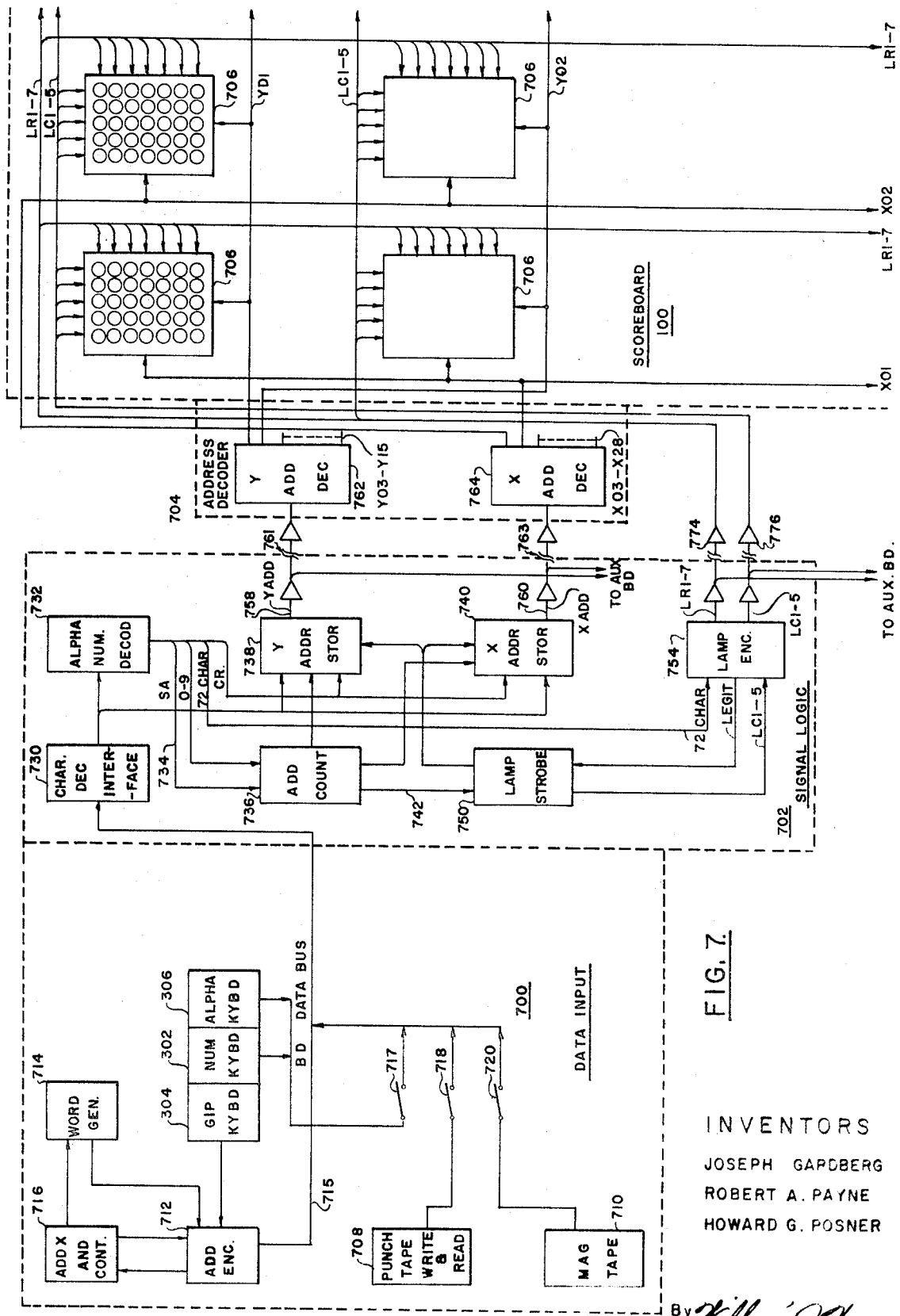


FIG. 7.

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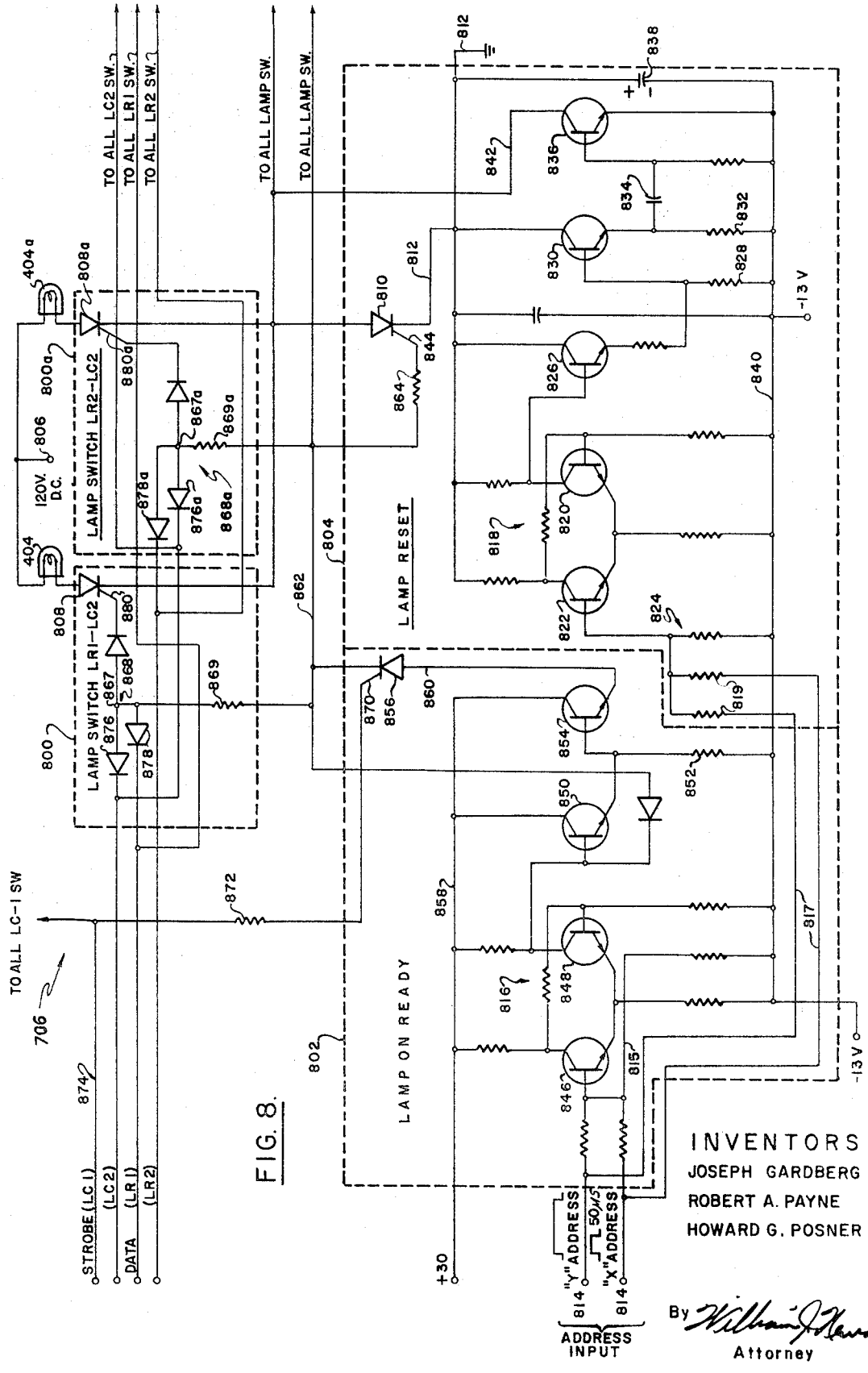


FIG. 8.

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MODIFIED ASCII CODE

b7	b6	b5	b4	b3	b2	b1	COLUMN / ROW	0	0	0	0	1	1	1	1
								0	0	1	1	0	0	1	1
								0	1	0	1	0	1	0	1
								0	1	2	3	4	5	6	7
			0	0	0	0	0 0			SPACE	0		P	ALL	ALL
			0	0	0	1	1 1			!	1	A	Q	SC1	SC16
			0	0	1	0	2 2				2	B	R	SC2	SC17
			0	0	1	1	3 3			#	3	C	S	SC3	SC18
			0	1	0	0	4 4			$	4	D	T	SC4	SC19
			0	1	0	1	5 5			%	5	E	U	SC5	SC20
			0	1	1	0	6 6			&	6	F	V	SC6	SC21
			0	1	1	1	7 7		ETB	'	7	G	W	SC7	SC22
			1	0	0	0	8 0				8	4	X	SC8	SC23
			1	0	0	1	9 1			)	9	I	Y	SC9	SC24
			1	0	1	0	10 2			*SA		J	Z	SC10	SC25
			1	0	1	1	11 3			+		K		SC11	SC26
			1	1	0	0	12 4			BLANK MESS ,		L		SC12	SC27
			1	1	0	1	13 5	CR		-		M		SC13	
			1	1	1	0	14 6			.		N		SC14	
			1	1	1	1	15 7			/	?	0		SC15	

FIG. 9.

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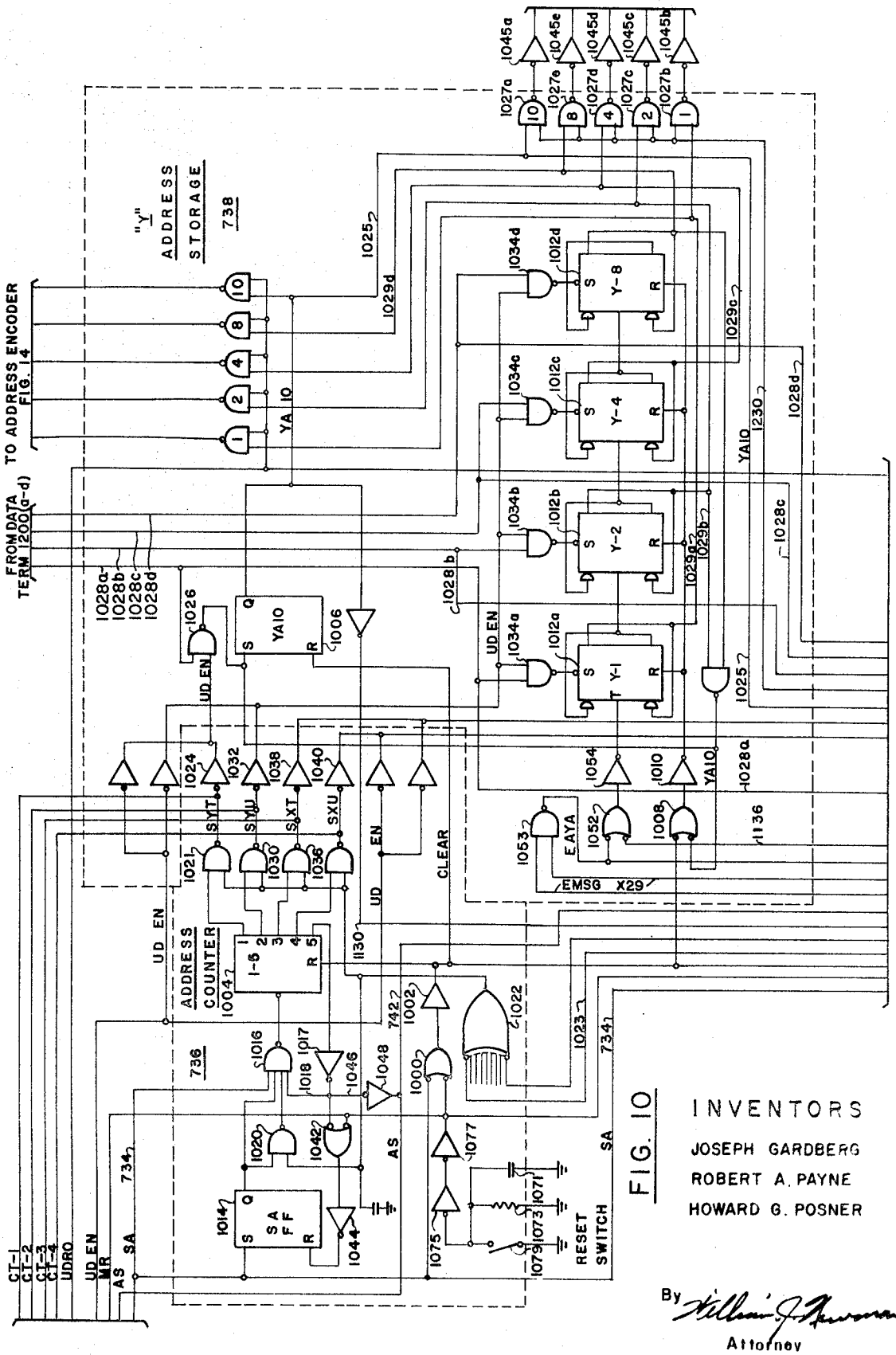


FIG. 10

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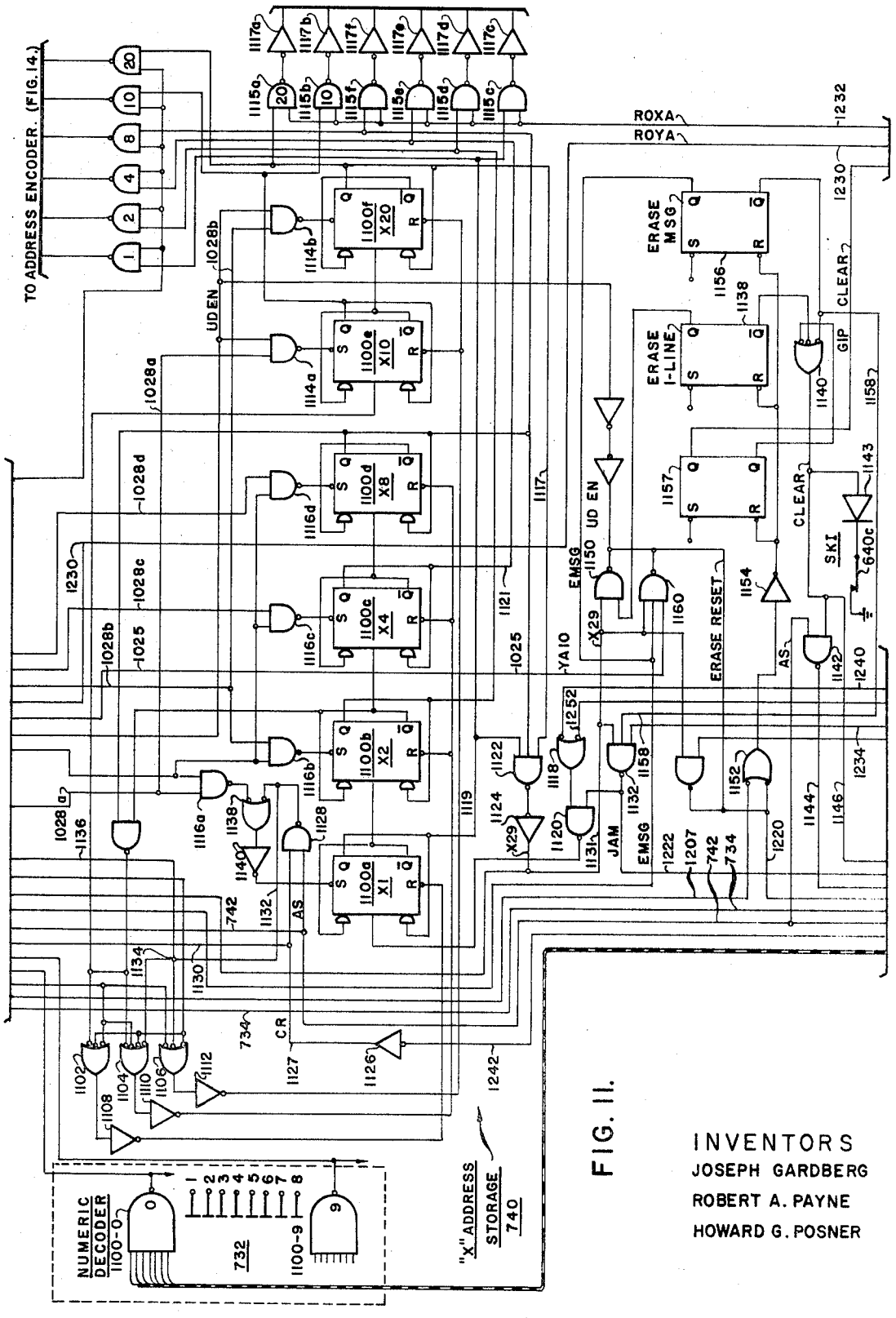


FIG. 11.

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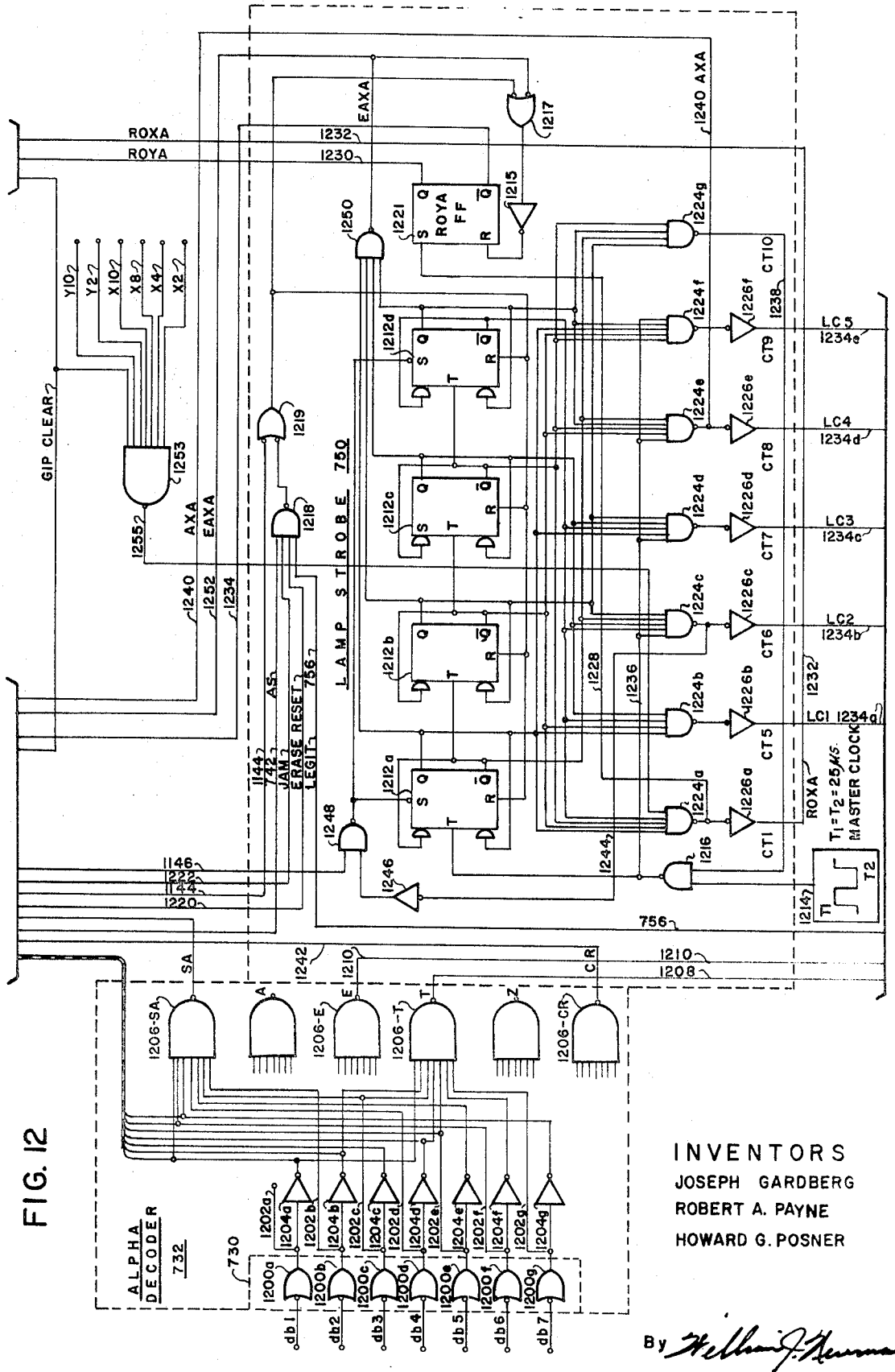


FIG. 12

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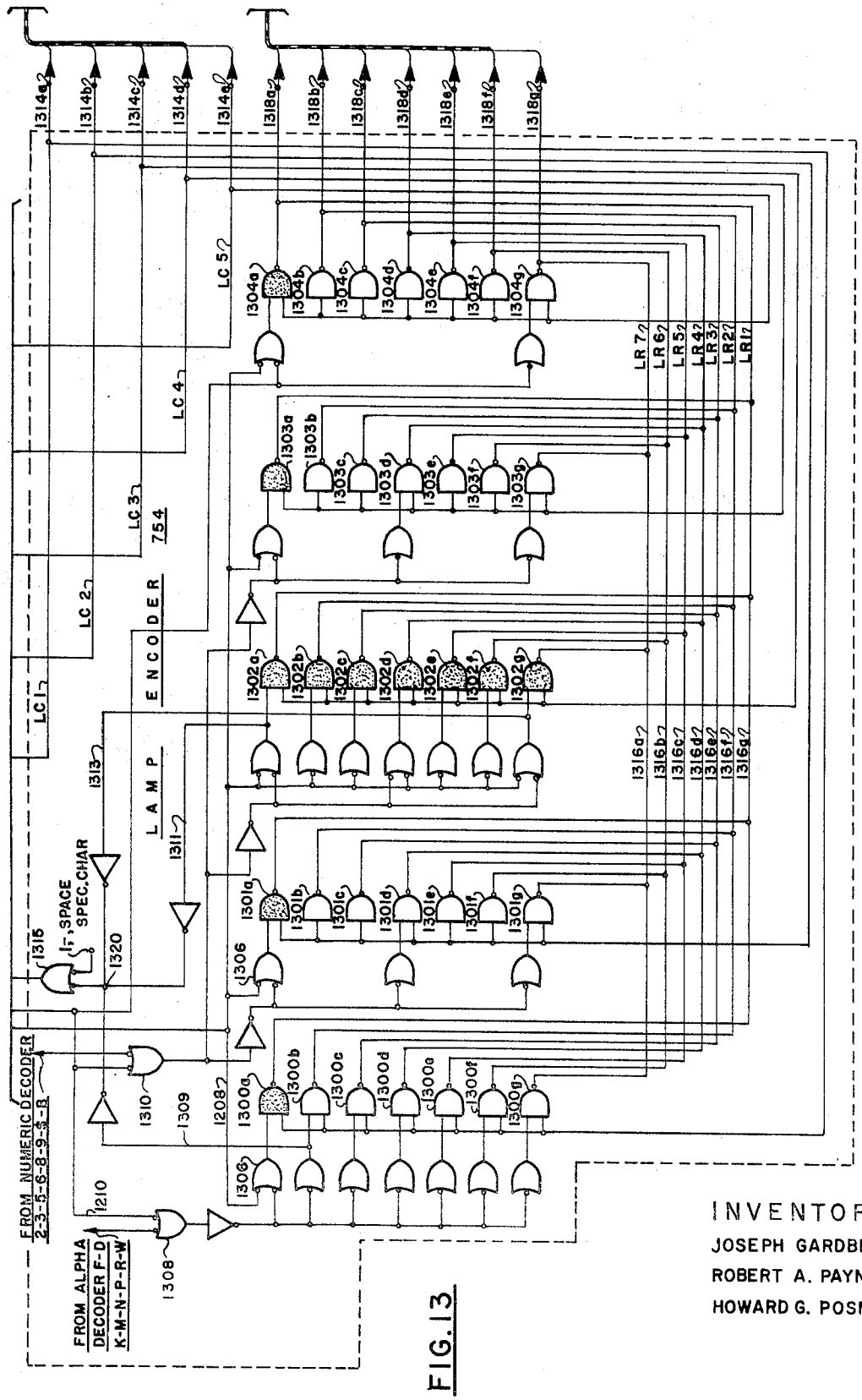
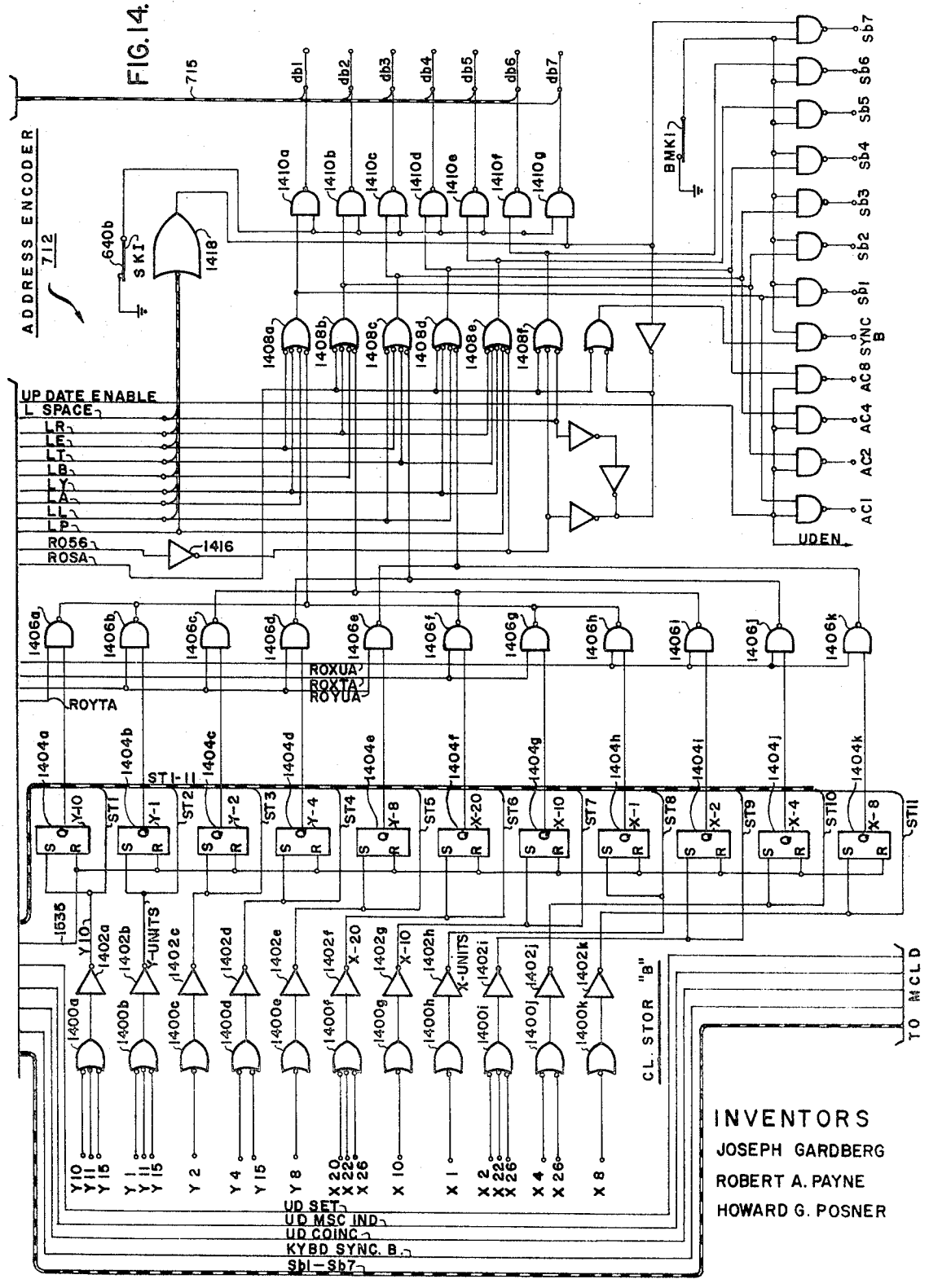


FIG. 13

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FIG. 14.



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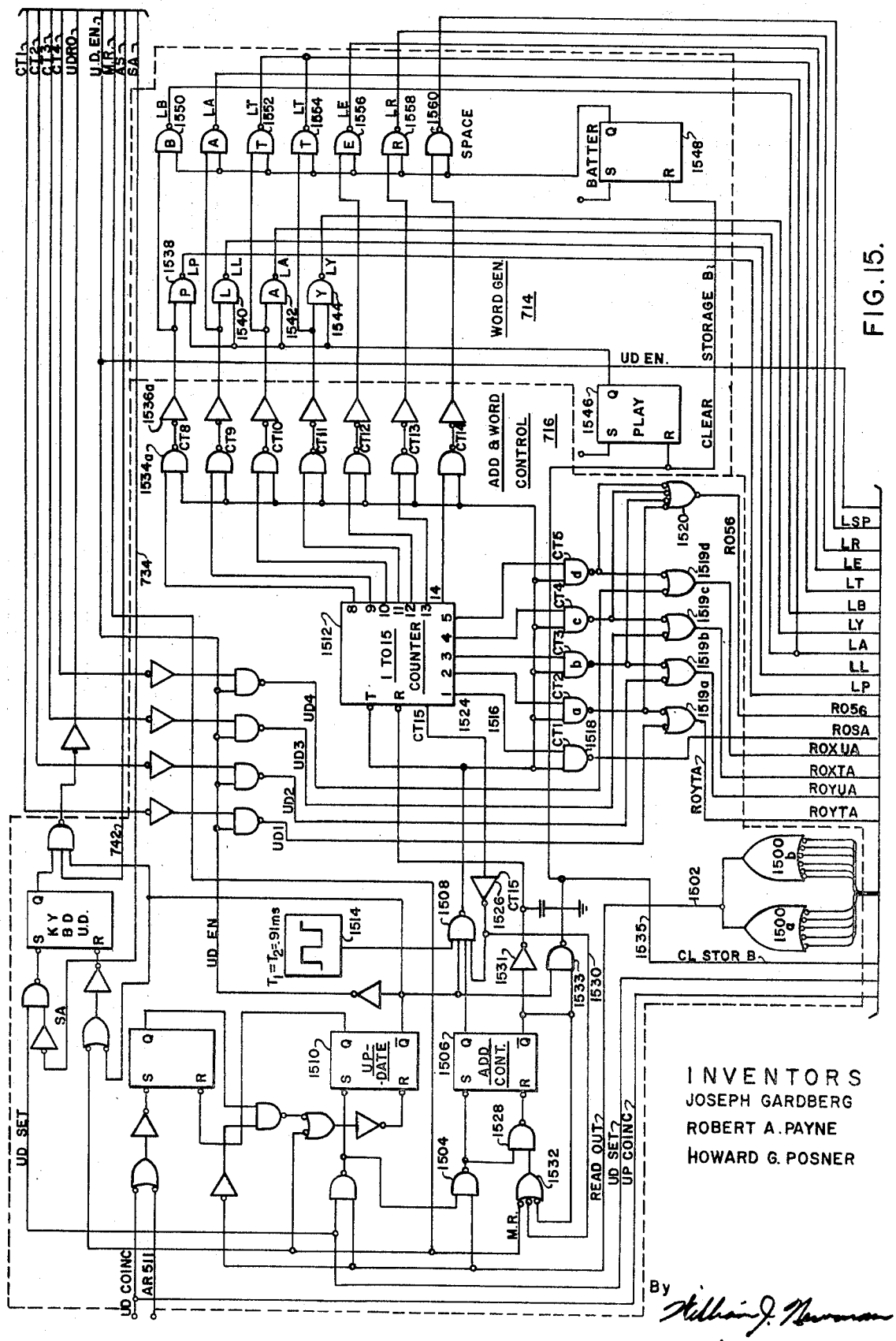
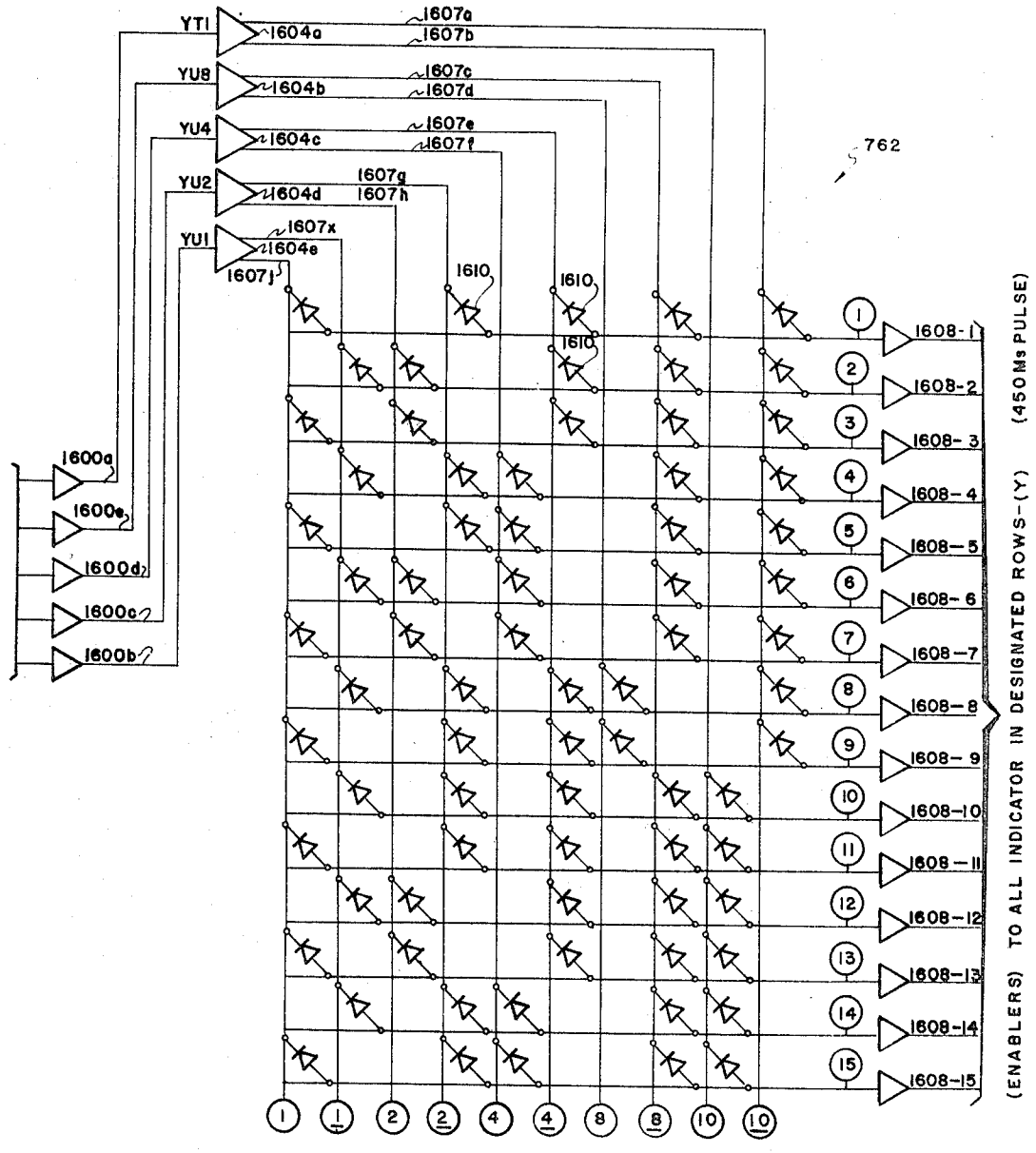


FIG. 15.

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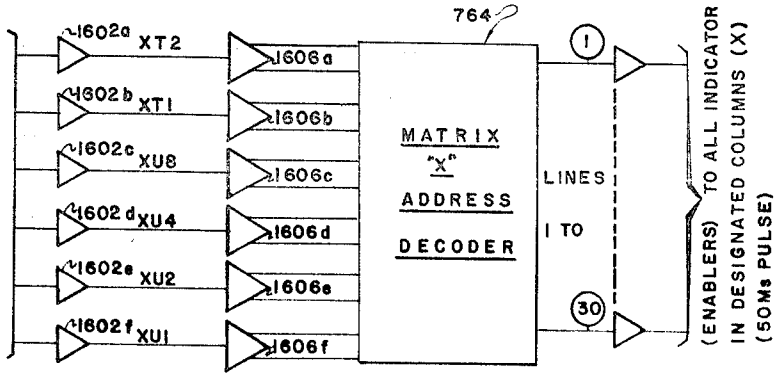


FIG. 16.

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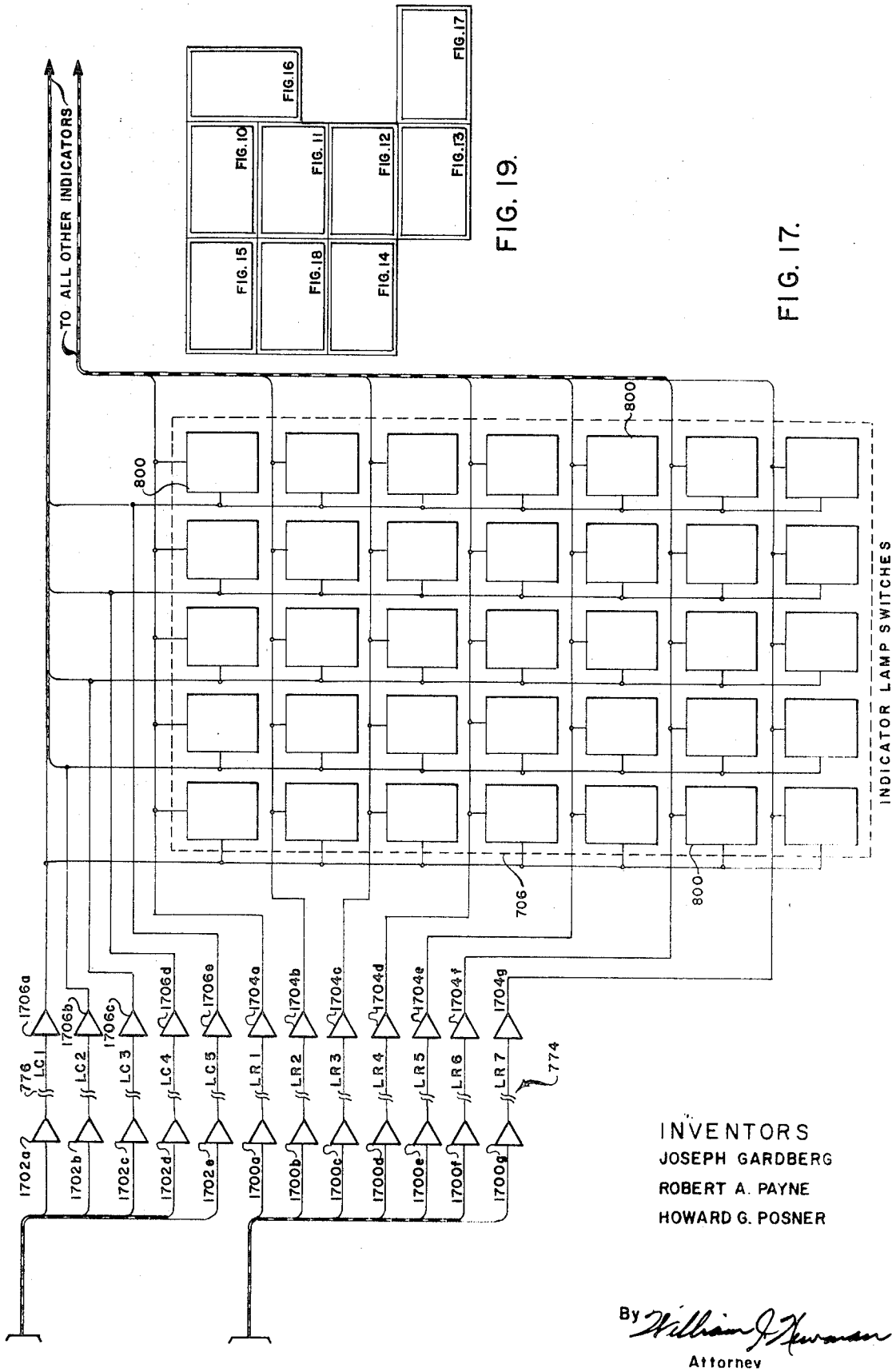


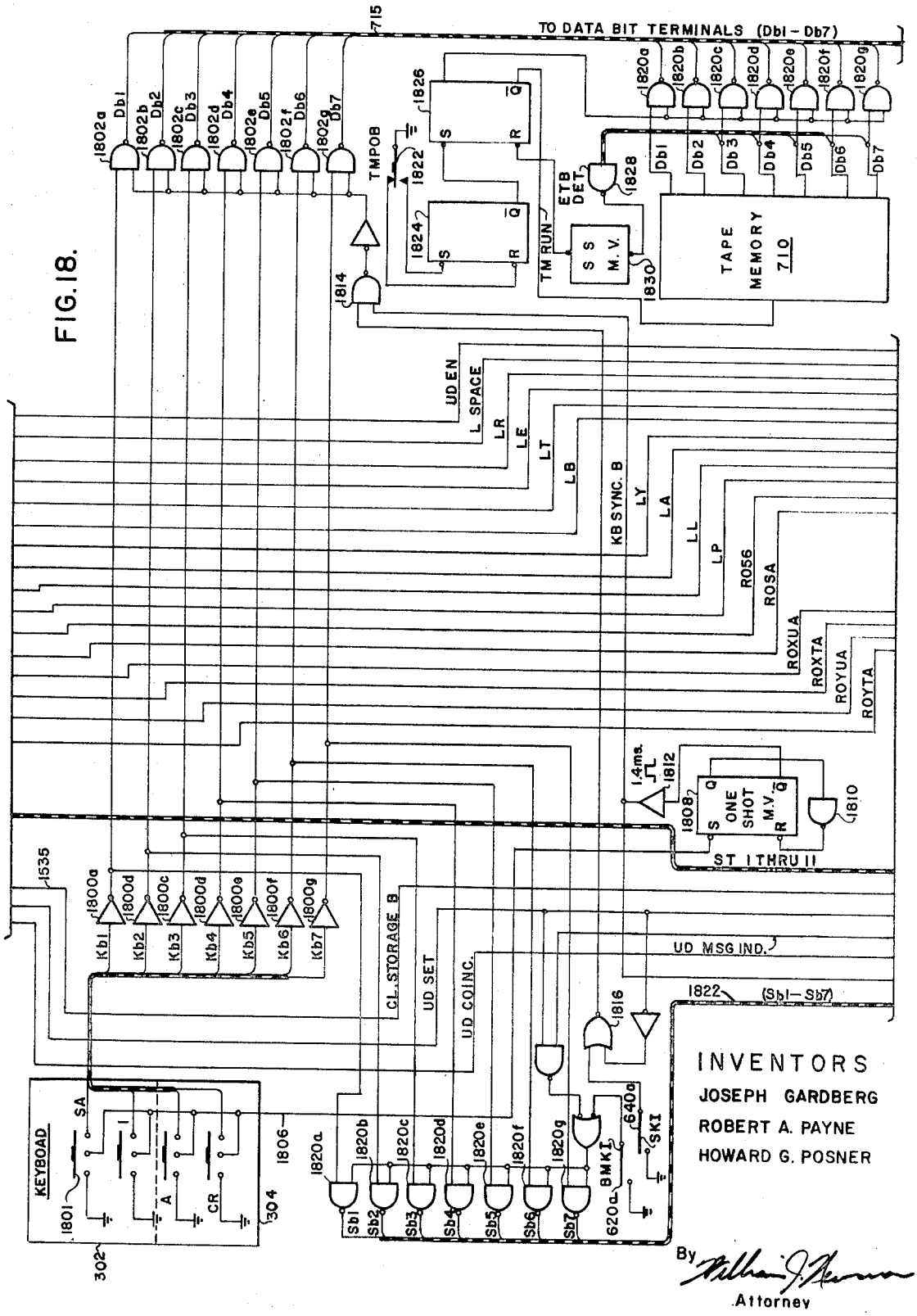
FIG. 19.

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FIG. 18.



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DISPLAY SYSTEM

The system herein described and claimed is a digital controlled, all electronic, semiconductor system having highly flexible input and display output capabilities operable at very high speeds. Basic to the system is its capability to address and read in display data to any location on the display board without having to switch through a number of other locations and without disturbing the data at any other location. That is, any display device or indicator at the display board may be reached and caused to display a desired character merely by inserting the proper address data followed by the desired character data. The address data enables the desired indicator at the desired location on the board and the display data triggers that indicator to operate in accordance with the desired character. Any other desired display device or indicator may then be addressed and triggered or, in the case of message information display, the next sequenced indicator may be automatically addressed to display the desired character. Hence, the system has full flexibility to provide an almost unlimited array of visual arrangements. Besides the usual alpha and numeric characters, the system includes capability to display pictures and even animated cartoons or caricatures.

Typical older type systems were generally electromechanical in nature. Usually an electrical mechanical stepping switch was used for each row of display devices or indicators. To select a desired indicator the operator would press a button to select the proper stepping switch and then pulse the stepping switch the required number of times to reach the desired indicator in that row. The stepping switches had multibanks of contacts by which the data information was sent to the selected indicator. The pulsing of the selector switch of course slowed up the addressing function so that it was difficult to randomly change the display on a particular indicator as is required in animated picture displays.

Because many display systems require that the display panel be located at a remote location from the data input and control console, the number of conductors between the console and the display panel becomes an important factor. In spite of the high flexibility of the system of this invention the number of conductors required is minimized because all of the address information is transmitted over one set of conductors in binary coded decimal form, and all the data display information is transmitted over another set of conductors. In other systems capable of displaying animated cartoons, etc. it has been required to have a separate line from the picture generator to the display panel for each display device or indicator at the display panel.

The system of the present invention also has single button addressing and word generating capabilities. For example, in a baseball scoreboard where it is desired to have ready access to the game in progress indicators for displaying the number of strikes, balls, outs etc. as the game proceeds, the present system has the capability of addressing the desired section of the board by pressing a single button and then inserting the proper numeric data for displaying the proper information.

The word generating capability enables a section of the scoreboard to be used for one or more different, but often repeatable data displays pertaining to the game. For example, there may be a section of the board on which it is desired to display the number of the batter at the plate and alternatively to indicate a particular play during the progress of the game. When the batter number is displayed it is desired to write the word BATTER in that location of the board with the batter's number, and when a rule is to be displayed the word PLAY is displayed at that same location with the proper description. The operator may select the proper display by operating a single button for BATTER or PLAY, whichever is desired, followed by the proper batter number or play information as required. In previous scoreboard systems single button addressing and/or single button addressing with word generating required separate lines between the console and the particular display panel indicators involved. In the system of this invention the address and word generating data is transmitted over the same conductors used for the address and data signals to any display indicator on the board.

This display system also includes a unique control circuit for each of the display devices or indicators at the display panel. No electrical mechanical devices, such as relays, are used in these indicators, but rather switch means are used which are completely electronic utilizing highly reliable and fast operating semiconductor devices such as silicon controlled rectifiers. Unique means are used to reset each indicator if, but only if, the indicator has been addressed, and then reenabled for operation responsive to the subsequent receipt of display data in accordance with the character to be displayed by that indicator.

It is therefore an object of this invention to provide a new display system for scoreboard, information message and/or advertising display materials.

It is also an object of this invention to provide a display system in which a display device or indicator located at any position on the board may be randomly addressed and caused to display desired data.

It is another object of this invention to provide a display system in which the number of conductors between the control console and the message display board is minimized.

Also it is an object of this invention to provide a display system in which particular locations on the board may be selected by means of one button addressing for the display of desired information.

A further object of the invention is to provide a system in which particular locations on the board may be addressed and caused to display predetermined information such as particular words upon the operation of a single button at the console.

Further it is an object of this invention to provide a display system in which a single display indicator encoder is utilized to cause any selected indicator on the display panel to display a desired data character.

Another object of this invention is to provide a control system in which animated characterizations may be displayed by means of the rapid input of serially stored address and display data inserted into the control system from a memory device such as magnetic or punched tape, or the like.

It is another object of this invention to provide a unique indicator circuit utilizing electronic semiconductor devices.

It is also an object of this invention to provide an indicator control circuit having a unique means for resetting the displayed contents of the display indicator.

Other objects and advantages of this invention will be readily apparent to the reader upon a further reading of this specification, especially when taken in view of the accompanying drawings in which:

FIG. 1 is an elevation view of a display board of the type to be used in an athletic stadium for the display of game statistics and message information;

FIG. 2 is an elevation view of an auxiliary scoreboard;

FIG. 3 is a plan view of the operator control console for operating the scoreboards of FIGS. 1 and 2;

FIG. 4 is an elevation view of an indicator of the type used in the scoreboards of FIGS. 1 and 2;

FIG. 5 depicts alpha-numeric and punctuation characters of the type which may be displayed on the indicator of FIG. 4;

FIG. 5*a* depicts special characters which may be displayed on the indicator of FIG. 4 for shaping pictures and/or designs on the message portion of the scoreboard of FIG. 1;

FIGS. 6*a*—6*e* depicts the type of figures that can be formed by the characters of FIG. 5*a*, showing figures in animated sequence for animated cartoon display;

FIG. 7 is a block diagram of the display control system of this invention;

FIG. 8 is a schematic diagram of a control circuit for each individual indicator;

FIG. 9 is a table of modified ASCII coded representations for the display characters shown in FIGS. 5 and 5*a*; and

FIGS. 10 through 17 are schematic diagrams of the control system to be arranged in the manner shown in FIG. 19.

Although the features of this invention pertain to any type of display system, they will be herein described with reference to a scoreboard system which embodies all of the claimed features. The scoreboard hereinafter described is essentially of the type now being used in the Anaheim Stadium at Anaheim, Calif. In the description to follow, the reference numbers used will be coded by means of the 100's and 1000's digits to the particular figure in which the component or element first appears and that component or element will retain that number in any subsequent figure in which it appears. Thus, an element with the number 246 would be found in FIG. 2 whereas an element with number **1216** would be found in FIG. **12**. Conductors extending between one or more figures will be numbered in accordance with the first figure to which they are referenced in the description.

GENERAL DESCRIPTION OF SCOREBOARD AND CONSOLE (FIGS. 1, 2 & 3)

The scoreboard display portion of the system comprises a main scoreboard **100** (FIG. 1) made up of a plurality of display devices or indicators **102** which may register alpha-numeric characters or other designs if desired as will be described hereinafter. If the main board is located in the park so that certain portions of the spectators cannot view it, one or more auxiliary scoreboards **200** (FIG. 2) may be located at appropriate locations. The auxiliary scoreboard **200** is also made up of display indicators **102** of essentially the same type utilized in the main board. The main scoreboard **100** is divided into two basic sections, namely, the game in progress section **104** and the message portion **106**, while the auxiliary scoreboard **200** is devoted strictly to game in progress information.

As shown in FIG. 1 the scoreboard display panel is arranged in rows (**Y01** through **Y15**) and columns (**X01** through **X28**) of indicators for the purpose of exact addressing of any desired indicator. Thus, any indicator on the display panel **100** may be referred to by stating its address in terms of its Y number and its X number. In the system described the first row of the message section **106** is designated **Y01** and the message portion continues through row **Y10** while the game in progress portion includes rows **Y11** through **Y15**. Thus, the indicator **105**, upon which the letter A in the word AMERICAN is portrayed, has the location address **Y01—X11**, whereas the indicator **107** displaying the letter G in the word ANGELS is located by the address **Y15—X03**. In the system described each Y and X address number must consist of two digits to satisfy the system logic as will be seen later. Hence, address numbers under 10 must be preceded by a zero, e.g. 01, 02 etc.

Any indicator on the board except certain fixed caption indicators in the game in progress section **104** may be reached to display a desired character by reading into the control system the proper address for that indicator. This is accomplished, for example, by the use of the numeric keyboard **302**, forming a part of the operators console **300** shown in FIG. **3**. Thus, indicator **105** may be reached to display the letter A by first punching the key marked SPEC. ADD. (Special Address) followed by the number 01 for the Y address, which is in turn followed by the number 11 for the X address. The subsequent actuation of the A key in the typewriterlike alpha keyboard **304** will then cause the latter A to be displayed on addressed indicator **105**. The following indicators are then automatically sequentially addressed so that the operator needs merely to punch the alpha keys M, E, R, I, C, A and N to display the whole word AMERICAN.

If the message is longer than the row, then further message display is impeded until the carriage return key **305** is actuated to cause the automatic addressing of the first indicator in the next row. The message may then be continued until the last indicator in the last row of the message section (**Y10—X28**) is reached. Further automatic advancing of the address is then prevented because the next numbered indicator row **Y11** is in the game in progress section **104**. Thus, the indicators in the Game in Progress Section cannot be inadvertently affected, when writing in a message on the Message Section **106**.

As previously mentioned, the game in progress section **104** of the main scoreboard **100** as well as the auxiliary scoreboard **200** are devoted to information pertaining to the particular game being played. The top two rows of indicators **Y11** and **Y12** are used for the display of play by play information while the next three rows **Y13** through **Y15** are used for the inning by inning or line score information as well as the game totals. This section of the board is controlled by the upper portion **305** of the operators console shown in FIG. **3**. The indicators in the top row **Y11** displaying the words BALL, STRIKE, OUT and BATTER are fixed caption indicators which are actuated by a power switch directly connected to those indicators and are not controlled by the control logic of the system hereinafter described. These indicators might also be arranged to display fixed captions for football games in which case the words DOWN, TO GO, QTR, and BALL ON will be displayed. The indicators in row **Y13** displaying the captions R, H, E and 1G are also fixed caption indicators not controllable by the control logic.

To display the desired play by play information the operator manipulates the proper button **306**, **308**, **310** or **312** which automatically addresses the related numeric indicators immediately below the appropriate fixed captions. The numeric information is then read in by means of the numeric keyboard **302**. Thus, the present batter's number is displayed by first operating key **306** which automatically addresses numeric indicator **Y12—X21** followed by the player's number inserted from the keyboard **302**. Each ball and strike of the batter is registered by operation of buttons **308** and **310**, followed by the insertion of the numeric data from keyboard **302**. When the next batter comes to bat the previous batter's number and the balls and strikes may be erased by operation of the CLEAR button **314**.

The ball, strike and out data is displayed on the auxiliary scoreboard **200** simultaneously with its display on the main board **100**. The numeric indicators immediately following the fixed captions on the auxiliary board **200** are designated by the same addresses as the corresponding numeric indicators on the main board so that they may be controlled together. Thus, the indicator immediately after the fixed caption indicators spelling BALL on the auxiliary board **200** has the same address, **Y12—X02**, as the indicator immediately under the fixed caption indicators spelling BALL on the main board **100**.

The group of indicators **206** are used for displaying various information including the present batter's number. However, since these indicators are used for other information, fixed caption indicators cannot be used and the word BATTER is automatically displayed by means of the control logic. Therefore, when the operator actuates button **306** on the console, the control logic automatically generates the word BATTER and causes it to be displayed on the first six indicators of the group **206**. The insertion of the batter's number automatically causes its display on the last two indicators of the group **206** on the auxiliary board. The addresses for the auxiliary board indicators of group **206** and the word is generated in a manner which will be hereinafter described with respect to the control logic system.

The line score information of rows **Y13** through **Y15** of the main board is also controlled by means of single button addressing in a manner similar to the play by play information of lines **Y11** and **Y12**. For example, the word ANGELS is written onto indicators **Y15—X01** through **Y15—X06** on the main board **100** by use of the home team button **318** in the team name format portion of the console **300** which automatically addresses indicator **Y15—X01**. This is followed by the insertion from the alpha character buttons on keyboard **304**, the letters spelling out the name ANGELS. The visiting team name format button **320** is used for the single button addressing of indicator **Y14—X01** for writing in the name of the

visiting team. Separate auxiliary board team name format buttons 322 and 324 are provided because the names are to be abbreviated in indicator groups 208 and 210 on the auxiliary board 200. However, if the same number of indicators were provided as in the main scoreboard, the names could be written in simultaneously on the two boards by giving them both the same address.

It is to be noted that the single button means of addressing is in addition to the multibutton addressing previously described for writing in the word AMERICAN, and this capability extends throughout all of the scoreboard so as to give double access to any indicators therein.

The line score statistics may be inserted in rows Y14 and Y15 for the visitor and home teams, respectively, by actuation of the appropriate team buttons 326, 328 followed by the appropriate inning button from inning button group 330 or one of the buttons 332, 334, 336 or 338, whichever is required for the information to be displayed. This addresses the proper indicator in the line score portion of the board and the subsequent input of a numerical character from keyboard 302 will cause the proper display. Thus, to indicate an Angels run in the third inning, the operator will press the home team button 328 followed by the third inning button 329 of the line score inning group 330, followed by the numeric character 1 button on numeric keyboard 302.

The auxiliary board only displays the total runs of each team on the indicators immediately following the team name groups 208 and 210 and are addressed simultaneously with the runs indicators Y14—X22 and Y15—X22 when the respective team buttons 326, 328 and the runs button 332 are actuated. A subsequent insertion of the numeric data from keyboard 302 will cause the data to be displayed simultaneously on the two boards. The inning number is entered into the auxiliary board following the fixed caption indicators displaying INN by operation of the AUX INN button 340, followed by the appropriate number from keyboard 302. The INN CAP button 342 is used for displaying the inning captions 1 through 0 in row Y13 of the main board 100.

The fact feature controls on the console, including buttons 344, 346, 348 and 350, are used for displaying pertinent facts about a particular play in the nine indicators in rows Y11 and Y12 at the upper right-hand corner of the main board 100 and in the group of indicators 206 on the auxiliary board 200. The FACT F. button 346 is a one button address selector for the group of four indicators 108 in row Y11 and is used for writing any desired two-, three- or four-letter word thereon. It also addresses the first four indicators in the group 206 on auxiliary board 200. Thus, if it is desired to display the rule book number pertaining to a particular play, the operator presses the FACT F. button 346 and writes in the word RULE from the alpha keyboard 304. The INFO button 350 is then pressed which addresses the first indicator in group 110 and the rule book number is entered into the indicators 110 from the numeric keyboard 302. This information is also displayed on the auxiliary board group 206.

The play button 348 automatically displays the word PLAY on the indicators of group 108 of the main board and also on the first four indicators of the group 206 on the auxiliary board. The indicator group 110 and the last five indicators of group 206 are then automatically addressed for insertion of the desired information. Thus, if the shortstop commits an error, the operator would press the play button 348 to display the word PLAY on the proper indicators and immediately enter the display data E6 from the keyboards 304, 302 to designate an error by the shortstop.

The erase function buttons 352, 358 and 360 perform the obvious function of extinguishing the bulbs in particular indicators on the scoreboards. The EGIP button 352, which stands for Erase Game In Progress, serves to erase all of the information displayed in the section 104 of the main scoreboard as well as the information on the auxiliary scoreboard, except for the fixed caption indicators. The EMSG button 358 provides for the erasure of all the information in the 10 rows forming the message section 106 of the message board. The group of buttons 360 provide for the erasure of a selected row in the message portion 106 of the scoreboard and that row is erased merely by depressing the particular button corresponding to the row desired to be erased.

The manner in which the manipulation of the various buttons on the console perform their indicated functions will be described in later sections of the specification relating to the control logic of the system.

DISPLAY CHARACTERS (FIGS. 4, 5, 5*a* and 6)

The display devices or indicators 102 utilized in the display system herein described are individual modules, each comprising a matrix of 35 lamps 400 arranged in seven rows (LR-1 through LR-7) and five columns (LC-1 through LC-5) as indicated in FIG. 4. The different characters are formed by illumination of the lamps in the desired pattern. FIG. 5 shows the standard alpha, numeric and punctuation displays as they would be formed on a 35-lamp matrix.

A large variety of other display characters may also be formed by the lamp matrix indicators 102 which can be used in forming pictures, designs or animated displays on the message portion 106 of the scoreboard. FIG. 5*a* shows a number of different display characters which may be programmed for use in this manner. The cheerleader figure 600 shown in FIG. 6 is but one example of how the characters in FIG. 5*a* may be used to form a pictorial representation. Each of the separate geometrical shapes in figure 600 is made up of a group of energized lamps in a particular indicator on the board. The head 602 of the figure is made up of an indicator having all its lamps lit while the arm portions 604 are made up of the lamp display referenced 14 in FIG. 5*a* with the top row of lamps lit. The figures 600*a* through 600*d* indicate how displays may be shown in a sequence of changing positions to portray an animated characterization. This is accomplished by the proper programming of information in a manner that will be described hereinafter.

It is to be understood that other indicator configurations might be utilized without departing from the teachings of this invention. For example, the lamps 400 need not necessarily be arranged in 5×7 matrices, but may be arranged in any convenient manner with any number of lamps. Also it may be desirable to use other visually observable elements than lamps depending upon the use of the board. Whereas light bulbs mounted in a board having a black surface is preferred for outdoor display systems where a wide range of ambient light conditions call for the use of transmitted light, indoor locations may call for other visually observable elements. For example, if the board is located in a constant high illumination ambient area, it may be desirable to utilize reflective members such as white painted discs or the like instead of lamps 400.

In addition, for certain aspects of this invention, it may be desirable to use other types of visual displays than the matrix type indicators. Some message board applications might call for alpha-numeric wheels or belts or any of the other well-known type of alpha-numeric character displays and where applicable the use of such are contemplated.

GENERAL DESCRIPTION OF CONTROL SYSTEM (FIG. 7)

The control system as shown in the block diagram of FIG. 7 comprises data input means 700 and signal logic means 702 usually located at the console, as well as the address decoder means 704 and the indicator circuits 706 (one for each indicator 102) located at the scoreboards 100 and 200.

The data input means 700 which is controllable by the operator, provides data in the form of a modified ASCII digital code such as shown in the Table of FIG. 9 to the signal logic 702 which then transforms it into appropriate signals for transmission over cables to the scoreboards. There the signals enable the desired indicators and actuate the appropriate lamps in the selected indicators to display any of the characters in

FIGS. 5 and 5a. The address data is generated in the data input 700 in binary coded decimal form utilizing the ASCII code while the display data is in ordinary binary form using the ASCII code. The data is presented to the signal logic by the alpha-numeric keyboards 304, 302 previously mentioned, by punch tape typewriter and reader 708, and by storage devices such as a magnetic tape memory 710. Also address and display data for certain words (e.g. BATTER or PLAY) can be automatically encoded into the modified ASCII code for serial transmission to the signal logic 702 by means of the address and word control circuit 716, address encoder 712 and word generator 714 in a manner to be described in more detail hereinafter.

Each of the separate data input devices 302, 304, 708, as well as the automatic address and word generator 712, 714 have seven line outputs for delivering the ASCII code to the Board Data Bus 715 leading to the signal logic 702. These outputs are connectable directly to the signal logic 702 through respective switching circuits 717, 718 and 720 in which case the data characters are displayed one by one on the scoreboard 100 as they are read from the input devices. The keyboard and typewriter inputs of course are limited by operator's capability as to data input speed but high speed, extended serial input such as required for animated cartoons is provided by the magnetic tape device 710.

The magnetic tape also provides a convenient storage for other types of messages which are often used during operation of the board and require quick recall. Punch tapes also provide permanent memories of any desired messages. These may be used at any time by passing the tape through the punch tape typewriter and reader 708 which transforms the punched data into ASCII code electric signals in a well-known manner.

The signal logic 702 provides the control function by which the proper indicators on the scoreboard 100 are addressed and actuated to display the desired character in accordance with the address and character display data received from the data input 700. The seven bit ASCII code signals are received from the data input 700 by the character decoder interface 730 in the signal logic. The alpha-numeric decoder 732 then transforms the ASCII code signals into a single conductor signal on one of the 72 output conductors, each of which is representative of one of the display characters in FIGS. 5 and 5a on a special instruction conductor such as the Special Address or Carriage Return.

As previously described, address data is always immediately preceded by a special address character which indicates to the signal logic that the immediately following two digits represent the Y, or row address, while the third and fourth digits indicate the column, or X address. The alpha-numeric decoder 732 recognizes the special address character and sends a signal over conductor 734 to start the operation of the address digit counter 736. The four address digits for the Y and X addresses are then received and stored in their respective address storage circuits 738 and 740 respectively. After the four address digits have been stored, the address counter 736 sends a signal over conductor 742 to the lamp strobe circuit 750 which enables the read out of the character display data when it is received in the lamp encoder circuit 754.

The character display data is received by the character decoder interface 730 and the alpha-numeric decoder 732 which furnishes a signal pulse on one of the 72 lines to the lamp encoder 754. If the lamp encoder 754 recognizes it as a legitimate character display signal which is able to be displayed by an indicator lamp matrix, a Legit signal is provided over line 756 to the lamp strober 750.

The receipt of the Address Stored signal and the Legit signal cause the lamp strober 750 to operate to read the address data from the Y and X address storage circuits 738, 740, in parallel fashion over their respective multiline conductors 758, 760 and cables 761, 763 to the Y and X address decoders 762, 764 at the scoreboards 100 and 200.

The parallel received signals at the Y and X address decoders 762 and 764 are transformed into a simultaneous single signal on one of the 15 output lines of the Y address decoder and one of the 28 output lines of the X address decoder. Each of the 15 lines of the Y address decoder is connected to a respective row of indicators Y01 through Y15 whereas each of the 28 output lines of the X address decoder 764 is connected to a respective column of indicators X01 through X28. Thus, each indicator 102 is connected to one line from the Y address decoder 762 and one line from the X address decoder 764 and when the particular indicator receives simultaneous signals from both it is enabled to receive the immediately following character display data to actuate its lamps 400 in accordance with the character to be displayed.

Immediately after the Y and X address data has been read out of the storage devices 738, 740 the lamp strobe 750 signals the lamp encoder 754 to transmit signals in accordance with the character display data over its output data conductors 768 and strobe conductors 770 through the respective cables 772, 774 to the particular preaddressed indicator circuit 706 at the scoreboard.

The lamp encoder data output and cable 774 are 7-line conductors each of which is connected to enable a respective row of lamps in the 5×7 lamp matrix indicators. The strobe output and cable 776 are 5-line conductors each of which is connected to enable a respective column of lamps in the 5×7 lamp matrix indicators. The five strobe conductors transmit five consecutive pulse signals, one on each line, which are delivered successively to the five lamp columns in sequential order from the left-hand column to the right-hand column of each lamp matrix indicator. The simultaneous receipt of lamp data signals over one or more of the seven data lines connected to the rows of indicator lamps in coincidence with the lamp column strobe signals causes the appropriate lamps in each column to be actuated in accordance with the particular character to be displayed.

Referring back to FIG. 4 for a more precise description of the lamp data and strobe signal operation of the indicator lamps 400, it will be noted that each of the rows of lamps are marked respectively LR1 through LR7 whereas each of the columns are marked LC1 through LC5. Each of the lamps in rows LR1 through LR7 are connected to be enabled by a signal on the corresponding one of the seven data lines from the lamp encoder 754 while the five columns of lamps LC1 through LC5 are connected to be actuated by a pulse on a respective one of the five strobe lines from the lamp encoder 754. Thus, to form the letter T as shown on the indicator 102 in FIG. 4, the first pulse LC1 on the first of the five strobe lines from the lamp encoder will correspond with a simultaneous signal on the first data line which corresponds to the lamp row or LR1 row of indicator lamps. Thus, lamp 402 is lit with the first strobe pulse. The second strobe pulse on the second strobe line of the 5-line strobe output of lamp encoder 754 is received simultaneously at the indicator 102 with another LR1 signal on the first lamp data line of the 7-line data output from the lamp encoder. Thus, lamp 404 is lit on the second or LC2 pulse. The LC3 strobe pulse on the third of the five strobe lines from the lamp encoder is received simultaneously with pulses on each one of the seven lamp data lines from the lamp encoder so that all seven of the lamps 406 through 406f are lit on the third or LC3 strobe pulse. Likewise, lamps 408 and 410 are lit on strobe pulses LC4 and LC5, respectively, to complete the letter T on the lamp indicator 102. Means are provided in the indicator circuit 706 for each indicator 102 for maintaining the actuated lamps lit until a reset signal is received by the indicator circuit 706 to turn out all energized lamps in a manner to be hereinafter described.

INDICATOR CIRCUIT (FIG. 8)

Reference is now made to FIG. 8 showing in schematic form an indicator circuit 706 which is used to control the lamps in each indicator 102 for the display of a desired character. The indicator circuit 706 includes 35 lamp switch circuits such as

800 and 800*a*, one for each lamp in the 5×7 matrix in the indicator. As will be seen switches 800 and 800*a* control lamps 404, 404*a* in matrix positions LR1–LC2 and LR2–LC2 respectively. There is also a lamp on-ready circuit 802 for preparing the circuit responsive to the receipt of the indicator address data corresponding to the particular indicator, and a lamp reset circuit 804 for turning off any previously lit lamps in the indicator responsive to the receipt of the particular indicator address data.

The energizing circuit for each of the lamps in the indicator extends from a 120 volt DC source 806 through the respective lamps 404, 404*a* and lamp switch silicon controlled rectifiers 808, 808*a* in the respective lamp switch circuits 800, 800*a*. The cathodes of all the lamp switch SCR's 808, 808*a* are connected together and to the anode of a reset SCR 810 in the lamp reset circuit 804, the cathode of which is connected to ground at 812. Thus, any lamp 400, 400*a* may be energized through the actuation of its respective lamp switch SCR 808, 808*a* and the reset SCR 810. All of the lamps may be extinguished or reset by the cutoff of reset SCR 810 in a manner to be hereinafter described.

The Y and X address data is received at terminals 814 in the form of simultaneously appearing positive going pulses. The X address pulse is 50 microseconds long and the Y address pulse is substantially longer being governed by the speed of data input as will become apparent hereinafter.

The Y and X address pulses are anded at the input 815 to a Schmidt monostable multivibrator circuit 816 in the lamp on-ready circuit 802 and, by means of conductors 817 and resistors 819, at the input 824 to another Schmidt monostable multivibrator circuit 818 in the lamp reset circuit 804. The Schmidt circuit 818 in the lamp reset circuit 804 has a short hysteresis curve so that its duty cycle is governed by the short X address data signal. Transistor 820 is normally conducting but transistor 822 goes into conduction upon receipt of the Y and X address signals at the input circuit 824 to the base of transistor 822. The conduction of transistor 822 causes 820 to cut off, and the positive pulse at the collector thereof is fed to the base of emitter follower transistor 826. The positive pulse across emitter resistor 828 pulses emitter follower transistor 830 into conduction, and the positive pulse across its emitter resistor 832 is transmitted through capacitor 834 to the base of transistor 836. The emitter-collector circuit of transistor 836 thus provides an effective shunt across reset SCR 810 from the grounded cathode 812 of the reset SCR 810 through capacitor 838, negative 13-volt conductor 840, the emitter-collector circuit of transistor 836, and conductor 842 to the anode of SCR 810. Thus, conduction of transistor 836 places −13 volts from the charged capacitor 838 directly across the reset SCR 810 to cut it off and open the energizing circuits to any previously lit lamps 400, 400*a*. After the 50 microsecond X address pulse the Schmidt circuit 818 restores to normal cutting off transistor 836 to remove the shunt from across the reset SCR 810. The reset SCR 810 will of course not conduct again until a positive signal is received on its gate 844.

The lamp on-ready circuit 802 operates responsive to the receipt of the Y and X address pulses to prepare the lamp switch circuits 800 and also to reactivate reset SCR 810 in the following manner. The two address signals are anded at the input 815 of the Schmidt multivibrator circuit 816 which in contrast to the Schmidt circuit 818 in the lamp reset circuit 804 has a long duty cycle of at least 450 microseconds. Thus, it will not follow the 50 microsecond X address pulse as does the lamp reset multivibrator 818. The normally off transistor 846 is triggered into conduction by the anded address pulses causing transistor 848 to cut off. The positive going signal at the collector of transistor 848 triggers emitter follower transistor 850 into conduction and the positive pulse across its emitter resistor 852 appears at the base of transistor 854. Positive 30 volts is thus placed on the anode of a triggering SCR 856 from the +30 volt conductor 858 through the collector to emitter circuit of transistor 854 and conductor 860. The cathode of SCR 856 is connected through conductor 862 and resistor 864 to the gate 844 of reset SCR 810 so that when SCR 856 goes into conduction it triggers the reset SCR into conduction. The gate 870 of SCR 856 is connected through resistor 872 to the first indicator lamp strobe signal (LC1) line 874 so that it is triggered into conduction at the initiation of data character input signals to the indicator after the indicator has been addressed.

The triggering SCR 856 also functions to enable each of the 35 lamp switch circuits 800 in the indicator. It does so by placing a positive signal to the respective gate circuits 868, 868*a* in each of the lamp switch circuits 800, 800*a* through resistors 869, 869*a* when it goes into conduction. The positive signal from the triggering SCR 856 to the lamp SCR gate circuits does not throw these SCR's into conduction unless and until positive signals are simultaneously received on the cathodes of both diodes 876, 878, 876*a*, 878*a* in each lamp switch circuit 800, 800*a*.

As will be seen in the later description of the lamp encoder circuit 754 the strobe signals and data signals provided therefrom to the scoreboard indicator circuits 706 are normally at negative potential and rise to positive potential to signify character display data. Thus if the character display data requires that lamp 404 be lit as in the letter T shown in FIG. 4, the diodes 876, 878 will receive simultaneous positive signals from the LR1 and LC2 inputs. Junction 867 goes high and the triggering SCR 856 supplies positive current to the gate 880 of the lamp switch SCR 806 causing it to conduct and complete the circuit for the lamp 404. The letter T does not call for lamp 404*a* to be lit so that while an LC2 signal will be received at diode 876*a* in the LR2–LC2 lamp switch circuit 800*a*, negative voltage remains at diode 878*a* and no current is delivered to the SCR gate 880*a*.

Once a lamp switch SCR 808 is triggered into conduction it remains conducting to keep the lamp lit until a subsequent receipt of address data indicates the selection again of that particular indicator which causes reset SCR 810 to be cut off in the manner previously described and in turn the lamp switch SCR's, including SCR 808.

The indicator circuit 706 as shown herein is characterized by the novel reset circuit which enables the erasure of displayed data on the indicator merely by the addressing of the indicator. The circuit is also characterized by its use of semiconductor devices throughout with no vacuum tubes and/or relays required. Relatively low power lamp switch SCR's 808, 808*a* may be used, and only one relatively heavy current conducting SCR is needed as the reset switch 810. The unique reset circuit enables the switching of the high lamp current through the reset SCR with the low current conducting transistor 836. An economical indicator circuit is thus provided with novel reset means which is highly reliable and substantially maintenance free except for replacement of the indicator lamps.

ADDRESS-CHARACTER SIGNAL LOGIC—(FIGS. 10—19)

Address Data Storage

This section describes the basic address and character data handling circuits of the signal logic 702 between the data input 700 and the scoreboard 100. This discussion will be best understood with reference to FIGS. 10 through 18 arranged in the format indicated in FIG. 19.

All of the address and character display data from the data input 700 is received on the data bus terminals *db*1 through *db*7 (FIG. 12) at the character decoder interface 730. The various code producing devices in the Data Input 700 deliver signals to the terminals *db*1 through *db*7 such that a low or ground signal represents the presence of a data bit and a high represents its absence. The signal at the output of each of the Nor gates 1200*a* through *g* in the character decoder interface therefore represents the data bits 1 through 7 of the modified ASCII code shown in the chart of FIG. 9. The code is thus

presented to the alpha numeric decoder **732** in the form of high and low signals corresponding, respectively, to the 1's and 0's in the table of FIG. **9**.

Conductors **1202***a* through *g* provide a straight pass through of the data bit **1** through **7** signals and negators **1204***a* through *g* provide the inverse of the data bit **1** through **7** signals, each of which is connected to appropriate Nand gates **1206** (FIG. **12**) and **1100** (FIG. **11**) in the alpha-numeric decoder **732** corresponding to a particular alpha, numeric, punctuation, or special characters or a special instruction (Special Address or Carriage Return). The alpha decoder Nand gates **1206** shown in FIG. **12**, and the numeric decoder Nand gates **1100**, shown in FIG. **11**, are all essentially the same (thus only representative gates are shown), and all of the gates are connected to the character decoder interface **730** so that each will present an output pulse when the ASCII code for its particular character is received. As an example, the alpha character T is represented by the modified ASCII code (FIG. **9**) 0010101, and the corresponding high and low signals will be presented at the outputs of Nor gates **1200***a* through **1200***g* of the character decoder interface **730**. It will be noted that the T Nand gate **1206**–T receives the negated data bit **1** signal, the negated data bit **2** signal, the straight data bit **3** signal, the negated data bit **4** signal, straight through data bit **5** signal, the negated data bit **6** signal and the straight data bit **7** signal. Thus, it will respond to the character T data, and not to any other data. The special address (SA) Nand gate **1206**–SA, carriage return (CR) Nand gate **1206**–CR, and the numeric decoder Nand gates **1100**–**0** through **9** (FIG. **11**) operate in the same manner to provide single conductor outputs responsive to the respective 7-bit data character input.

As previously described every time it is desired to insert address data into the system to seek a desired indicator, the numerical data pertaining to the Y and X coordinates must be preceded by the special address character (SA). This may be performed by the operator punching the special address button on the numeric keyboard **302** at the console **300** which initiates the code 0101010 at the input to the alpha-numeric decoder **732**. Seven high inputs are presented to the SA Nand gate **1206**–SA to produce a low on the special address conductor **734**.

The SA signal readies the Y and X address storage circuits **738** (FIG. **10**) and **740** (FIG. **11**) for storage of the Y and X address data by presenting a low or ground pulse signal to Nor gate **1000** (FIG. **10**) in the address counter circuit **736**. The high at the output of Nor gate **100** is inverted by negator **1002**, and the resulting ground on the CLEAR conductors resets a 5-count address digit counter **1004** and the Y tens digit storage flip-flop **1006**. The Y tens storage device **1006** is a set-reset type flip-flop which performs a storage function by flipping to its Q state (high voltage at Q output) responsive to a ground pulse at its set S input and remains in that state until a ground pulse is applied to its reset R input.

The clear signal is Nor'd at gate **1008** and inverted at **1010**, so that a ground reset signal is also applied to the reset terminals of the four Y units digit storage flip-flops **1012***a* through **1012***d*. These flip-flops are each of the conventional triggered type which is reset to its $\overline{Q}$ state by a ground signal at its reset R terminal and set to its Q state by a ground signal at the set S terminal. Also the circuit may be flipped between its Q and $\overline{Q}$ states responsive to low signals at the trigger input T provided ground does not appear at the R or S inputs.

In addition the clear signal feeds to the X address storage circuit **740** (FIG. **11**) where it similarly resets the X tens and units flip-flops **1100***a* through **1100***f* through Nor gates **1102**, **1104**, **1106** and negators **1108**, **1110** and **1112**. Thus, pressing the SA button resets all of the X and Y storage flip-flops as well as the 5-count address digit counter **1004**.

In addition, the SA ground signal also sets the set-reset type flip-flop **1014** in the address counter circuit **736**, the set or Q output of which goes high responsive to the low SA signal at the set input. The high Q output of flip-flop **1014** is applied to Nand gate **1016** which also has three other inputs as follows: a normally high input on conductor **1018** at the output of negator **1017** which goes low at count 5 of the address digit counter **1004**; a high output from Nand gate **1020** which goes low when a numeral button is pushed as will be hereinafter described; and the SA signal on conductor **734** which is low until the special address button is released. To facilitate this explanation it will be assumed that the keyboard buttons actuate grounding switches directly connected to the data bus terminals *db*1—*db*7. The actual keyboard circuits will be described in detail later. Therefore, when the special address button is released all four inputs to the Nand gate **1016** go high and a ground output is applied to the counter **1004**.

The address digit counter **1004** actually counts the number of digits in the address data inserted into the Y and X storages and prepares the logic for receipt of character display data upon completion of the address data input. The counter **1004** is a conventional type made up of three set-reset type flip-flops (not shown) and provides a high signal successively on the output lines 1 through 5 responsive to the first five successive low pulses at its input following its reset. Thus, the first low at the address digit counter input caused by the cessation of the SA signal provides a high pulse to Nand gate **1021** connected to the count 1 output of the counter, and it remains there until the operator punches the first numerical key at keyboard **302** representing the tens digit of the Y address to be stored.

As an example, assume that the desired address is Y09—X25. After punching the SA button the numeral button "0" is pressed to produce seven high inputs to the zero Nand gate **1100**–**0**. The low output on the zero line **1023** from the gate **1100**–**0** is applied to one of the inputs of Nor gate **1022** which acts as a numerical input detector. It is connected to the outputs of each of the numeric Nand gates **1100**–**0** through **1100**–**9** to produce a high signal at its output responsive to the input of any number. The high output from the numeral detector Nor gate **1022** is Nanded with the count 1 signal of the counter **1004** at gate **1021** to cause a set Y tens storage signal through negator **1024** to Nand gate **1026**. The other input to Nand gate **1026** is through conductor **1028***a* which is connected (not shown) to the output of Nor gate **1200***a* in the character decoder interface. The conductors **1028***a* through **1028***d* carry signals according to the first four bits of the ASCII code with the respective binary weights 1, 2, 4 and 8. These conductors thus provide the address data input to the storage circuits 738 and 740 as will be further shown. Therefore, if the Y address is any one of the numbers 10 to 15 a coincidence will appear at the output of Nand gate **1026** and provide a ground signal to the set terminal of the Y tens storage flip-flop **1006**. The Y tens flip-flop would flip to its Q state placing a high voltage on the YA**10** line **1025** to the Y**10** readout Nand gate **1027***a* signifying tens digit in the Y address. Since the Y address in our example was 09 no pulse appears on **1028***a* and the Y tens storage flip-flop **1006** is not set.

When the operator released the zero keyboard button at the console the input to Nand gate **1020** from the numeral detector Nor gate **1022** goes low to provide a high to the counter input Nand gate **1016**. Since the special address conductor is high, the set output of the special address flip-flop **1014** is still high, and the count 5 conductor **1018** is high, the gate **1016** is satisfied and produces a ground signal to the counter **1004**. The counter then advances to its count **2** state to send an enabling signal to Nand gate **1030** in readiment for storage of the Y units digit.

The operator next presses the keyboard button **9** and the alpha-numeric decoder **732** sends a low signal which is Nor'd in gate **1022** causing gate **1020** to inhibit the counter input gate **1016**. The high output of gate **1022** is Nanded at gate **1030** with the count 2 output signal of counter **1004** and the low therefrom is inverted by negator **1032**. The high at the output of negator **1032** is applied to the Y unit bits Nand gates **1034***a* through *d* which have their other inputs connected to separate ones of the *b*1 through *b*4 data bit lines **1028***a* through *d*. Since the units digit of the Y address is the numeral

9, highs will appear on the *b*1 and *b*4 bit lines **1028***a* and **1028***d* to Nand gates **1034***a* and **1034***d* and the ground pulses therefrom will set the Y unit flip-flop **1012***a* (having binary weight 1) and flip-flop **1012***d* (having binary weight 8). The Q outputs of Y units storage flip-flops **1012***a* through **1012***d* are connected via conductors **1029***a* through **1029***d* to the binary weighted readout Nand gates **1027***b* through **1027***e*, respectively. For the number 9 in the example address Y09—X25 Nand gates **1027***b* and **1027***e* will have high inputs at one of their inputs. A readout signal will later appear at the second input as will be hereinafter described. It is to be noted that the bit 5 through bit 7 data channels are not used for storing the address number because, as may be seen in the code chart of FIG. **9**, they are not required to distinguish the numerals 0 through 9.

When the operator releases the **9** keyboard button, the counter input gate **1016** delivers a low to the counter **1004** to step it to its count **3** condition enabling the set X tens digit Nand gate **1036**. The operator presses the keyboard button for the number two representing the tens digit of the X address **25** causing numeral detector Nor gate **1022** to open the set X tens digit Nand gate **1036**. The high from negator **1038** is presented to the Nand gates **1114***a*, **1114***b* at the set inputs to the X tens digit storage flip-flops **1100***e*, **1100***f* in the X storage circuit **740** (FIG. **11**). Since the number **2** has been pressed a high appears on the conductor **1028***b* (FIG. **10**) to the Nand gate **1114***b* thus setting the **X20** storage flip-flop **1100***f*. A high signal is thus delivered to one input of the **X20** readout Nand gate **1115***a* over conductor **1117**. If the X address had been a number 10 through 19 the bit **1** conductor **1028***a* would have carried a high to satisfy the Nand gate **1114***a* and set the **X10** flip-flop **1100***e*. Likewise, if the X address had been between 1 and 9 neither the **X10** nor the **X20** flip-flops would have been set.

Release of the keyboard numeral **2** button by the operator advances the counter **1004** to its step count **4** condition to prepare for storage of the X address units digit in the X units digit flip-flops **1100***a* through **1100***d*. Depression by the operator of the digit 5 for the units digit of the example X address **25** produces high outputs on the binary weight 1 line **1028***a* and the binary weight 4 line **1028***c*. These are each Nanded with the set X unit signal at Nand gates **1116***a* and **1116***c* to set the X1 and X4 flip-flops **1100***a*, **1100***c* and send high signals to the first inputs of X units read out Nand gates **1115***c* and **1115***e* via lines **1119** and **1121**.

Release of the numeral **5** keyboard button steps the counter **1004** to its count **5** condition which closes the counter input gate **1016** by placing a ground on the conductor **1018**. The address digit counter is thus inhibited from further pulsing until it receives a subsequent reset signal. The count **5** output of the counter also causes the SA flip-flop **1014** to be reset by means of Nor gate **1042** and negator **1044**.

The count **5** output of the counter **1004** also produces the addressed stored signal (AS) at the output of negator **1048** which is fed by the negator **1017**. The addressed stored (AS) signal is transmitted via conductor **742** to the lamp strober **750** (FIG. **12**) indicating that the full address has been stored. The signal logic is thus set to receive the character display data for actuating the desired lamps in the addressed indicator.

Although the explanation of the address storage circuits contemplated the manual input of data by the operator, the circuits operate in precisely the same manner when the input is from the memory input device **710**, the tape reader **709**, or the automatic address encoder **712** since all of these devices feed data to the character decoder interface in the same serial sequence beginning with the special address character data followed in order by the Y tens digit, the Y units digit, the X tens digit and the Y units digit.

Display Character Lamp Encoding

To display the desired character after addressing the proper indicator, the operator presses one of the alpha or numeric buttons on the respective keyboards **302**, **304** which causes the proper signals to appear at the data bit **1** through data bit **7** terminals at the character decoder interface **730**. The alpha-numeric decoder **732** produces a single line output from the proper Nand gate in the series **1206** or **1100** in the manner previously described, and the single line output signal is presented to the lamp encoder **754** shown in detail in FIG. **13**.

The lamp encoder **754** comprises a matrix of 35 Nand gates **1300***a* through *g*, **1301***a* through *g*, **1302***a* through *g*, **1303***a* through *g*, and **1304***a* through *g*. The matrix corresponds to the 5×7 matrix of lamps **400** in the indicators **102** so that each Nand gate is associated with a particular lamp position in the indicator matrix. The Nand gates in the column marked **1300** correspond to the lamps in column LC–1 of the indicator and similarly the column **1301** corresponds to the column LC–2 etc. Likewise, the Nand gates in the a row correspond to the lamps in lamp row LR–1 of the indicator matrix, those in row *b* correspond to lamp row LR–2, etc.

To describe the detailed operation of the lamp encoder **754** it will be assumed that the alpha character T is desired to be displayed on the previously addressed indicator Y09—X25. The code table of FIG. **9** shows that the code for the letter T is 0010101 and tracing the circuits in the decoder **732** (FIG. **12**) will show that this code will open the gate **1206** T to produce a low signal on conductor **1208**.

The signal on the "T" conductor **1208** is applied through appropriate Nor gates **1306** to Nand gate **1300***a* in the first column of gates, to Nand gate **1301***a* in the second column, to gates **1302***a* through *g* in the third column, to gate **1303***a* in the fourth column, and to gate **1304***a* in the fifth column which as may be seen by the shading of these Nand gates forms a letter T. The high signals at the first inputs to the selected Nand gates remain as long as the data signal from the data input lasts. During this time the address data is strobed out of the address data storages followed by the strobing of the display data from the encoder Nand gates, one column at a time in a manner described in the next section of this specification.

In a similar manner any other of the display characters may be encoded by the lamp encoder **754**. For example, if the letter "E" is selected, the signal from the output of the E Nand gate **1206**–E in the alpha numeric decoder **732** is delivered to the appropriate Nand gates **1300***a* through *g* in the first column, gates **1301***a*, *d* and *g* in the second column, gates **1302***a*, *d* and *g* in the third column, gates **1303***a*, *d* and *g* in the fourth column and gates **1304***a* and *g* in the fifth column.

The number of input Nor gates **1306** to the lamp encoder Nand gates may be materially reduced by combining inputs to various gates which are common to a number of different display characters. For example, each of the letters E, F, D, K, M, N, P, R and W as well as the all-lamps-lit character and a number of the other special characters shown in **5***a* call for all of the lamps in the first column LC–1 to be lit. Thus, the output lines from the decoder Nand gate, for all of these characters are Nor'd at gate **1308** to produce a single line for signalling the first column of Nand gate **1300***a* through *g* for all of these display characters. Likewise, the characters **2**, **3**, **5**, **6**, **8**, **9** and $ as well as the alpha characters B and E all have common thereto the LR1, LR4 and LR7 lamps in column LC2, LC3 and LC4. Nor gate **1310** provides for these common displays. Other lamp groups may also be so combined to limit the number of input Nor gates **1306** which may be calculated from an analysis of the display characters.

If display character data has been encoded by the circuit **754** in the manner set forth a signal is generated to start the readout of the address and character display data to the scoreboard. If one of the display characters is encoded a legit signal is sent to the lamp strober **750** which controls the readout of the address and display character data. The legit

signal is derived from the inputs of certain Nand gates making up the matrix in the lamp encoder **754**. Nand gate **1300***b*, which corresponds to the second lamp from the top in the first column of lamps (LD1—LR2), is actuated whenever any of the alpha-numeric characters is selected except I, J, T, Z, -, ', ., !, 1, 3, 7 and various special characters shown in FIG. 5*a*. Thus, a high signal on conductor **1309** from the input to Nand gate **1300***b* will indicate a legitimate character display when any but the above listed characters are encoded by the lamp encoder Nand gate matrix. It may be seen that the characters I, J, T, Z, ', 1, !, 3 and 7 all have either the top lamp (LR1) or bottom lamp (LR7) in the third column (LC3) of lamps lit and therefore conductors **1311** and **1313** connected respectively to the inputs of Nand gates **1302***a* and **1302***g*, will carry signals indicating the legitimate display of any of those characters. The inverted signals from the lines are joined with the inverted signal from conductor **1309** at junction **1320** and are Nor'd with signals generated by the selection of the remaining characters (1, -, space) not having a previously discussed legitimate signal, at Nor gate **1315**.

The high-going legit signal at the output of Nor gate **1315** is applied to the lamp strober enabling gate **1218** via conductor **756**.

Address and Display Character Readout

The lamp strober circuit **750** (FIG. **12**) performs the function of a master timer for controlling the readout of the address data to the scoreboard as well as the readout and display of the character data. It comprises a 15 count counter made up of four conventional triggered flip-flops **1212***a* through *d* pulsed by a master oscillator **1214** which constantly produces 25 microsecond pulses at its output to Nand gate **1216**. The other input to gate **1216** is connected to the normally high count 10 output of the counter so that the trigger input to the first flip-flop **1212***a* receives clock pulses from multivibrator **1214** only until count **10** is reached.

The lamp strober counter is inhibited from counting, however, until the storage of the address data and the encoding of the display character data because of the inhibit gate **1218**. The normally high output of gate **1218** is inverted by Nor gate **1219** presenting ground reset and inhibit voltage to the reset terminals of the counter flip-flops. The ground voltage also serves to reset the readout Y address (ROYA) flip-flop **1221** through the double inversion of Nor gate **1217** and negator **1215**.

The lamp strober inhibiting Nand gate **1218** is satisfied by the completion of storage of the address as indicated by the address stored AS signal on conductor **742**, and the encoding of a legitimate display character in the lamp encoder as indicated by the legit signal on conductor **756**. The erase reset input from line **1220** to gate **1218** is normally positive and remains so except for an occurrence during the message board erase function as will be hereinafter described. The jam conductor input is also high as long as the last indicator **X28** in a particular row has not been previously addressed as will be discussed in detail later.

Thus, upon the receipt of the legit signal the gate **1218** releases the inhibit from the counter flip-flop reset terminals and the trigger input to the first flip-flop **1212***a* is pulsed by the multivibrator clock **1214** through the Nand gate **1216** to start the timing function.

Count **1** of the lamp strober timer is utilized to initiate the readout of the Y and X address data from the respective storage circuits to the scoreboard. Count **1** is initiated by the first 25 microsecond multivibrator pulse after the inhibit is released and appears as a 50 microsecond long ground pulse at the output of the count **1** Nand gate **1224***a* and as a high pulse at the output of negator **1226***a*. The ground pulse from gate **1224***a* is applied over conductor **1228** to the set input of the readout Y address (ROYA) flip-flop **1221** which puts a high at its Q output. The high output from the Q output of the ROYA flip-flop is applied over the ROYA conductor **1230** to the Y address output Nand gates **1027***a* through *e* where it is Nanded with the binary code address signals from the Y storage flip-flops **1012***a* through *d*, **1006** in accordance with the Y address of the desired indicator to read out the address data through amplifying negator circuits **1045***a* through *e* and over the cables to the scoreboards. The ROYA signal remains as long as the legit signal appears at the counter inhibit gate **1218** and when it terminates the ROYA flip-flop is reset through Nor gate **1219**, Nor gate **1217** and negator **1215** as previously discussed.

The 50 microsecond high going count **1** signal at the output of negator **1226***a* is the readout X address (ROXA) signal and provides a high over conductor **1232** to the X address readout Nand gates **1115***a* through *f* where it is Nanded with the X address storage data from the X address storage flip-flops **1100***a* through **1100***e* and read out through amplifying negator circuits **1117***a* through *f* and over the cable to the scoreboards.

Counter outputs **2** through **4** of the lamp strober counter are unused. At count **5** the strobe LC1 pulse for reading out the first column of display character data is derived at Nand gate **1224***b* which therefore appears as a 50 microsecond high pulse on line **1234***a* at the output of negator **1226***b*. At count **6** the strobe LC2 pulse for column 2 information is derived on line **1234***b*. Likewise the LC3, LC4 and LC5 pulses are derived, respectively, from the count 7, count 8 and count 9 outputs on the lines **1234***c* to **1234***e*. However, whereas the LC1 signal pulse is a 50 microsecond pulse, the LC2 through LC5 pulses are 25 microsecond pulses because of the connection via conductor **1236** from the output of the timer clock output Nand gate **1216** to the fifth inputs of the Nand gates **1224***c*—**1224***f*.

The LC1 through LC5 pulses are directed to respective columns of lamp encoder Nand gates **1300** through **1304**, as well as to the LC1 through LC5 output terminals **1314***a* through *e* to the cable leading to the scoreboard. Thus, each of the LC1 through 5 strobe pulses is Nanded with the appropriate display character data encoded signals appearing at the Nand gates in the lamp encoder matrix to provide LR1 through LR7 signals on the 7-lamp row output conductors **1316***a* through *g* and lamp row data terminals **1318***a* through *e* to the cable leading to the scoreboard. Thus, the strobe signals comprising the single pulses in sequential time relationship from LC1 through LC5 appear at terminals **1314***a* through *e*, and simultaneous with each LC pulse the data pulses corresponding to the required lamps to be lit for forming the desired display character sequentially appear at the lamp row 1 through 7 terminals **1318***a* through **1318***g*.

The address and character display data having all been readout to the scoreboard, the lamp strober counter advances to count **10** which develops a ground pulse over conductor **1238** to the clock timer output gate **1216**. Further clock pulses are inhibited from being transmitted to the lamp strober counter flip-flops and the counter stops. Reset of the counter occurs when the legit signal to inhibit gate **1218** disappears to place ground at the reset terminals of the flip-flops **1212***a*—*d* and **1221**.

The lamp strober **750** also causes the X address storage **740** to advance its stored number to the next succeeding address number thus causing the automatic addressing of the next succeeding scoreboard indicator **102** without the operator having to insert the address data. It will be seen that at count **8** of the lamp strobe counter, a ground signal appears on the advance X address (AXA) conductor **1240** from the output of count **8** Nand gate **1224***e*. The signal is inverted at Nor gate **1118** to present a high input to Nand gate **1120**. The jam signal at the other input to Nand gate **1120** is also high except when X29 designating the end of a row is addressed, so the output of the gate **1120** goes low to provide a trigger pulse to the X1 flip-flop **1100***a* in the X address storage circuit **740**. The trigger pulse advances the count registered therein by one digit in a well-known manner to raise the address one number. The Y address storage circuit **738** maintains the Y address data previously stored so that data is now stored in the address

storage circuits indicative of the next succeeding indicator in the desired row.

When the last indicator in a row has been addressed and the character display data pertaining thereto has been transmitted, it is desirable to stop the automatic advancing of the X address until the next row of indicators is addressed. A jam signal is therefore generated which prevents further data input until a carriage return signal is received by the logic which automatically causes the storage circuit **738** and **740** to register the address of the first indicator in the next row.

The X address designating the end of the row (No. 29, or one more than the number of indicators) is detected by Nand gate **1122** which is fed by the Q outputs of the X20, X8 and X1 flip-flops of the X address storage. When all three are high indicating the X address number 29 the gate **1122** opens to provide a high signal on the X29 conductor **1131** through negator **1124** to the jam Nand gate **1132**. Conductor **1158** at the second input of Nand gate **1132** from the erase function circuits to be hereinafter discussed, is normally high, as in conductor **1234** to the third input from the $\overline{Q}$ output of the ROYA flip-flop **1221**. This $\overline{ROYA}$ signal prevents jamming until after readout to the scoreboard of the data pertaining to the 28th indicator in the row.

As previously discussed the output of the jamming Nand gate **1132** forms an input to the lamp strober inhibit gate **1218** over conductor **1222**. When the jam signal goes low indicating the end of the row, the gate **1218** is closed placing a low signal on the reset terminals of the lamp strober counter flip-flops preventing any further strobe cycling until the signal on the jam line **1222** again goes high.

The low jam signal from the jam Nand gate **1132** is also sent to Nand gate **1120** closing that gate to prevent any further advancing of the X address in the X address storage.

The signal logic stays in the jammed condition until a carriage return (CR) signal is received. The ASCII code for the carriage return arriving at the character decoder interface **730** is detected by the carriage return alpha decoder Nand gate **1206**CR sending a low signal on conductor **1242** and inverted to a high by negator **1126** connected to the input of a Nand gate **1128** in the X address storage. The carriage return signal CR is received via conductor **1127** by the Nand gate **1128**.

The other input to the gate **1128** is the address stored (AS) signal on conductor **742** derived from the count 5 output of the 5-count counter **1004** in the address counter circuit **736**. It will be recalled that the counter **1004** remains in the count 5 condition until reset. The ASCR signal from the output of gate **1128** triggers the Y address storage to advance to the next number via conductor **1132**, junction **1134**, conductor **1136**, Nor gate **1052** and negator **1054** to the trigger input of the Y1 flip-flop **1012***a* of the Y address storage circuit. The ASCR signal appearing at junction **1134** also resets the X address storage to the number 1 to indicate the first indicator in the next row by causing low signals to the reset terminals of the binary weighted 2, 4 and 8 flip-flops **1100***b*, *c* and *d*, as well as X10, X20 flip-flops **1100***e* and *f*, through the Nor gates **1104**, **1106** and negators **1110**, **1112**, respectively. The binary weighted 1 flip-flop **1100***a* is set to its 1 condition by the ASCR signal through Nor gate **1138** and negator **1140** whose output is connected to the set terminal of the flip-flop **1100***a*.

The shift of the X address storage from the X29 address to the X1 address causes the X29 detector Nand gate **1122** to close, removing the high from the first input of the jam Nand gate **1132**, and hence restoring the high on the jam signal line **1222** to the lamp strober inhibit gate **1218**.

It is desirable to jam the further readin of data after the last row Y10 of the message board has been actuated to prevent message information from interfering with the ballgame information in the upper portion **104** of the scoreboard (rows 11 through 15). If the Y address stored in the Y address storage circuit is 10 or higher, ground appears on the YA$\overline{10}$ conductor **1130** due to the set condition of the YA10 storage flip-flop **1006** in the Y address storage circuit **738**. Thus, the carriage return CR signal does not reach the ASCR gate **1128** if the Y address is ten or greater preventing the advance of the Y address, and the jam signal continues until the logic is subsequently reset.

Master Reset

It is desirable that the X and Y address storage, the counter and the SA flip-flops be reset to zero when the equipment power is first turned on. This is effected by capacitor **1071** and resistor **1073** connected to the input of negator **1075**. The negator **1075**, being the type that ordinarily has a momentary high input when power is on, has a ground signal at its input when the power is initially turned on due to the action of capacitor **1071**. Thus, a momentary ground appears at the output of negator **1077** (needed for loading purposes) and feeds through Nor gate **1000** and negator **1002** to reset the address counter **1004** and the Y and X address storage flip-flops in the same manner as the SA signal, as previously described. The output of negator **1077** is also directed to Nor gate **1042** which through negator **1044** provides a ground reset pulse to the SA flip-flop **1014**. A switch **1079** between the input of negator **1075** and ground is also provided for resetting the address storage address counter and SA flip-flops without having to previously turn off the power or generate an SA character signal. The reset switch thus enables reset of the address storage circuits when necessary for service procedures.

DATA INPUT

Keyboard Generation of Address and Character Data (FIG. 18)

The keyboards **302**, **304** are shown schematically in FIG. **18** to show how the ASCII code signals are generated and transmitted to the data bus terminals db1—db7 in FIG. **12**. Depressing any one of the keys **1801** at the keyboards provides ground to the inputs of one or more of the negators **1800***a* through *g* with resulting enabling high voltages at the first input of the respective data Nand gates **1802***a* through **1802***g*. The input signals to these Nand gates correspond to the 1's and 0's representing the particular ASCII code notation shown in the chart of FIG. **9** for the selected character to be read into the signal logic.

Depressing any one of the keys **1801** also places ground on conductor **1806** leading to the set input of flip-flop **1808**. The flip-flop has its Q output connected through an inverting Nand gate **1810** to its reset input so that it acts as a one shot multivibrator in a well-known manner. Thus the $\overline{Q}$ output produces a low going pulse having a duration of about 1.4 millisecond. This pulse is inverted at negator **1812** and Nanded at gate **1814** with a high from the output of Nor gate **1816**. The input of gate **1816** is in receipt of ground voltage through the S.K.I. switch contacts (Scoreboard Keyboard Input) **1411***a*. This switch is actuated whenever it is desired to reach the scoreboard directly from the console keyboards and buttons at the console **300**.

The gate **1814** serves as a strobe gate providing a high synchronizing pulse signal to the second input of the previously enabled ones of data gates **1802***a* through *g*. Thus simultaneous low signals appear at the output of the data gates which are transmitted to the db1—db7 terminals (FIG. **12**) via the 7-conductor board data bus **715**.

It will be recalled that the explanation of the signal logic assumed the direct connection of the keyboard keys to the data bus terminals to facilitate that explanation. The present description indicates that the console keys produce synchronized pulses instead which, although not absolutely necessary, do a better job of controlling the signal logic and eliminating the effects of any contact bounce at the keyboard.

Single Button Addressing

The previous sections described the operation of the signal logic assuming that all of the address data and the character display data is generated by the operator manipulation of the

keyboards 302, 304 in the console 300 which is the input mode most frequently used in the message section 106 of the scoreboard. For game in progress information to be displayed in the section 104 of the scoreboard, the data indicators associated with the fixed captions such as BALL, STRIKE, OUT, LINE SCORE, etc. may be automatically selected by the button on the console 300 having the caption name associated therewith as previously described. The words "batter" or "play" may also be generated and displayed by pressing the appropriate button. These functions are performed by the address encoder 712, shown in detail in FIG. 14, as well as the word generator 714 and address and word control 716, shown in detail in FIG. 15.

As an example of the operation of single button addressing, assume it is desired to address the indicator which displays the total errors of the home team as the game progresses. The indicator address where this information is to be displayed is Y15–X26 as indicated on the scoreboard of FIG. 1. Depressing home button 328 and error button 336 produces ground signals on the Y15 and X26 input conductors, respectively, to the appropriate gates of the series of input Nor gates 1400*a* through 1400*k*. Thus the three ground Y15 inputs to the respective Nor gates 1400*a*, 1400*b* and 1400*d* provide set pulses through the respective ones of inverters 1402*a*–*k* to the appropriately weighted Y address encoder flip-flops 1404*a* through *e* to store the number 15 in binary coded decimal notation. The X26 grounded inputs cause setting pulses through the respective Nor gates and negators to the appropriately weighted X address encoder flip-flops 1404*f* through *k* to store the X address number 26 in binary coded decimal notation. Thus, to register the address Y15–X26 flip-flops 1404*a*, *b*, *d*, *f*, *i* and *j* will be set to provide high inputs to the address storage Nand gates 1406*a*, 1406*b*, 1406*d*, 1406*f*, 1406*i* and 1406*j*.

The stored address is then converted to ASCII code as it is serially read out from the storage Nand gates 1406 one digit at a time for presentation to the data bit terminals in the character encoder interface 730. To read the address data out of the address storage Nand gates 1406*a*—*k*, properly sequenced pulses are received at the first inputs to the gates 1406. The pulses are preceded by a readout special address signal (ROSA) followed by the four digit readout pulses—readout Y tens address (ROYTA), readout Y units address (ROYUA), readout X tens address (ROXTA), readout X units address (ROXUA). This will be recognized as the same order that the operator keys in the Y and X address data as explained in the previous section.

The readout signals are generated in the address and word control circuit 714, shown in FIG. 15, responsive to the storage of the one button address data. It will be noted that the outputs of the negators 1402*a* through 1402*k* leading to the set terminals of the X and Y storage flip-flops 1404*a* through *k* each connect to one of the lines indicated ST1 through ST11 which lead to the Nor gates 1500*a*, 1500*b* (FIG. 15) in the address and word control 716. Nor gate 1500*a* is associated with the X storage flip-flops 1404*a*—*e* and Nor gate 1500*b* is associated with Y storage flip-flops 1404*f*—*k*, so that if both X and Y data is presented the coincident highs at the output of the Nor gates 1500*a* and 1500*b* are sent over conductor 1502 to the input of Nand gate 1504. The other input to Nand gate 1504 is always high except for a message update function which will not be described herein and does not form a part of the present invention. The low output from Nand gate 1504 sets the address control set-reset type flip-flop 1506 to its high Q output state. This high prepares the address and word control timer enabling gate 1508 at its third input. The second input to Nand gate 1508 is already high by means of the message update flip-flop 1510 which remains in its high $\overline{Q}$ output state during the operation of the system in the manner herein described. The fourth input to gate 1508 is also high because of the low count 15 output of the address and word control counter 1512 which had been previously reset to its zero state at the end of its last cycle of operation as will become apparent hereinafter. The gate 1508 is thus enabled to pass 0.91 millisecond pulses from the multivibrator timing clock 1514 to the trigger input of the 15-count counter 1512. The counter 1512 begins to count producing a 1.82 millisecond pulse at its first output on conductor 1516 to the count 1 Nand gate 1518. There it is Nanded with a 0.91 millisecond pulse from gate 1508 to produce a 0.91 millisecond ground on the ROSA (Read Out Special Address) conductor. The ROSA signal generated by the clock count 1 is delivered to the ASCII code bit encoder formed by the Nor gates 1408*a* through *f* and Nand gates 1410*a* through *g* in the address encoder 712 (FIG. 14). Specifically the ground ROSA pulse is fed to Nor gates 1408*b*, 1408*d* and 1408*f* with the high outputs therefrom being delivered to the Nand gates 1410*b*, 1410*d* and 1410*f*. The data inputs to the gates 1410*a* through 1410*g* are nanded with a high signal from the direct to scoreboard (SKI) switch contacts 1411*b* which is actuated by the operator if the encoded information is to go directly to the scoreboard for display. The resulting low outputs from the Nand gates 1410*b*, *d* and *f* along with the normally existing high outputs of gates 1410*a*, *c*, *e* and *g* represent the inverted ASCII code for the special address character presented to the character decoder interface 730 as previously explained.

Returning to the readout signals from the address and word control, the count 2 signal from Nand gate 1518*a* establishes the readout Y tens address on conductor ROYTA through Nor gate 1519*a* which leads to the Nand gate 1406*a* (FIG. 14) at the output of the Y tens flip-flop 1404*a*. Since our example address (15–26) caused the y10 flip-flop 1404*a* to be set, the Nand gate 1406*a* is satisfied and its output is transmitted through the first encoder Nor gate 1408*a* to the first encoder Nand gate 1410*a*.

It will be noted from the ASCII code table in FIG. 9 that for the numeric character 1 as well as all other numeric characters the data bits 5 and 6 must also be present which indicate that Nand gates 1410*e* and 1410*f* must be satisfied whenever address data is being generated. Therefore, simplified circuitry is utilized to provide high signals to these gates for each of the four readout address signals which appear at counts 2 through 5 from the address and word control counter 1512. Each of the count signals 2 through 5 from the address and word control 1512. Each of the count signals 2 through 5 from the counter circuit are fed to a Nor gate 1520 (FIG. 15), the output of which is termed the readout five and six bits (RO5+6). The RO5+6 signal is fed to the address encoder circuit 712, inverted by negator 1416 and fed to encoder Nor gates 1408*e* and *f*. These gates produce the high signals to the 5 and 6 bit Nand gates 1410*e*, 1410*f* as required for each of the numeric character ASCII code notations. The ASCII code 1000110 for the numeral 1 representing the Y tens digit therefore appears at the input to Nand gates during count 2 from the Address and Word Control and consequently read out to the Y address storage 738 in the signal logic.

The count 3, count 4 and count 5 signals from the address and rod control counter 1512 actuate respectively the readout Y units address (ROYUA), readout X tens address (ROXTA) and readout X units address (ROXUA), the numeric data for each digit being encoded by the Nor gates 1408*a* through *f* and Nand gates 1410*a* through *g* and sent to the respective storage circuits in the signal logic. The circuits may be readily traced out to show how the ASCII code bits are generated for each of the remaining digits of the example address 15—26.

The home team errors indicator Y15—X26 having been single button addressed with the information stored in the Y and X storage circuits 738 and 740, the signal logic only awaits the operator's input of the desired character display data indicating the number of errors. When the operator presses the proper number button at the console 300, the character is encoded in the lamp encoder 754, and if it is a legitimate signal, the lamp strober 750 is caused to readout the address and character display data over the cables to the scoreboard.

It may be seen that only the first five counts of the 15-count address and word control 1512 are utilized for single button

addressing. The counter continues to cycle through the rest of its counts, however, until count 15 is reached which places a high on conductor 1524. The high is inverted by negator 1526 to close the gate 1508 between the multivibrator clock 1514 and the trigger input to the counter 1512. The flip-flop 1506 is reset to its $\overline{Q}$ state, and the counter 1512 is reset to its zero condition when the operator releases the one button address button at the console. Release of the button removes all of the ST signals from the inputs to Nor gates 1500*a* and 1500*b* which in turn removes the high from the second input of Nand gate 1504. The resulting high is applied to the input of Nand gate 1528 which had previously received a high at its other input when the counter reaches count 15 from the output of negator 1526, conductor 1530 and Nor gate 1532. The low signal from gate 1528 applied to the reset terminal of flip-flop 1506 resets it to this high $\overline{Q}$ condition for its next operation. The high $\overline{Q}$ signal from flip-flop 1506 is inverted at negator 1531, the low signal resetting counter 1512 to its zero state. The high $\overline{Q}$ signal from flip-flop 1506 is also Nanded at 1533 with the normally high signal from the update flip-flop 1510 and the resulting low provides a Clear Storage B signal on conductor 1535 to reset the Address Encoder flip-flops 1404*a*—1404*k*.

Word Generation

As previously described, during the progress of a baseball game it is desirable to display the word play in the group of indicators marked 108 on the scoreboard 100 (FIG. 1) and on the first four indicators of the group marked 206 of the auxiliary board shown in FIG. 2. Since these indicators are used for the display of other information also, means are provided in the control system for automatically writing the word "PLAY" on these indicators. The first indicator in each of these groups has been given the address Y11—X20.

The scoreboard operator causes the word PLAY to be displayed on the two boards by depressing the PLAY button 348 in the fact feature portion of the console 300 (FIG. 3). The operation of the PLAY button first generates the address data for selecting the first indicator 11—20 in the display groups 108, 206. The address data is generated in the same manner as previously described for one button addressing. That is, ground signals appear on all of the Y11 and X20 input lines to the Nor gates 1400*a*, *b* and *f* to set the appropriate flip-flops 1404*a*, *b* and *f*. High inputs are thus provided to the Nand gates 1406*a*, *b* and *f* to await the readout signals from the address and word counter as previously described.

It will be recalled that the readout signals are initiated by the appearance of one or more signals on the ST1 through 5 conductors and one or more signals on the ST6 through 11 conductors which through the input circuitry previously described begins the operation of the address and word control counter 1512.

The counter 1512 being triggered produces the count 1 through count 5 pulses to readout the special address character and each of the digits forming the Y and X address to the signal logic 702 in the manner described in the previous section of the specification describing single button addressing.

The counter continues, count 6 and 7 not being used, and count 8 begins the readout of the character display data for displaying the word PLAY. Count 8 from the output of Nand gate 1534*a* and negator 1536*a* is applied to the P Nand gate 1534*a* and negator 1536*a* is applied to the P Nand gate 1538. The other input to the P gate 1538, as well as the second inputs to the L gate 1540, A gate 1542 and Y gate 1544 are previously set to a high from the PLAY generator flip-flop 1546 which has its set input connected directly to the PLAY button 348 on the console.

A low signal, therefore, appears on the P conductor LP responsive to count 8 which is transmitted to the encoder circuit in FIG. 14 where the encoder Nor gates 1408*a* through *f* and Nand gates 1410*a* through *g* convert it to ASCII type 7-bit code signals. It will be noted that the LP line is connected to the Nor gate 1408*e* which feeds a high to the first input of Nand gate 1410*e*. Also the LP line is connected to Nor gate 1418 which places a high at the second input to Nand gate 1410*g*. The high inputs to gates 1410*e* and 1410*g* which represent data bits 5 and 7, along with the low inputs to the Nand gates 1410*a* through 1410*d* and 1410*f* which represent data bits 1 through 4 and 6 are indicative of the ASCII code for the letter P as shown in the table of FIG. 9. The outputs of the gates 1410*a* through *g* are fed to the character decoder interface 730 and applied to the alpha-numeric decoder 732 which signals the lamp encoder and lamp strober to encode the letter P and read out the address and character display data to the scoreboard in the manner described previously. The address in the X address storage 740 is automatically advanced to the next indicator address in the row (Y11—X21) and the system is ready for the display of the next character L in the word "Play."

The letter L is generated at count 9 of the address and word control counter 1512 which causes a ground signal to be produced on the LL line to the inputs of the appropriate Nor gates 1408*a* through 1408*f*. Tracing of the circuits will show that the gates 1408*a* through *f* and 1410*a* through *g* will develop the proper signals for the ASCII code representation of the letter L to the signal logic circuits. The letter A is generated at count 10 of the address and word control counter 1512 and the last letter Y is generated at count 11 in a similar manner, counts 12 through 14 not being used for generation of the word PLAY.

After display of the letter Y in the word PLAY the X address storage is again automatically advanced to the next number. The address now stored is 11—24. It will be noted that the first indicator in the group 110 (FIG. 1) for the display of the particular play information has the address Y11—X24 so that the automatic address advance feature causes the first indicator in group 110 to be automatically addressed at the end of the read out of the word PLAY. Count 15 then resets the address counter 1506 which then causes the Clear Storage B signal to reset the PLAY flip-flop 1546 as well as the address encoder flip-flops 1404*a*—*k*.

The display of the word BATTER on the group of indicators 206 on the auxiliary board 200 is performed in substantially the same manner with the proper address being encoded in the address encoder circuit 712 and the word BATTER being generated in the word generator circuit 714. The selection of the button 306 on the console marked BATR causes the automatic encoding of the proper address for the first indicator in the group 206 on the auxiliary board during the first 5 counts of the address and word control counter 1512 and also sets the batter flip-flop 1548 to enable the word generating Nand gates 1550 through 1560. Counts 8 through 13 of the counter 1512 successively trigger each of the Nand gates 1550 through 1558 to cause the encoding of each of the letters in the word BATTER by the encoding gates 1408*a* through *f* and 1410*a* through *g*. On count 14 the space character is generated from Nand gate 1560. After the word and space character has been automatically generated and displayed onto the board, the first indicator (Y12—X21) for registering the batter data is automatically addressed. It will be noted in FIGS. 1 and 2 that the first indicator directly under the word BATTER on the main board 100 and the eighth indicator of the group 206 on the auxiliary board both have the same address so that both boards are addressed for display of the batter data after the word BATTER has been generated and displayed on the auxiliary board.

ERASE FUNCTION

As will be recalled the erase function is used to clear display data off of desired indicators. During the erase function the signal logic is caused to automatically generate sequential address signals pertaining to the particular section of the board it is desired to erase. As described in the detailed explanation of

the indicator circuits, addressing of an indicator automatically causes it to be extinguished in preparation for the receipt of character display data. Thus, an indicator need merely be addressed to erase previous data on display.

Assuming the operator wishes to erase one line of the message section **106** of the scoreboard, he selects the button from the group **360** on the console **300** for the line he desires. This button produces the address of the first indicator in the selected line, the one button address being produced by the address encoder **712** (FIG. **14**) in the manner previously described, and this address is stored in the Y and X address storage circuits **738, 740**.

The button also has a contact which feeds a ground to the set terminal of the erase 1 line flip-flop **1138** (FIG. **11**) in the signal logic. The $\overline{Q}$ output of flip-flop **1138** goes to ground which is inverted to a positive clear signal on conductor **1146** by Nor gate **1140**. The positive clear signal is transmitted to Nand gate **1142** provided the direct to scoreboard switch is closed putting positive potential through S.K.I. switch contacts **1411***c* to the cathode of diode **1143**. The S.K.I. (direct to scoreboard) switch contacts **1411***c* and diode **1143** are used to insure that the erasure function takes place only if the signal logic is connected directly to the scoreboard. The positive clear signal is Nanded with the address stored (AS) signal by Nand gate **1142**, the ground output therefrom on conductor **1144** being inverted by Nor gate **1219** to provide a positive enabling signal to the reset terminals of the lamp strober counter flip-flops **1212***a*—**1212***d*. The ground trigger pulses from the multivibrator clock **1214** and Nand gate **1216** actuate the lamp strober counter to begin its count. Count 1 occurs normally to read out the Y and X address to the boards which causes any lamps which were previously lit on the addressed indicator to be extinguished in the manner discussed earlier. Count 5 produces the strobe LC1 pulse.

No further strobing to the scoreboard indicators is required so that at count 6 of the counter the following occurs: The negative count 6 pulse from the output of Nand gate **1224***c* on conductor **1244** is inverted to a positive pulse by negator **1246** and nanded at gate **1248** with the positive clear pulse on conductor **1146** leading from the output of the Nor gate **1140** (FIG. **11**). The ground at the output of Nand gate **1248** is applied to the set terminals of counter flip-flops **1212***a* and **1212***d* to set them to their high Q states. Since flip-flops **1212***b* and **1212***c* already are in their high Q states at count 6 the effect is to instantaneously change the count to **15** bypassing count stages **7** through **14**. Therefore, strobes LC2 through LC5 pulses are not produced and count **10** is also bypassed which otherwise would close the gate **1216** between the multivibrator clock **1214** and the trigger input to stop the count. The four high Q outputs of the lamp strober counter flip-flops **1212***a* through **1212***d* are nanded by gate **1250** to produce a ground signal to reset the readout Y address flip-flop **1221** and also to automatically advance the X address (EAXA) via conductor **1252** and Nor gate **1118** (FIG. **11**) to Nand gate **1120**. As long as the jam Nand gate **1132** has a high output indicating that the last indicator in the row has not been reached, gate **1120** sends a ground pulse to the trigger input of X address storage flip-flop **1100***a* to advance the X address stored number up one count, signifying the next indicator.

The next pulse from clock **1214** to the lamp strober counter then restarts it from count zero again counting through to count **6** and converting to count **15** to extinguish the next indicator and automatically address the following indicator. This occurs repeatedly until number **29** at the end of the row has been addressed, at which time Nand gate **1122** is satisfied to provide a high signal from the output negator **1124** to the input of the jam Nand gate **1132** via conductor **1131**. The low output from jam gate **1132** closes gate **1120** preventing the further advance of the X address storage.

The number **29** signal is also applied to Nand gate **1150** which also receives a high signal from the Q output of the erase 1 line flip-flop **1138**, and the resulting ground erase reset signal causes the reset of the erase 1 line flip-flop **1138** through Nor gate **1152** and negator **1154**. When the erase 1 line flip-flop **1138** resets, its $\overline{Q}$ output goes high producing a low to Nand gate **1142** and hence a high on conductor **1144** to Nor gate **1219** in the lamp strober. At the same time the low erase reset signal on conductor **1220** from Nand gate **1150** (FIG. **11**) insures that the lamp strober inhibit gate **1218** is closed to provide a high at the other input of Nor gate **1219**. The ground output signal therefrom thus resets the lamp strober flip-flops to zero and the signal logic is reset to receive succeeding data from its various inputs.

If the operator wishes to erase all 10 message lines of the message section **106** of the scoreboard, he selects the EMSG erase button **358** on the console **300**. This button automatically produces the address of the first indicator in line 1 of the scoreboard (YO1—XO1) which is automatically read in to the X and Y address storage circuits. Also the one button feeds a ground to the set terminal of the erase message flip-flop **1156**. The low going $\overline{Q}$ output thereof initiates the counter in the lamp strober **750** and erase of the first line occurs just as described for the erase of 1 line. However, at address YO1—X29, no jam signal is desired because the next row must be automatically addressed and erased. The jam Nand gate **1132** which controls Nand gate **1120** and the advance X address ground pulses to the X address storage is not actuated because of the low at the second input of gate **1132** on conductor **1158** connected to the $\overline{Q}$ output of the erase message flip-flop **1156**. That is, during the erase message function the second input of the jam Nand gate **1132** is maintained low to keep gate **1120** open for the passage of the erase advance X address (EAXA) pulses to the X address storage from the lamp strober counter through Nor gate **1118**.

The address in the Y address storage **738** is automatically advanced to the next row of indicators when the last indicator in the previous row has been erased by means of Nand gate **1053** which feeds the trigger input to the first Y address storage flip-flop **1012***a* through Nor gate **1052** and negator **1054**. The Nand gate **1053** is satisfied by the Erase message signal (EMSG) from the high Q output of the erase message flip-flop **1156**, and the X number **29** signal (X29) indicating the end of the row. The low pulse output from gate **1053** thereby causes the advance of the Y address in the Y address storage flip-flops. The output of Nand gate **1053** also provides inputs to gates **1102**, **1104**, and **1106** which are used to reset the X address flip-flops to count **0**.

The lamp strobe counter continues to cycle until the address Y10—X29 is reached. This condition is detected by Nand gate **1160** which has inputs connected to the Q output of the YA10 flip-flop **1006** (YA10), the X29 line, and the high Q output of the erase message flip-flop **1156** (EMSG). The concurrence of these signals produces a ground erase reset signal on the erase reset line **1220** to the lamp strober inhibit gate **1218** to stop and reset the lamp strobe counter. The erase reset signal also causes the reset of the erase message flip-flop **1156**, and the reset of the remaining signal logic circuits as hereinbefore described.

The erase game in progress button (EGIP) **352** is used to erase all of the indicators in the section **104** of the scoreboard as previously described. Depressing the EGIP button causes the automatic address encoding for the first indicator of the game in progress section **104**. The button also set another erase flip-flop (not shown) and causes the automatic addressing and hence erasing from that address on through the last indicator X15—Y28 on the board in essentially the same manner as described for the erasure of the message portion of the board.

The clear button **314** for erasing the batter number and the number of balls and strikes operates in essentially the same manner as any one of the erase 1 line buttons **360** previously described except for the fact that we do not want to erase the number of outs on indicator Y12—X12. Thus, we want to erase by the operator of button **314**, indicator Y12—X02, Y12—X09, Y12—X10, skipping indicator Y12—X12 and erasing indicators Y12—X21, Y12—X22. Depressing the

clear button 314 automatically addresses the first indicator in row Y12 and sets flip-flop 1157 to begin the automatic erasure of the indicator therein. It will be noted, however, that the high Q output of flip-flop 1157 is also delivered to gate 1253 (FIG. 12) in the lamp strober where it is Nanded with the Q outputs of the Y10 flip-flop 1006, Y2 flip-flop 1012*b*, X10 flip-flop 1100*e* and the X2 flip-flop 1100*b*. Also Nanded therewith are the $\overline{Q}$ outputs of X8 flip-flop 1100*d* and X4 flip-flop 1100*c*. It will be noted that the gate 1253 is satisfied by highs at all of its inputs when the address Y12—X12 appears in the X and Y storages to provide a low at conductor 1255 leading to the input of the count 1 Nand gate 1224*a*. This prevents readout of the X and Y addresses at that point to prevent the indicator Y12—X12 from being addressed and hence erased. The erase function continues, however, until the end of row 12 is completed at which time the jam signal occurs and the erase reset signal resets flip-flop 1157.

Any one indicator at any address location on the scoreboards may be erased by the operator merely by use of the console keyboards 302, 304. He may select the address of the desired indicator by depressing first and special address button, then the four numbers indicating the Y and X address and followed by operation of the space bar on the alpha character keyboard 304, the space bar providing a high at the input to Norgate 1315 and therefore a legit signal to initiate the lamp strobe causing all indicator lights to be extinguished. Succeeding indicators may then be extinguished merely by continuous releasing and depressing of the space bar which causes the automatic address advance and turn out of the indicator lamps.

SCOREBOARD ADDRESS DECODING AND CHARACTER DATA DISTRIBUTION

The previous discussion has shown how the address and character data signals are generated for transmission to the scoreboards. The five Y address signals YT1, YU1, YU2, YU4 and YU8 as well as the six X address signals XT1, XT2, XU1, XU2, XU4 and XU8 are all amplified by line drivers 1600*a* through *e* and 1602*a* through *f*, respectively (FIG. 16), after being transmitted over the respective cables to the scoreboard. The signals are again amplified by matrix drivers 1604*a* through *e* and 1606*a* through *f* which, besides amplifying the signals, also provide the real and the inverse of each of the signals. The real and inverse signals from the matrix drivers 1604*a* through *e* and 1606*a* through *f* form he inputs to the Y and X address decoder circuits 762 and 764 which are essentially diode matrices of the standard type. Since the X address decoder matrix is the same as the Y address decoder matrix except for the number of addresses that must be handled, only the Y matrix is shown in detail.

The diode matrix address decoder 762 converts the binary coded decimal address signals at its input into a single line signal on one of its 15 output conductors 1608–1 through 1608–15 to the respective rows of indicators. As is well known an output line 1608–1 through 1608–15, passes a positive signal when a high going signal is received on each of the real and inverse conductors 1607*a* through *j* connected thereto by the diodes 1610. As an example, suppose the indicator being addressed is in the row 15. High signals will appear on the real tens line 1607*b*, the real 4 line 167*f* and the real ones line 1607*j*, as well as on the 8 line 1607*c* and the 2 line 1607*g*. All other conductors will have low signals thereon. It will be noted that the row 15 output conductor 1608–15 has diodes connected therefrom to each of the lines 1607*b*, 1607*c*, 1607*f*, 1607*g* and 1607*j* so that the simultaneously received high signals will be passed therethrough to the output line 1608–15. No other output conductor 1608–1 through 1608–14 will pass a signal because one or more of the diodes connected to those lines would have their cathodes connected to low signal conductors and thus shunt any high going signals on the other conductors connected thereto.

Each of the outputs 1608–1 through 1608–15 is connected to all of the indicators in the row designated by that Y address. Likewise, the outputs from the X address matrix 764, which operates in the precise manner described for the Y matrix, are each connected to all of the indicators in the column of indicators designated by the respective X address. These Y and X address signals are those appearing at terminals 814 shown in the lamp indicator circuit diagram (FIG. 8). Their simultaneous receipt extinguish all previously lit lamps and reset the circuit for the immediately following character display data.

The character display data is transmitted from lamp encoder output terminals 1318*a* through *g*, 1314*a* through *e* over the cables 774 and 776 after being amplified by line driver amplifiers 1700*a* through *g* for the lamp row data signals and line driver amplifiers 1702*a* through *e* for the lamp column strobe signals. At the scoreboard the signals are again amplified by the character data lamp row drivers 1704*a* through *g* and the lamp column strobe signal line drivers 1706*a* through *e*. The seven lamp row drivers 1704*a* through *g* have their outputs connected to the seven rows of lamp switches 800 in every indicator circuit 706 on the scoreboards. Likewise the lamp column drivers 1706*a* through *e* have their outputs connected to the respective columns of lamp switches in every indicator circuit 706 on the scoreboard. The signals from the lamp row and lamp column drivers form the LR data signals and the LC strobe signals to the indicator circuits 706 shown in FIG. 8 and cause the display of the desired character on the indicator having the immediately preceding address transmitted from the signal logic to the scoreboard.

It is to be noted that while the cable between the console location and the remotely located display boards are shown in the present example to extend between the output of the signal logic 702 and the display boards 100, 200, there are some situations in which it would be more advantageous to provide the cables in front of the signal logic where the data is transmitted on substantially fewer conductors. If many remotely located boards are to be controlled from a central location, it may be more economical to have a signal logic section 702 at each display board and the console would include only the various data input devices. Such a system is being installed for the Expo 1967 Trade Fair in Montreal, Canada.

AUXILIARY INPUTS

Magnetic Tape

A magnetic tape may be programmed in the same manner as the punched tape to cause the display of messages on the board. It may also be used for rapidly displaying succeeding character displays to give animated cartoon effects, flashing messages and many others of an unlimited variety.

For example, the animated cheerleader of FIG. 6 may be displayed by programming each of the figures 600*a* through 600*e* in individual frames one after the other in properly timed sequence. The indicator address and character display data for the complete first figure 600*a* is programmed on the tape by using the proper codes for the individual indicator characters, spaces where indicators are blank and carriage returns for sequencing each row. A predetermined interval after the frame for figure 600*a*, data is programmed to cause the erasure of the figure in preparation for the display of figure 600*b*. A figure may be erased by addressing the necessary indicators followed by the data for a space (see table of FIG. 9). The next figure 600*b* is programmed for the second frame, again followed by blanking in preparation for the third figure 600*c*, for the complete cartoon.

If desired the whole display need not be erased for each frame, but rather only the desired indicators by individually addressing and actuating the desired indicators. Thus, if only the arms of the FIG. 600*a* are to move the appropriate indicators only are addressed and the remaining indicators will stay lit during the sequence.

The magnetic tape memory **710** (FIG. **18**) reads the address and character data from its output logic input terminals db1 through db7 via Nand gates **1820***a* through *g* and the board data bus **715**. The gates **1820***a*—*g* are enabled by means of the Tape Memory Post on Board (TMPOB) switch **1822** which momentarily sets flip-flop **1824**. The momentary low at its $\overline{Q}$ output causes flip-flop **1826** to be set with the high Q output enabling the gates **1820***a* through *g*. The low $\overline{Q}$ output is used to signal the tape memory to start running in the read out mode. The address and character data is thus fed to the signal logic **702** to display the message on the board.

When the desired message has been completed the tape memory reads out a special End of Tape Block (ETB) coded signal which is detected by Nand gate detector **1828**. The low output thereof triggers a single shot multivibrator **1830** which delivers a reset pulse to flip-flop **1826**.

Tape Typewriter and Reader

As previously mentioned data may be displayed on the boards by means other than the keyboards and buttons on the console **300**. A punch tape typewriter and reader **708** may be used to insert data in the same direct manner as the keyboards **302** and **304** on the console, or data may be inserted from a previously prepared punched tape having the necessary address and character display data coded thereon.

The address data for the first indicator to be used is coded in binary coded decimal form followed by the data for each of the desired display characters to make up the message. The carriage return (CR) signals are appropriately programmed at the end of each indicator row if the message is to extend onto the next row of indicators. When the complete message has been read from the tape onto the board the signal logic automatically resets itself to receive the data for the next message leaving the first message displayed until cleared for the next message.

The actual circuits of the tape typewriter and reader input to the signal logic are not shown in the schematic drawing of FIGS. **10** through **18** because they do not form a part of this invention. However, they would be similar to console keyboard circuit of FIG. **18** with the device providing the data and synchronizing signals.

What we claim is:

1. An information display system comprising a message board, a plurality of display devices arranged in groups at sequential address locations on said board, input means for inserting address data segments pertaining to any desired group of display devices and display data segments pertaining to desired patterns to be displayed on a group of display devices, means for storing an inserted address data segment means for preparing for subsequent actuation the group addressed in response to said stored address segment, means responsive to a first inserted display data segment following a stored address data segment for actuating the prepared group of display devices to display the desired pattern of said first display data segment, means operable responsive to said actuating means for automatically advancing the address data in said storing means to the next sequential address, and means responsive to the insertion of each subsequent display data segment not preceded by an inserted address data segment for causing said actuating means to actuate the advanced address group of display devices to display the pattern pertaining to the display data segment and for causing said address advancing means to advance the stored address data to successive sequential addresses.

2. The display system of claim **1** wherein said display device groups are arranged in substantially an X and Y coordinate system wherein said data input means comprises means for entering the address segments in separate X and Y coordinate numerical data in binary coded decimal character form, and wherein said address storage means comprises means for storing each digit of the X and Y coordinate address data separately.

3. The display system of claim **1** wherein said data input means comprises a typewriter type keyboard.

4. The display system of claim **1** wherein means are provided for jamming the automatic advance of said address data in said address storing means responsive to the address data in said address storing means corresponding to the last group of display devices.

5. The display system of claim **1** wherein said data input means comprises a data memory device capable of having said address and display data stored therein.

6. The display system of claim **1** wherein said address data input means comprises a manually operable key for selecting a certain desired group of display devices, and means operable responsive to said key for encoding and transmitting to said address storing means the address data pertaining to said desired indicator.

7. The display system of claim **1** wherein said data input means comprises a manually operable key, means operable responsive to said key for automatically encoding and transmitting to said address storing means address data pertaining to a particular desired group of display devices, and means also responsive to said key for generating and transmitting to said actuating means and said causing means predetermined successive display data segments for displaying characters making up a predetermined message.

8. The information display system of claim **1** wherein said display device groups comprise a matrix of lamps arranged in rows and columns and means interconnecting corresponding rows of each of said indicator lamps, wherein said display device actuating means comprises a lamp encoder having a matrix of gate elements arranged in rows and columns corresponding to said lamp rows and columns, means connecting corresponding rows of said gate elements to corresponding rows of said lamps, each of said gate elements actuatable to enable the corresponding lamp in the selected lamp block, means responsive to the input of display data for enabling certain gate elements in said matrix dependent on the particular data to be displayed, means responsive to the storage of the address data and the input of the display data for producing strobe signals to sequentially strobe each of said columns of gate elements to thereby actuate said certain enabled elements and to simultaneously strobe each of said columns of lamps for actuating certain lamps in the selected lamp block corresponding to the certain actuated elements in said lamp encoder, and means in each of said indicators for maintaining the lamps actuated therein until said lamp block is again addressed.

9. The information display system of claim **7** wherein said display data segment generating and transmitting means comprises a plurality of gates each of which corresponds to a character in the message to be displayed, means including a clock operable responsive to the operation of said key for sequentially opening each of said gates momentarily, and a data generator operable responsive to the opening of each gate to generate data pertaining to the respective message character.

10. A system for displaying an animated characterization comprising a display board made up of a plurality of display devices, a memory for storing multibit coded data in data frames pertaining to patterns for forming said animated characterization, means for reading said data frames from said memory in sequence including electric signal conductor means having a sufficient number of conductors to transmit said multibit coded data but substantially less than the number of display devices making up said display board, and means in receipt of the data signals on said conductor means for operating said display devices in accordance with said sequenced data frames.

11. An information display system comprising a message board, a plurality of display lamp groups blocks at address locations on said board, a logic control system, a storage memory input means for serially entering address data and display data into said logic control system corresponding to

desired lamp groups blocks and desired display characters, said memory having stored therein a plurality of serially time sequenced segments of address and display data for automatically displaying a series of display characters on said board to form an animated display sequence, and means in said logic control system operative responsive to the input of each data segment for selecting each addressed lamp groups block and actuating said addressed lamp groups block to display the desired display character.

12. A system for displaying an animated characterization made up of a sequence of visual display frames comprising a display board having display devices arranged in addressable locations, a memory for storing coded address and display data in data frames pertaining to a desired pattern for each of said visual display frames, means for reading the coded address and display data in said data frames from said memory in sequence, means responsive to the coded address data from said memory for preparing the addressed display devices and means responsive to the display data from said memory for actuating the addressed display devices to form the patterns of each frame.

13. In the system of claim 12 wherein said memory comprises a magnetic tape storage.

14. An information display system comprising a message board, a plurality of groups of display devices at sequential address locations on said board, means for inserting address data and display data to display desired characters at desired locations, means for storing the address and display data connected to said data inserting means, address data decoder means at said board and connected to said address storing means for selecting an addressed display device group, a display device group encoder actuatable by said data inserting means to actuate an addressed display device group to display the desired character, means operable responsive to the storage of the address data and the insertion of the display data for transmitting the address data stored in said address storage means to said address decoder and for transmitting the desired character display data to the addressed display device group, and means for maintaining each addressed display device group actuated until subsequently readdressed, said data inserting means comprising a memory capable of storing discreet segments of address and display data and continuously transmitting said discreet segments in serial mode to said address storage means and said display device group encoder, whereby said actuated display device groups form an animated display.

15. For use in an information display system having a plurality of display indicators at address locations, each display indicator comprising a plurality of lamps, an electric current power supply, an electronic lamp switch in series with each of said lamps and one terminal of said power supply, an electronic reset switch connected between the other terminal of said power supply and said series connected lamps and lamp switches, means adapted to receive address signals peculiar to said indicator, means operable responsive to said address signal receiving means for opening said reset switch to open the connection between said lamps and the other side of said power supply, means adapted to receive lamp signals peculiar to selected lamps in said indicator, means operable responsive to said lamp signal receiving means for actuating each lamp switch corresponding to a selected lamp.

16. The display indicator of claim 15 wherein said power supply is a direct current source.

17. The display indicator of claim 16 wherein said electronic lamp switches and said reset switch are SCR's.

18. The display indicator of claim 17 wherein said reset SCR opening means comprises a monostable multivibrator having a short duty cycle with respect to the address signals and a transistor operable responsive to said multivibrator for temporarily shunting said reset SCR.

19. The display indicator of claim 17 wherein said reset SCR reactuating means comprises a monostable multivibrator having a long duty cycle with respect to said address signals and a triggering SCR operable responsive to the simultaneous operation of said multivibrator and the receipt of a lamp signal to trigger said reset SCR into conduction.

20. The display indicator of claim 19 wherein said lamp SCR actuating means comprises a gate circuit operative responsive to the receipt of said selected lamp signals and the operation of said triggering SCR for triggering each lamp SCR in the selected indicator corresponding to a selected lamp.

21. An information display system comprising a message board, a plurality of display indicators at address locations on said board, each of said indicators comprising a matrix of lamps arranged in rows and columns, address and display data input means, means for storing the address data inserted by said input means, address data decoder means connected to said address storing means for producing address signals corresponding to a desired indicator, a lamp encoder having a matrix of elements arranged in rows and columns corresponding to said lamp rows and columns, means interconnecting the outputs of corresponding rows of said elements, means responsive to the input of display data for enabling certain elements in each row dependent on the particular data to be displayed, means for producing strobe signals to cause said address storing means to transmit the address data to said address decoder to produce said address signals and for subsequently producing column strobe signals to sequentially strobe each of said columns of elements to thereby actuate and produce row lamp signals at the outputs of said certain enabled elements; each display indicator further comprising an electric current power supply, an electronic lamp switch in series with each of said lamps and one terminal of said power supply, an electronic reset switch connected between the other terminal of said power supply and said series connected lamps and lamp switches, means in receipt of address signals corresponding to said indicator for opening said reset switch to open the connection between said lamps and the other side of said power supply, means operable responsive to the first strobe signal for reactuating said reset switch, means operable responsive to said address signal and the first column strobe signal for preparing each lamp switch in said indicator, and means responsive to the simultaneous receipt of column strobe lamp signals and row lamp signals for actuating corresponding lamp switches to energize the corresponding lamps in accordance with the display data to be displayed.

22. The display system of claim 21 wherein said indicators are arranged in substantially an X and Y coordinate system, wherein said data input mean comprises means for entering the indicator address in separate X and Y coordinate numerical data into binary coded decimal form, and wherein said address storage comprises means for storing each digit of the X and Y coordinate numerical data and means for encoding the address coordinate numerical data into binary coded decimal form, and wherein said address storage comprises means for storing each digit of the X and Y coordinate address data separately.

23. The display system of claim 22 wherein said address storage means comprises means responsive to said input means for recognizing a first input character indicating the immediately following data relates to an indicator address and a counter operative responsive to the input of said first character and a predetermined number of address significant digits for preparing said strobe signal producing means, and wherein said lamp encoder comprises means responsive to the receipt of legitimate display data for actuating said strobe signal producing means.

24. The display system of claim 23 wherein means are provided for automatically advancing the address data for one coordinate in said address storing means to the next highest number responsive to said strobe signal producing means.

25. The display system of claim 24 wherein means are provided for jamming the automatic advance of said address data in said address storing means responsive to the address data in said address storing means corresponding to the last indicator in said one coordinate.

26. The display system of claim 21 wherein said lamp switches and said reset switch are SCR's.

27. The display system of claim 26 wherein said reset SCR opening means comprises a monostable multivibrator having a short duty cycle with respect to the address signals and a transistor operable responsive to said multivibrator for temporarily shunting said reset SCR.

28. The display system of claim 26 wherein said reset SCR reactuating means comprises a monostable multivibrator having a long duty cycle with respect to said address signals and a triggering SCR operable responsive to the simultaneous operation of said multivibrator and the receipt of said first column strobe signal to trigger said reset SCR into conduction.

29. An information display system comprising a message board, a plurality of display indicators at address locations on said board, each of said indicators comprising a matrix of light devices arranged in rows and columns, means interconnecting corresponding rows of each of said indicator light devices, a logic control system, operator controlled means for inserting numerical address data and display data to display desired characters at desired locations on said board, said data inserting means having a multiline output for transmitting signals to said logic control system in binary coded decimal form, said logic control system comprising a separate gate for each number and character, address storage means for each significant digit of said address data, an address counter, means responsive to the input of a special character for triggering said address counter one count and for enabling said digit storage means, means responsive to the input of each significant digit of said address data for enabling the respective digit storing means to receive and store its respective digit, a light device encoder having a matrix of elements arranged in rows and columns corresponding to said light device rows and columns, means connecting corresponding rows of said elements to corresponding rows of said indicator light devices, each of said elements actuatable to enable the corresponding light device in an addressed indicator, each of said elements actuatable to enable certain elements in said matrix of elements dependent on the particular data to be displayed on the addressed indicator, a strobe counter operable responsive to a signal from said address counter indicating the receipt and storage of the address data and a signal from said encoder indicating the encoding of a legitimate character for producing strobe signals to cause said address data storage devices to simultaneously transmit the stored data to said address decoder and thereafter to sequentially strobe each of said columns of elements to thereby actuate said certain enabled elements and to simultaneously strobe each of said columns of indicator light devices for actuating certain light devices in the selected indicator corresponding to the certain actuated elements in said light device encoder.

30. The information display system of claim 29 wherein said light devices comprise electric lamps and wherein said indicator has a control circuit comprising a lamp switch for each lamp in said indicator, means responsive to the receipt of the address data corresponding to said indicator for preparing each of said switches in said indicator and for extinguishing any lamps in said indicator previously actuated, means responsive to the first strobe signal for enabling said indicator lamps, and means responsive to the concurrent receipt of said strobe signals and signals from said certain lamp and coder elements for actuating the lamp switches corresponding to the certain actuated elements in said lamp and coder.

31. In an information display system for displaying characters on a matrix of light devices arranged in rows and columns, a light device encoder comprising a matrix of gate elements arranged in rows and columns corresponding to said matrix of light devices, said means connecting corresponding rows of elements to corresponding rows of devices, character display data input means, each of said elements actuatable to enable the corresponding device in said matrix, means responsive to the input of display data for enabling certain elements in said matrix dependent on the particular character to be displayed, and means for sequentially strobing each of said columns of elements and each of said columns of light devices to control the transfer of encoding data in said gates to said light devices to thereby actuate corresponding light devices.

32. In an information display system for displaying characters in a matrix arrangement of display devices arranged in rows and columns, a display device encoder comprising a matrix of elements arranged in rows and columns corresponding to said matrix arrangement, means connecting corresponding rows of elements to corresponding rows of display devices, said elements actuatable to enable certain devices in said matrix, character display data input means, means responsive to the input of display data for enabling certain elements in said matrix dependent on the particular character to be displayed, and means for sequentially strobing each of said columns of elements to thereby actuate display devices corresponding to said enabled elements.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,594,762 Dated July 20, 1971

Inventor(s) Joseph Gardberg et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 28, line 72, "blocks" should be canceled. Column 29, lines 1, 7 and 8, cancel "blocks", each occurrence; line 61, after "indicator," the remainder of the line and all the matter through line 63 should be cancelled and insert -- means operable responsive to said lamp signal receiving means for reactuating said reset switch, and means operable responsive to said address signal receiving means and said lamp signal receiving means for actuating each lamp switch corresponding to a selected lamp. --. Column 30, line 47, "mean" should read -- means --; lines 48, 49 and 50, cancel "into binary coded decimal form ... Y coordinate numerical data". Column 31, lines 38 and 39, "elements actuatable" should read -- gates adapted --.

Signed and sealed this 6th day of June 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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