Fig. 3

Fig. 4

Fig. 5
This invention relates to annunciators of the type which embody saturable core elements or other static devices to perform the various annunciator logic functions. An object of this invention is to provide in a static element annunciator a static element means for actuating an alarm in response to the operation of a condition responsive device and including means for continuing actuation of the alarm even after termination of operation of the condition responsive device.

Another object of this invention is to provide in an annunciator, static logic means for energizing an indicator in response to the operation of a signal initiating device and including static logic means for energizing an alarm in response to the termination of operation of the signal device.

A further object of this invention is to provide in a static logic annunciator, static logic means which responds to an abnormal signal to sound a first alarm and energize an indicator, then responds to an acknowledge signal to deenergize the alarm and change the energized condition of the indicator, and then responds to the termination of the abnormal condition to again change the energized condition of the indicator and at the same time to energize a second alarm and finally to respond to a second acknowledge signal to deenergize both the indicator and the second alarm.

It is also an object of this invention to provide in a static element annunciator a static element means having circuit terminals releasably plugged in to connector means in a power track or bus arrangement which connects the static elements to alarms, an indicator, signal devices and a power supply to thus provide a complete annunciator.

Another object of this invention is to provide in a plug-in static element circuit having circuit terminals for connecting to each of an indicator, one or more alarms, a power supply, a plurality of switch means, and a flasher to provide a complete annunciator.

It is also an object of this invention to provide in an annunciator system a plurality of static element annunciators each adapted to actuate an individual alarm in response to an individual signal initiating device and each adapted to respond to a single test means connected in common to all annunciators to test all the annunciator circuits and indicators.

It is a further object of this invention to provide in an annunciator system a plurality of static element plug-in units each releasably connected to a power track or bus unit which connects each plug-in unit to a common power supply, common alarms and common signal switches.

It is a further object of this invention to provide a static flasher unit having an oscillator stage comprised of static elements and having a buffer stage comprised of static elements.

Other objects of the invention will in part be obvious and will in part appear hereinafter.

This static logic annunciator is of the type which employs static elements to provide various logic functions which actuate audio alarms and visual indicators in response to predetermined conditions at monitored points. In this annunciator the magnetic amplifiers provide the basic logic functions AND, OR, AND-NOT and INHIBITED AND-NOT.

As used in this application, a static logic AND is an element which provides an output signal only when all of a given number of input signals are present. As used in this application, a static logic OR is an element which provides an output signal when any one of a plurality of input signals are present.

A static logic AND-NOT is an element which provides an output signal in response to one input signal, but only in the event that a second input signal is absent.

A static logic INHIBITED AND-NOT is an element which provides an output signal when a first input signal is present and when a second input signal is not present or when the first and second input signals are present and when a third input signal is present.

This annunciator is designed to respond to digital monitors of conventional types including pressure switches, ratio switches, temperature switches, limit switches and proximity switches, all of which operate to close a contact to thus provide an input signal to the annunciator.

The basic annunciator is comprised of an audio alarm system, a visual indicator system and an acknowledge system. When an abnormal condition is signalled by the monitor device, the alarm system actuates an audio alarm such as a bell, and the visual system flashes a lamp. When the operator closes a momentary switch to activate the acknowledge system, the bell is deactuated and the flashing lamp signal is changed to a steady signal. When the abnormal condition is corrected, the lamp is turned off. In the abnormal condition is corrected before the acknowledge system is actuated, the annunciator returns to normal to thus silence the alarm and extinguish the indicator. It is seen that a transitory abnormal condition would produce transitory alarm signals and indicator signals. If desired, the visual indicator system may be modified to cause the lamp to glow steady in response to the abnormal condition as well as in response to the acknowledge signal.

A lock-in system can be added to the basic system hereinafore described. The lock-in system provides for continuous actuation of the audio alarm and continuous flashing of the lamp even though the fault or abnormal condition is only transitory. The operation of the combined basic system and lock-in system is otherwise identical to the basic system alone as hereinafore described.

A ringback system can be added to the basic system or to the combined basic system and lock-in system. The ringback system provides for actuation of a different audio signal when the abnormal condition has been eliminated. When the ringback system is included in the annunciator, an abnormal condition is indicated by a flashing visual indicator and a sounding audio alarm as in the annunciator hereinafore described. Similarly, when the abnormal condition is acknowledged, the audio alarm is silenced and the flashing signal is changed to a steady signal also as hereinafore described. When the abnormal condition is eliminated, the ringback system causes the visual indicator to return to the flashing condition and simultaneously actuates a different audio alarm, such as a buzzer. Thereafter, when the operator again actuates the same momentary acknowledge switch, the buzzer is turned off and the lamp is extinguished.

A composite annunciator system may be constructed comprising a plurality of annunciators of different types as hereinafore described, each annunciator responding to one particular point or monitored variable and each having its individual visual indicator. The annunciators may otherwise be connected to a common power supply to energize the static elements, a common buzzer, a common bell, a common acknowledge switch and a common flasher unit for flashing the visual signal as described.
above. In addition, the annunciators may be connected in common to a single test switch for applying a test signal to duplicate a fault or abnormal condition signal. In such a test circuit, a rectifier is connected to each annunciator to isolate each point and its monitor from all the other points but at the same time allows simultaneous testing of all the logic, indicators and alarms at all points. Each of the logic functions of the individual annunciators in the hereinafore described composite annunciator may be arranged, fixed, and encapsulated in a compact manner in a relatively small container unit having plug-in terminals at one end and additional terminals at the other end. The plug-in terminals at the one end extend into the container unit with the sockets connected to the annunciators by the various static elements, to serve as signal inputs from the flasher, acknowledge switch, and test switch, and to serve as signal outputs to the bell and buzzer. Thus, the terminals at the one end are related to common characteristics of all the annunciators. The terminals at the other end of each container unit serve as inputs from a monitor device and as an output to a visual indicator. Thus, the terminals at the other end of each plug-in container are related to characteristics individual to each annunciator. The plug-in terminals at the one end of each container are adapted to be received in a power track having a socket connector means for each annunciator container, with the sockets connected to a plurality of bus bars for connecting the annunciators in common to the buzzer, bell, test switch, acknowledge switch and power supply as described above. A single flasher unit is encapsulated in a separate container unit having appropriate plug-in terminals on one end for insertion in one of the channel sockets to connect to appropriate power bus bars and to connect to a flasher input bus bar common to all annunciators.

For a more complete understanding of the nature and scope of our invention, reference may be made to the following detailed description which may be read in conjunction with the accompanying drawings, in which:

FIGURE 1 is a schematic diagram of an annunciator embodying the invention in one of its forms;

FIG. 2 is a symbolic schematic circuit of the annunciator of FIG. 1;

FIG. 3 is a symbolic schematic circuit of a modification of the annunciator of FIG. 1 and FIG. 2;

FIG. 4 is a symbolic schematic circuit of another modification of the annunciator of FIG. 1 and FIG. 2;

FIG. 5 is a symbolic schematic circuit of another modification of the annunciator of FIG. 1 and FIG.2;

FIG. 6 is a symbolic schematic circuit of another annunciator embodying the invention;

FIG. 7 is a top plan view of a plug-in annunciator static logic container;

FIG. 8 is an end view of the plug-in container of FIG. 7;

FIG. 9 is a bottom plan view of the printed circuit board;

FIG. 10 is a schematic diagram of an annunciator system; and

FIG. 11 is a schematic diagram of a flasher.

Static Logic Elements

The static elements which perform the hereinafore described logic functions will be individually described in order to facilitate a better understanding of the annunciator. Thereafter, the annunciator and its modifications will be described in terms of interrelationships between and among the static elements.

Referring now to FIG. 1, there is disclosed a static logic AND element A10 including a toroid SL2, a gate circuit and a reset circuit. The toroid SL2 is comprised of a saturable core 11, gate winding 12 and reset winding 17. The gate winding is energized from a voltage supply tap Ga of secondary winding 14 of transformer 13 (FIG. 10) through an appropriate one of bus bars 210, to connect to annunciator power input terminal 14Ga (FIG. 75).
It is seen that for a proper operation of the static AND element A10, the reset voltage must be 180 degrees out of phase with respect to their associated reset voltage and gate voltage, respectively. Transformer 13 includes eight taps on its secondary winding 14 for achieving these relative phase relationships. The reset tap Gb, a gate voltage tap, is positive going with respect to common taps Ca or Co, tap Ra, a reset voltage tap, is negative going with respect to common. Thus, these two taps provide the alternate gate and reset half cycles for a given static element. The tap Gb is a gate voltage tap 180 degrees out of phase with the first mentioned gate tap Gb and may be used to provide the 180 degrees out of phase relationship between a gate voltage from tap Gb and its associated non-linear impedance or may be used in association with the reset tap Rb to operate a different static element having different phasing.

In much as the hereinafter described annunciator systems require a plurality of static elements to be arranged so that one drives another, it is necessary that an in-phase relationship exist between the gate voltage of the driving saturable core device and the reset voltages and phase relationships provided to drive the desired blocking action. The various taps of the transformer 13 as described above provide means for accomplishing this type of phase relationship as is seen in comparing the circuits of the individual static elements as hereinafter described. Practical values which may be used are 15 volts for the gate taps Ga and Gb and 8 volts for the reset taps Ra and Rb. The transformer 13 steps down the conventional 115 volts and 60 cycles to these gate and reset voltage values. The taps Rb and Ra provide reset voltages of 8 volts to the amplifier only.

The reset taps Rb and Ra of transformer 13 cooperate with a saturable reactance SR to provide distorted reset voltages for the various static element reset circuits. The distorted reset voltage is necessary to compensate for the distorted output voltages which result because of the failure of practical magnetic core materials to produce the theoretically desirable perfectly square hysteresis loop. The distortion is cumulative through a plurality of cascaded elements and may eventually cause the system to cease operation. The saturable reactor SR produces a reset voltage distortion similar to the gate voltage distortion to thus provide a signal which can be completely blocked by the distorted gate voltage of the preceding static element. For a detailed description of the structure and operation of this saturable reactor in a transformer of the type disclosed herein, reference is again made to a pending application Serial Number 640,006, entitled "Magnetic Amplifier Systems," filed February 13, 1957, and assigned to the same assignee as this application.

Also in FIG. 1 there is disclosed a static logic AND-NOT element AN2 including a toroid SL4, a gate circuit and two reset circuits. The toroid SL4 is comprised of a saturable core 65, gate winding 66, reset winding 67 and reset winding 68. The gate winding 66 is energized from a transformer supply tap Ga, a bus bar 210, through annunciator power input terminal 14Ga, terminal 14, conductor 15, terminal 16, conductor 69, winding 66 and rectifier 71, all taken in conjunction with a non-linear impedance including transformer common tap Ca, a bus bar 210, terminal 34Ga, terminal 41Ca, terminal 42, conductor 43, terminal 44, conductor 45, terminal 46, conductor 47, terminal 48, rectifier 49, terminal 50, rectifier 83 of pair of rectifiers 76, resistor 84, terminal 80, conductor 87, terminal 16, conductor 15, terminal 14, annunciator terminal 14Ga, a bus bar 210 and transformer tap Ga. The reset winding 68 is connected to a NOT input terminal 88 through conductor 89 in circuit with a rectifier 90 of pair of rectifiers 78 and in circuit with a non-linear impedance circuit including transformer common tap Ca, a bus bar 210, annunciator terminal 41Ca, terminal 42, conductor 43, terminal 44, conductor 45, terminal 46, conductor 47, terminal 48, rectifier 49, terminal 50, rectifier 83 of pair of rectifiers 76, resistor 84, terminal 80, conductor 87, terminal 16, conductor 15, terminal 14, annunciator terminal 14Ga, a bus bar 210 and transformer tap Ga. The reset winding 68 is connected to a NOT input terminal 88 through conductor 89 in circuit with a rectifier 90 of pair of rectifiers 78 and in circuit with a non-linear impedance circuit including transformer common tap Ca, a bus bar 210, annunciator terminal 41Ca, terminal 42, conductor 43, terminal 44, conductor 45, terminal 46, conductor 47, terminal 48, rectifier 49, terminal 50, rectifier 83 of pair of rectifiers 76, resistor 84, terminal 80, conductor 87, terminal 16, conductor 15, terminal 14, annunciator terminal 14Ga, a bus bar 210, and transformer tap Ga.

With the transformer 13 energized, the gate winding 66 will be energized on alternate half cycles to produce positive saturation of core 65. The reset winding 67 will be energized on successive half cycles following positive saturation to produce negative saturation of core 65 to thus effect reset. Accordingly, all the voltage through tap 14Ga will appear across the gate winding 66 and no effective output voltage will appear at the output terminal 73. If a signal having the same phase and voltage as the reset voltage across 67, as may be provided by the gate output from another static element, be applied to the AND terminal 82 through rectifier 83, the flow of reset will be blocked and gate winding will result with the transformer voltage appearing across the output terminal 73 and rectifier 82. If a like operating voltage be applied to the NOT terminal 88, reset winding 68 is energized to produce negative saturation of core 65 causing reset of core 65 whether or not an input is present at AND terminal 82, thus terminating the output from the gate circuit of AN2.

The static logic AND-NOT element AN3 is structurally and operatively identical to AND-NOT element AN2 previously described and includes a toroid SL7 having a saturable core, a gate winding 113 and two reset windings 114 and 115. The gate winding 113 is energized through transformer tap Gb, a bus bar 210, terminal 28Gb, conductors 22, 24, 115, 116 and 117, winding 113, rectifier 118 through a non-linear impedance including transformer tapCb, conductors 32, 100 and 119, terminal 102, rectifier 103, resistor 104, conductor 62, terminal 14Ga, a bus bar 210, and transformer tap Ga. The reset winding circuit 115 includes NOT input conductor 137, winding 115 and a non-linear impedance including tap Cb, terminal 33Cb, conductors 32 and 100, terminal 101, rectifier 122, resistor 123, conductors 117, 116, 115, 24 and 22, terminal 20Gb, a bus bar 210 and tap Gb. The reset winding 114 is energized from transformer tap Ra, a bus bar 210, terminal 122Ra, conductor 120, winding 114, rectifier 301, all taken in conjunction with a non-linear impedance including tap 41Ca, rectifier 125 of rectifier pair 126, conductor 127, rectifier 123, resistor 129, conductors 117, 116, 115, 24 and 22, terminal 20Gb, a bus bar 210 and tap Gb.

The static logic INHIBITED AND-NOT element IAN1 includes a toroid SL3, a gate circuit and two reset circuits. The toroid SL4 is comprised of a saturable core 91, gate winding 92 and reset windings 93 and 94. The gate winding 92 is energized from transformer tap Ga, a bus bar 210, annunciator terminal 14Ga, terminal 14, conductor 60, winding 92, to output terminal 94, conductor 181 and a non-linear impedance including transformer tap Ca, a bus bar 210, annunciator terminal 41Ca, rectifier 125, conductor 181, resistor 228, conductor 154, terminal 20Gb, a bus bar 210 and transformer Gb. The reset winding 93 is energized from transformer terminal Ra, a bus bar 210, terminal 34Gb, conductors 35 and 37, conductor 95, reset winding 93, rectifier 96 of pair of rectifiers 98, to AND input terminal 99, through a non-linear impedance including transformer tap Ca, a bus bar 210, annunciator common input.
put terminal 33Cb, conductors 32 and 100, terminal 101, terminal 102, rectifier 103, rectifier 105, resistor 106, conductor 62 to terminal 14Ga, a bus bar 210 and transformer tap Ga. Rectifiers 105 and 177 comprise the two inputs of OR element OR4 having an output coinciding with AND input terminal 99. The reset winding 94 is energized through NOT input conductor 100, winding 94, rectifier 108 of pair of rectifiers 109 and a non-linear impedance including common tap Cb, annulator terminal 33Cb, conductors 32, 100, 119, rectifier 110 of rectifier pair 109, resistor 111, and conductor 62 connected to terminal 14Ga, a bus bar 210, and transformer tap Ga. The INHIBITED AND-NOT element IAN1 as described thus far is structurally and operationally the same as AND-NOT elements AN2 or AN3 previously described. However, INHIBITED AND-NOT element IAN1 is provided with an input rectifier 112 for passing an input signal having the same phase and voltage as that across reset winding 94 to oppose the reset voltage through rectifier 108, as previously described, to thus oppose and inhibit the function of the NOT reset circuit. Accordingly, an INHIBIT signal from the gating output of another static element is provided in opposition to a NOT signal at the same time the AND signal is present, core 91 is not reset and on the next half cycle of the transformer an output signal is gated through rectifier 38.

The static logic INHIBITED AND-NOT element IAN2 is structurally and operationally identical with the element IAN1 described immediately above and includes a toroid SL1 having a saturable core 130, a gate winding 131, and two reset windings 132 and 303. The gate winding is energized from tap Gb, a bus bar 210, terminal 29Cb, conductors 22, 24 and 115, winding 131, through rectifier 300 in conjunction with a non-linear impedance including tap Ca, a bus bar 210, terminal 41Ca, conductors 43, 45 and 47, rectifier 49, conductor 51, resistor 133, conductors 58, 60 and 62 to terminal 14Ga, a bus bar 210 and tap Ga. The reset winding 303 is energized from NOT input conductor 104, winding 303, rectifier 302 of rectifier pair 155 and is connected to INHIBIT terminal 136 through a non-linear impedance including tap Ca, a bus bar 210, terminal 41Ca, conductors, 43, 45, 47, bridge rectifier 137, conductors 138, 139 and 140, rectifier 141 of rectifier pair 135, resistor 142, conductors 116, 115, 24, 22 to terminal 20Gb, a bus bar 210 and tap Ga. The reset winding 132 is energized from tap Ra, a bus bar 210, terminal 122Ra, winding 132, rectifier 143 of rectifier pair 144 and is connected to the AND input terminal 145 in conjunction with a non-linear impedance including common tap Cc, bridge rectifier 146 (FIG. 10), a bus bar 210, annulator terminal 215, rectifier 148 of pair of rectifiers 144, resistor 149, conductors 116, 115, 24 and 22 to terminal 20Gb, a bus bar 210 and tap Gb. Rectifiers 148 and 150 comprise the two inputs of OR element OR5 which provides the input to AND terminal 145.

The static element amplifier A11 is operationally identical to the previously described AND element A10. Amplifier A11 differs thereover only in respect to obvious changes such as a decrease in the number of windings on the core to change the power output. Amplifier A11 includes a toroid SL5 having a saturable core 151, a gate winding 152 and a reset winding 153. The reset winding is energized from tap Gb, a bus bar 210, terminal 20Gb, conductor 154, winding 152, and rectifier 155 and is connected to output terminal 212. The reset winding 153 is energized from tap Rg, a bus bar 210, terminal 156Rc, through winding 153 and is connected to each of three AND input terminals 157, 158 and 159 through a rectifier individual to each input, with each rectifier taken in conjunction with a non-linear impedance individual to each input terminal. Rectifier 160 of rectifier pair 161 connects winding 153 to AND input terminal 157 in conjunction with a non-linear impedance including common tap Cb, terminal 33Cb, conductor 32, rectifier 29, conductor 27, conductor 63, signal input rectifier 162 of pair of rectifiers 161, resistor 163, terminal 25, conductors 24 and 22 to terminal 20Gb, a bus bar 210, and tap Gb. Rectifiers 162 and 169 constitute static OR element OR1 having an output coinciding with AND input terminal 158. Rectifier 164 of pair of rectifiers 165 connects winding 154 to AND input terminal 158 through a non-linear impedance including rectifier 29, conductors 27 and 63, rectifier 166 of pair of rectifiers 167, resistor 168, conductors 24 and 22 and terminal 20Gb, a bus bar 210 to tap Gb. Rectifiers 166 and 170 comprise static OR2 having an output coinciding with AND input terminal 158. Rectifier 171 of rectifier pair 165 connects winding 153 to AND input terminal 159 through a non-linear impedance including tap Ca, a bus bar 210, terminal 41Ca, conductors 43, 45, 47, bridge rectifier 137, conductors 138, 139, 172, rectifier 173 of rectifier pair 174, resistor 175, conductors 24 and 22, terminal 20Gb, a bus bar 210 and tap Gb. Rectifiers 176 and 173 comprise OR3 having an output coinciding with AND input terminal 159.

The Annunciator

The hereinbefore described static logic elements are interconnected with each other and are connected with various signal switches, alarms, and indicators so as to provide the hereinbefore described annunciator functions. Referring now to FIG. 1 and to FIG. 2 and to the plug-in arrangement and power supply 13 of FIG. 10 to be taken in conjunction herewith, there is disclosed such an annunciator having both lock-in and ringback. It will be seen that an abnormal condition at a monitored point will cause normally open contact 176 to close to thus provide an input signal from source 305 to the annunciator. A direct current source DC1 including a transformer 304 in conjunction with resistor 225 and a rectifier 137 may be used to step-down voltage to a suitable for operation of the static logic elements. For example, a conventional 115 volt, 60 cycle signal may be stepped-down to 15 volts whereas the bridge rectifier 137, comprised of a first pair of rectifiers 226 and a second pair of rectifiers 227, provides a full wave rectified positive input through signal conductors 138, 139 and 172 through rectifier 177 of OR4 to block reset of core 91 through winding 93 of INHIBITED AND-NOT IAN1 which then gates an output through conductors 178 and 179 through rectifier 180 to sound the bell alarm. The output from IAN1 also provides a signal through conductor 151 and rectifier 169 of Gb to AND input terminal 157 of amplifier A11. A flasher, hereinafter described in detail, provides a pulsing output signal through terminal 213, signal conductor 182, and rectifier 176 of OR3 to AND input terminal 159 of A11 and further provides a signal through conductor 182 and rectifier 170 of OR2 to AND input terminal 158 of A11. The input signal through contact 176 also is provided through conductor 172 and rectifier 173 of OR3 to AND terminal 159 of A11. Thus, the combined steady input signals to AND 157 and AND 159 and the pulsing input to AND 158 provides a pulsing or flashing output signal from A11 to the lamp. The output signal from IAN1 also provides a signal through signal conductors 178 and 127 to AND input terminal 124 of AND-NOT element AN3 which blocks reset of its saturable core to cause it to gate an output through rectifier 165 of OR4 to AND input terminal 99 of IAN1 to thus provide IAN1 with an input even if the fault signal from tap Rg disappear. Thus, it is seen that AN3 with its INHIBIT connection to IAN1, its OR4 connection to IAN1 and its feedback connection from the output of IAN1 provides the lock-in system. The input signal through contact 176 also provides an input signal through signal conductor 140 to INHIBIT terminal 136 of INHIBITED AND-NOT element IAN2 and provides an input signal through signal conductor 89.
to the NOT input of AND-NOT element AN2, neither of which signals have any immediate effect because the lack of signal inputs at their respective AND inputs permits resetting their respective cores.

When the acknowledge switch 147 is momentarily closed, a direct current source DC3 including transformer 193 (FIG. 10) steps-down the 115 volt signal to 15 volts whereverafter bridge rectifier 146 provides a full wave rectified input acknowledge signal to signal conductor 184. The acknowledge signal AN1 is routed through a bus bar 104 to acknowledge input terminal 215, signal conductor 134 as a NOT input to IAN2 and through signal conductor 185 and rectifier 148 of OR5 to AND terminal 145 of IAN2. Since the input signal through contact 176 is providing an input to the INHIBIT input of IAN2, the NOT signal will be inhibited and IAN2 will gate an output through rectifier 132 to provide an input to AND terminal 55 of AND element A10. The AND element A10 then gates an output through signal conductor 27 which provides a feedback through rectifier 150 of OR5 to AND terminal 145 of IAN2 to permit IAN2 and A10 to continue gating an output signal after the acknowledge signal is removed. Static elements IAN2 and A10 thus constitute an AND-MEMORY. The output of A10 through rectifier 19 provides a steady input to AND terminal 157 of A11 through rectifier 162 of OR1. The output of A10 also provides a steady signal to AND terminal 158 through rectifier 166 of OR2. These two input signals in conjunction with the previously described steady input signal to AND terminal 159 through rectifier 173 of OR3 block reset of A11, causing it to change its flashing output signal to a steady output signal for the lamp. The acknowledge signal provides an input to the NOT reset winding of AN3 through signal conductor 121 to reset its core and terminate its output to IAN1. At the same time, the output of IAN2 provides a NOT signal through signal conductor 107 to IAN1 to thus reset its core and eliminate its output to silence the bell. The output of IAN2 also provides a signal through signal conductor 51 to AND terminal 82 of AN2, but since the abnormal signal is still providing a NOT input to AN2 to reset its core, no output is gated.

When the abnormal condition is eliminated, contact 176 reopens to terminate its output signal. When this occurs, the input signal is removed from the AND terminal of IAN1 which has no immediate effect because its core is previously reset by an output from IAN2, the INHIBIT signal is removed from IAN2 having no immediate effect, the steady AND input signal is removed from AND terminal 159 through OR3, causing the lamp to resume its flashing condition, and the NOT input is removed from AN2, thus permitting the AND input through conductor 51 to block reset of AN2 then which gates an output through rectifier 82 to actuate the buzzer, thus providing the ringback system.

When the acknowledge momentary switch 147 is again closed, a signal is applied through conductor 184 to the NOT input of IAN2, thus causing reset of its core since the abnormal signal is no longer present at INHIBIT terminal 136 to inhibit the NOT signal. Thus IAN2 ceases to gate an output to A10 and, accordingly, A10 likewise ceases gating an output to the two AND input terminals 157 and 158 of A11 through OR1 and OR2 respectively, thus causing the lamp to go off. Since the termination of an output from IAN2 eliminates an input to AND terminal 82 of AN2, the output signal from AN2 is terminated to silence the buzzer. The system is thus returned to normal.

To substitute a steady visual condition for the aforementioned flashing visual condition, a signal of the same phase as the reset voltage of amplifier A11 and having a voltage equal to or greater than the reset voltage thereof is substituted for the flasher input signal at flasher input terminal 213. This is achieved through a two-way throw switch 307 which may connect either the flasher or an appropriate transformer tap Or for energizing OR elements OR2 and OR3. Thus the flasher may be entirely omitted if desired. It is to be understood that such an arrangement may be included in any of the annunciator systems disclosed in this application.

A test switch 186 is provided to duplicate an abnormal condition to thus test all the logic elements, alarms and indicators of the annunciator. The test switch 186 is provided to provide a full wave rectified signal of 15 volts from a direct current source DC4 (FIG. 10) including a step-down transformer 187 (FIG. 10) and bridge rectifier 188, and a rectifier device 189 to signal conductor 138 leading from and connected to the contact 176 so as to duplicate an abnormal signal through the same annunciator input signal conductor 138 which provides an abnormal signal in response to the closing of contact 176.

Referring now to FIG. 3, there is disclosed a symbolic diagram of an annunciator having the same type of basic system and ringback system as that disclosed in FIG. 1 and FIG. 2 but showing modifications to be made when the lock-in system is removed. When an abnormal condition occurs, contact 176a closes to provide a signal to the AND input of AND-NOT element AN4, causing it to gate an output signal through rectifier 186a to energize the bell and also to provide an input signal through OR7 to output amplifier A13. At the same time the abnormal signal contact 176a provides an inhibit signal to INHIBITED AND-NOT element IAN3, provides another AND input signal through OR9 to AN13, and provides a NOT signal to AND-NOT element AN5. These signals to IAN3 and AN5 have no immediate effect; but since A13 is now provided with two steady input signals through OR7 and OR9 and a flashing input signal through OR8 from the flasher unit, A13 will gate a flashing output to the lamp. When the momentary acknowledge switch 147a is momentarily closed, a signal is provided to both the AND input and the NOT input of IAN1, but since the abnormal signal inhibits the NOT signal, IAN3 gates an output signal to AND element A12, which in turn gates an output that is fed back through OR6 to the AND input of IAN3 to thus complete the memory loop causing IAN3 and A12 to continue gating an output even after the acknowledge signal is removed. The output of IAN3 provides a NOT signal to AN4 to eliminate its output and thus silence the bell. The output signal of IAN3 also provides an AND input signal to AN5, but the abnormal signal to the NOT input of AN5 prevents an output signal from being gated to the buzzer. The output signal of A12 provides two steady input signals to A13 through OR7 and OR8 which cooperate with the abnormal signal through OR9 to cause A13 to gate a steady output to the lamp. The correction of the abnormal condition removes the steady input through OR9, causing the lamp to resume its flashing condition, and also removes the NOT input signal to AN5, permitting it to gate an output to sound the buzzer. When the acknowledge switch 147a is again closed, a NOT signal is provided to IAN3, causing it to cease gating an output since the abnormal signal is no longer present to inhibit the NOT signal. A12 ceases gating an output to OR7 and OR8 to thus extinguish the lamp. AN5 ceases gating an output to thus silence the buzzer.

Comparing the annunciator of FIG. 3 with that of FIG. 1 and FIG. 2, it will be noted that INHIBITED AND-NOT element IAN1 of FIG. 1 and FIG. 2 has been changed to an AND-NOT element AN1 and 3. An AND-NOT element AN3 of FIGS. 1 and 2 and its associated signal conductors have been completely eliminated. It is considered to be obvious to those skilled in the art how the schematic diagram of FIG. 1 may be modified to eliminate the lock-in system as disclosed in the modified symbolic diagram of FIG. 3.

Referring now to FIG. 4, there is disclosed an annunciator having the same basic system combined with lock-in and ringback as disclosed in FIG. 1 and FIG. 2 but show-
ing modifications to be made when the ringback system is removed. When an abnormal condition occurs, contact 176b closes to provide an abnormal signal through OR10 to the AND input of IAN17, causing it to gate an output to energize the bell and also to provide a feedback signal to the AND input of AN16. Since the NOT input signal does not exist at the NOT terminal of AN16, it gates an output which provides an input signal through OR10 to the AND terminal of IAN17 so that IAN17 will continue to gate an output even though the abnormal signal is terminated. The output of IAN17 also provides an input through OR12 to one AND input of A19 while a flasher unit provides a pulsing input signal through OR13 which causes the lamp to flash. When the acknowledge switch 1476 is closed, an acknowledge signal is provided to the NOT input of AN16 to reset its core and terminates its output which in turn removes the input through OR10 to IAN17 since the abnormal signal has terminated. Thus IAN17 ceases gating an output to thus silence the bell and to terminate the input through OR12 to A19 to thus extinguish the light.

Comparing FIG. 4 with FIGS. 1 and 2, it will be noted that the element AN2 of FIGS. 1 and 2 with its attending buzzer and signal conductors has been completely eliminated, that a two-input AND element A15 has been substituted for the inhibited AND-NOT element IAN2 of FIGS. 1 and 2, that the abnormal signal input is connected to provide an inhibit signal to HIHIBITED AND-NOT element IAN2, that the two-input AND preamplifier A19 has been substituted for the three-input AND preamplifier A11 of FIGS. 1 and 2, and that the flasher provides an input signal to only one of two OR units in FIG. 4, while in FIGS. 1 and 2 the flasher provides an input signal to two of three OR elements connected to a three-input AND amplifier A11.

The hereinafore described feedback cooperation between AND-NOT element AN16 and INHIBITED AND-NOT element IAN17 of FIG. 4 and between elements AN3 and IAN1 of FIGS. 1 and 2, provides a MEMORY circuit having a retentive memory. For example, in FIG. 4 the INHIBIT signal input to IAN17 as provided by the output of AN16 provides this retentive memory in the event of power failure. It is possible that reappearance of power after a power failure will cause A15 to gate an output when momentarily acknowledge switch 1476 has not been closed to thus provide a false or superfluous acknowledge signal to the NOT terminal of IAN17 to turn off the MEMORY when it should stay on. The output from AN16 to the INHIBIT terminal of IAN17 will block and nullify the effect of such an output from A15.

Referring now to FIG. 5, there is disclosed an annunciator comprised of the basic system such as that disclosed in FIG. 1 and FIG. 2, but without the ringback system and without the lock-in system. When an abnormal condition occurs, contact 176c closes to provide an input signal to the AND terminal of AN21 which causes it to gate an output to actuate the bell and also to provide a signal through OR22 to one AND input of amplifier A24. A flasher unit provides a pulsing signal through OR23 to the other AND input of A24, causing it to gate a pulsing output to flash a lamp. The abnormal signal is also provided to one AND input of A18. When the acknowledge switch 147c is closed, an acknowledge signal is provided at the other AND input of A18, causing it to gate an output to the NOT CIRCUIT of AN21 to rest its core and terminate its output to thus silence the bell. The output signal from A18 provides an input signal to A20, causing it to gate an output signal which is fed back through OR39 to one of the AND inputs of A18 to maintain the MEMORY loop signal even when the acknowledge signal is removed. The output signal from A20 also provides a steady input through OR22 to one input of A24 and through OR23 to the other input of A24 so that it will now gate a steady output signal to the lamp. When the abnormal condition is eliminated, the contact 176c reopens to terminate an input signal to A18. Therefore, A18 gates no output to A20, which then gates no output to A24 to thus extinguish the light.

The basic annunciator system of FIG. 5 discloses means for interconnecting a plurality of annunciators in such fashion that each may be actuated by its individual contact for signalling an abnormal condition, and each may actuate its individual visual indicator, but at the same time all annunciators may be connected in common to a single flasher, a single bell, a single buzzer and a single test system. The additional rectifiers 189d and 180c represent audio alarm outputs from other switches identical to that shown in detail in FIG. 5. Thus, rectifiers 189c, 189d and 180e comprise an OR element OR50 connecting the audio alarm systems of plural annunciators to a single bell. The additional flasher output conductors 182d and 182e lead to the other annunciator systems, thus connecting a single flasher in common with all annunciators. The additional conductors 184d and 184e lead to said other annunciators to connect the acknowledge switch 147c in common with all annunciators. The additional rectifiers 189d and 189e lead to the other annunciators (not shown) where each additional rectifier is associated with an abnormal signal contact in the same manner that rectifier 189c is associated with contact 176c. The rectifiers thus arranged provide for a single audio alarm system to simultaneously provide a test signal to actuate all the logic systems, alarms and indicators in all annunciators, but at the same time provide isolation of each contact from all others so that each annunciator will respond only to an abnormal signal provided by its individual contact.

It is to be understood that the aforementioned annunciator connector means may be used to couple annunciators of the type shown in any of FIGS. 2 through 6. The annunciators may be all the same or mixed indiscriminately.

Referring now to FIG. 6, there is disclosed a symbolic diagram of an annunciator not hereinbefore disclosed but which performs the same functions as the previously described annunciator having a lock-up and a ringback system. The symbolic elements of FIG. 6 represent static magnetic elements of the type disclosed in FIG. 1. It will be obvious to one skilled in the art how these static elements of the type shown in FIG. 1 may be interconnected to provide the logic functions disclosed in FIG. 6 and described in the following subject matter relating thereto.

In FIG. 6, an abnormal condition causes a monitor device (not shown) to close normally open contact 308 which provides an input signal through OR25 to the AND input of AND-NOT element AN26, causing it to gate an output signal to the AND input of AND-NOT element AN27 which then gates an output signal to actuate the bell. The output signal from AN27 also provides an input signal through OR28 to an AND input of an amplifier A29 to cooperate with a pulsing input signal from the flasher through OR30 to provide a pulsing or flashing output to the other AND input of A29. The output signal from AN27 also feeds back through OR25 to the AND input of AN26 to provide a lock-in system. The output signal from AN26 also provides a signal to an AND input of AND element A31, which input is temporarily ineffective since no signal is provided at the other AND input of A31. The input signal through contact 308 also provides a signal through OR32 to the NOT input of AND-NOT element AN33, which signal is temporarily ineffective since no signal is provided to the AND input of AN33. When momentarily acknowledge switch 309 is closed, an acknowledge signal is provided through OR34 to the NOT input of AN27 which causes AN27 to cease gating an output to thus silence the
The acknowledge switch also provides a signal through OR32 to the other AND input of A31, thus causing A31 to gate an output through OR30 to an AND input of A29, which then operates with a steady output signal through contact 308 and OR28 to A29 to change the flashing lamp signal to a steady lamp signal. The output signal from A31 also feeds back through OR35 to the AND input of AND-NOT element AN36 which responds to gate an output through OR30 to an AND input of A31, thus providing a MEMORY to persist in gating a steady output through OR30 to A29 even after the acknowledge signal ceases. The output signal from AN36 also provides a signal through OR34 to continue a signal to the NOT input of AN27 to maintain the bell in a silenced condition after the acknowledge signal has terminated. When the abnormal condition is eliminated, contact 308 reopens to terminate the signal through OR25 to AN26 which responds to cease gating an output signal to an AND input of A31. Accordingly, A31 no longer gates an output signal through OR30 to A29, the abnormal signal no longer is provided through OR25 to A29. Also with the removal of the abnormal signal through OR32 to the NOT input of AN33, an output signal is gated from AN33 to the buzzer and through OR28 to an AND input of A29 to cooperate with the flasher input signal through OR30 to again flash the lamp. When the output signal from A31 is terminated because of a lack of input from AN26 as described above, the memory loop including A31 to AN36 is destroyed simultaneously with the forming of another MEMORY loop including AN36 and AN33. The output from AN33 through OR35 causes AN36 to gate an output signal to the AND input of AN33. When the acknowledge switch is opened, an acknowledge signal is provided through OR32 to the NOT input of AN33 to terminate the output from AN33, which termination silences the buzzer, disrupts the MEMORY loop through OR35 to AN36, and terminates the signal through OR28 to A29, thus causing the lamp to be extinguished. The function of capacitor 310 and the NOT input of AN36 is described below.

When the annunciator of FIG. 6 is operating at low voltage, due to normal fluctuations in the power supply system, the hereinbefore described MEMORY loop comprised of AN36 and AN33 may not be formed as the other MEMORY loop is being terminated, because the two MEMORY loops coexist for only one gating pulse from AN36. At low voltage, one pulse is insufficient to lock-out MEMORY loop AN36 and AN33 because the saturable magnetic cores in the magnetic devices are wound for maximum voltage. Accordingly, at low voltage, a single pulse is insufficient to gate an output from AN33 which requires two input pulses to gate its first output pulse at half maximum voltage. To operate the annunciator at voltages as low as one-half normal, a capacitor 310 is provided and connected as shown in the output of A31. This capacitor is charged when A31 is gating an output through OR36 in the manner hereinbefore described. When the abnormal signal terminates to cause AN26 to cease gating an input to A31 thus causing A31 to terminate its output signal, capacitor 310 discharges through the feedback MEMORY loop through OR39 to AN36 to thus effectively delay removal of the output from A31 and to thus cause AN36 to provide several output pulses to assure lock-in of the MEMORY comprised of AN36 and AN33 when the abnormal signal is removed.

The NOT input to AN36 from the output of AN27 is provided to compensate for the capacitor in the event of a power failure output when capacitor 310 provided is an abnormal condition occurred, but prior to acknowledge- ment of such abnormal condition, a reaplication of power normally should cause the lamp to flash and the bell to ring. The addition of the capacitor as above described gives rise to the possibility of its discharge upon reaplication of power to form MEMORY loop AN36 and A31 which would then operate in the manner hereinbefore described to provide a false acknowledge output signals. Therefore, inasmuch as AN27 gates an output until there is an acknowledgement signal, AN27 provides a NOT input signal to AN36 to thus prevent the occurrence of the false acknowledge signal resulting from operation of the capacitor 310.

Plug-in Units

As hereinbefore described, the static logic elements of any of the annunciators of FIGS. 2 through 6 may be arranged, fixed and encapsulated in a compact manner in a relatively small container unit having suitable plug-in terminals at both ends. The plug-in terminals extend internally of the unit to be connected to the logic elements therein, and extend externally of the unit for connection to an appropriate power supply and other devices to thus complete the annunciator system.

Referring now to FIGS. 7, 8 and 9, there is disclosed a static element plug-in unit 200 with the cover (not shown) removed. The unit 200 is rectangular in form and is comprised of two sides 201 and 202, two ends 203 and 204, and a bottom 205. The sides, ends and bottom may be rigidly connected to each other in any suitable manner. Within the container 200 are arranged a plurality of elements representative of conventional toroids, rectifier boxes and resistors which are interconnected with each other through a printed circuit board 206 of conventional type and having a plurality of conductors 207 thereon. The printed circuit board 206, shown in a top plan view in FIG. 7, may be fixed in the container unit in any suitable manner. FIG. 9 shows the printed circuit board in bottom plan view.

The various toroids, rectifier boxes, resistors and conductors in container 200 correspond to the comparable toroids, single rectifiers, rectifier pairs, resistors and conductors as disclosed in the schematic diagram of FIG. 1 as modified by the teachings of the symbolic diagram of FIG. 3 showing the lock-in feature omitted. The toroids, rectifiers, rectifier pairs in the container 200 have been given the same reference numerals as their comparable elements of FIG. 1. The individual conductors of FIG. 1 have not been identified in the circuit board of FIG. 9 to avoid confusion in the drawings; however, the individual toroids, resistors, rectifiers and rectifier pairs of FIG. 7 have been superimposed in outline form on the printed circuit board 206 to clearly illustrate the relative positioning thereof with respect to the printed circuitry.

It will be obvious that the omission of the lock-in system from FIG. 1 eliminates toroid SL7, conductors 121, 120, 117 and 127, rectifiers 122, 208, 123, 126, 118, 103, 112 and 177, resistors 129, 123 and 104, and requires that conductor 172 be disconnected from point 99 and reconnected to provide an input through rectifier 105 adjacent point 99.

In view of the foregoing, it is considered obvious how other plug-in container units may be provided with appropriate printed circuit boards and associated static elements to provide the basic annunciator logic system of FIG. 5, the basic logic system with lock-in of FIG. 4, the basic logic system with ringback and lock-in of FIGS. 1 and 2, and the annunciator of FIG. 6.

A plurality of plug-in terminals 209 extend internally and externally of end 203 of container 200 to serve as means for connecting the encapsulated static elements to a plurality of bus bars 210 (FIG. 10) which carry power inputs to the container 200 and which provide outputs to the various alarm devices. In FIG. 9 the plug-in terminals 209 are shown connected to their respective annunciator terminals having the same reference numerals as the corresponding input or output terminals of the annunciator circuit of FIG. 1 and thus the function of each of
the plug-in terminals 209 is obvious. It should be noted that though the internal circuitry of each of the annunciators hereinbefore described is different from the others, the input and output terminals are identical. Thus, it is seen that terminal A is the bell output terminal, terminal B is the test input terminal, terminal C is the flasher input terminal, terminals D, E, F, H, I, and J are power terminals, terminals G and L are blank terminals, terminal M is the acknowledge input terminal, and terminal N is the buzzer output terminal.

A plurality of terminals 216 extend internally and externally of end 204 of container 200. The terminals 216a and 216b are connected internally to terminals 217 and 218 of the logic system of FIG. 1 to provide external connections to the contact 176 (FIG. 10) and to a power source 305 to provide the abnormal input signal. If desired, the contact 176 may be connected across the power source of transformer 13. The terminal 216c connects internally to light terminal 212 (FIG. 1) to provide an output terminal for connection to its individual lamp (FIG. 10).

Referring now to FIG. 10, there is disclosed a complete annunciator system of the type hereinbefore described including the static logic plug-in unit 200 positioned so that its plug-in connector terminals 209 may be inserted into a group of mating connector terminals 219 comprising a connector position in a power track 220 which includes a plurality of such positions and a plurality of bus bars 210 with each bus bar connected internally of the power track in any suitable manner to one terminal of every position and with no terminal connected to more than one bus bar. The power track 220 may be comprised of two laterally connected power tracks of the type disclosed in detail in a pending application Serial No. 651,085, filed April 5, 1957, to thus provide a single power track having sixteen bus bars therein and having sixteen plug-in mating connector terminals for each plug-in connector position. Inasmuch as the disclosed plug-in container unit 200 utilizes only 14 terminals 209, some of the bus bars will be unused as signal carriers but their mating terminals may be used as base supports for the hereinbefore described blank container terminals G and L of FIG. 9. The bus bars 210 extend from the power track 220 and are connected to appropriate terminals of the power supply, the bell, the buzzer, the acknowledgment signal switch 147 and the test switch 186, in the manner disclosed, to provide the hereinbefore described annunciator functions. The unused bus bars are shown extended from the power track and unconnected to other devices. It is obvious, if desired, to eliminate all unused bus bars and blank terminals. Thus, it is seen that bell output terminal A is connected through corresponding bus bar AA to the bell, test output terminal B is connected through corresponding bus bar BB to the test switch 186, and flasher input terminal C is connected to corresponding flasher output bus bar CC. It is seen that the remaining terminals C through N are connected through corresponding bus bars CC through NN respectively to the appropriate power supply taps of transformer 13, to the acknowledge signal switch 147, and to the buzzer. It is obvious that additional plug-in container units 200b may be plugged in to the power track 220 at other plug-in connector positions to thus provide a complete annunciator system for monitoring plural points as hereinbefore described. The additional plug-in containers may be identical to plug-in container 200 in internal static logic elements or they may be different therefrom to provide the basic annunciator logic system alone or in combination with either the lock-in system or the ringback system as hereinbefore described. A plug-in flasher unit 221, to be hereinafter described in detail, is provided in its own plug-in container unit having appropriate plug-in connector terminals to connect to appropriate transformer power supply bus bars in the power track 220, and to connect to bus bar LL to provide a pulsing output signal to each of the flasher input terminals of the individual plug-in container units 200 and 200a.

A second power track 220a, identical in structure to power track 220, is provided to operate additional plug-in units (not shown) of the same structure as units 200 and 200a. It will be noted that bus bars AA through NN leading from track 220 are connected to correspondingly arranged bus bars in power track 220a with the exception of the power input bus bars and other changes described below. Thus, the bus bars EE and JJ leading to opposed gate supply voltages have been interchanged in their connection to power track 220a while bus bars FF and II leading to opposed reset supply voltages also have been interchanged in their connections to power track 220a. This interchanging of bus connections reverses the operating phase of the annunciator units and flasher unit in power track 220a with respect to the units and flasher of power track 220, thus permitting a single transformer 13 to utilize the full cycle of each tape to operate all the units and flashers in the two power track elements in keeping with this phase reversal, the flasher output bus bar of track 220a is connected through a two-way throw switch 310 to the power tap Gb, having a phase opposite that of tap Ga. Also, in keeping with this phase reversal, the bus bar for driving the reset circuit of the amplifier is connected to tap Rd, having a phase opposite that of tap Kr.

Flasher

The flasher disclosed in FIG. 11 provides the pulsating signal to the lamp preamplifier in the manner hereinbefore described and is comprised of a static element oscillator stage 222 and a static element buffer stage 223. The oscillator stage 222 is comprised of two static magnetic NOT elements N224 and N225 interconnected with each other and a pair of resonant elements to provide regenerative feedback to sustain oscillation. The buffer stage 223 is comprised of two static magnetic INHIBITED NOT elements IN273 and IN275 interconnected with each other and connected to the oscillator to provide high output power, to isolate the oscillator from its load, and to provide a fast switching action.

In the oscillator stage 222, the first flip-flop element N224 is comprised of a magnetic core 226 having a gating winding 227 which may be energized from transformer terminal Ga (FIG. 10) which may be connected to flasher terminal 228Ga, conductor 229, winding 227, rectifier 230, rectifier 231 of non-linear impedance 232, common conductor 233 and flasher terminal 234Ca which may be connected to transformer common terminal Ca. The non-linear impedance includes transformer terminal Gb, flasher terminal 235Gb, conductors 236 and 236a, resistor 237, rectifier 231, conductor 233, terminal 234Ca, a bus bar 210 and transformer terminal Ca. Rectifier 230 and non-linear impedance 232 connect gate winding 227 to output terminal 240. It is to be understood that appropriate conductors such as bus bars 210 (FIG. 10) may interconnect the transformer terminals with their respective flasher terminals. The NOT reset winding 228 is connected to a NOT input terminal 238 in circuit with a rectifier 239, rectifier 241 of non-linear impedance 242, conductor 233, terminal 234Ca, and transformer terminal Ca. Thus winding 228 is energized in response to a positive signal applied to NOT input terminal 238. The non-linear impedance includes transformer terminal Ca, flasher terminal 234Ca, conductor 233, rectifier 241, resistor 311, conductor 229, flasher terminal 228Ge and transformer terminal Ga.

The NOT element N225 of oscillator 222 is comprised of a magnetic core 232 having a gating winding 243 which may be energized from transformer terminal Gb, through flasher terminal 235Gb, conductor 236, winding 243, rectifier 244, rectifier 245 of non-linear impedance 246, common conductor 233a, flasher terminal 234Ca.
and transformer terminal Ca. The non-linear impedance 246 includes transformer terminal Ca, flasher terminal 234Ca, rectifier 245, resistor 247, conductors 229a and 229, flasher terminal 228Ga and transformer terminal Ga. Rectifier 244 and impedance 246 connect gate winding 243 to output terminal 253. The magnetic core 312 is also provided with a NOT reset winding 247 connected to NOT input terminal 248, rectifier 247, and capacitor 251 of non-linear impedance 250, capacitor 233a, flasher terminal 234Ca, and transformer terminal Ca. Thus, reset winding 247 is connected to respond to a positive input applied at NOT terminal 248. The non-linear impedance 250 includes transformer terminal Ca, flasher terminal 234Ca, conductor 233a, rectifier 251, resistor 252, conductor 256, terminal 235Gb and transformer terminal Gb.

The output terminal 240 of NOT element N224 is connected through a capacitor 254 to the NOT input 248 of NOT element N225. The capacitor 254 is also connected in circuit with a resistor 255 and rectifiers 256 and 259 which complete a hereinafter described discharge circuit for capacitor 254. Similarly, the output terminal 253 of NOT element N225 is connected through a capacitor 257 to the NOT input 238 of NOT element N224. Capacitor 257 is also connected in circuit with a resistor 258 and rectifiers 259 and 256 which complete a hereinafter described discharge circuit for capacitor 257. The output terminal 240 of NOT element N224 and the output terminal 253 of NOT element 224 are each connected to an input of the buffer stage 223 in a manner hereinafter described.

In the buffer stage 223, the first static INHIBITED-NOT element IN273 is comprised of a magnetic core 256, having a gate winding 251 and a reset winding 262. The gate winding 261 may be energized from transformer terminal Gb, through flasher terminal 235Gb, conductors 236 and 236a, winding 261, rectifier 262, rectifier 264, of non-linear impedance 265, conductor 233, flasher terminal 234Ca to transformer terminal Ca. The non-linear impedance 265 includes transformer terminal Ca, flasher terminal 234Ca, conductor 233, rectifier 264, resistor 266, conductor 229, flasher terminal 228Ga and transformer terminal Ga. Rectifier 263 and non-linear impedance 265 connect gate winding 261 to output terminal 267. The reset winding is connected to NOT input terminal 268 through rectifier 269, reset winding 262, INHIBIT input terminal 270, rectifier 271 of non-linear impedance 272, conductor 233, flasher terminal 234Ca to transformer terminal Ca. The non-linear impedance 272 includes transformer terminal Ca, flasher terminal 234Ca, conductors 233, rectifier 271, resistor 274, conductors 240a and 236, flasher terminal 235Gb and transformer terminal Gb.

The other INHIBITED-NOT element IN275 is comprised of a magnetic core 276, a gate winding 277 and a reset winding 278. The gate winding 277 is energized from transformer terminal Ga, flasher terminal 228Ga, conductors 229 and 239a, winding 277, rectifier 279, rectifier 280 of non-linear impedance 281, conductor 233a, flasher terminal 234Ca, to transformer terminal Ca. The non-linear impedance includes transformer terminal Ca, flasher terminal 234Ca, conductor 233a, rectifier 280, resistor 282, conductor 235, flasher terminal 240a and transformer terminal Ga. The rectifier 279 and non-linear impedance 281 connect gate winding 277 to output terminal 267. The reset winding 278 is connected to NOT input terminal 268 through rectifier 283, and is connected through INHIBIT input terminal 284, rectifier 285 of non-linear impedance 266, conductor 233a, and transformer terminal Ca. The non-linear impedance includes transformer terminal Ca, flasher terminal 234Ca, conductor 233a, rectifier 285, resistor 289, conductors 229a and 229, flasher terminal 228Ga and transformer terminal Ga.

The output terminal 240 of the oscillator 222 is connected through rectifier 287 to the INHIBIT input terminal 270 of the buffer stage 223. Similarly, the output terminal 253 of the oscillator 222 is connected through rectifier 288 to the INHIBIT input terminal of the buffer stage 223. In describing the operation of the flasher 221 as hereinbefore described, it is assumed that as a prime condition, the oscillator N224 is generating an output signal through output terminal 240 to NOT element N225 to reset its core 312 to thus prevent an output from being gated through output terminal 253. The output terminal 240 also charges capacitor 254 with a charging current which is determined by the coercive force of the core 312, the resistor 252 and the output terminal 240. The capacitor 254 continues to be charged with each additional gating pulse through terminal 240, the other capacitor 257 is discharging through output terminal 253, rectifier 258, resistors 247 and 239, conductors 229a and 229, rectifier 259, and resistor 255 back to the capacitor 257. Additionally, capacitor 254 may discharge through transformer winding connected across terminals 228Ga and 234Ca. The NOT element N224 thus receives no effective input to reset its core 226 and accordingly continues to gate an output to capacitor 254. As capacitor 254 continues to charge, it eventually blocks the reset signal to NOT input terminal 248 as at the same time reduces its own charging rate. The termination of the output input to reset winding 247 causes NOT element N225 to begin gating an output through its output terminal 253 to begin charging capacitor 257 and to cause reset of core 226 through NOT input terminal 238. The NOT element N224 now ceases gating an output through 240, thus permitting charged capacitor 254 to discharge through terminal 240, rectifier 287, resistors 237 and 274, conductors 236a and 236, rectifier 256 and resistor 255 back to capacitor 254. Additionally, capacitor 254 may discharge through transformer winding 228Ga and 235Gb connected across the transformer. The NOT element N225 thus receives no effective input to reset its core and accordingly continues to gate an output to reset core 226 of NOT element N224 and to continue charging capacitor 257. As capacitor 257 continues to charge, it eventually blocks the reset signal to NOT input terminal 253, and at the same time reduces its own charging rate. The NOT element N224 begins gating an output to begin a new cycle of operation and thus N224 and N225 cooperate to provide the desired oscillations.

As the NOT element N225 is gating an output signal through terminal 240 to charge its associated capacitor 254 and reset core 312 of NOT element N224, the manner hereinbefore described, the output through terminal 240 also is providing a signal through rectifier 287 to INHIBIT terminal 270 of INHIBITED-NOT element IN273 in the buffer stage 223. This INHIBIT input voltage signal is the same phase and opposite in direction to the reset voltage across reset winding 262. This input signal 270 increases as capacitor 257 charges to prevent full reset of core 226. When the INHIBIT signal reaches a predetermined level, reset of core 260 is blocked, causing it to gate an output through terminal 265, 267 and flasher output terminal 290. The output signal from IN273 is provided through NOT input terminal 260 and rectifier 288 to reset winding 278 of INHIBITED-NOT element IN275 to thus reset core 276 which prevents gating winding 277 from gating an output through rectifier 279 to output terminal 267 and flasher output 290. The INHIBITED-NOT element IN273 continues gating an output to flasher terminal 290 so long as the NOT element N224 of the oscillator stage 222 is gating an output. While NOT element N224 is gating an output, capacitor 257 is discharging to provide a signal through output terminal 253 and rectifier 288 to INHIBIT input terminal 268 in the manner previously described. But,
the NOT input signal is not blocked, as the voltage level on the capacitor is too low at this time, and thus the capacitor will discharge signal to INHIBIT terminal 284 and thereafter to INHIBITED-NOT element IN274.

In a similar fashion, when NOT element N225 is giving an output signal to charge capacitor 257 and reset the NOT element N224 in the manner previously described, the output signal from N225 through output terminal 253 is providing an input signal through rectifier 228 to INHIBIT terminal 284 of INHIBITED-NOT element IN275. This INHIBIT signal opposes the NOT signal which then gates an output through rectifier 279, and output terminal 267 to flasher output terminal 290. At the same time, the output from IN275 provides a signal through NOT terminal 269 to reset winding 262 causing reset of core 260 to thus terminate its output signal to flasher output terminal 290.

Thus, it is seen that the buffer stage 223 responds to oscillations of the oscillator stage 222 to alternately provide signals of opposite phase to the flasher output terminal 290. Accordingly, if the output terminal 290 is connected to an input terminal of a static element such as phase amplifier A13 of FIG. 5 or any of the preamplifiers as hereinbefore described, the output signal from 290 will periodically be in phase with the reset voltage of said static element thus providing a pulsing "on" input signal.

It is obvious that appropriate toroids, rectifier boxes, resistors and a printed circuit board representing a flasher 221 of FIG. 11 may be encapsulated in a plug-in container in a manner clearly taught by the plug-in container 260 of FIG. 7. Accordingly, the details of the particular plug-in container for the flasher are not shown. It is clear that such a plug-in container would have a plug-in terminal for connecting terminal 228Gr to bus line J1, a plug-in terminal connecting terminal 290 to bus line CC, a plug-in terminal connecting terminal 224Cx to bus line KK, and a plug-in terminal connecting terminal 235 to bus line EE. The flasher unit 221 is shown in a container unit 313 and plugged in to power track 220 in FIG. 10 to provide a flasher output signal to each of the plug-in containers 200 and 200B through bus bar 218 connected in common to the flasher input terminal of each plug-in container.

Inasmuch as the annunciator embodying the features of this invention is comprised of static logic elements having no moving parts, the annunciator is highly reliable in operation and requires substantially no maintenance.

Since certain of the above-described features may be changed without departing from the spirit and scope of this invention, it is intended that all the matter contained in the above description and shown in the accompanying drawings should be considered as illustrative only.

We claim as our invention:

1. In an annunciator: a static AND-NOT element having an output connected to an alarm and to an input of a first static OR element, said first static OR element having an output connected to one AND input of a two input AND amplifier having an output for controlling an indicator; an output from a signal device connected to the AND input of said static AND-NOT element and connected to one AND input of a static MEMORY; said static MEMORY having an output connected to one input of said first static OR element and connected to an input of a second static OR element; said second static OR element connected to the second AND input of said AND amplifier; an output from a pulse producing means for altering said control signal and connected to an input of said second static OR element; an output from an acknowledge signal means connected to the second input of said static MEMORY; and an output from said MEMORY connected to the NOT input of said static AND-NOT element.

2. In an annunciator: a first static AND-NOT element having an output connected to an alarm and connected to one AND input of a three input AND amplifier having an output for connection to an indicator; a static three input AND MEMORY having a first output connected to one AND amplifier input and connected to a second AND input of said AND amplifier, and having a second output connected to the NOT input of said first static AND-NOT element and connected to an AND input of a second static AND-NOT element; said second static AND-NOT element having an output for controlling an additional alarm; a flasher having an output connected to the second and third AND inputs of said AND amplifier; means for providing an abnormal signal and having an output connected to the AND input of said first static AND-NOT element, to a first input of said static AND-MEMORY, to the NOT input of said second static AND-NOT element and to the third AND input of said AND amplifier; means for providing an acknowledge signal and having an output connected to the second and third inputs of said static AND-MEMORY.

3. In an annunciator: a static INHIBITED AND-NOT element having an output connected to a plurality of inputs including an alarm input, a first input of a two input AND amplifier, and the AND input of a static AND-NOT element; said static AND-NOT element having an output connected to the AND input and the INHIBIT input of said INHIBITED AND-NOT element; a static AND-MEMORY element having two inputs and two outputs with one of said outputs connected to both inputs of said static AND amplifier and with the second output connected to the NOT input of said INHIBITED AND-NOT element; a flasher element having an output connected to one input of said AND amplifier; means for providing an abnormal signal and having an output connected to the AND input of said static AND-NOT MEMORY; means for providing an acknowledge signal and having an output connected to the other input of said static AND-MEMORY.

4. In an annunciator: a static INHIBITED AND-NOT element having an output connected to a plurality of inputs including an alarm input, a first input of a three input AND amplifier, and the AND input of a first static AND-NOT element; said static AND-NOT element having an output connected to the AND input and the INHIBIT input of said INHIBITED AND-NOT element; a second INHIBITED AND-NOT element having an output connected to the NOT input of the first INHIBITED AND-NOT element, the single input of a static AND memory, and the AND input of a second static AND-NOT element, said second AND-NOT element having an output connected to a second alarm; said single input AND element having an output connected to the first and second AND inputs of said three input AND amplifier, and to the AND input of the second INHIBITED AND-NOT element; a flasher having an output connected to second and third AND inputs of said three input AND amplifier; means for providing an abnormal signal and having an output connected to the AND input of the first INHIBITED AND-NOT element, to the INHIBIT input of the second INHIBITED AND-NOT element, to the NOT input of the second AND-NOT element, and to the third AND input of the three input AND amplifier; and means for providing an acknowledge signal and having an output connected to the NOT input of the first AND-NOT element, and to the AND input and the NOT input of the second INHIBITED AND-NOT element.

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