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(54) **Solid state imaging device having high-sensitivity and low-noise characteristics by reducing electrostatic capacity of interconnection**

Festkörper-Bildaufnehmer mit hoher Empfindlichkeit und geringem Rauschen durch Verringerung der elektrostatischen Kapazität der Verdrahtung

Dispositif d'imagerie semi-conducteur ayant une haute sensibilité et des caractéristiques de faible bruit par réduction de capacité électrostatique d'interconnexion

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- **PATENT ABSTRACTS OF JAPAN vol. 17, no. 378 (E-1398)15 July 1993 & JP-A-05 063 177 (SONY CORP)**
- **PATENT ABSTRACTS OF JAPAN vol. 9, no. 328 (E-369)24 December 1985 & JP-A-60 160 659 (HITACHI SEISAKUSHO KK)**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a solid state imaging device. More particularly, the invention relates to enhancement in sensitivity of a solid state imaging device having a vertical overflow drain structure.

2. Description of the Prior Art

[0002] As the solid state imaging device, taking an example of an interline transfer type area image sensor, the prior art will be explained below.

[0003] Fig. 5 shows the overall construction of a common interline transfer type area image sensor. Optical information incident on a matrix-arrayed photoelectric conversion section 21 is converted into a signal charge by the photoelectric conversion section 21. Then the signal charge is transferred to a charge detecting section 24 connected to a horizontal transfer section 23 via a vertical transfer section 22 and the horizontal transfer section 23. The charge detecting section 24 is comprised of a floating diffusion layer (forming a cathode side portion of a diode D1) for converting the signal charge in voltage, and a two-stage source follower circuit connected thereto for impedance conversion. This source follower circuit comprises transistors T1, T2 serving as its driver transistors, and transistors T3, T4 serving as its load transistors, where a DC voltage V_{GG} is applied to gates of the transistors T3, T4. Also, DC voltage is applied to a RD terminal and an OD terminal. After the diode D1 is reset by a reset pulse ϕR applied to a gate of a reset transistor TR, the signal charge transferred from the horizontal transfer section 23 is further transferred to the floating diffusion layer via an output gate 25. Depending on the amount of this signal charge, voltage at point A changes, and the resulting voltage change is converted in impedance by the two-stage source follower circuit, and outputted from an output terminal OS.

[0004] Referring to Fig. 5, when a ray of intense light impinges on part of the matrix-arrayed photoelectric conversion section 21, there will occur the so-called blooming phenomenon that excess charges generated stretch over the peripheral regions. To suppress this blooming phenomenon, a vertical overflow drain structure has been adopted heretofore.

[0005] Fig. 8 illustrates in section the vertical transfer section 22 and the photoelectric conversion section 21 having the vertical overflow drain structure. In detail, a FP (flat p-type) well 53 is formed on an n-type semiconductor substrate 51, and the vertical transfer section 22 and the photoelectric conversion section 21 are formed within the FP well 53. The vertical transfer section 22 comprises an n-type semiconductor layer 54, a p-type semiconductor layer 55 for preventing injection of charges and inflow of charges of smear components from the n-type semiconductor substrate 51 into the vertical transfer section 22, a vertical transfer electrode 58, and a light-screening film 60 for light screening. The photoelectric conversion section 21, on the other hand, comprises an n-type semiconductor layer 56, and a p^+-type semiconductor layer 57 for pixel isolation. It is noted that reference numerals 50 and 59 each denote a SiO_2 film, and that a Si_3N_4 film(not shown) is provided between the SiO_2 film 50 and the transfer electrode 58. The FP well 53 is set approximately to a concentration of dopants of 5×10^{14} cm^{-3} and a thickness of 3 μm, perfectly depleted due to the low concentration of dopants. Accordingly, excess charges generated in the photoelectric conversion section 21 will overflow beyond the barrier of the depleted FP well 53 toward the n-type semiconductor substrate 51 (vertical overflow drain structure).

[0006] Meanwhile, between the n-type semiconductor layer 54 of the vertical transfer section 22 and the n-type substrate 51 is provided the p-type semiconductor layer 55, which is thicker in dopant level than the FP well 53, for preventing inflow and outflow of charges. Further, although not shown in Fig. 8, the aforementioned horizontal transfer section and the floating diffusion layer are, in general, also formed on the p-type semiconductor layer 55 within the FP well 53.

[0007] Fig. 6 shows the planar layout of the charge detecting section 24 in the vicinity of a floating diffusion layer 31 in the vertical overflow drain structure. The floating diffusion layer 31 is connected to a metal wiring 33 at a contact 32, and the metal wiring 33 in turn is connected to a gate electrode of the first-stage source follower driver transistor T1 at a contact 34. Normally, the photoelectric conversion section (not shown in Fig. 6), the vertical transfer section (not shown in Fig. 6), the horizontal transfer section 23, an output gate 25, the floating diffusion layer 31, and the reset transistor TR are formed within the FP well 53 on the n-type semiconductor substrate 51 shown in Fig. 8. Meanwhile, as shown in Fig. 6, the first-stage source follower driver transistor T1 is formed within another deep p-type well more heavily doped and formed deeper than the FP well 53 (hereinafter, referred to as "DP well") for preventing charges from flowing into the source and drain regions from the n-type semiconductor substrate. As a result, the FP well and the DP well are adjoining to each other by the ends at a boundary 35.

[0008] Fig. 7 shows a section of the first-stage source follower driver transistor T1 (taken from a line S - D in Fig. 6). In the figure, a DP well 42 is formed on an n-type semiconductor substrate 41, the DP well 42 having a gate electrode 48, an n-type source 49a, and a drain 49b formed therein to make up the transistor T1. The source 49a and the drain 49b are formed in some self-alignment fashion with respect to the gate electrode 48. It is to be noted that a Si_3N_4 film(not shown) is provided

between the SiO_2 film 50 and the gate electrode 48. Also, as disclosed in Japanese Patent Laid-Open Publication Hei 1-283870 (1989), a lightly doped region may be provided between the gate electrode 48 and the drain 49b to reduce the capacity between the gate electrode 48 and the drain 49b.

[0009] As one method for enhancing the sensitivity of the solid state imaging device, charge-to-voltage conversion efficiency of the charge detecting section 24 as shown in Fig. 5 may be elevated. If the amount of charges transferred to the floating diffusion layer (a cathode side portion of diode D1) is Q, total capacity relative to the floating diffusion layer is C, and gain of the source follower circuit is G, then the output voltage V can be represented as $V = G \cdot Q/C$. Also, the total capacity C contains, as capacity components, a junction capacity C1 between the floating diffusion layer and the well having the floating diffusion layer provided therein, a capacity C2 between the floating diffusion layer and the gate of the reset transistor TR adjoining thereto, a capacity C3 between the floating diffusion layer and the output gate 25 adjoining thereto, a capacity C4 had by an interconnection between the floating diffusion layer and the gate of the first-stage source follower driver transistor T1 (including capacity between interconnections, capacity between interconnections and semiconductor substrate, and capacity between gate and channel of the first-stage source follower driver transistor), and a capacity C5 between gate and drain of the first-stage source follower driver transistor. Accordingly, the total capacity C can be represented as $C = C1 + C2 + C3 + C4 + C5$, so that these capacities may be reduced to enhance the charge-to-voltage conversion efficiency.

[0010] The above-described prior art structure would require such an arrangement that the floating diffusion layer 31 be separated sufficiently apart from the boundary 35 between FP and DP wells and besides that the first-stage source follower driver transistor T1 be separated sufficiently apart from the boundary 35 between FP and DP wells. More specifically, since the two kinds of wells would diffuse through heat treatment, after ion implantation, to stretch laterally, the DP well would affect the characteristics of the reset transistor TR, the horizontal transfer section 23, the output gate 25, and the floating diffusion layer 31, while the FP well would affect the characteristics of the first-stage source follower driver transistor T1. Due to this, the boundary 35 between the DP well and the FP well needs to be separated sufficiently apart from both the floating diffusion layer 31 and the first-stage source follower driver transistor T1. Of course, the boundary 35 needs to be separated also from the reset transistor TR, the horizontal transfer section 23, and the output gate 25, but these do not matter in terms of layout. In fact, as shown in Fig. 9, at the boundary 35 between the FP well and the DP well, a dopant profile varies laterally over a width of about 10 μm. Therefore, in order to make the concentration of dopants constant within each of the FP well 53 and the DP well 42, and to thereby obtain stable characteristics, the distance between the floating diffusion layer 31 and the first-stage source follower driver transistor T1 as shown in Fig. 6 needs to be at least 10 μm or so. As a result of this, in the conventional structure, the interconnection 33 that connects the floating diffusion layer 31 and the gate of the first-stage source follower driver transistor T1 would be lengthened, so that an interconnection capacity C4 (more precisely, a capacity between interconnections and a capacity between the interconnection and semiconductor substrate, out of the C4) would result in a large one. For this reason, the charge-to-voltage conversion efficiency of the charge detecting section 24 would lower, causing its sensitivity to also lower, disadvantageously.

[0011] Also, there has been another problem that the capacity C5 between gate and drain of the first-stage source follower driver transistor T1 is too large.

[0012] Further, due to conduction by punch-through between source and drain of the first-stage source follower driver transistor Tl, gate length of the transistor could not be shortened, so that the capacity between gate and channel of the first-stage source follower driver transistor T1 out of the interconnection capacity C4 could not be reduced, as a further problem.

[0013] Furthermore, due to concentration of electric fields in the vicinity of the drain of the first-stage source follower driver transistor T1 there would be generated electron and hole pairs by the impact ionization phenomenon, which would cause great noise.

[0014] JP 5063177 discloses a solid state imaging device according to the preamble of claim 1. More particularly, it discloses a CCD image sensor with a source follower circuit. The source and drain regions of a transistor in the source follower circuit and a floating diffusion layer are formed in the same impurity region.

[0015] JP 60160659 relates to a solid state image pickup device having a CCD section in a first well and a signal output circuit in a second well.

SUMMARY OF THE INVENTION

[0016] It is desirable to provide a solid state imaging device which solves the above problems of the prior art without involving any complex processes of fabrication and yet which exhibits high-sensitivity and low-noise characteristics.

[0017] The present invention provides a solid state imaging device as set out in claim 1.

[0018] In the solid state imaging device, the channel, source, and drain regions of the output transistor are provided within the same well as the floating diffusion layer is provided within. Therefore, the output transistor and the floating diffusion layer may be made closest to each other as far as the design rules permit or as fine machining permits. In such a case, length of the interconnection that connects the floating diffusion layer and the gate electrode of the output transistor is shortened

so that capacity had by the interconnection (more precisely, a capacity between interconnections and a capacity between an interconnection and the semiconductor substrate) can be reduced. Accordingly, the solid state imaging device is improved in sensitivity, compared with the prior art. Further, the output transistor (generally, forming a source follower circuit) is improved in gain by being provided within a thinly doped well.

[0019] Also, since the fifth semiconductor layer of the second conductive type which is higher in concentration of dopants than the well is provided under the source and drain regions of the output transistor, charges are prevented from injection from the semiconductor substrate into the source and drain regions and from outflow from the source region to the semiconductor substrate. As a result, a vertical overflow drain structure is formed by the output transistor within the well. Besides, since the conduction by punch through between source and drain is suppressed by the fifth semiconductor layer, gate length of the output transistor can be shortened. As a result, out of the capacities had by the interconnection that connects the floating diffusion layer and the gate electrode of the output transistor, the capacity between the gate electrode and channel can be reduced. Accordingly, the solid state imaging device can be further improved in sensitivity.

[0020] Further, in a solid state imaging device of another embodiment, the fifth semiconductor layer and the third semiconductor layer are the same layer.

[0021] In the solid state imaging device of the embodiment, since the fifth semiconductor layer and the third semiconductor layer are of the same layer, they are formed at the same time. Accordingly, there will be involved no complex processes for fabrication of the solid state imaging device.

[0022] In a solid state imaging device of an embodiment, the source and drain regions of the output transistor are comprised of a sixth semiconductor layer of the first conductive type, and a seventh semiconductor layer of the first conductive type which is provided under the sixth semiconductor layer and on a gate side and is thinner in concentration of dopants than the sixth semiconductor layer.

[0023] In the solid state imaging device of the embodiment, a capacity between the gate electrode and drain of the output transistor is reduced by virtue of the thinly doped seventh semiconductor layer. Accordingly, the solid state imaging device can be further improved in sensitivity. Further, concentration of electric fields in the vicinity of the drain can be relaxed by the seventh semiconductor layer, whereby electron and hole pairs can be prevented from occurring due to an impact ionization phenomenon. As a result, noise of the solid state imaging device can be reduced.

[0024] In a solid state imaging device of an embodiment, the second semiconductor layer and the seventh semiconductor layer are the same layer.

[0025] In the solid state imaging device of that embodiment, since the second semiconductor layer and the seventh semiconductor layer are of the same layer, they are formed at the same time. Accordingly, there will be involved no complex processes for fabrication of the solid state imaging device.

[0026] The present invention also provides a method of fabricating a solid state imaging device as set out in claim 5.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Fig. 1(a) is a view showing a structure in section of a first-stage source follower driver transistor of a solid state imaging device according to an embodiment of the present invention;

Fig. 1(b) is a view showing a structure in section of a photoelectric conversion section, and a vertical transfer section of the solid state imaging device;

Fig. 1(c) is a sectional view of a charge detecting section of the solid state imaging device;

Fig. 2 is a plan view showing the charge detecting section of the solid state imaging device;

Figs. 3(a-1), 3(a-2), 3(b-1), 3(b-2), 3(c-1), 3(c-2), 3(d-1), 3(d-2), 3(e-1), 3(e-2) are views showing a fabrication process of the solid state imaging device;

Fig. 4 is a chart showing input and output characteristics of a source follower circuit;

Fig. 5 is a view showing an overall construction of the above embodiment and the prior art solid state imaging device;

Fig. 6 is a plan view showing a charge detecting section of the prior art solid state imaging device in the vicinity of a floating diffusion layer;

Fig. 7 is a view showing a structure in section of a first-stage source follower driver transistor of the prior art solid state imaging device;

Fig. 8 is a view showing the structure in section of a photoelectric conversion section and a vertical transfer section of the prior art solid state imaging device; and

Fig. 9 is a chart showing a dopant profile at the boundary between FP well and DP well.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] The solid state imaging device of the present invention is described hereinbelow in more detail with reference to an embodiment thereof.

[0029] The following description is made by way of example in the case of an interline transfer type area image sensor having an equivalent circuit identical to the

equivalent circuit shown in Fig. 5.

[0030] Fig. 1(a) shows a section of a first-stage source follower driver transistor T1 in a solid state imaging device of one embodiment of the invention, Fig. 1(b) shows a section of a photoelectric conversion section 21 and a vertical transfer section 22 of the solid state imaging device, and Fig. 1(c) shows a section of part of a charge detection section. In the figures, there are shown an n-type semiconductor substrate 11, a FP(flat p-type) well 13, an n-type semiconductor layer 14, a p-type semiconductor layer 15, an n-type semiconductor layer 16, which constitutes part of the photoelectric conversion section 21, a p^+-type semiconductor layer 17 for pixel isolation, an electrode 18, a source 19a being a heavily doped n-type semiconductor layer, a drain 19b being a heavily doped n-type semiconductor layer, a channel 19c, and a light-screening film 20. In this arrangement, the p-type semiconductor layer 15 is thicker in concentration of dopants than the FP well 13; the p-type semiconductor layer 15 is thinner in concentration of dopants than the n-type semiconductor layer 14; and the drain 19b is thicker in concentration of dopants than the n-type semiconductor layer 14. Further, SiO_2 films are designated by numerals 10 and 29, and a Si_3N_4 film(not shown) is provided between the SiO_2 film 10 and each electrode 18.

[0031] In this solid state imaging device, the relatively thinly doped FP well 13 as shown in Figs. 1(a), 1(b) and 1(c) is provided with the first-stage source follower driver transistor T1, a floating diffusion layer 51 (cathode side portion of diode D1 in Fig. 5), the photoelectric conversion section 21, and the vertical transfer section 22, all of which are shown in Figs. 2 and 5. Fig. 2 in a plan view showing the charge detection section 54, and Fig. 1(c) is a sectional view taken a dot-dash line C-C in Fig. 2. This arrangement that the first-stage source follower driver transistor T1 and the floating diffusion layer 51 and others are provided within the common well 13 allows the first-stage source follower driver transistor T1 to be made closest to a reset transistor TR, an output gate 25, and the floating diffusion layer 51 as far as the design rules permit or as fine machining permits. As a result of this, an interconnection capacity C4 between the floating diffusion layer and the gate of the first-stage source follower driver transistor T1 connected thereto (more precisely, a capacity between interconnections and a capacity between an interconnection and the semiconductor substrate) can be reduced. Accordingly, the solid state imaging device can be improved in sensitivity, compared with the prior art.

[0032] Further, the n-type semiconductor layer 14 of the vertical transfer section 22 as shown in Fig. 1(b) serves as the transfer section, while the p-type semiconductor layer 15 of the vertical transfer section 22 serves to prevent injection of charges and inflow of smear component charges from the n-type semiconductor substrate 11 into the n-type semiconductor layer 14. Also, the n-type semiconductor layer 14 of the first-stage source follower driver transistor T1 as shown in Fig. 1 (a) reduces a capacity C5 between gate and drain of the transistor T1. Accordingly, the solid state imaging device can be further improved in sensitivity. The n-type semiconductor layer 14 further serves to relax concentration of electric fields in the vicinity of the drain, to prevent occurrence of electron and hole pairs due to an impact ionization phenomenon, and to reduce noise. The p-type semiconductor layer 15 of the first-stage source follower driver transistor T1 prevents injection of charges from the n-type semiconductor substrate 11 into the source 19a and the drain 19b, or overflow of charges from the source 19a to the n-type semiconductor substrate 11. As a result, the first-stage source follower driver transistor T1 can be formed within the FP well 13 of such a low concentration of dopants as to allow formation of a vertical overflow drain. Besides the p-type semiconductor layer 15 serves to suppress conduction by punch through between source and drain, allowing the gate length of the transistor T1 to be shortened. As a result of this, the capacity between gate and channel out of the interconnection capacity C4 can be reduced. Accordingly, the solid state imaging device can be further improved in sensitivity.

[0033] As understood from Fig. 2, the charge detection section 54 of this solid state imaging device has the same elements as those in Fig. 6. Therefore, the same elements are shown by the same reference numerals as those in Fig. 6, and description thereof is omitted

[0034] The solid state imaging device is fabricated in the following manner. First, as shown in Figs. 3 (a-1) and 3 (a-2), a FP well (concentration of dopants: 5×10^{14} cm^{-3}; thickness: approx. 3 μm) 13 is formed on the n-type semiconductor substrate 11 by a p-type ion implantation process and a diffusion process.

[0035] Next, as shown in Figs. 3 (b-1) and 3 (b-2), with resist R applied to a surface, photolithography process is performed for patterning to form the source and drain regions of the first-stage source follower driver transistor T1 and the vertical transfer section 22. Subsequently, the n-type semiconductor layer 14 and the p-type semiconductor layer 15 are formed by simultaneously implanting ions both in the source and drain regions of the first-stage source follower driver transistor T1 and in the vertical transfer section 22. Thus, the p-type semiconductor layer 15 is formed at one time for both the first-stage source follower driver transistor T1 and the vertical transfer section 22 , while the n-type semiconductor layer 14 is formed at one time for both the first-stage source follower driver transistor T1 and the vertical transfer section 22. In this process, the n-type semiconductor layer 14 is arranged to have a surface density of 2×10^{17} cm^{-3} and a junction depth of 0.4 μm while the p-type semiconductor layer 15 is arranged to have a peak concentration of 3×10^{16} cm^{-3} and a peak depth of 0.9 μm. Since the n-type semiconductor layer 14 and the p-type semiconductor layer 15 are respectively formed by implanting ions at the same time both in the

source and drain regions of the first-stage source follower driver transistor T1 and in the vertical transfer section 22, there will be involved no complex processes in fabrication.

[0036] Then, as shown in Figs. 3 (c-1) and 3 (c-2), gate oxidation is carried out to form a SiO_2 film 10 and a Si_3N_4 film(not shown), which is followed by patterning and ion implantation by which a p^+-type semiconductor layer 17 for pixel isolation is formed. Also, polysilicon as the material for the gate electrode is deposited by a CVD process or the like. Then this is followed by patterning, where the polysilicon and the Si_3N_4 film are etched in succession. By this process, a transfer electrode 18 of the vertical transfer section 22 and the horizontal transfer section (not shown) and a gate electrode 18 of the first-stage source follower driver transistor are formed. It is noted that the gate electrodes 18 are connected to the floating diffusion layer in a later process.

[0037] Then, as shown in Fig. 3 (d-2), the n-type semiconductor layer 16 is formed in the photoelectric conversion section 21 by patterning and ion implantation. Thereafter, as shown in Figs. 3 (d-1) and 3 (d-2), the source 19a and drain 19b, which are each a heavily doped n-type semiconductor layer, are formed by application of resist R', patterning, and ion implantation. In this example, the drain 19b is formed so as to be spaced from the gate electrode 18 by 0.4 μm. As a result of this, the capacity C5 between gate and drain can be further reduced, compared with the case where both the source 19a and the drain 19b are formed in some self alignment fashion with respect to the gate electrode 18.

[0038] Next, as shown in Figs. 3 (e-1) and 3 (e-2), the p-type semiconductor layer 17' is formed on the surface of the n-type semiconductor layer 16 in self alignment with respect to the gate electrode 18 for the purpose of reducing dark current of the photoelectric conversion section 21.

[0039] Thereafter, the light-screening film 20 is provided to the vertical transfer section 22 by a known method, thus completing the fabrication of the solid state imaging device with high sensitivity and low noise.

[0040] In fact, the capacity C4 (including the interconnection capacity, the capacity between the interconnection and semiconductor substrate, and capacity between gate and channel of the first-stage source follower driver transistor T1) and the capacity C5 was reduced in their sum total by 35%. In proportion to this, the solid state imaging device was improved in sensitivity.

[0041] In this embodiment, the first-stage source follower driver transistor T1, the photoelectric conversion section 21, the vertical transfer section 22, the horizontal transfer section 23, and the floating diffusion layer all have been formed on the FP well. However, all of these may conversely be formed on the DP well as was stated in the prior art. Nevertheless, since the FP well is generally lower in concentration than the DP well, a back gate effect is suppressed in the case of formation on the FP well, compared with that on the DP well, which contributes to increase in the gain of the source follower circuit. Accordingly, the present embodiment arrangement is preferred.

[0042] It is to be noted that the present invention may be changed and modified in various ways within the scope of the appended claims, thus not limited to the above embodiment.

[0043] As apparent from the above description, the solid state imaging device of the present invention comprises a semiconductor substrate of a first conductive type; a well of a second conductive type provided on the semiconductor substrate, the second conductive type of the well being the conductive type reverse to the first conductive type of the semiconductor substrate; a photoelectric conversion section having a first semiconductor layer of the first conductive type provided within the well and serving for converting incident light into signal charges at a junction plane between the first semiconductor layer and the well; a transfer section having a second semiconductor layer of the first conductive type provided within the well and a third semiconductor layer of the second conductive type provided under the second semiconductor layer and thicker in concentration of dopants than the well, and serving for transferring signal charges received from the photoelectric conversion section through the second semiconductor layer; a floating diffusion layer being comprised of a fourth semiconductor layer of the first conductive type provided within the well and serving for receiving the signal charges outputted by the transfer section; and an output transistor having a gate electrode connected to the floating diffusion layer via an interconnection and serving for outputting a signal corresponding to a potential of the floating diffusion layer, wherein channel, source, and drain regions of the output transistor are provided within the well. Therefore, the output transistor and the floating diffusion layer may be made closest to each other as far as the design rules permit or as fine machining permits. Accordingly, length of the interconnection that connects the floating diffusion layer and the gate electrode of the output transistor can be shortened so that capacity had by the interconnection (more precisely, a capacity between interconnections, and a capacity between interconnection and the semiconductor substrate) can be reduced. Accordingly, the solid state imaging device can be improved in sensitivity, compared with the prior art. Further, the output transistor (generally, forming a source follower circuit) can be improved in gain by being provided within a thinly doped well.

[0044] Also, the solid state imaging device of the invention is provided with a fifth semiconductor layer of the second conductive type which is higher in concentration of dopants than the well, under the source and drain regions of the output transistor. Therefore, charges can be prevented from injection from the semiconductor substrate into the source and drain regions or from overflow from the source region to the semiconductor substrate, allowing a vertical overflow drain struc-

ture to be formed by the output transistor within the well. Moreover, conduction by punch through between source and drain is suppressed by the fifth semiconductor layer, so that gate length of the output transistor can be shortened. As a result, out of the capacities had by the interconnection that connects the floating diffusion layer and the gate electrode of the output transistor, the capacity between the gate electrode and channel can be reduced. Accordingly, the solid state imaging device can be further improved in sensitivity.

[0045] Further, the solid state imaging device of an embodiment is so arranged that the fifth semiconductor layer and the third semiconductor layer are the same layer, and therefore formed at the same time. Accordingly, the process of fabricating the solid state imaging device can be prevented from being complicated.

[0046] Further, the solid state imaging device of an embodiment is so arranged that the source and drain regions of the output transistor are comprised of a sixth semiconductor layer of the first conductive type, and a seventh semiconductor layer of the first conductive type which is provided under the sixth semiconductor layer and on the gate side and is thinner in concentration of dopants than the sixth semiconductor layer. In such a case, a capacity between the gate electrode and drain of the output transistor can be reduced by virtue of the thinly doped seventh semiconductor layer. Accordingly, the solid state imaging device can be further improved in sensitivity. Further, concentration of electric fields in the vicinity of the drain can be relaxed by the seventh semiconductor layer, whereby electron and hole pairs can be prevented from occurring due to the impact ionization phenomenon. As a result, the noise of the solid state imaging device can be reduced.

[0047] Yet further, the solid state imaging device of an embodiment is so arranged that the second semiconductor layer and the seventh semiconductor layer are of the same layer. Therefore, the layers are formed at the same time. Accordingly, the process of fabricating the solid state imaging device can be prevented from being complicated.

[0048] The invention being thus described, it will be obvious that the same may be varied in many ways.

Claims

1. A solid state imaging device comprising:

a semiconductor substrate (11) of a first conductive type;
a well (13) of a second conductive type provided on the semiconductor substrate (11), the second conductive type of the well (13) being the conductive type reverse to the first conductive type of the semiconductor substrate (11);
a photoelectric conversion section (21) having a first semiconductor layer (16) of the first conductive type provided within the well (13) and serving for converting incident light into signal charges at a junction plane between the first semiconductor layer (16) and the well (13);
a transfer section (22) having a second semiconductor layer (14) of the first conductive type provided within the well (13) and a third semiconductor layer (15) of the second conductive type provided under the second semiconductor layer (14) and higher in concentration of dopants than the well (13), and serving for transferring signal charges received from the photoelectric conversion section (21) through the second semiconductor layer (14);
a floating diffusion layer (51) comprising a fourth semiconductor layer (51) of the first conductive type provided within the well (13) and serving for receiving the signal charges outputted by the transfer section (22); and
an output transistor (T1) having a gate electrode (18) connected to the floating diffusion layer (51) via an interconnection (33) and serving for outputting a signal corresponding to a potential of the floating diffusion layer (51),
wherein channel, source, and drain regions (19c, 19a, 19b and 14) of the output transistor (T1) are provided within the well (13), characterised in that under the source and drain regions (19a, 19b, 14) of the output transistor (T1) there is further provided a fifth semiconductor layer (15) of the second conductive type which is higher in concentration of dopants than the well (13).

2. A solid state imaging device as claimed in claim 1, wherein the fifth semiconductor layer (15) and the third semiconductor layer (15) of the transfer section (22) are the same layer.

3. A solid state imaging device as claimed in claim 1 or claim 2, wherein the source and drain regions (19a, 19b and 14) of the output transistor (T1) comprise a sixth semiconductor layer (19a, 19b) of the first conductive type, and a seventh semiconductor layer (14) of the first conductive type which is provided under the sixth semiconductor layer (19a, 19b) and on a gate side and is thinner in concentration of dopants than the sixth semiconductor layer (19a, 19b).

4. A solid state imaging device as claimed in claim 3, wherein the second semiconductor layer (14) of the transfer section and the seventh semiconductor layer (14) are the same layer.

5. A method of fabricating a solid state imaging device comprising providing

a semiconductor substrate (11) of a first conductive type;
a well (13) of a second conductive type provided on the semiconductor substrate (11), the second conductive type of the well (13) being the conductive type reverse to the first conductive type of the semiconductor substrate (11);
a photoelectric conversion section (21) having a first semiconductor layer (16) of the first conductive type provided within the well (13) and serving for converting incident light into signal charges at a junction plane between the first semiconductor layer (16) and the well (13);
a transfer section (22) having a second semiconductor layer (14) of the first conductive type provided within the well (13) and a third semiconductor layer (15) of the second conductive type provided under the second semiconductor layer (14) and higher in concentration of dopants than the well (13), and serving for transferring signal charges received from the photoelectric conversion section (21) through the second semiconductor layer (14);
a floating diffusion layer (51) comprising a fourth semiconductor layer (51) of the first conductive type provided within the well (13) and serving for receiving the signal charges outputted by the transfer section (22); and
an output transistor (T1) having a gate electrode (18) connected to the floating diffusion layer (51) via an interconnection (33) and serving for outputting a signal corresponding to a potential of the floating diffusion layer (51),
wherein channel, source, and drain regions (19c, 19a, 19b and 14) of the output transistor (T1) are provided within the well (13), characterised in that the method comprises providing under the source and drain regions (19a, 19b, 14) of the output transistor (T1) a fifth semiconductor layer (15) of the second conductive type which is higher in concentration of dopants than the well (13).

6. A method as claimed in claim 5 wherein the third and fifth semiconductor layers (15) are formed simultaneously.

7. A method as claimed in claim 6 wherein the third and fifth semiconductor layers (15) are formed by implanting ions of dopants of the second conductive type in an ion implantation process.

8. A method as claimed in any one of claims 5 to 7 for fabricating a device as claimed in claim 3 wherein the second and seventh semiconductor layers (14) are formed simultaneously.

9. A method as claimed in claim 8 wherein the second and seventh semiconductor layers (14) are formed by implanting ions of dopants of the first conductive type in an ion implantation process.

Patentansprüche

1. Festkörper-Bildaufnehmer mit:

- einem Halbleitersubstrat (11) von erstem Leitungstyp;
- einer Wanne (13) von zweitem Leitungstyp, die auf dem Halbleitersubstrat (11) vorhanden ist, wobei der zweite Leitungstyp der Wanne (13) derjenige Leitungstyp ist, der zum ersten Leitungstyp des Halbleitersubstrats (11) umgekehrt ist;
- einem photoelektrischen Wandlerabschnitt (21) mit einer ersten Halbleiterschicht (16) vom ersten Leitungstyp, der innerhalb der Wanne (13) vorhanden ist und dazu dient, ein fallendes Licht an einer Übergangsebene zwischen der ersten Halbleiterschicht (16) und der Wanne (13) in Signalladungen umzusetzen;
- einem Übertragungsabschnitt (22) mit einer zweiten Halbleiterschicht (14) vom ersten Leitungstyp innerhalb der Wanne (13) und einer dritten Halbleiterschicht (15) vom zweiten Leitungstyp unter der zweiten Halbleiterschicht (14) und mit höherer Dotierstoffkonzentration als der der Wanne (13), und der dazu dient, vom photoelektrischen Wandlerabschnitt (21) empfangene Signal ladungen durch die zweite Halbleiterschicht (14) zu übertragen;
- einer potentialungebundenen Diffusionsschicht (51) mit einer vierten Halbleiterschicht (51) vom ersten Leitungstyp innerhalb der Wanne (13), die dazu dient, die vom Übertragungsabschnitt (22) ausgegebenen Signal ladungen zu empfangen; und
- einem Ausgangstransistor (T1) mit einer Gateelektrode (18), die über eine Verdrahtung (33) mit der potentialungebundenen Diffusionsschicht (51) verbunden ist und dazu dient, ein Signal entsprechend dem Potential der potentialungebundenen Diffusionsschicht (51) auszugeben;
- wobei der Kanalbereich, der Sourcebereich und der Drainbereich (19c, 19a, 19b und 14) des Ausgangstransistors (T1) innerhalb der Wanne (13) vorhanden sind; **dadurch gekennzeichnet, dass** unter dem Source- und dem Drainbereich (19a, 19b, 14) des Ausgangstransistors (T1) ferner eine fünfte Halbleiterschicht (15) vom zweiten Leitungstyp vorhanden ist, die höhere Dotierstoffkonzentration als die Wanne (13) aufweist.

2. Festkörper-Bildaufnehmer nach Anspruch 1, bei dem die fünfte Halbleiterschicht (15) und die dritte Halbleiterschicht (15) des Übertragungsabschnitts (22) dieselbe Schicht bilden.

3. Festkörper-Bildaufnehmer nach Anspruch 1 oder Anspruch 2, bei dem der Source- und der Drainbereich (19a, 19b und 14) des Ausgangstransistors (T1) eine sechste Halbleiterschicht (19a, 19b) vom ersten Leitungstyp sowie eine siebte Halbleiterschicht (14) vom ersten Leitungstyp aufweisen, die unter der sechsten Halbleiterschicht (19a, 19b) und auf einer Gateseite vorhanden ist und geringere Dotierstoffkonzentration als die sechste Halbleiterschicht (19a, 19b) aufweist.

4. Festkörper-Bildaufnehmer nach Anspruch 3, bei dem die zweite Halbleiterschicht (14) des Übertragungsabschnitts und die siebte Halbleiterschicht (14) dieselbe Schicht bilden.

5. Verfahren zum Herstellen eines Festkörper-Bildaufnehmers mit folgendem:

- einem Halbleitersubstrat (11) von erstem Leitungstyp;
- einer Wanne (13) von zweitem Leitungstyp, die auf dem Halbleitersubstrat (11) vorhanden ist, wobei der zweite Leitungstyp der Wanne (13) derjenige Leitungstyp ist, der zum ersten Leitungstyp des Halbleitersubstrats (11) umgekehrt ist;
- einem photoelektrischen Wandlerabschnitt (21) mit einer ersten Halbleiterschicht (16) vom ersten Leitungstyp, der innerhalb der Wanne (13) vorhanden ist und dazu dient, ein fallendes Licht an einer Übergangsebene zwischen der ersten Halbleiterschicht (16) und der Wanne (13) in Signalladungen umzusetzen;
- einem Übertragungsabschnitt (22) mit einer zweiten Halbleiterschicht (14) vom ersten Leitungstyp innerhalb der Wanne (13) und einer dritten Halbleiterschicht (15) vom zweiten Leitungstyp unter der zweiten Halbleiterschicht (14) und mit höherer Dotierstoffkonzentration als der der Wanne (13), und der dazu dient, vom photoelektrischen Wandlerabschnitt (21) empfangene Signal ladungen durch die zweite Halbleiterschicht (14) zu übertragen;
- einer potentialungebundenen Diffusionsschicht (51) mit einer vierten Halbleiterschicht (51) vom ersten Leitungstyp innerhalb der Wanne (13), die dazu dient, die vom Übertragungsabschnitt (22) ausgegebenen Signalladungen zu empfangen; und
- einem Ausgangstransistor (T1) mit einer Gateelektrode (18), die über eine Verdrahtung (33) mit der potentialungebundenen Diffusionsschicht (51) verbunden ist und dazu dient, ein Signal entsprechend dem Potential der potentialungebundenen Diffusionsschicht (51) auszugeben;
- wobei der Kanalbereich, der Sourcebereich und der Drainbereich (19c, 19a, 19b und 14) des Ausgangstransistors (T1) innerhalb der Wanne (13) vorhanden sind;

dadurch gekennzeichnet, dass bei diesem Verfahren unter dem Source- und dem Drainbereich (19a, 19b, 14) des Ausgangstransistors (T1) eine fünfte Halbleiterschicht (15) vom zweiten Leitungstyp hergestellt wird, die höhere Dotierstoffkonzentration als die Wanne (13) aufweist.

6. Verfahren nach Anspruch 5, bei dem die dritte und die fünfte Halbleiterschicht (15) gleichzeitig hergestellt werden.

7. Verfahren nach Anspruch 6, bei dem die dritte und die fünfte Halbleiterschicht (15) dadurch hergestellt werden, dass Dotierstoff ionen vom zweiten Leitungstyp bei einem Ionenimplantationsprozess implantiert werden.

8. Verfahren nach einem Ansprüche 5 bis 7 zum Herstellen eines Aufnehmers nach Anspruch 3, bei dem die zweite und die siebte Halbleiterschicht (14) gleichzeitig hergestellt werden.

9. Verfahren nach Anspruch 8, bei dem die zweite und die siebte Halbleiterschicht (14) dadurch hergestellt werden, dass Dotierstoff ionen vom ersten Leitungstyp bei einem Ionenimplantationsprozess implantiert werden.

Revendications

1. Dispositif de formation d'image à semi-conducteur comprenant:

un substrat en semi-conducteur (11) avec un premier type de conduction;
un caisson (13) avec un second type de conduction prévu sur le substrat en semi-conducteur (11), le second type de conduction du caisson (13) étant le type de conduction inverse au premier type de conduction du substrat en semi-conducteur (11);
une section de conversion photoélectrique (21) comportant une première couche de semi-conducteur (16) avec le premier type de conduction, prévue à l'intérieur du caisson (13) et servant à convertir une lumière incidente en des charges de signal au niveau d'un plan de jonction entre la première couche de semi-conduc-

teur (16) et le caisson (13);
une section de transfert (22) comportant une seconde couche de semi-conducteur (14) avec le premier type de conduction, prévue à l'intérieur du caisson (13), et une troisième couche de semi-conducteur (15) avec le second type de conduction, prévue sous la seconde couche de semi-conducteur (14) et ayant une concentration de dopants supérieure à celle du caisson (13), et servant à transférer des charges de signal reçues de la section de conversion photoélectrique (21) par l'intermédiaire de la seconde couche de semi-conducteur (14);
une couche de diffusion flottante (51) comprenant une quatrième couche de semi-conducteur (51) avec le premier type de conduction, prévue à l'intérieur du caisson (13) et servant à recevoir les charges de signal délivrées par la section de transfert (22); et
un transistor de sortie (T1) comportant une électrode de grille (18) connectée à la couche de diffusion flottante (51) par l'intermédiaire d'une interconnexion (33) et servant à délivrer un signal correspondant à un potentiel de la couche de diffusion flottante (51),
dans lequel des régions de canal, de source et de drain (19c, 19a, 19b, et, 14) du transistor de sortie (T1) sont prévues à l'intérieur du caisson (13), caractérisé en ce que sous les régions de source et de drain (19a, 19b, 14) du transistor de sortie (T1) est également prévue une cinquième couche de semi-conducteur (15) avec le second type de conduction qui a une concentration de dopants supérieure à celle du caisson (13).

2. Dispositif de formation d'image à semi-conducteur selon la revendication 1,

dans lequel la cinquième couche de semi-conducteur (15) et la troisième couche de semi-conducteur (15) de la section de transfert (22) sont constituées par la même couche.

3. Dispositif de formation d'image à semi-conducteur selon la revendication 1 ou 2,

dans lequel les régions de source et de drain (19a, 19b et 14) du transistor de sortie (T1) comprennent une sixième couche de semi-conducteur (19a, 19b) avec le premier type de conduction, et une septième couche de semi-conducteur (14) avec le premier type de conduction qui est prévue sous la sixième couche de semi-conducteur (19a, 19b) et sur un côté de grille et a une concentration de dopants inférieure à celle de la sixième couche de semi-conducteur (19a, 19b).

4. Dispositif de formation d'image à semi-conducteur selon la revendication 3,

dans lequel la seconde couche de semi-conducteur (14) de la section de transfert et la septième couche de semi-conducteur (14) sont constituées par la même couche.

5. Procédé pour fabriquer un dispositif de formation d'image à semi-conducteur comprenant la fourniture

d'un substrat en semi-conducteur (11) avec un premier type de conduction;
d'un caisson (13) avec un second type de conduction prévu sur le substrat en semi-conducteur (11), le second type de conduction du caisson (13) étant le type de conduction inverse au premier type de conduction du substrat en semi-conducteur (11);
d'une section de conversion photoélectrique (21) comportant une première couche de semi-conducteur (16) avec le premier type de conduction, prévue à l'intérieur du caisson (13) et servant à convertir une lumière incidente en des charges de signal au niveau d'un plan de jonction entre la première couche de semi-conducteur (16) et le caisson (13);
d'une section de transfert (22) comportant une seconde couche de semi-conducteur (14) avec le premier type de conduction, prévue à l'intérieur du caisson (13), et une troisième couche de semi-conducteur (15) avec le second type de conduction, prévue sous la seconde couche de semi-conducteur (14) et ayant une concentration de dopants supérieure à celle du caisson (13), et servant à transférer des charges de signal reçues de la section de conversion photoélectrique (21) par l'intermédiaire de la seconde couche de semi-conducteur (14);
d'une couche de diffusion flottante (51) comprenant une quatrième couche de semi-conducteur (51) avec le premier type de conduction, prévue à l'intérieur du caisson (13) et servant à recevoir les charges de signal délivrées par la section de transfert (22); et
d'un transistor de sortie (T1) comportant une électrode de grille (18) connectée à la couche de diffusion flottante (51) par l'intermédiaire d'une interconnexion (33) et servant à délivrer un signal correspondant à un potentiel de la couche de diffusion flottante (51),
dans lequel des régions de canal, de source et de drain (19c, 19a, 19b et 14) du transistor de sortie (T1) sont prévues à l'intérieur du caisson (13), caractérisé en ce que le procédé comprend la fourniture sous les régions de source et de drain (19a, 19b, 14) du transistor de sortie (T1) d'une cinquième couche de semi-conducteur (15) avec le second type de conduction qui a une concentration de dopants supérieure à

celle du caisson (13).

6. Procédé selon la revendication 5, dans lequel les troisième et cinquième couches de semi-conducteur (15) sont formées simultanément.

7. Procédé selon la revendication 6, dans lequel les troisième et cinquième couches de semi-conducteur (15) sont formées en implantant des ions de dopants du second type de conduction lors d'une opération d'implantation d'ions.

8. Procédé selon l'une quelconque des revendications 5 à 7 pour fabriquer un dispositif tel que revendiqué dans la revendication 3, dans lequel les seconde et septième couches de semi-conducteur (14) sont formées simultanément.

9. Procédé selon la revendication 8, dans lequel les seconde et septième couches de semi-conducteur (14) sont formées en implantant des ions de dopants du premier type de conduction lors d'une opération d'implantation d'ions.

Fig.1(a)

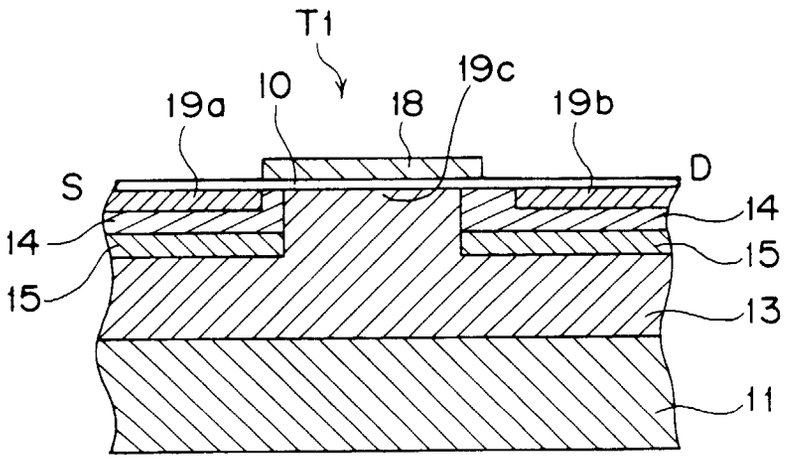

T1
19a
10
18
19c
19b
S
D
14
15
14
15
13
11

Fig.1(b)

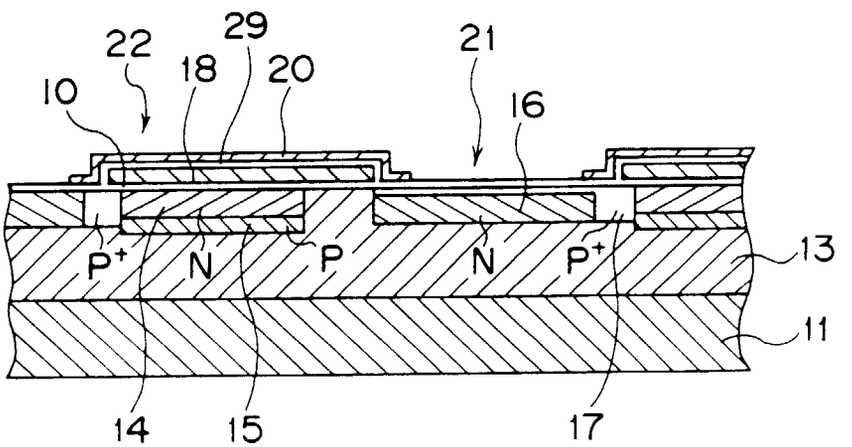

22
29
18
20
21
10
16
P+
N
P
N
P+
13
11
14
15
17

Fig. 1(c)

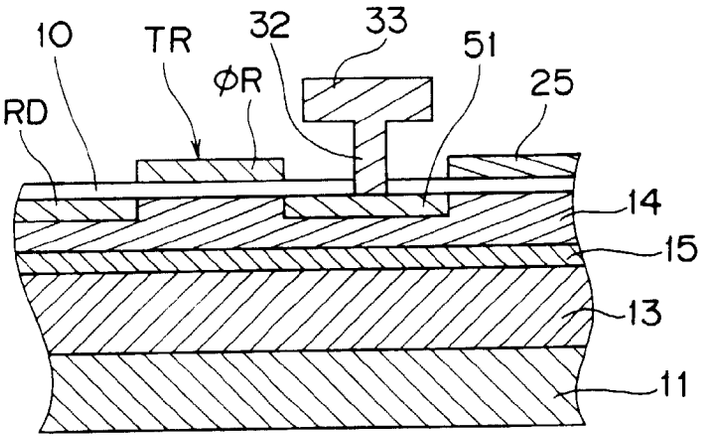
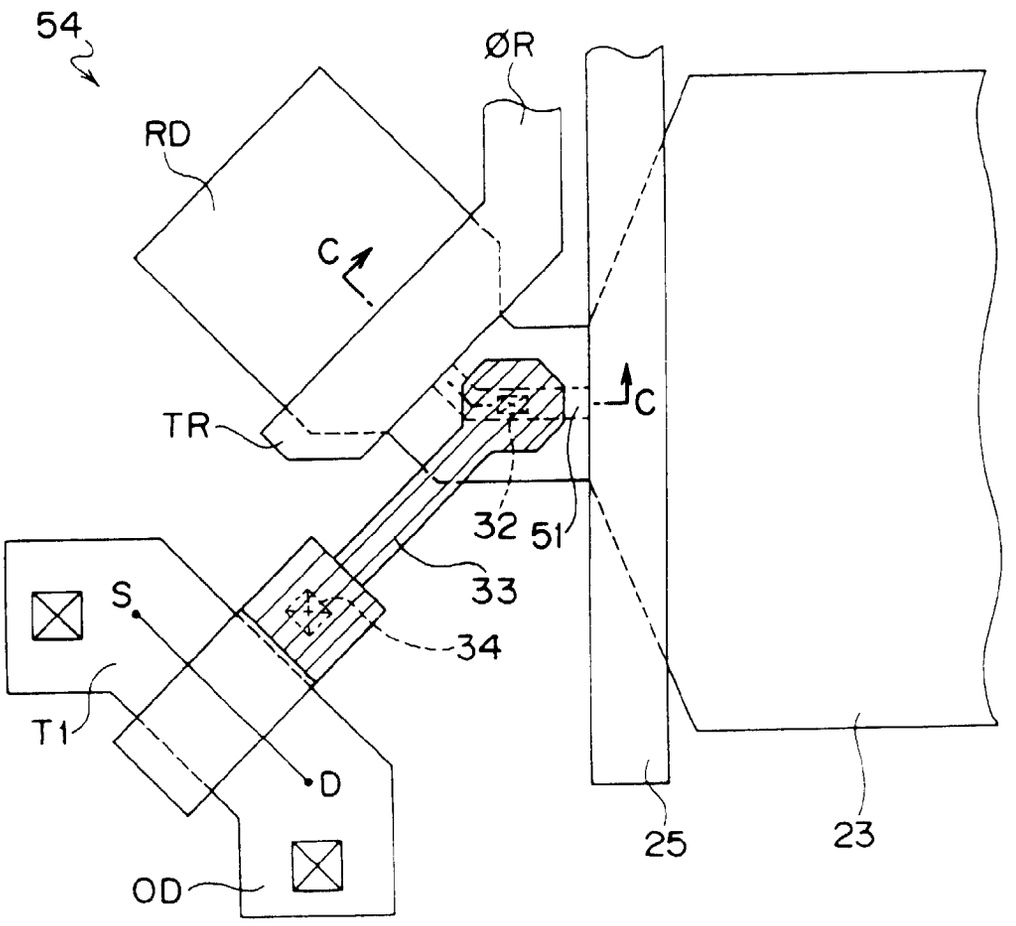

10
TR
32
33
51
25
RD
ØR
14
15
13
11

Fig. 2


54
ØR
RD
C
C
TR
32
51
33
34
S
T1
D
OD
25
23

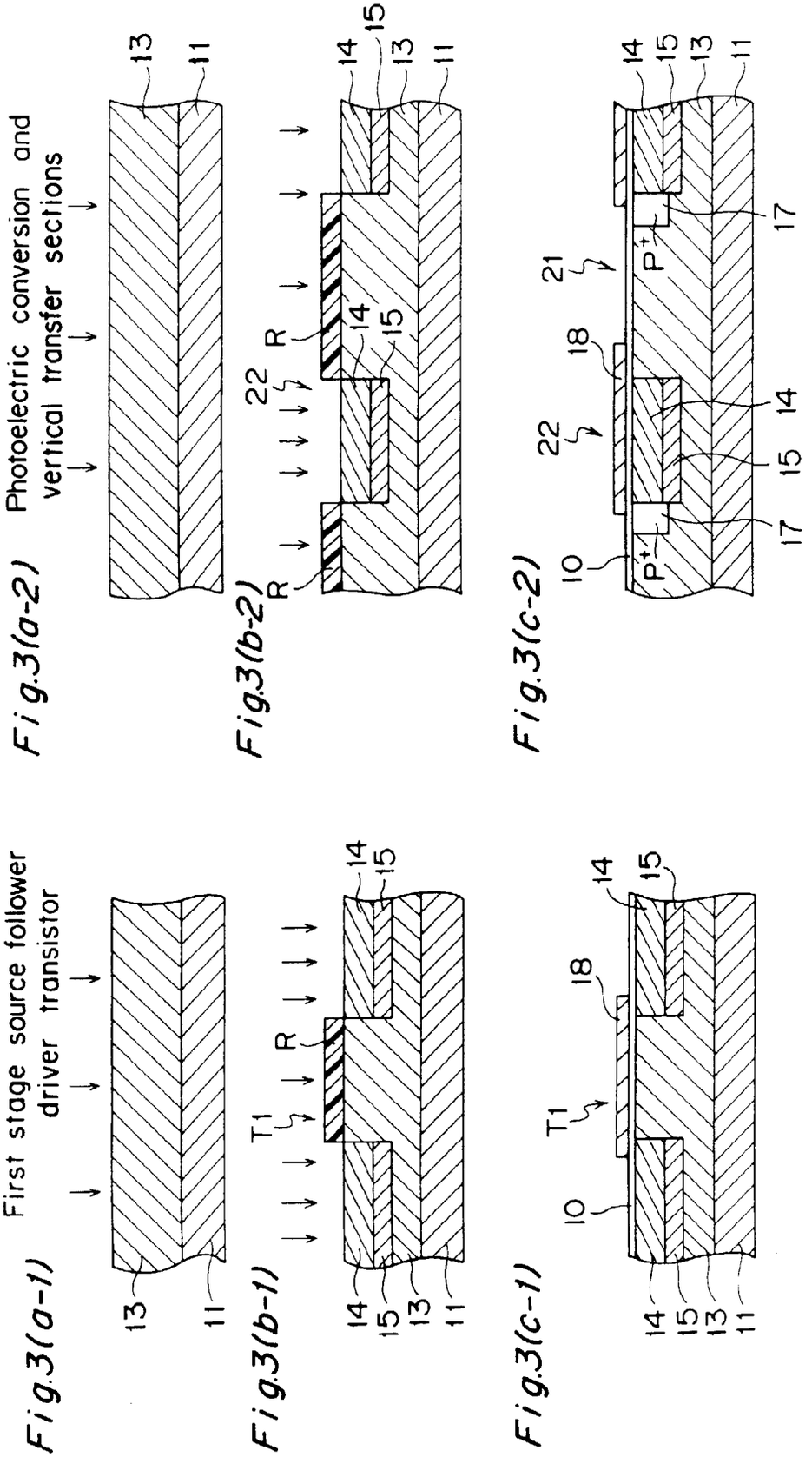


Fig.3(a-2)

Fig.3(b-2)

Fig.3(c-2)

Fig.3(a-1)

Fig.3(b-1)

Fig.3(c-1)

Fig.3(d-1) First stage source follower driver transister

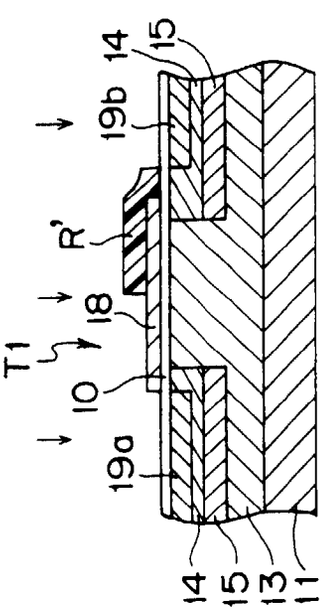


Fig.3(d-2) Photoelectric conversion and vertical transfer section

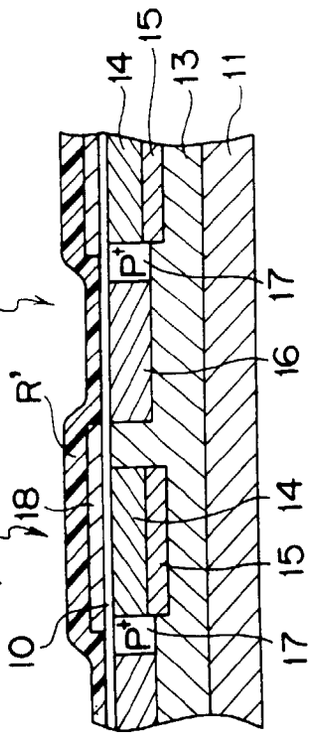


Fig.3(e-1)

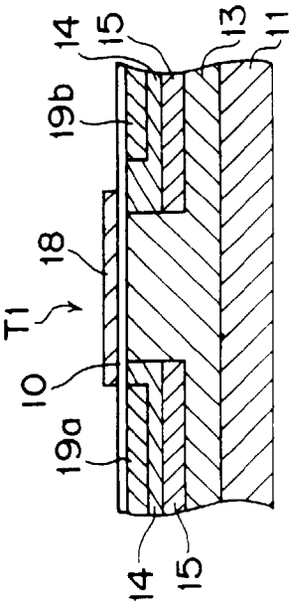


Fig.3(e-2)

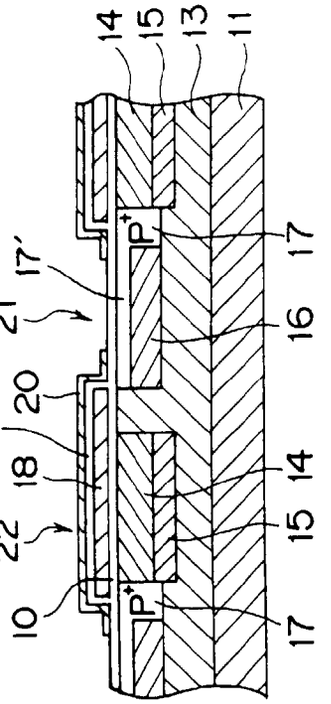


Fig.4

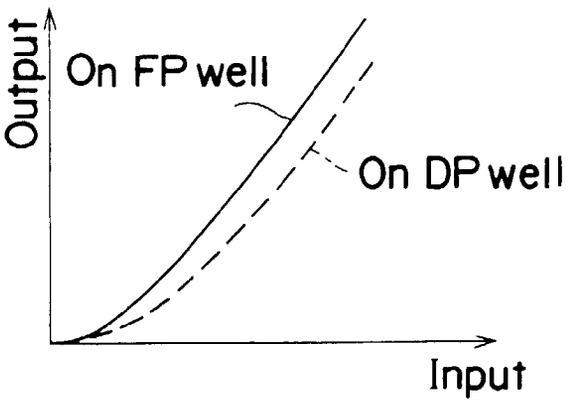


Fig.5 PRIOR ART

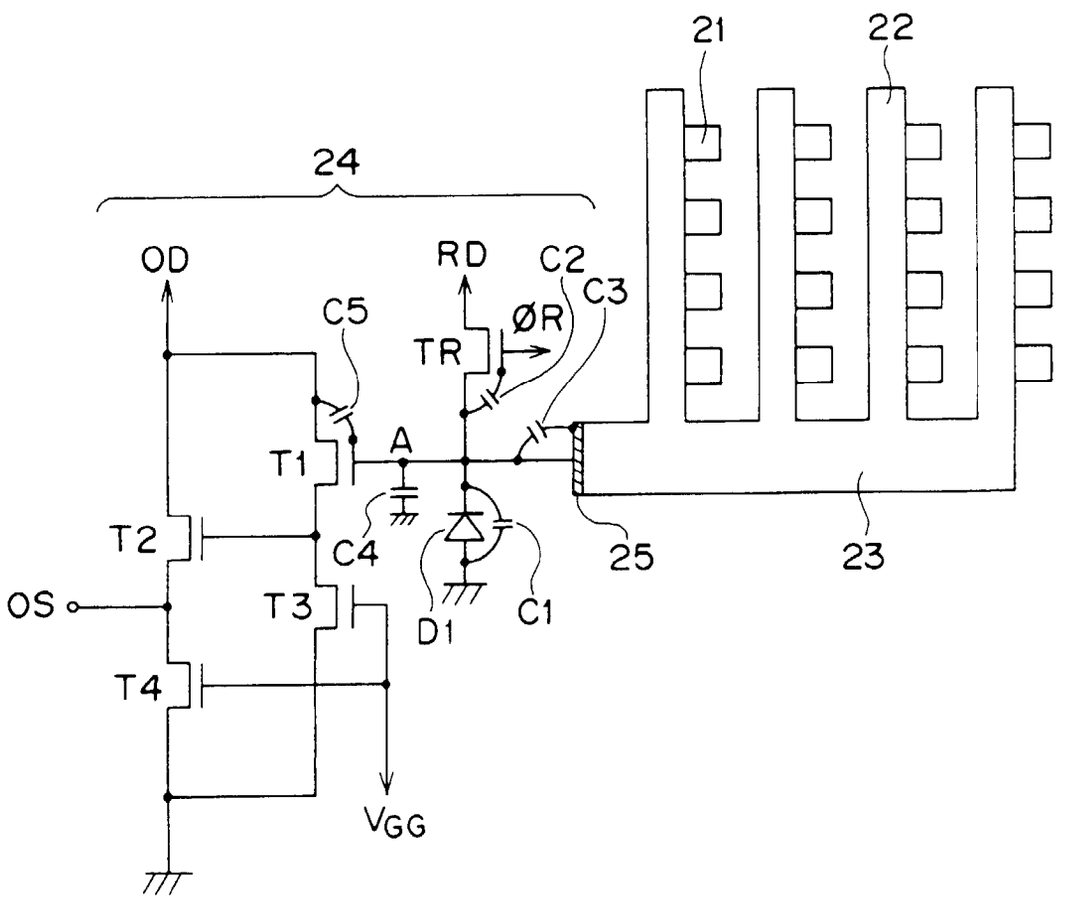


Fig.6 PRIOR ART

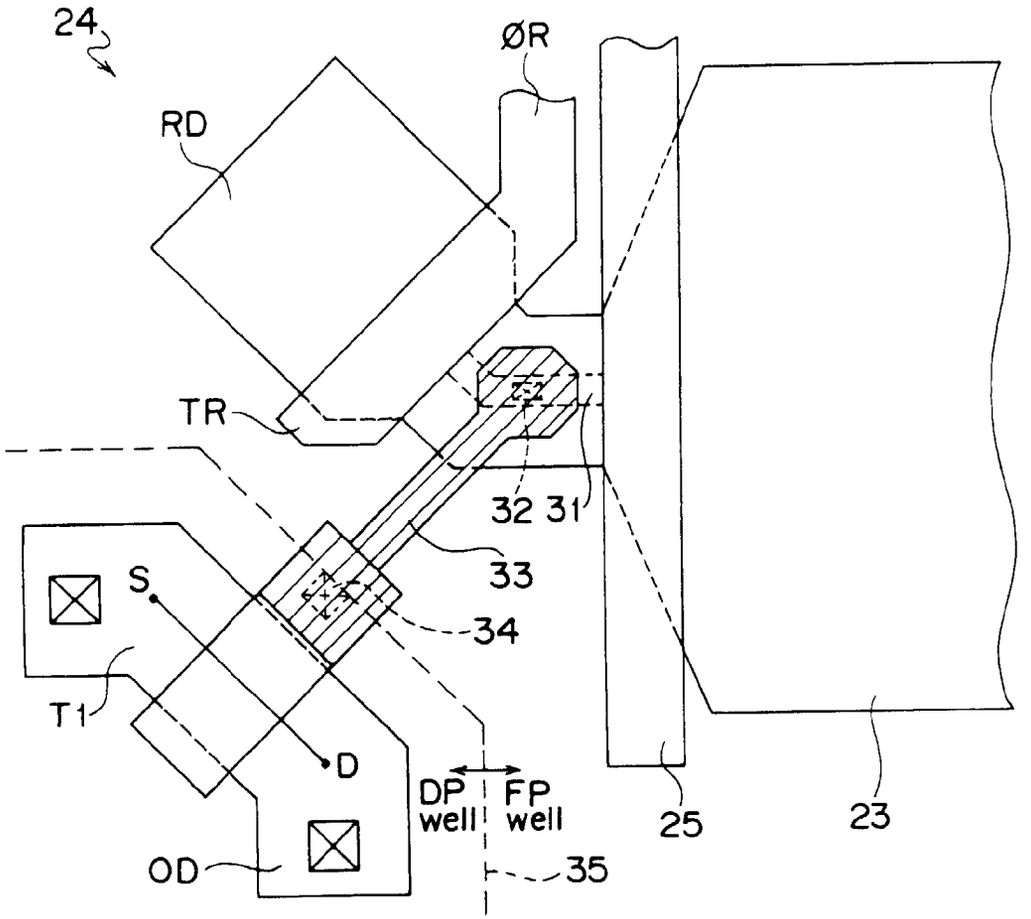


Fig.7 PRIOR ART

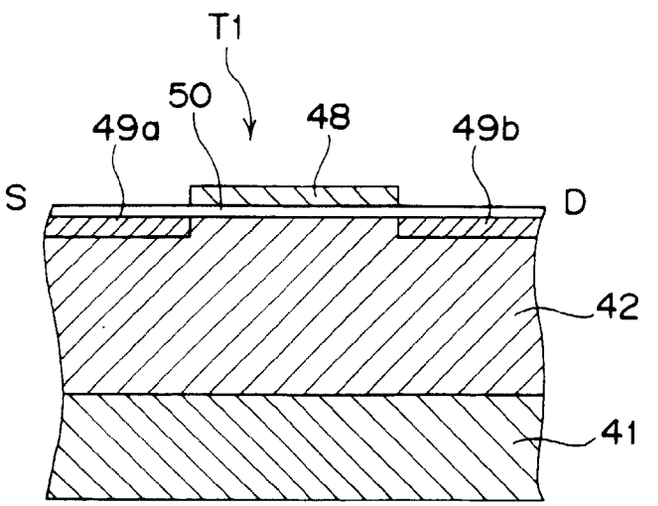


Fig.8 PRIOR ART

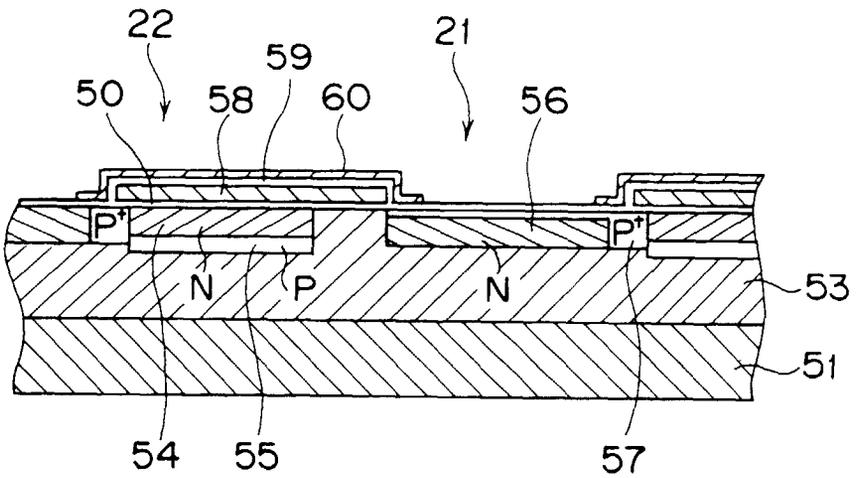


Fig.9 PRIOR ART

