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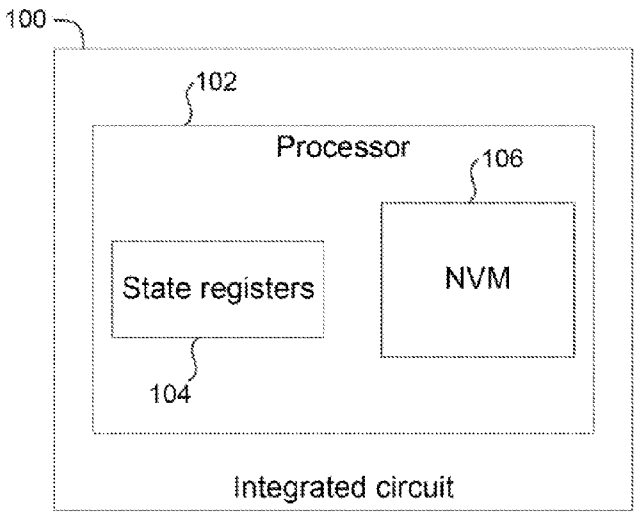


FIG. 1

(57) Abstract: Example implementations relate to storing state machine information in a non-volatile memory (NVM) in a processor. In example implementations, a plurality of state registers may hold state machine information of a processor. The processor may pause operation in response to a trigger indication. An NVM in the processor may store, in response to the trigger indication, state machine information that is in the plurality of state registers when operation of the processor is paused.

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STORING STATE MACHINE INFORMATION IN A NON-VOLATILE MEMORY

BACKGROUND

[0001] Server and storage systems may have many different components. When a component malfunctions, it may be removed from its server/storage system and returned to its manufacturer. A manufacturer may test returned components to determine causes of failure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The following detailed description references the drawings, wherein:

[0003] FIG. 1 is a block diagram of an example integrated circuit that includes a processor having a non-volatile memory (NVM) to store state machine information;

[0004] FIG. 2 is a block diagram of an example integrated circuit that includes a processor having shadow registers, environmental sensors, and an NVM;

[0005] FIG. 3 is a block diagram of an example system that includes a processor having an NVM for storing state machine information;

[0006] FIG. 4 is a block diagram of an example system that includes environmental monitoring and cache copying modules to transfer data to an NVM;

[0007] FIG. 5 is a flowchart of an example method for storing state machine information in an NVM;

[0008] FIG. 6 is a flowchart of an example method for storing prior state machine information in an NVM; and

[0009] FIG. 7 is a flowchart of an example method for storing processor-related data in an NVM in accordance with received instructions.

DETAILED DESCRIPTION

[0010] Manufacturers of hardware components (e.g., components in server/storage systems) may test returned components for causes of failure. Components may be returned with little or no information indicating the reason for failure. Call data related to a returned processor chip at the time the processor's

failure may be stored in a location external to the processor (e.g., in file or paper logs), but correlating call data to individual parts may be complicated and unreliable. If a cause of failure cannot be determined for a returned component, the component may be marked NDF (no defect found). NDF returns may erode profit margins for manufacturers since time/material/shipping costs for exchanging hardware may be much higher than the cost of the component being replaced, and because NDF returns may indicate that customers' problems have not been resolved, reducing customer satisfaction and brand value.

[0011] In light of the above, the present disclosure provides for storing, in a non-volatile memory in a processor, the processor's state and environmental conditions when the processor fails. Such stored information retained by the processor may be analyzed by the manufacturer when the processor is returned, and may enable targeted testing to determine cause(s) of failure. Thus, the number of NDF returns may be reduced, saving manufacturers time and money.

[0012] Referring now to the drawings, FIG. 1 is a block diagram of an example integrated circuit 100 that includes a processor having a non-volatile memory (NVM) to store state machine information. Integrated circuit 100 may be in, for example, an electronic user device (e.g., notebook computer, desktop computer, workstation, tablet computing device, mobile phone, or electronic book reader) or in a server. In FIG. 1, integrated circuit 100 includes processor 102, which may include a central processing unit (CPU), microprocessor (e.g., semiconductor-based microprocessor), and/or other hardware device suitable for retrieval and/or execution of instructions stored in a machine-readable storage medium. As used herein, the terms "include", "have", and "comprise" are interchangeable and should be understood to have the same meaning.

[0013] Processor 102 may include a plurality of state registers 104 to hold state machine information of processor 102. State registers 104 may include hardware registers. State machine information may include, for example, status flag bits, interrupt flags, parity flags, values of locally stored variables, retirement unit information, instruction decoding information, and/or instruction pipeline information.

[0014] Processor 102 may pause operation in response to a trigger indication. As used herein, the term "trigger indication" should be understood to refer to an indication of a non-recoverable error for which immediate attention/action is needed. A trigger indication may be generated in response to, for example, a detection of bad parity, a system bus error, or an overstressed/failed hardware component. In some implementations, a trigger indication may be a hardware error indication or system management interrupt (SMI). A hardware error indication may be, for example, a machine check exception or a non-maskable interrupt. Pausing operation of processor 102 may involve, for example, halting all normal processes running on processor 102 and suspending an operating system (OS). In some implementations, processor 102 may enter a special-purpose operating mode (e.g., System Management Mode, or SMM) in response to a trigger indication, after operation is paused. In some implementations, processor 102 may cause an error message to be displayed while operation is paused. After operation of processor 102 is paused in response to a trigger indication, processor 102 may need to be restarted/rebooted to resume normal operation.

[0015] Processor 102 may include NVM 106 to store, in response to a trigger indication, state machine information that is in state registers 104 when operation of processor 102 is paused. NVM 106 may include, for example, a flash memory, a memristor, and/or any other non-volatile memory suitable for storing state machine information of a processor. NVM 106 may be fabricated in a region of processor 102 such that NVM 106 is part of the processor chip. Information stored in NVM 106 may be retained across reboots and power cycles of processor 102. If processor 102 is returned to a manufacturer, the manufacturer may use state machine information stored in NVM 106 to, for example, recreate circumstances (e.g., populate state registers in processor 102) under which processor 102 failed, for testing and failure analysis purposes.

[0016] FIG. 2 is a block diagram of an example integrated circuit 200 that includes a processor having shadow registers, environmental sensors, and an NVM. Integrated circuit 200 may be in, for example, an electronic user device (e.g., notebook computer, desktop computer, workstation, tablet computing device,

mobile phone, or electronic book reader) or in a server. In FIG. 2, integrated circuit 200 includes processor 202, which may include a CPU, microprocessor (e.g., semiconductor-based microprocessor), and/or other hardware device suitable for retrieval and/or execution of instructions stored in a machine-readable storage medium.

[0017] Processor 202 may include a plurality of state registers 204 and NVM 206. State registers 204 may be analogous to (e.g., have functions and/or components similar to) state registers 104 of FIG. 1. Processor 202 may pause operation in response to a trigger indication and NVM 206 may store, in response to the trigger indication, state machine information that is in state registers 204 when operation of processor 202 is paused, as discussed above with respect to FIG. 1. NVM 206 may be fabricated in a region of processor 202 such that NVM 206 is part of the processor chip. NVM 206 may include, for example, a flash memory, a memristor, and/or any other non-volatile memory suitable for storing state machine information of a processor. Information stored in NVM 206 may be retained across reboots and power cycles of processor 202.

[0018] In some implementations, processor 202 may include a plurality of shadow registers 208 to store prior state machine information of processor 202. Shadow registers 208 may include hardware registers, latches, and/or a dedicated segment of a volatile memory in processor 202. As used herein, the term "prior state machine information" should be understood to refer to information that was previously held in a state register (i.e., information that reflects a previous state of a processor). For example, prior state machine information of processor 202 may include information that was held in state registers 204 during the previous clock cycle, or two clock cycles ago. In some implementations, information held in state registers 204 may be transferred to shadow registers 208 before state registers 204 are updated with current state machine information of processor 202 (e.g., data may be transferred from state registers 204 to shadow registers 208 on each rising clock edge before contents of state registers 204 are updated). NVM 206 may store, in response to a trigger indication, prior state machine information that is in shadow registers 208 when operation of processor 202 is paused.

[0019] If processor 202 is returned to a manufacturer, the manufacturer may examine prior state machine information stored in NVM 206 to, for example, better understand and/or recreate circumstances leading up to the failure of processor 202, for testing and failure analysis purposes. In some implementations, processor 202 may receive, before runtime operation of processor 202, instructions specifying whether prior state machine information should be stored when trigger indications are detected. When a trigger indication is detected during runtime of processor 202, NVM 206 may store or not store prior state machine information in NVM 206 in accordance with the received instructions. Such instructions may be received from/modified by, for example, a system administrator.

[0020] In some implementations, processor 202 may include thermal sensor 210, voltage sensor 212, and power usage monitor 214. Thermal sensor 210 may monitor thermal conditions on processor 202. For example, thermal sensor 210 may measure the temperature in a particular region of processor 202. Voltage sensor 212 may monitor voltage conditions on processor 202. For example, voltage sensor 212 may measure voltage in a circuit of processor 202. Power usage monitor 214 may determine power usage of processor 202. For example, power usage monitor 214 may use current and voltage readings taken on processor 202 to calculate power consumption. NVM 206 may store, in response to a trigger indication, a reading of thermal sensor 210 when operation of processor 202 is paused, a reading of voltage sensor 212 when operation of processor 202 is paused, and a reading of power usage monitor 214 when operation of processor 202 is paused. If processor 202 is returned to a manufacturer, the manufacturer may use such readings stored in NVM 206 to, for example, recreate environmental conditions that existed at the time processor 202 failed, for testing and failure analysis purposes. Although FIG. 2 illustrates one thermal sensor, one voltage sensor, and one power usage monitor, it should be understood that processor 202 may include multiple thermal sensors, voltage sensors, and/or power usage monitors to monitor environmental conditions in various parts of processor 202, and readings of each of such sensors/monitors may be stored in NVM 206 in response to a trigger indication.

[0021] In some implementations, processor 202 may receive, before runtime operation of processor 202, instructions specifying which environmental conditions should be stored when trigger indications are detected. When a trigger indication is detected during runtime of processor 202, NVM 206 may store a subset of a thermal sensor reading (or readings), a voltage sensor reading (or readings), and a power usage monitor reading (or readings) in accordance with the received instructions. Such instructions may be received from/modified by, for example, a system administrator.

[0022] In some implementations, processor 202 may include a plurality of caches 216. Caches 216 may include, for example, an instruction cache, data cache, and/or translation lookaside buffer (TLB). Caches 216 may be implemented in a volatile memory in processor 202. NVM 206 may store, in response to a trigger indication, data that is in caches 216 when operation of processor 202 is paused.

[0023] If processor 202 is returned to a manufacturer, the manufacturer may use cache data stored in NVM 206 to, for example, recreate circumstances (e.g., populate caches in processor 202) under which processor 202 failed, for testing and failure analysis purposes. In some implementations, processor 202 may receive, before runtime operation of processor 202, instructions specifying whether cache data should be stored when trigger indications are detected. When a trigger indication is detected during runtime of processor 202, NVM 206 may store or not store cache data in accordance with the received instructions. Such instructions may be received from/modified by, for example, a system administrator.

[0024] FIG. 3 is a block diagram of an example system 300 that includes a processor having an NVM for storing state machine information. System 300 may be implemented, for example, in an electronic user device (e.g., notebook computer, desktop computer, workstation, tablet computing device, mobile phone, or electronic book reader) or in a server. In FIG. 3, system 300 includes processor 302, which may include a CPU, microprocessor (e.g., semiconductor-based microprocessor), and/or other hardware device suitable for retrieval and/or execution of instructions stored in a machine-readable storage medium.

[0025] Processor 302 may include a plurality of state registers 304, NVM 306, and state capture module 308. A module may include a set of instructions encoded

on a machine-readable storage medium and executable by a processor. In addition or as an alternative, a module may include a hardware device comprising electronic circuitry for implementing the functionality described below.

[0026] State registers 304 may hold state machine information of processor 302. State registers 304 may include hardware registers. State machine information may include, for example, status flag bits, interrupt flags, parity flags, values of locally stored variables, retirement unit information, instruction decoding information, and/or instruction pipeline information.

[0027] Processor 302 may pause operation in response to a trigger indication. The trigger indication may be, for example, a hardware error indication (e.g., machine check exception or non-maskable interrupt) or SMI. Pausing operation of processor 302 may involve, for example, halting all normal processes running on processor 302 and suspending an operating system (OS). In some implementations, processor 302 may enter a special-purpose operating mode (e.g., SMM) in response to a trigger indication, after operation is paused. In some implementations, processor 302 may cause an error message to be displayed while operation is paused. After operation of processor 302 is paused in response to a trigger indication, processor 302 may need to be restarted/ rebooted to resume normal operation.

[0028] State capture module 308 may transfer to NVM 306, in response to a trigger indication, state machine information that is in state registers 304 when operation of processor 302 is paused. NVM 306 may include, for example, a flash memory, a memristor, and/or any other non-volatile memory suitable for storing state machine information of a processor. In some implementations, NVM 306 may be fabricated in a region of processor 302 in an integrated circuit. Information stored in NVM 306 may be retained across reboots and power cycles of processor 302. If processor 302 is returned to a manufacturer, the manufacturer may use state machine information stored in NVM 306 to, for example, recreate circumstances (e.g., populate state registers in processor 302) under which processor 302 failed, for testing and failure analysis purposes.

[0029] FIG. 4 is a block diagram of an example system 400 that includes environmental monitoring and cache copying modules to transfer data to an

NVM. System 400 may be implemented, for example, in an electronic user device (e.g., notebook computer, desktop computer, workstation, tablet computing device, mobile phone, or electronic book reader) or in a server. In FIG. 4, system 400 includes processor 402, which may include a CPU, microprocessor (e.g., semiconductor-based microprocessor), and/or other hardware device suitable for retrieval and/or execution of instructions stored in a machine-readable storage medium.

[0030] Processor 402 may include a plurality of state registers 404, NVM 406, and state capture module 408. State registers 404 may be analogous to state registers 304 of FIG. 3. Processor 402 may pause operation in response to a trigger indication and state capture module 408 may transfer to NVM 406, in response to the trigger indication, state machine information that is in state registers 404 when operation of processor 402 is paused, as discussed above with respect to FIG. 3. A module may include a set of instructions encoded on a machine-readable storage medium and executable by a processor. In addition or as an alternative, a module may include a hardware device comprising electronic circuitry for implementing the functionality described below.

[0031] In some implementations, processor 402 may include a plurality of shadow registers 410 to store prior state machine information of processor 402. Shadow registers 410 may include hardware registers, latches, and/or a dedicated segment of a volatile memory in processor 402. State capture module 408 may transfer to NVM 406, in response to a trigger indication, prior state machine information that is in shadow registers 410 when operation of processor 402 is paused. In some implementations, state capture module 408 may transfer information held in state registers 404 to shadow registers 410 before state registers 404 are updated with current state machine information of processor 402 (e.g., state capture module 408 may transfer data from state registers 404 to shadow registers 410 on each rising clock edge before contents of state registers 404 are updated).

[0032] If processor 402 is returned to a manufacturer, the manufacturer may examine prior state machine information stored in NVM 406 to, for example, better understand and/or recreate circumstances leading up to the failure of

processor 402, for testing and failure analysis purposes. In some implementations, processor 402 may receive, before runtime operation of processor 402, instructions specifying whether prior state machine information should be stored when trigger indications are detected. When a trigger indication is detected during runtime of processor 402, state capture module 408 may transfer or not transfer prior state machine information to NVM 406 in accordance with the received instructions. Such instructions may be received from/modified by, for example, a system administrator.

[0033] In some implementations, processor 402 may include environmental monitoring module 412 communicatively coupled to processor 402. Environmental monitoring module 412 may measure, in response to a trigger indication, thermal and voltage conditions on processor 402 when operation of processor 402 is paused, and determine, in response to the trigger indication, power utilization of processor 402 immediately before operation of processor 402 is paused. In some implementations, environmental monitoring module 412 may include a thermal sensor (e.g., thermal sensor 210), a voltage sensor (e.g., voltage sensor 212), and/or a power usage monitor (e.g., power usage monitor 214). In some examples, processor 402 and environmental monitoring module 412 may be on separate dies in the same multi-die package. In some examples, environmental monitoring module 412 may be implemented partially or fully in processor 402 (e.g., environmental monitoring module 412 may be fabricated in a region of the processor chip).

[0034] Environmental monitoring module 412 may transfer to NVM 406, in response to the trigger indication, the measured thermal and voltage conditions and the determined power utilization. If processor 402 is returned to a manufacturer, the manufacturer may use the measured thermal and voltage conditions and the determined power utilization stored in NVM 406 to, for example, recreate environmental conditions that existed at the time processor 402 failed, for testing and failure analysis purposes. In some implementations, processor 402 may receive, before runtime operation of processor 402, instructions specifying which environmental conditions should be stored when trigger indications are detected. When a trigger indication is detected

during runtime of processor 402, environmental monitoring module 412 may transfer to NVM 406 a subset of measured thermal and voltage conditions and determined power utilization in accordance with the received instructions. Such instructions may be received from/modified by, for example, a system administrator.

[0035] In some implementations, processor 402 may include a plurality of caches 416 and cache copying module 414. Caches 416 may include, for example, an instruction cache, data cache, and/or TLB. Caches 416 may be implemented in a volatile memory in processor 402. Cache copying module 414 may copy to NVM 406, in response to a trigger indication, data that is in caches 416 when operation of processor 402 is paused.

[0036] If processor 402 is returned to a manufacturer, the manufacturer may use cache data stored in NVM 406 to, for example, recreate circumstances (e.g., populate caches in processor 402) under which processor 402 failed, for testing and failure analysis purposes. In some implementations, processor 402 may receive, before runtime operation of processor 402, instructions specifying whether cache data should be stored when trigger indications are detected. When a trigger indication is detected during runtime of processor 402, cache copying module 414 may copy or not copy cache data to NVM 406 in accordance with the received instructions. Such instructions may be received from/modified by, for example, a system administrator.

[0037] Methods related to capturing data when processor operation is paused are discussed with respect to FIGS. 5-6. FIG. 5 is a flowchart of an example method 500 for storing state machine information in an NVM. Although execution of method 500 is described below with reference to processor 102 of FIG. 1, it should be understood that execution of method 500 may be performed with respect to other suitable devices, such as processors 202, 302, and 402 of FIGS. 2, 3, and 4, respectively. Method 500 may be implemented in the form of executable instructions stored on a machine-readable storage medium and/or in the form of electronic circuitry.

[0038] Method 500 may start in block 502, where a plurality of state registers in processor 102 may be used to hold state machine information of processor 102. Processor 102 may include an NVM. The NVM (e.g., NVM 106) may include, for

example, a flash memory, a memristor, and/or any other non-volatile memory suitable for storing state machine information (e.g., information in state registers 104) of a processor. The NVM may be fabricated in a region of processor 102 such that the NVM is part of the processor chip.

[0039] In block 504, it may be determined whether a trigger indication has been detected in processor 102. If a trigger indication has not been detected, method 500 may loop back to block 502. If a trigger indication has been detected, method 500 may proceed to block 506, in which operation of processor 102 may be paused in response to the trigger indication.

[0040] In block 508, state machine information, that is in the plurality of state registers when operation of processor 102 is paused, may be stored in the NVM in response to the trigger indication. If processor 102 is returned to a manufacturer, the manufacturer may use state machine information stored in the NVM to, for example, recreate circumstances (e.g., populate state registers in processor 102) under which processor 102 failed, for testing and failure analysis purposes.

[0041] FIG. 6 is a flowchart of an example method 600 for storing prior state machine information in an NVM. Although execution of method 600 is described below with reference to processor 202 of FIG. 2, it should be understood that execution of method 600 may be performed with respect to other suitable devices, such as processors 102, 302, and 402 of FIGS. 1, 3, and 4, respectively. Some blocks of method 600 may be performed in parallel with and/or after method 500. Method 600 may be implemented in the form of executable instructions stored on a machine-readable storage medium and/or in the form of electronic circuitry.

[0042] Method 600 may start in block 602, where a plurality of shadow registers in processor 202 may be used to hold prior state machine information of processor 202. Processor 202 may include an NVM. The NVM (e.g., NVM 206) may include, for example, a flash memory, a memristor, and/or any other non-volatile memory suitable for storing prior state machine information (e.g., information in shadow registers 208) of a processor. The NVM may be fabricated in a region of processor 202 such that the NVM is part of the processor chip.

[0043] In block 604, it may be determined whether a trigger indication has been detected in processor 202. If a trigger indication has not been detected, method 600

may loop back to block 602. If a trigger indication has been detected, method 600 may proceed to block 606, in which operation of processor 202 may be paused in response to the trigger indication.

[0044] In block 608, prior state machine information, that is in the plurality of shadow registers when operation of processor 202 is paused, may be stored in the NVM in response to the trigger indication. If processor 202 is returned to a manufacturer, the manufacturer may examine prior state machine information stored in the NVM to, for example, better understand and/or recreate circumstances leading up to the failure of processor 202, for testing and failure analysis purposes.

[0045] FIG. 7 is a flowchart of an example method 700 for storing processor-related data in an NVM in accordance with received instructions. Although execution of method 700 is described below with reference to processor 202 of FIG. 2, it should be understood that execution of method 700 may be performed with respect to other suitable devices, such as processors 102, 302, and 402 of FIGS. 1, 3, and 4, respectively. Some blocks of method 700 may be performed in parallel with and/or after method 500 or 600. Method 700 may be implemented in the form of executable instructions stored on a machine-readable storage medium and/or in the form of electronic circuitry.

[0046] Method 700 may start in block 702, where processor 202 may receive, before runtime operation of processor 202, instructions specifying which of thermal data, voltage data, power utilization data, and cache data to store when trigger indications are detected. The instructions may be received from, for example, a system administrator. Processor 202 may include an NVM and a plurality of caches. The NVM (e.g., NVM 206) may include, for example, a flash memory and/or a memristor. The NVM may be fabricated in a region of processor 202 such that the NVM is part of the processor chip.

[0047] In block 704, runtime operation of processor 202 may occur. In block 706, thermal and voltage conditions on processor 202 when operation of processor 202 is paused may be measured in response to a trigger indication. Thermal and voltage conditions on processor 202 may be measured by, for

example, thermal sensor 210 and voltage sensor 212, respectively, as discussed above with respect to FIG. 2.

[0048] In block 708, power utilization of processor 202 immediately before operation of processor 202 is paused may be determined in response to the trigger indication. The power utilization may be determined by, for example, power usage monitor 214, as discussed above with respect to FIG. 2.

[0049] In block 710, data in the plurality of caches when operation of processor 202 is paused may be identified in response to the trigger indication. Although blocks 708 and 710 are shown below block 706 in FIG. 7, it should be understood that the elements of blocks 706, 708, and 710 may be performed in any order, and/or in parallel.

[0050] In block 712, a subset of the measured thermal and voltage conditions, the determined power utilization, and the identified data in the plurality of caches may be stored in the NVM in response to the trigger indication, in accordance with the instructions received in block 702. If processor 202 is returned to a manufacturer, the manufacturer may use data stored in the NVM to, for example, recreate circumstances under which processor 202 failed, for testing and failure analysis purposes.

[0051] The foregoing disclosure describes storing, in a non-volatile memory in a processor, the processor's state and environmental conditions when the processor fails. Example implementations described herein enable reduction of the number of NDF returns, saving manufacturers time and money.

We claim:

1. A processor in an integrated circuit, wherein the processor is to pause operation in response to a trigger indication, the processor comprising:

a plurality of state registers to hold state machine information of the processor; and

a non-volatile memory (NVM) to store, in response to the trigger indication, state machine information that is in the plurality of state registers when operation of the processor is paused.

2. The processor of claim 1, further comprising a plurality of shadow registers to store prior state machine information of the processor, wherein the NVM is further to store, in response to the trigger indication, prior state machine information that is in the plurality of shadow registers when operation of the processor is paused.

3. The processor of claim 1, further comprising:

a thermal sensor to monitor thermal conditions on the processor;

a voltage sensor to monitor voltage conditions on the processor; and

a power usage monitor to determine power usage of the processor;

wherein the NVM is further to store, in response to the trigger indication:

a reading of the thermal sensor when operation of the processor is paused,

a reading of the voltage sensor when operation of the processor is paused, and

a reading of the power usage monitor when operation of the processor is paused.

4. The processor of claim 1, further comprising a plurality of caches, wherein the NVM is further to store, in response to the trigger indication, data that is in the plurality of caches when operation of the processor is paused.

5. The processor of claim 1, wherein the NVM comprises a flash memory or memristor.

6. The processor of claim 1, wherein the trigger indication is a hardware error indication or system management interrupt (SMI).

7. A system comprising:

a processor comprising:

a plurality of state registers to hold state machine information of the processor, wherein the processor is to pause operation in response to a trigger indication;

a non-volatile memory (NVM); and

a state capture module to transfer to the NVM, in response to the trigger indication, state machine information that is in the plurality of state registers when operation of the processor is paused.

8. The system of claim 7, wherein the NVM is fabricated in a region of the processor in an integrated circuit.

9. The system of claim 7, wherein:

the processor further comprises a plurality of shadow registers to store prior state machine information of the processor; and

the state capture module is further to transfer to the NVM, in response to the trigger indication, prior state machine information that is in the plurality of shadow registers when operation of the processor is paused.

10. The system of claim 7, further comprising an environmental monitoring module communicatively coupled to the processor, the environmental monitoring module to:

measure, in response to the trigger indication, thermal and voltage conditions on the processor when operation of the processor is paused;

determine, in response to the trigger indication, power utilization of the processor immediately before operation of the processor is paused; and

transfer to the NVM, in response to the trigger indication, the measured thermal and voltage conditions and the determined power utilization.

11. The system of claim 7, wherein the processor further comprises a plurality of caches, the processor further comprising a cache copying module to copy to the NVM, in response to the trigger indication, data that is in the plurality of caches when operation of the processor is paused.

12. A method comprising:

using a plurality of state registers in a processor to hold state machine information of the processor, the processor comprising a non-volatile memory (NVM);

pausing operation of the processor in response to a trigger indication; and

storing in the NVM, in response to the trigger indication, state machine information that is in the plurality of state registers when operation of the processor is paused.

13. The method of claim 12, further comprising:

using a plurality of shadow registers to store prior state machine information of the processor; and

storing in the NVM, in response to the trigger indication, prior state machine information that is in the plurality of shadow registers when operation of the processor is paused.

14. The method of claim 12, wherein the processor further comprises a plurality of caches, the method further comprising:

measuring, in response to the trigger indication, thermal and voltage conditions on the processor when operation of the processor is paused;

determining, in response to the trigger indication, power utilization of the processor immediately before operation of the processor is paused; and

identifying, in response to the trigger indication, data in the plurality of caches when operation of the processor is paused.

15. The method of claim 14, further comprising:

receiving, before runtime operation of the processor, instructions specifying which of thermal data, voltage data, power utilization data, and cache data to store when trigger indications are detected; and

storing in the NVM, in response to the trigger indication and in accordance with the received instructions, a subset of the measured thermal and voltage conditions, the determined power utilization, and the identified data in the plurality of caches.

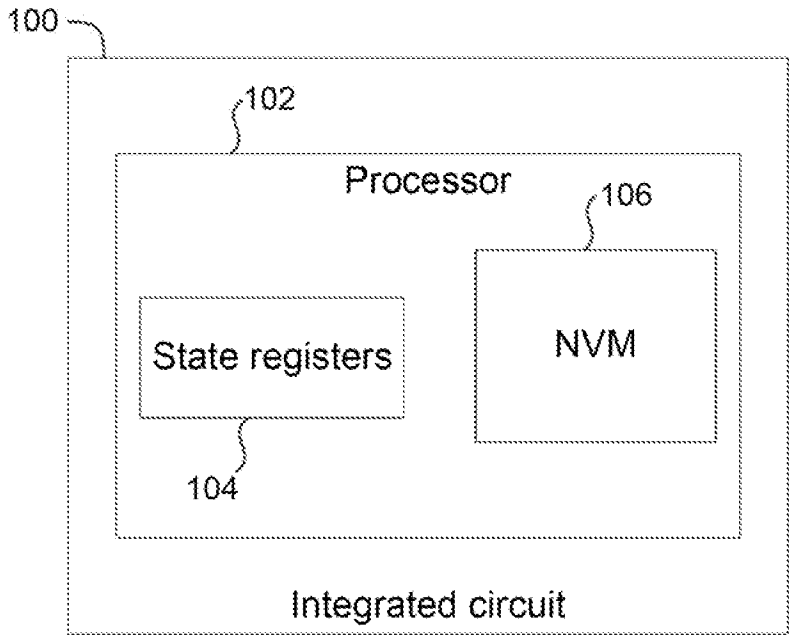

100
102
Processor
106
State registers
NVM
104
Integrated circuit

FIG. 1

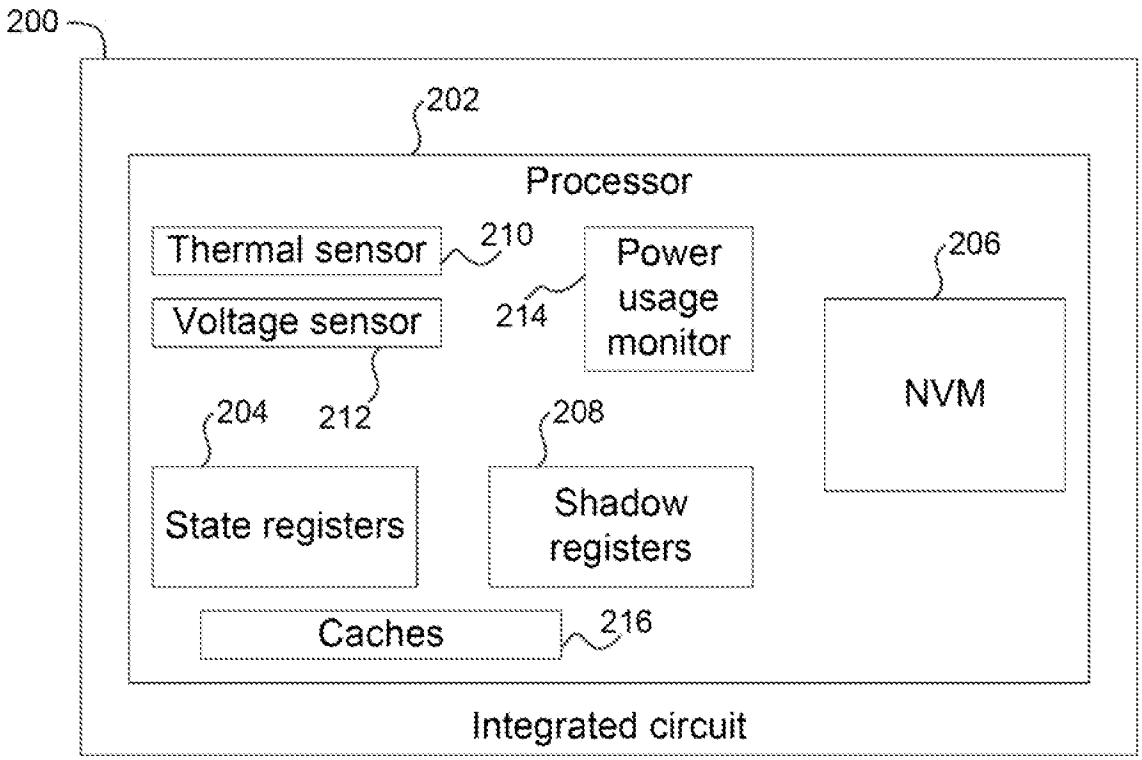

200
202
Processor
Thermal sensor
210
Power usage monitor
214
206
Voltage sensor
NVM
204
212
208
State registers
Shadow registers
Caches
216
Integrated circuit

FIG. 2

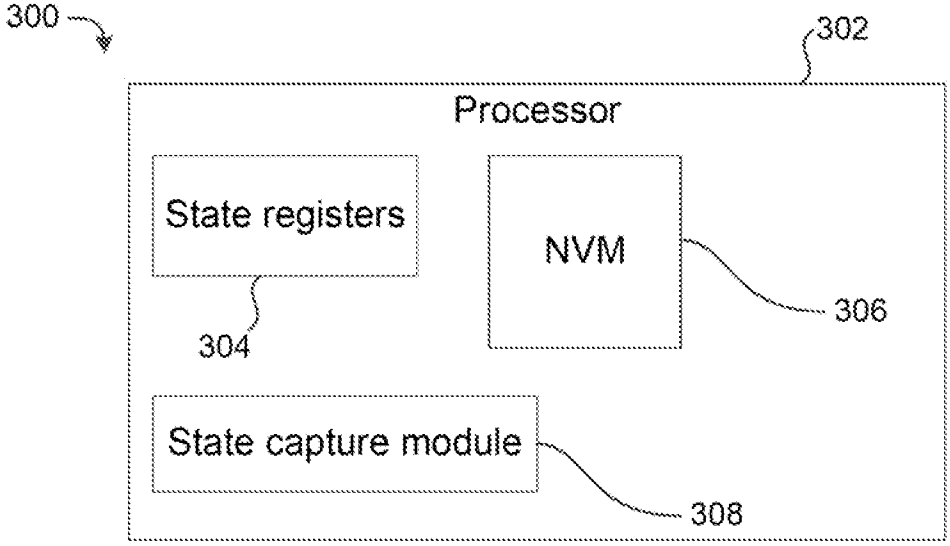

300
302
Processor
State registers
NVM
306
304
State capture module
308

FIG. 3

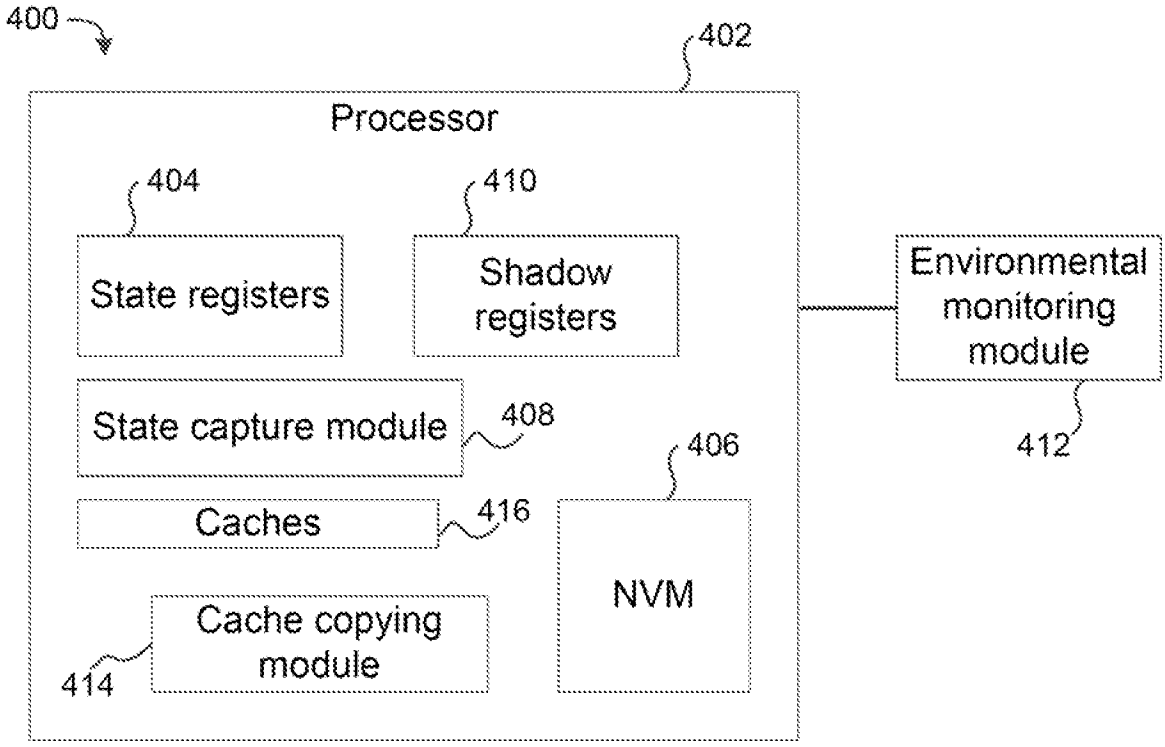

400
402
Processor
404
410
State registers
Shadow registers
Environmental monitoring module
412
State capture module
408
406
Caches
416
NVM
Cache copying module
414

FIG. 4

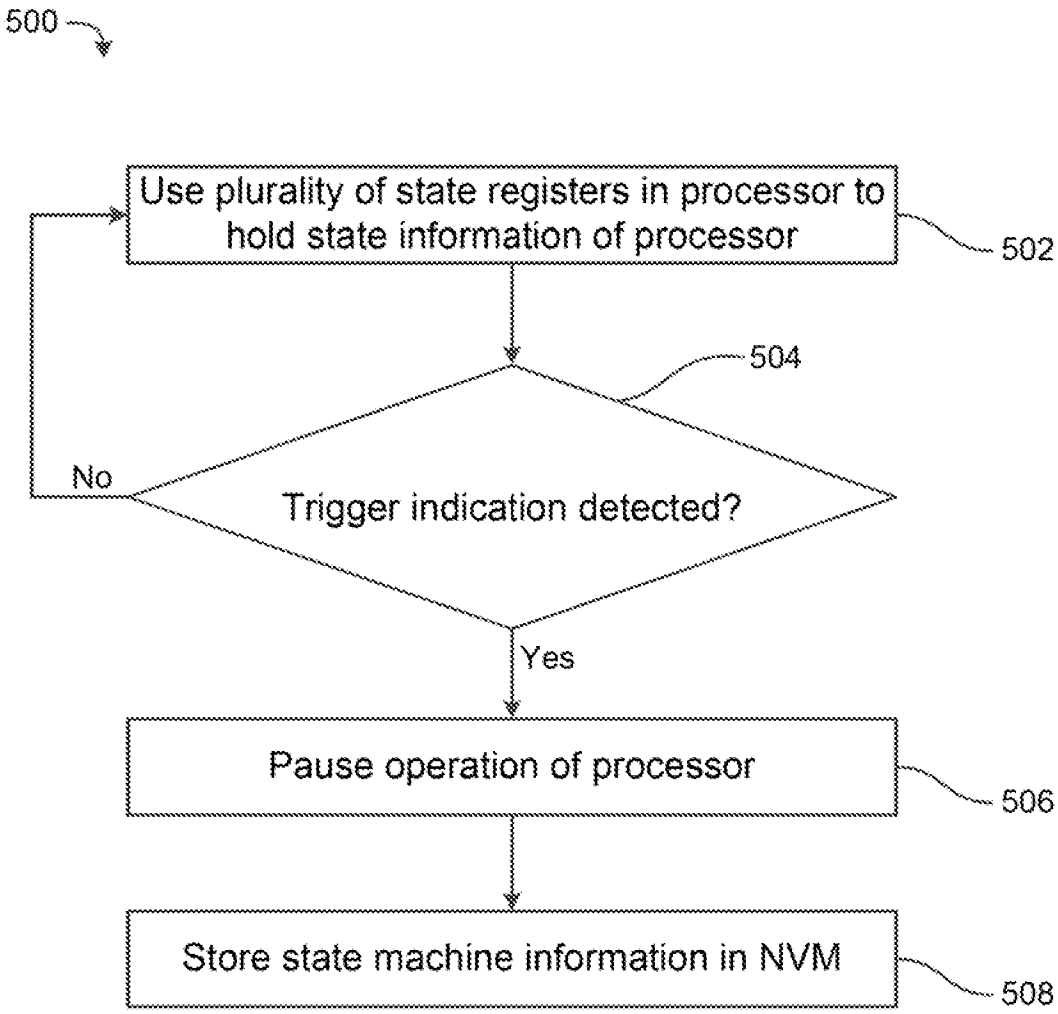

500
Use plurality of state registers in processor to hold state information of processor
502
504
Trigger indication detected?
No
Yes
Pause operation of processor
506
Store state machine information in NVM
508

FIG. 5

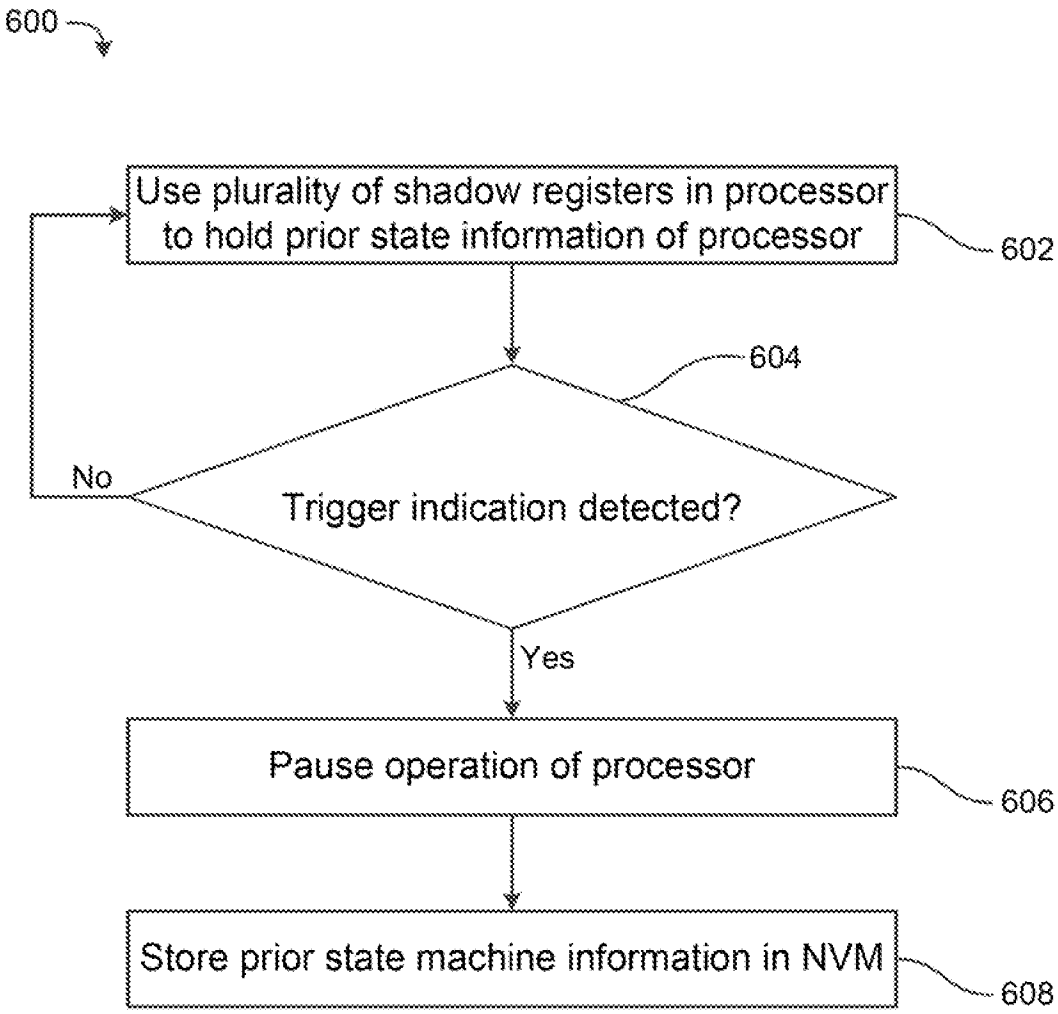

600
Use plurality of shadow registers in processor to hold prior state information of processor
602
604
Trigger indication detected?
No
Yes
Pause operation of processor
606
Store prior state machine information in NVM
608

FIG. 6

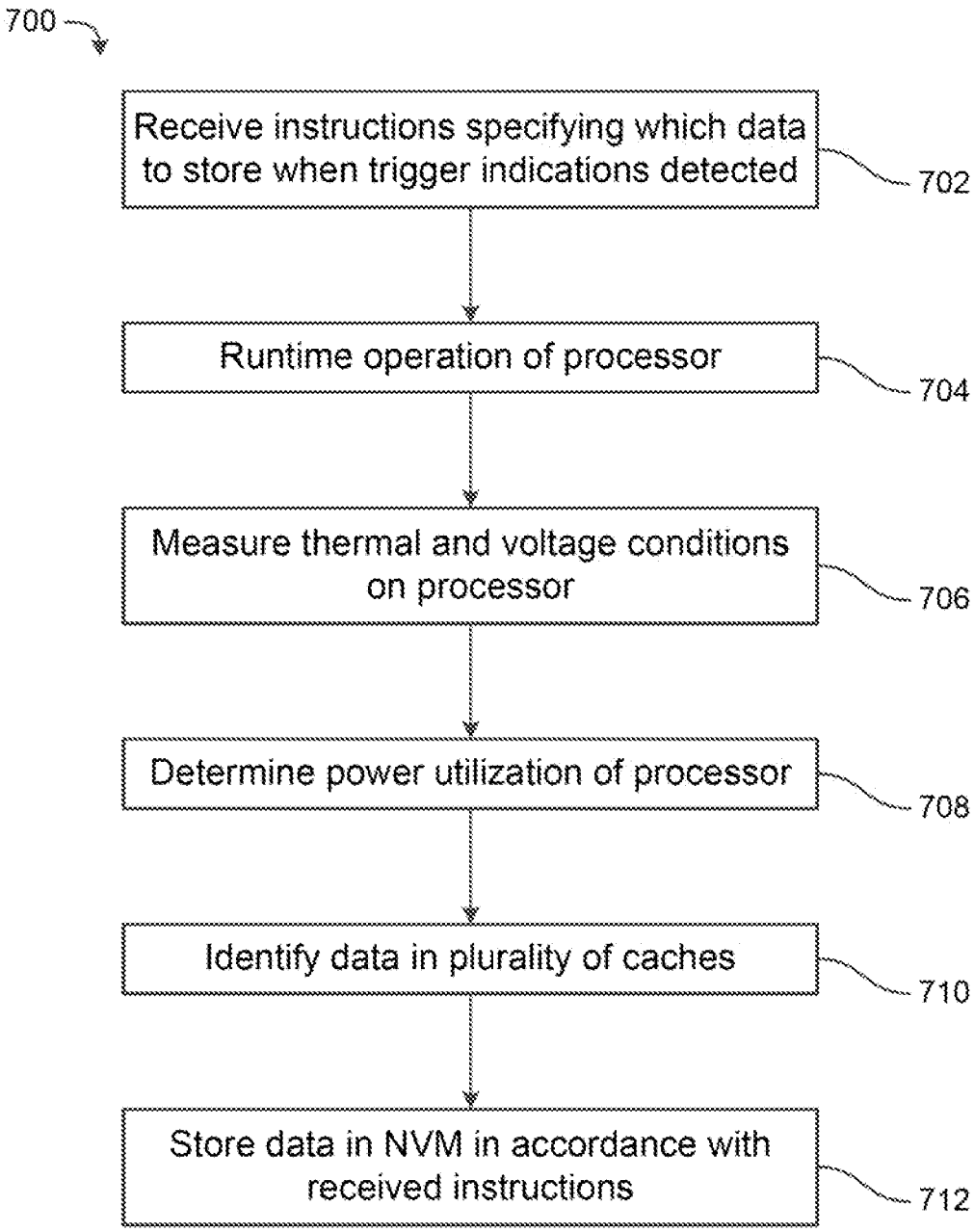

700
Receive instructions specifying which data to store when trigger indications detected
702
Runtime operation of processor
704
Measure thermal and voltage conditions on processor
706
Determine power utilization of processor
708
Identify data in plurality of caches
710
Store data in NVM in accordance with received instructions
712

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/026305

A. CLASSIFICATION OF SUBJECT MATTER

G06F 9/06(2006.01)i, G06F 9/30(2006.01)i, G06F 11/30(2006.01)i, G06F 12/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 9/06; G06F 15/16; G06F 11/34; G06F 7/00; G06F 1/32; G06F 11/00; G06F 9/30; G06F 11/30; G06F 12/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: processor, state, information, register, NVM.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0166840 A1 (MICHAEL A. ROTHMAN et al.) 28 June 2012 See abstract, paragraphs [0025]-[0037], claims 1,8 and figures 3,4.	1-15
Y	US 2008-0244331 A1 (ANDREW W. GRIMES et al.) 02 October 2008 See abstract, paragraphs [0088]-[0095], claim 1 and figures 5,6.	1-15
A	JP 08-030565 A (FUJI XEROX CO., LTD.) 02 February 1996 See abstract, paragraphs [0019]-[0038], claim 1 and figures 1-6.	1-15
A	JP 02-015340 A (FUJITSU LTD.) 19 January 1990 See pages [4]-[6], claim 1 and figures 1,2.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 December 2015 (22.12.2015)	**23 December 2015 (23.12.2015)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/026305

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JP 08-030565 A	02/02/1996	None	
JP 02-015340 A	19/01/1990	None	