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(54) Title: IMPEDANCE COMPENSATION FOR OPERATIONAL AMPLIFIERS USED IN VARIABLE ENVIRONMENTS

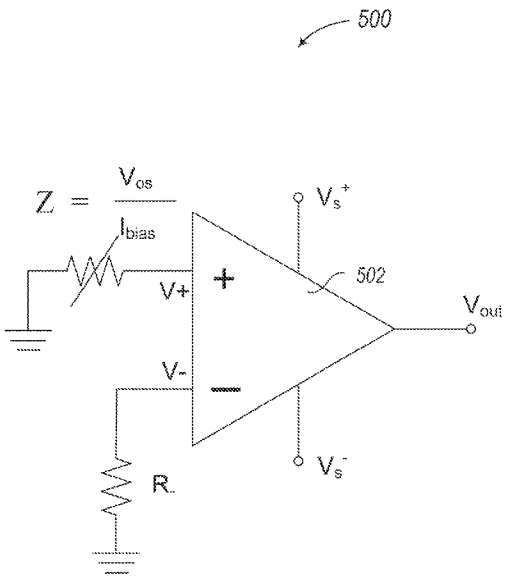

Fig. 5

(57) Abstract: A dual compensation operational amplifier is suitable for use in an environment that experiences fluctuations in ambient energy levels. A dual compensation impedance can be determined to nullify or compensate for effects of an input offset voltage or an input bias current or both. Adjustments to the dual compensation impedance can be made based on calibration data for various environmental conditions so that the dual compensation impedance can be either pre-set for anticipated conditions in different target operational environments, or automatically adjusted in-situ. Target operational environments that may benefit from such a dual compensation impedance include remote areas that experience extreme or variable temperatures, high altitudes, space, or high radiation environments.

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IMPEDANCE COMPENSATION FOR OPERATIONAL AMPLIFIERS USED IN VARIABLE ENVIRONMENTS

BACKGROUND

Technical Field

The present disclosure generally relates to operational amplifiers used in electrical and electronic circuitry and, in particular, to ways of adjusting operational amplifiers to compensate for variations in performance that arise in certain environments.

Description of the Related Art

Operational amplifiers ("op-amps") are general purpose differential voltage amplifiers commonly used in electric circuits for many different applications. For example, op-amps are frequently used as building blocks in audio systems that involve complex signal processing circuitry to amplify sound. An idealized op-amp 100, shown in Figure 1A, is a three-terminal device that has two input terminals, V^+ (a non-inverting input), V^- (an inverting input), and one output terminal, V_{out}. (Additional terminals are provided to connect a power source (*e.g.,* battery) at V_s^+ and V_s^-). The differential input voltage to be amplified is $\Delta V = V^+ - V^-$. Components internal to the idealized op-amp 100 cause the differential input voltage ΔV to appear at the output terminal, multiplied by an amplification factor, or gain, so that $V_{out} = A \Delta V$. Amplification factors for op-amps can be in the range of about 1000 – 100,000. This characteristic makes op-amps suitable to be used as sensors in many applications in which changes in a small signal can be exaggerated so the changes are easier to monitor and detect.

If a fixed reference voltage V_{ref} is applied to the non-inverting input, the op-amp acts as a comparator device 150, shown in Figure 1B, that compares an input voltage at the inverting input$^-$ to V_{ref}. If the input voltage V_{in} is about equal to V_{ref}, the amplified output V_{out} remains small. As V_{in} deviates

slightly from V_{ref}, the deviation is amplified so that V_{out} becomes very large and can serve as a trigger signal to a downstream device.

One way to test the accuracy of an op-amp used as a sensor or a comparator is to deliberately set the differential input voltage ΔV to zero (for example, by connecting the two inputs together, or grounding both of the inputs), and verifying that V_{out} is also zero. However, intrinsic errors in the various internal components of the op-amp can compound and cause a detectable zero error referred to as an input offset voltage V_{os}. If a non-zero potential V_{os} exists across the two inputs, V_{os} itself can be amplified, producing a significant erroneous non-zero voltage at the output. The zero error associated with an op-amp can be thought of as analogous to the zero error associated with a scale, which is evident when the scale registers a non-zero weight prior to an object being placed on the scale. Scales typically come equipped with mechanical zeroing adjustments to correct these zero errors. In a similar fashion, the input offset voltage V_{os} of an op-amp can be corrected, or nullified, by electrically coupling an "offset null" stage to the V_- input of the op-amp.

Figure 2 shows one example of an existing voltage-compensated op-amp 200 in which a conventional op-amp 202 that exhibits an input offset voltage V_{os} features such an offset null stage 204. In this example, the offset null stage is in the form of a voltage source V_{null} that effectively zeroes out the erroneous input offset voltage. The input offset voltage V_{os} to be nullified is typically within the range of about a microvolt (μV) to about a millivolt (mV). The offset null stage 204 can take other forms, such as, for example, one or more of a fixed resistor, variable resistor, potentiometer, current source, or thyristor. If the input offset voltage V_{os} is known to be constant, an offset null having a constant resistance (*e.g.,* a fixed resistor or a network of fixed resistors) can be applied. If the input offset voltage V_{os} fluctuates, causing a ΔV_{os}, an offset null including an adjustable resistance, or a potentiometer, can be applied. The offset null can be applied at one or both of the inputs to the op-

amp, or the offset null can be provided as a built-in offset null stage that is internal to the op-amp.

Figure 3 shows another embodiment of a voltage-compensated op-amp 300, in which a conventional op-amp 302 (with its internal components shown), that exhibits an input offset voltage, is provided with a built-in offset null stage 304.

With reference to Figure 4, a conventional op-amp 400 is shown in which there exists a difference between the currents at the two inputs, I_+ and I_-, referred to as an input offset current, $I_{io} = |I_+ - I_-|$. The average of those two input currents is referred as input bias current, $I_{bias} = (I_+ + I_-)/2$. In an ideal op-amp, the input resistance is so high that the input currents I_+ and I_- are both negligible, therefore $I_{bias} = 0$. Any current appearing at the input terminals of the op-amp 400 is then a small leakage current which is negligible in most applications, even those in which attention is paid to cancelling an input offset voltage. Input bias currents typically range from about a micro-amp to as small as a pico-amp. In some applications, however, a nonzero input bias current I_{bias} brings about another environmentally-dependent, fluctuating source of error, $\Delta I_{bias,}$ that warrants cancellation. Therefore, when an input bias current is present, use of an offset null stage to simply cancel V_{os} (or ΔV_{os}) may be insufficient. An input bias current can be nullified by addition of resistors to the circuit, for which the resistor values are preferably carefully selected to precisely cancel the bias current without otherwise affecting circuit performance.

BRIEF SUMMARY

Fluctuations in either the input offset voltage ΔV_{os} or in the input bias current ΔI_{bias}, or both, can be caused by changes in environmental conditions such as, for example, temperature variation. These drifts in V_{os} and I_{bias} occur because material properties of electronic components internal to the op-amp (*e.g.*, resistivity, mobility) are, in general, temperature-dependent properties. In consideration of these and other environmentally-dependent

characteristics, the input offset voltage and the input bias current of an op-amp generally may vary depending on the operational environment of the amplifier. In most applications a temperature-induced drift may not be problematic because op-amps located inside electronic equipment are typically maintained at a moderate temperature that is close to room temperature, or at least in a controlled temperature environment. However, if the op-amp is to be used in vehicles, aircraft, spacecraft, ships, submarines, and the like, or if the op-amp is expected to function according to military and/or environmental specifications that generally include extreme temperatures or widely varying temperature or radiation conditions, it may be necessary to address the question of how best to control or adjust environmentally-dependent intrinsic errors, or to find an alternative way to correct them.

One way to avoid the effects of both ΔI_{bias} and ΔV_{os} is to increase the signal level to be so high that changes in the input bias current and the input offset voltage have less impact on the circuit performance. However, this approach can cause unnecessarily high stresses within the circuit and can lead to an excessive amount of electrical power dissipation. Another solution is to balance the impedance at each input (*e.g.,* R^+ and R^- in Figure 4), which can compensate for $I_{bias,}$ but does not address ΔV_{os}. Other solutions that employ thermistors having an exaggerated temperature dependence to reduce temperature sensitivity fail to address radiation effects. Furthermore, in many applications, such as in a space environment, or in a vacuum chamber, for example, radiation effects may be non-negligible. Nevertheless, designers may fail to consider effects from other ambient energy sources such as high-energy electromagnetic radiation, or other sources of ionizing radiation encountered in the presence of ionized particles.

An operational amplifier that exhibits a variable input offset voltage and a variable input bias current that can arise due to fluctuations in temperature and other ambient energy levels can be corrected for both sources of error by using a dual compensation impedance that is a function of both V_{os} and $I_{bias.}$ The dual compensation impedance can take the form of, for example,

one or more resistors, potentiometers, thyristors, current sources, and voltage sources, or combinations of these. Various methods of determining V_{os} and I_{bias} provide ways to either offset or compensate for these errors in anticipation of operating the op-amp in different target environments that may subject the device to extreme or fluctuating environmental conditions.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

In the drawings, identical reference numbers identify similar elements or acts. The sizes and relative positions of elements in the drawings are not necessarily drawn to scale. For example, the shapes of various elements and angles are not drawn to scale, and some of these elements are arbitrarily enlarged and positioned to improve drawing legibility. Further, the particular shapes of the elements as drawn are not intended to convey any information regarding the actual shape of the particular elements, and have been solely selected for ease of recognition in the drawings.

Figures 1A and 1B are schematic diagrams of a generic op-amp (differential amplifier) and a conventional comparator, respectively.

Figure 2 is a schematic diagram of a conventional op-amp that exhibits an input offset voltage, to which an external offset null correction is applied.

Figure 3 is a schematic diagram of a conventional op-amp, showing its internal components, that exhibits an input offset voltage, to which a built-in offset null correction is applied.

Figure 4 is a schematic diagram of a conventional op-amp that exhibits an input bias current.

Figure 5 is a schematic diagram of an op-amp that exhibits an environmentally-induced input offset voltage and an environmentally-induced input bias current, to which a dual compensation impedance stage is applied as taught herein.

Figure 6 is a schematic diagram of a dual-compensated op-amp, showing its internal components, that exhibits an input offset voltage for which a

built-in offset null correction is applied, and an input bias current for which a compensation impedance is applied.

Figure 7 is a schematic diagram of an op-amp that exhibits an environmentally-induced input offset voltage and an environmentally-induced input bias current, to which a network of resistors is applied as an unbalanced dual compensation impedance stage.

Figure 8 is a flow diagram showing a method of variable impedance compensation for fluctuations in ambient energy levels affecting an op-amp according to one illustrated embodiment.

Figures 9A and 9B illustrate a method of variable impedance compensation for fluctuations in anticipated ambient energy levels affecting a target environment according to another illustrated embodiment that entails use of calibration data.

Figures 10A and 10B illustrate a method of variable impedance compensation for fluctuations in ambient energy levels during operation in a target environment, according to another illustrated embodiment that entails use of a sensor in combination with calibration data.

Figures 11A and 11B illustrate a method of variable impedance compensation for fluctuations in ambient energy levels during operation in a target environment, according to another illustrated embodiment that entails use of an in-situ sensor apparatus that can periodically adjust the impedance compensation at selected time intervals.

DETAILED DESCRIPTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of various disclosed embodiments. However, one skilled in the relevant art will recognize that embodiments may be practiced without one or more of these specific details, or with other methods, components, materials, etc. In other instances, well-known structures associated with operational amplifiers and associated circuits have not been

shown or described in detail to avoid unnecessarily obscuring descriptions of the embodiments.

Unless the context requires otherwise, throughout the specification and claims which follow, the word "comprise" and variations thereof, such as, "comprises" and "comprising" are to be construed in an open, inclusive sense, that is as "including, but not limited to."

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

As used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the content clearly dictates otherwise. It should also be noted that the term "or" is generally employed in its sense including "and/or" unless the content clearly dictates otherwise.

The headings and Abstract of the Disclosure provided herein are for convenience only and do not interpret the scope or meaning of the embodiments.

With reference to Figure 5, a dual-compensated op-amp 500 addresses environmental sensitivities within a conventional op-amp 502. The conventional op-amp 502 represents a device that exhibits both types of intrinsic error, V_{os} and I_{bias}, and the dual-compensated op-amp 500 simultaneously compensates for both the input bias current and the input offset voltage. The dual compensated op-amp 500 introduces a dual compensation impedance stage in which a dual compensation impedance Z is generally set to be about equal to an input impedance that is a function of both V_{os} and $I_{bias.}$ For example, if the input impedance is the ratio of V_{os} / I_{bias} . the dual compensation

impedance Z can be set about equal to this ratio to offset the input impedance. Alternatively, the dual compensation impedance Z may be otherwise related to V_{os} and I_{bias} or to their ratio. Furthermore, an environmental effect that causes a change ΔV_{os} in the input offset voltage will also tend to cause a commensurate change ΔI_{bias} in the input bias current, and both changes can be taken into account by applying a variable dual compensation impedance $\Delta Z = \Delta V_{os} / \Delta I_{bias}$ to the non-inverting input of the dual-compensated op-amp 500. For example, if a temperature change causes V_{os} to increase by a factor of 2, I_{bias} may also increase by a factor of 2, in which case the effects cancel out and the variable dual compensation impedance ΔZ does not change. Instead of engaging in the usual practice of balancing both input currents to the op-amp, providing the dual compensation impedance $Z \pm \Delta Z$ at one of the inputs creates an imbalance that simultaneously compensates for both inherent sources of error, as well as for environmentally-induced variations in the error.

With reference to Figure 6, in one embodiment, a partially compensated op-amp 600 includes a dual compensation impedance stage applied to the non-inverting input V_+ of the op-amp 302, which already includes the internal offset null 304 to compensate for V_{os}. In this case, the dual compensation impedance Z can be adjusted to compensate only for I_{bias} or to provide additional offset voltage compensation if the internal offset null 304 turns out to be insufficient. For each of the dual-compensated op-amp 500 and the partially-compensated op-amp 600, a dual compensation impedance stage may take the form of a single resistance or the dual compensation impedance may include one or more resistive components such as resistors, thyristors, thermistors, resistor networks, variable resistors, potentiometers, and the like. The dual compensation impedance stage may also be built into the partially-compensated op-amp 600.

With reference to Figure 7, in one embodiment of a dual-compensated op-amp 700, a dual compensation impedance stage can be applied to the op-amp 502, as a network of resistances selectively electrically coupled to the non-inverting input terminal V^+ the inverting input terminal V^-, the

output terminal, V_{out}, or combinations thereof. For example, the dual compensation impedance Z can be applied to correct the op-amp 502 by electrically coupling a second resistance R_2 at the inverting terminal V^-, providing a third resistance R_3 electrically coupled between the positive input terminal and a ground, and providing a fourth resistance R_4 electrically coupled between the inverting input terminal V^- and the output terminal V_{out}, or combinations of these.

Various embodiments of the compensated op-amps 500, 600, and 700 can further be distinguished by differences in methods of providing an accurate and useful value of the dual compensation impedance Z, that is derived from values of V_{os} and I_{bias}. To adjust the dual compensation impedance Z, values of V_{os} and I_{bias} are needed, which can be obtained from sensors, calculations, or extrapolations, or combinations of these. Moreover, in a fluctuating energy environment, or in a remote environment, the dual compensation impedance Z may need to be updated periodically. For example, a value for the dual compensation impedance Z can be set while the op-amp is in a laboratory, manufacturing facility, or other calibration environment, after which the op-amp can be installed in a vehicle and sent to its intended target operational environment. Or, determination of the dual compensation impedance Z can be made in-situ, in the target environment, based on either direct measurements or sensing environmental parameters and extrapolating the necessary compensation.

In one scenario, described in Figure 8, the dual compensation impedance Z can be set so as to cancel out V_{os} and I_{bias} as closely as possible according to a method 800 in which actual zero measurements of a particular op-amp are made either in the target environment or in a simulated target environment (802). This can be done after the device reaches a remote target operational environment, or, the op-amp can be configured in a simulated target environment. The target environment may or may not be the laboratory calibration environment itself, or an equivalent ground-based environment. At 804, electrical characteristics (voltages and currents) of the op-amp can be

sensed so that V_{os} can be determined at 808. For example, V_{os} can be determined by connecting the two input terminals V^+ and V^- together, measuring V_{out}, and dividing by the known gain factor A. Then I_{bias} can be determined at 810 by measuring leakage currents I^+ and I^- at the two input terminals under operation of the op-amp, and calculating their difference. Finally, the dual compensation impedance Z can be determined at 812 by taking the ratio of V_{os} to I_{bias} so that the op-amp can then be configured with a compensation resistance, and supplied to a customer with the impedance correction already in place. The dual compensation impedance Z is then applied to the op-amp at 814, and the device is then ready to operate in its target environment at 816. If the op-amp has been configured in an environment that simulates remote conditions, the op-amp can first be transported to its target environment before being switched on for operation.

According to one embodiment illustrated in Figures 9A and 9B, the dual compensation impedance Z can be deliberately set to compensate for one or both sources of error (V_{os} and I_{bias}), at an anticipated level. For example, if an op-amp is to be used in an avionics system on-board an aircraft that is operable in a target environment having a known extreme temperature T, the value of the dual compensation impedance Z can be estimated ahead of time to cancel effects of the anticipated future ambient temperature T, instead of being set to cancel effects due to the local ambient temperature of the present environment. As shown in Figures 9A and 9B, this can be done by generating a set of calibration curves for each device at a lab or manufacturing facility prior to distributing devices to customers. For example, a calibration method 900 can be carried out in a calibration environment (*e.g.,* lab) 901 to generate calibration curves 908 and 910. The calibration curves 908 and 910 can later be used to extrapolate predictions for an impedance setting 912 that conforms to conditions in a remote target environment 951 (*e.g.,* an airplane flying at a certain altitude). A particular op-amp can be measured first in the calibration environment 901 to determine values of the input offset voltage V_{osc} (902) and the input bias current I_{biasc} (904) at a lab temperature T_c. Then at 902 and 904,

the temperature in the calibration environment can be changed and successive measurements of V_{os} and I_{bias} can be made to generate (906) the V_{os} calibration curve 908 and the I_{bias} calibration curve 910, respectively, as a function of temperature, T. Finally, for a known target environment 951 having a known temperature T_t, a prediction for the correct value of the dual compensation impedance Z for use in the target environment 951 can be obtained by calculating the ratio V_{ost} / I_{biast} using error values indicated on the calibration curves 908 and 910 at the known temperature T_t, and the op-amp can be set accordingly. The set of curves 908 and 910 can be stored for future reference in a non-transitory storage medium such as an electronic memory for future reference, and the calibration data may be provided to a customer along with the device. Instead of, or in addition to, generating the temperature-based calibration curves 908 and 910, other sets of curves can be generated by varying other environmental conditions such as ambient radiation levels.

A method 950, illustrated in Figure 9B, can be used to update the setting for the dual compensation impedance Z if the target environment changes. At 952, a new target temperature can determined, *e.g.,* by an in-situ measurement or from known characteristics of a new operational destination. At 954, a value of the dual compensation impedance Z is determined from the existing calibration curves 908 and 910 as described above. At 956, the new value of the dual compensation impedance Z is applied to the op-amp in the new target environment, and operation continues at 958 until the target environment changes again at 960, thus triggering a repeat of the method 950. At 954, extrapolating the dual compensation impedance Z can be executed semi-automatically using one or more processors to extract values from the calibration curves, or from calibration tables derived from the calibration curves, and perform the determination of the dual compensation impedance Z electronically.

Alternatively, an exemplary feedback control method 1000 can be used to maintain the dual compensation impedance Z at an accurate value throughout operation of the op-amp in a changing target environment 1001, as

illustrated in Figures 10A and 10B. In this embodiment, the dual compensation impedance Z can be set automatically, in-situ, using an exemplary feedback control system 1003 located within the target environment 1001. Using the method 1000, the dual compensation impedance Z is adjusted according to measurements of fluctuating ambient conditions in the target environment 1001 such as temperature and radiation. The exemplary feedback control system 1003 includes one or more energy level sensors 1005 that provide signals indicative of an ambient energy level in the target environment. The feedback control system 1003 also includes one or more computing devices 1007 that include at least a processor and a non-transitory storage medium such as an electronic memory. At 1002, the sensor(s) 1005 are used to capture information (*e.g.,* temperature) characterizing a particular ambient environment. The sensed information can then be used at 1004 and 1006 to computationally determine an appropriate value of the dual compensation impedance Z by calculation, look-up tables, or other methods. For example, the calibration curves 908 and 910 described above can be saved in the electronic computer memory within the computing device 1007. Thus, when the op-amp 500 enters its destination environment, a temperature measurement can be obtained by the sensor 1005, the error values V_{ost} and I_{biast} can be extrapolated at 1004 from the saved calibration curves, and an input impedance value can be calculated accordingly at 1006. The dual compensation impedance Z can then be applied to offset the input impedance at 1008, for use until another temperature measurement becomes available, or until the temperature shifts, requiring the dual compensation impedance Z to be updated again.

The feedback control method 1000 can be implemented as an automated method by using a processor-based system 1003, in which the determination of the dual compensation impedance Z is made according to programmed instructions and the resulting dual compensation impedance Z adjustment is applied directly to the op-amp in response to an output signal from the processor-based system 1003. One advantage of this automated feedback control method 1000 is that the procedure can be repeated as many

times as needed to ensure that the dual compensation impedance Z remains optimally tuned to the present environment as the environment changes. A second advantage is that the feedback control method 1000 does not require human intervention. A third advantage is that the feedback control method 1000 is based on actual ambient conditions, instead of relying on an extrapolation of a representative set of calibration data.

In another embodiment, a periodic in-situ calibration method 1100 can be performed in the target environment at selected time intervals using an in-situ calibration apparatus 1101, as shown in Figures 11A and 11B. An exemplary in-situ calibration apparatus 1101 can include an electronic multimeter 1103, and a computing device 1105 for collecting signals from and applying signals to the dual-compensated op-amp 500. The calibration apparatus 1101 can take on different forms, for example the calibration apparatus 1101 can be external to the op-amp 500, or the calibration apparatus 1101 can be built into a chip that includes the op-amp 500. According to the in-situ calibration method 1100, at 1102, the dual-compensated op-amp 500 can be temporarily released from its operational mode and placed into an error-adjustment mode for re-calibration. (Alternatively, the value of the dual compensation impedance Z can be adjusted on the fly in response to sensing a drift in op-amp performance.) During re-calibration, the input voltage and input current at the non-inverting input can be sensed at 1104, and the voltage and current at the inverting input can be sensed at 1106. From these measurements, the V_{os} and I_{bias} errors can be determined at 1108 and 1110, respectively, and the input impedance can be determined accordingly at 1112. The dual compensation impedance Z can then be applied at 1114 by providing more or less resistance, for example, at the non-inverting input of the dual-compensated op-amp 500, or by adjusting any of R_1, R_2, R_3, or R_4. Once an impedance adjustment has been made at 1114, the op-amp can be placed back in operating mode at 1116 until the decision block 1118 determines that another update is due, according to a clock that shows whether the present time interval has yet expired.

The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, schematics, and examples. Insofar as such block diagrams, schematics, and examples contain one or more functions and/or operations, it will be understood by those skilled in the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof. In one embodiment, the present subject matter may be implemented via Application Specific Integrated Circuits (ASICs). However, those skilled in the art will recognize that the embodiments disclosed herein, in whole or in part, can be equivalently implemented in conventional integrated circuits, as one or more computer programs running on one or more computers (*e.g.*, as one or more programs running on one or more computer systems), as one or more programs running on one or more controllers (*e.g.*, microcontrollers) as one or more programs running on one or more processors (*e.g.*, microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and or firmware would be well within the skill of one of ordinary skill in the art in light of this disclosure.

Those of skill in the art will recognize that many of the methods or algorithms set out herein may employ additional acts, may omit some acts, and/or may execute acts in a different order than specified.

In addition, those skilled in the art will appreciate that the mechanisms taught herein, for example, calibration curves or lookup tables, are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment applies equally regardless of the particular type of signal bearing media used to actually carry out the distribution. Examples of signal bearing media include, but are not limited to, the following: recordable type media such as floppy disks, hard disk drives, CD ROMs, digital tape, and computer memory.

The various embodiments described above can be combined to provide further embodiments. To the extent that they are not inconsistent with the specific teachings and definitions herein, all of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification are incorporated herein by reference, in their entirety. Aspects of the embodiments can be modified, if necessary, to employ systems, circuits and concepts of the various patents, applications and publications to provide yet further embodiments.

These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

U.S. Patent Application No. 13/609,107, filed September 10, 2012 is incorporated herein by reference in its entirety.

CLAIMS

1. A circuit for use with an operational amplifier in an environment that experiences fluctuations in ambient energy levels, the operational amplifier including a first input terminal that accepts a first input signal, the first input terminal associated with a first input impedance, a second input terminal that accepts a second input signal, the second input terminal associated with a second input impedance, an output terminal that produces an output signal based on the first and the second input signals, and internal components that generate an input offset voltage and an input bias current, the circuit comprising:

a dual compensation impedance stage having a dual compensation impedance that compensates for environmentally-induced changes in the input offset voltage and the input bias current without balancing the first and second input impedances.

2. The circuit of claim 1, further comprising the operational amplifier, wherein the input offset voltage and the input bias current vary in response to the fluctuations in the ambient energy levels.

3. The circuit of claim 2, wherein the dual compensation impedance is an integral unitary portion of the operational amplifier.

4. The circuit of claim 1, wherein the first input terminal is a non-inverting input terminal, and the dual compensation impedance includes an added first resistance electrically coupled to the first input terminal.

5. The circuit of claim 4, wherein the added first resistance includes a potentiometer selectively operable to adjust the dual compensation impedance.

6. The circuit of claim 1, wherein the operational amplifier further includes an internal offset null, and the dual compensation impedance is applied to the first input terminal to compensate for the input bias current.

7. The circuit of claim 1, wherein the dual compensation impedance is proportional to a ratio of the input offset voltage and the input bias current.

8. The circuit of claim 7 wherein values of the input offset voltage and the input bias current are determined from measured data while operating the operational amplifier in a target environment.

9. The circuit of claim 7, wherein values of the input offset voltage and the input bias current are determined from a set of calibration data stored in a non-transitory storage medium, to compensate for effects of ambient energy levels in an anticipated target environment.

10. The circuit of claim 9, wherein values of the input offset voltage and the input bias current are extrapolated from the calibration data by a logic circuit.

11. The circuit of claim 10, further comprising: one or more energy level sensors, and wherein the logic circuit includes one or more energy level sensors responsive to an ambient energy level in the target environment.

12. The circuit of claim 10, wherein the energy level sensors include one or more of a temperature sensor and a radiation level sensor.

13. The circuit of claim 1, wherein a value of the dual compensation impedance is determined from data obtained in a simulated target environment.

14. The circuit of claim 4, wherein the second input terminal is an inverting input terminal, and the dual compensation impedance stage further includes a second resistance electrically coupled to the second input terminal.

15. The circuit of claim 14, wherein values of the first resistance and the second resistance are unbalanced so as to nullify effects of one or more of the input offset voltage and the input bias current.

16. The circuit of claim 14, wherein the first resistance and the second resistance are unbalanced so as to provide over-compensation for effects of one or more of input offset voltage and the input bias current.

17. The circuit of claim 14, wherein the dual compensation impedance stage further includes a ground coupled to the first input terminal and a third resistance electrically coupled between the first input terminal and the ground.

18. The circuit of claim 17, wherein the dual compensation impedance stage further includes a fourth resistance electrically coupled between the second input terminal and the output terminal.

19. A method of variable compensation for fluctuations in ambient energy levels affecting an operational amplifier, the method comprising:

sensing a first voltage and a first current at a first input terminal of the operational amplifier;

sensing a second voltage and a second current at a second input terminal of the operational amplifier, the second input terminal electrically coupled to a ground;

determining an input offset voltage based on a difference between the first voltage and the second voltage;

determining an input bias current based on a difference between the first current and the second current;

determining an input impedance from the input offset voltage and the input bias current, wherein the input impedance varies according to the fluctuations in ambient energy levels; and

electrically coupling a dual compensation impedance stage to the operational amplifier compensate for the input impedance.

20. The method of claim 19, wherein the electrically coupling a dual compensation impedance stage includes providing a first resistance that is proportional to a ratio of the input offset voltage and the input bias current.

21. The method of claim 19, further comprising

repeating the sensing and the determining in different simulated environmental conditions to generate a set of calibration data; and

determining, from the calibration data, a value of the first resistance for operation of the in an anticipated target environment.

22. The method of claim 21, further comprising sensing, in-situ, an ambient energy level in the target environment, and determining from the calibration data and the ambient energy level a value of the first resistance for operation of the operational amplifier while in the target environment.

23. The method of claim 19 further comprising adjusting the dual compensation impedance stage to adapt to environmental changes by repeating the method upon expiration of a time interval.

24. The method of claim 20, further comprising providing a second resistance at the second input terminal.

25. The method of claim 24, wherein providing the first resistance at the first input terminal, in combination with providing the second resistance at the second input terminal, creates an imbalance that nullifies an electrical effect of the input impedance.

26. The method of claim 24, wherein providing the first resistance at the first input terminal, in combination with providing the second resistance at the second input terminal, creates an imbalance that compensates for an electrical effect of the input impedance.

27. The method of claim 24, further comprising grounding the first input terminal and providing a third resistance between the first input terminal and the ground.

28. The method of claim 27, further comprising providing a fourth resistance between the second input terminal and an output terminal of the operational amplifier.

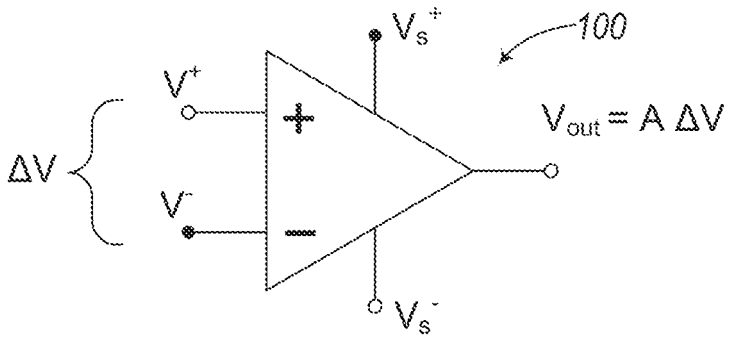

Fig. 1A
(Prior Art)

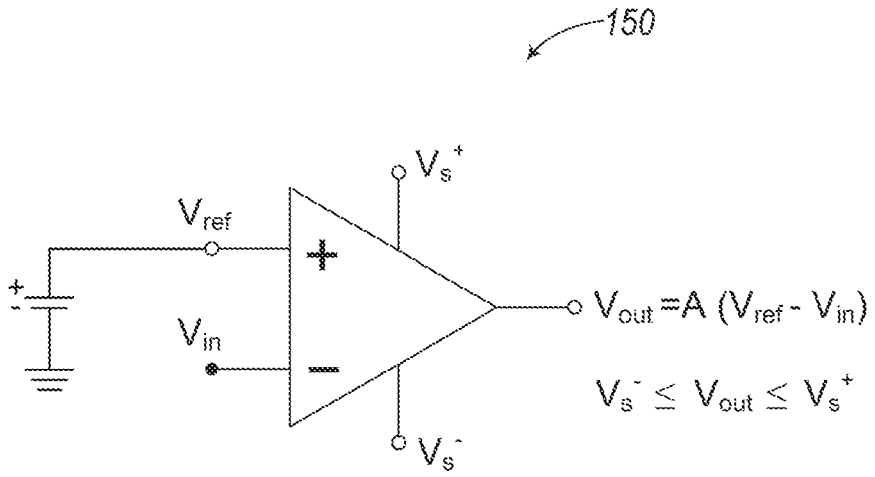

Fig. 1B
(Prior Art)

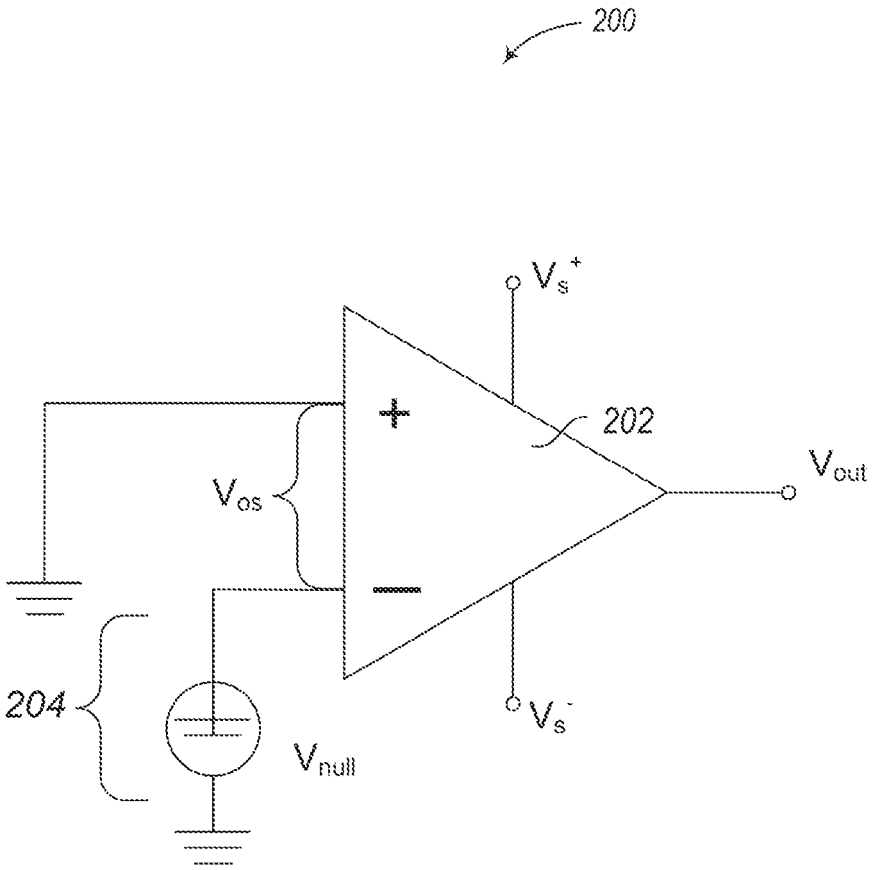

Fig. 2
(Prior Art)

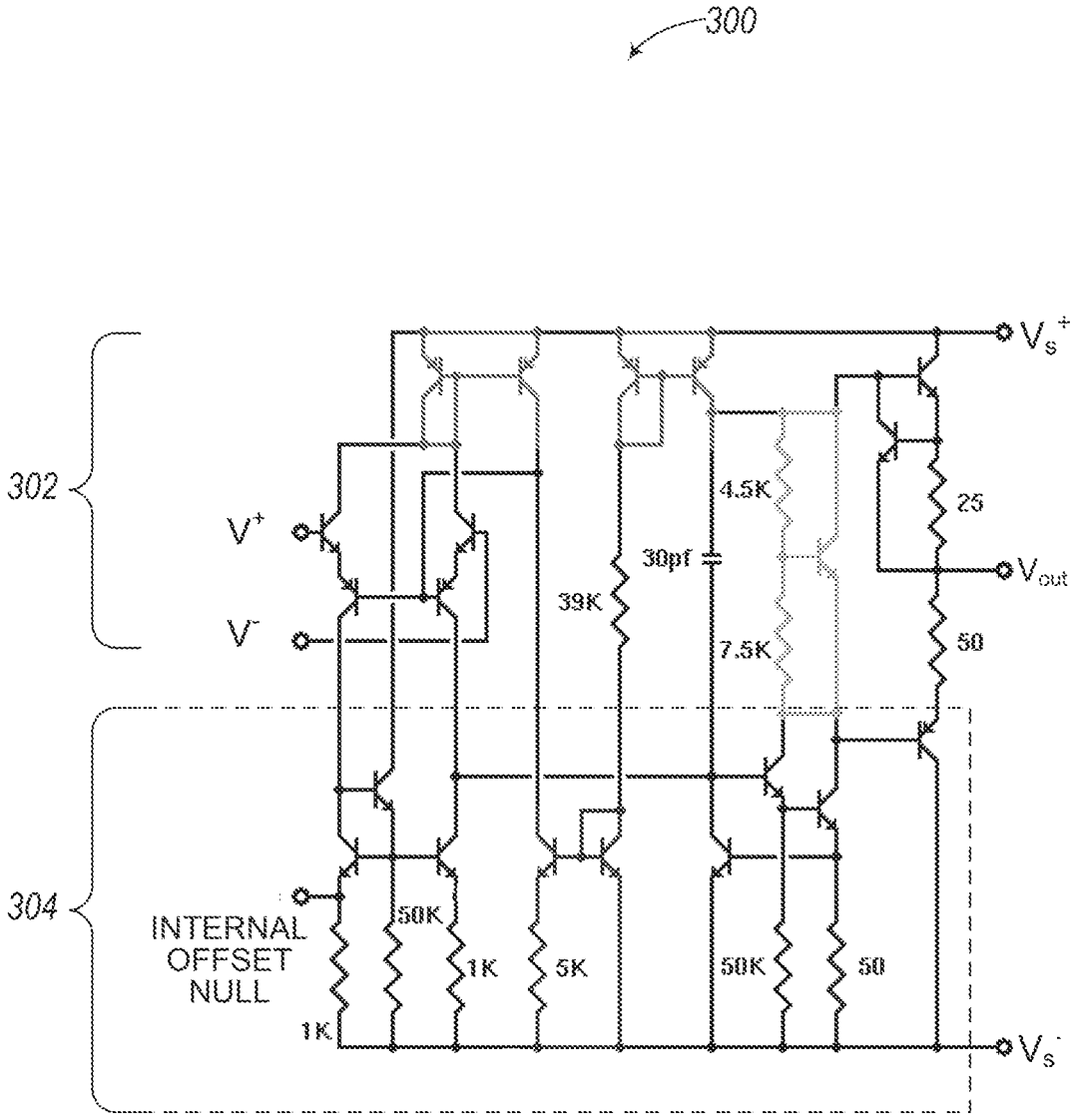

Fig. 3
(Prior Art)

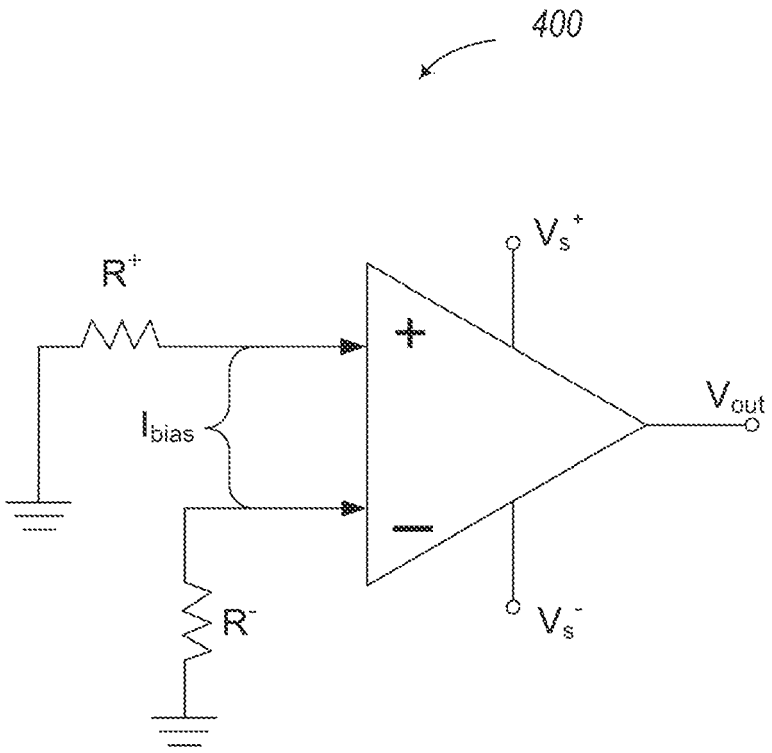

Fig. 4
(Prior Art)

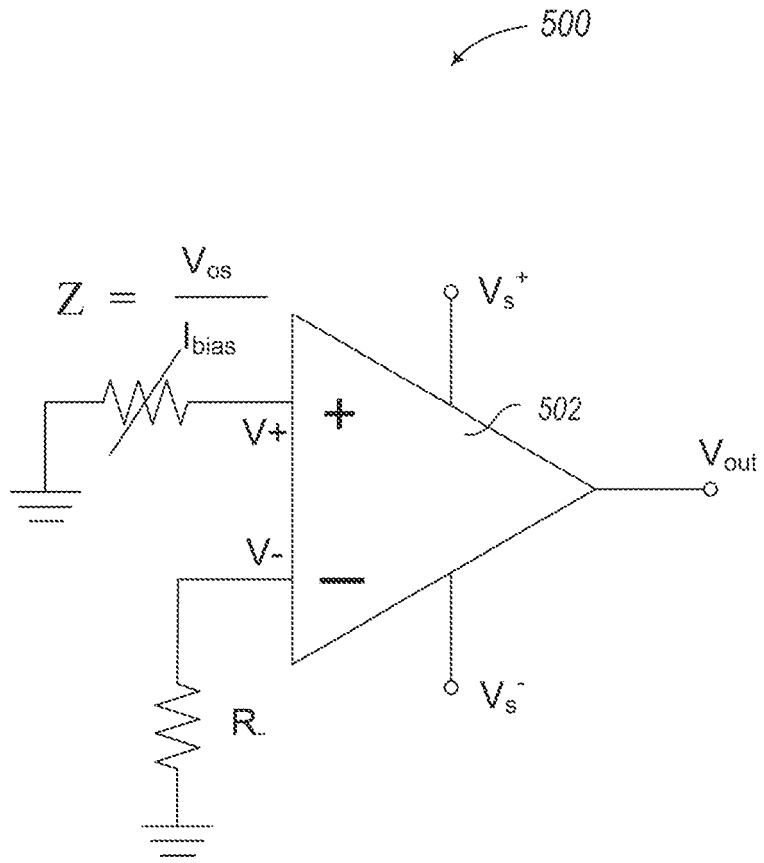

Fig. 5

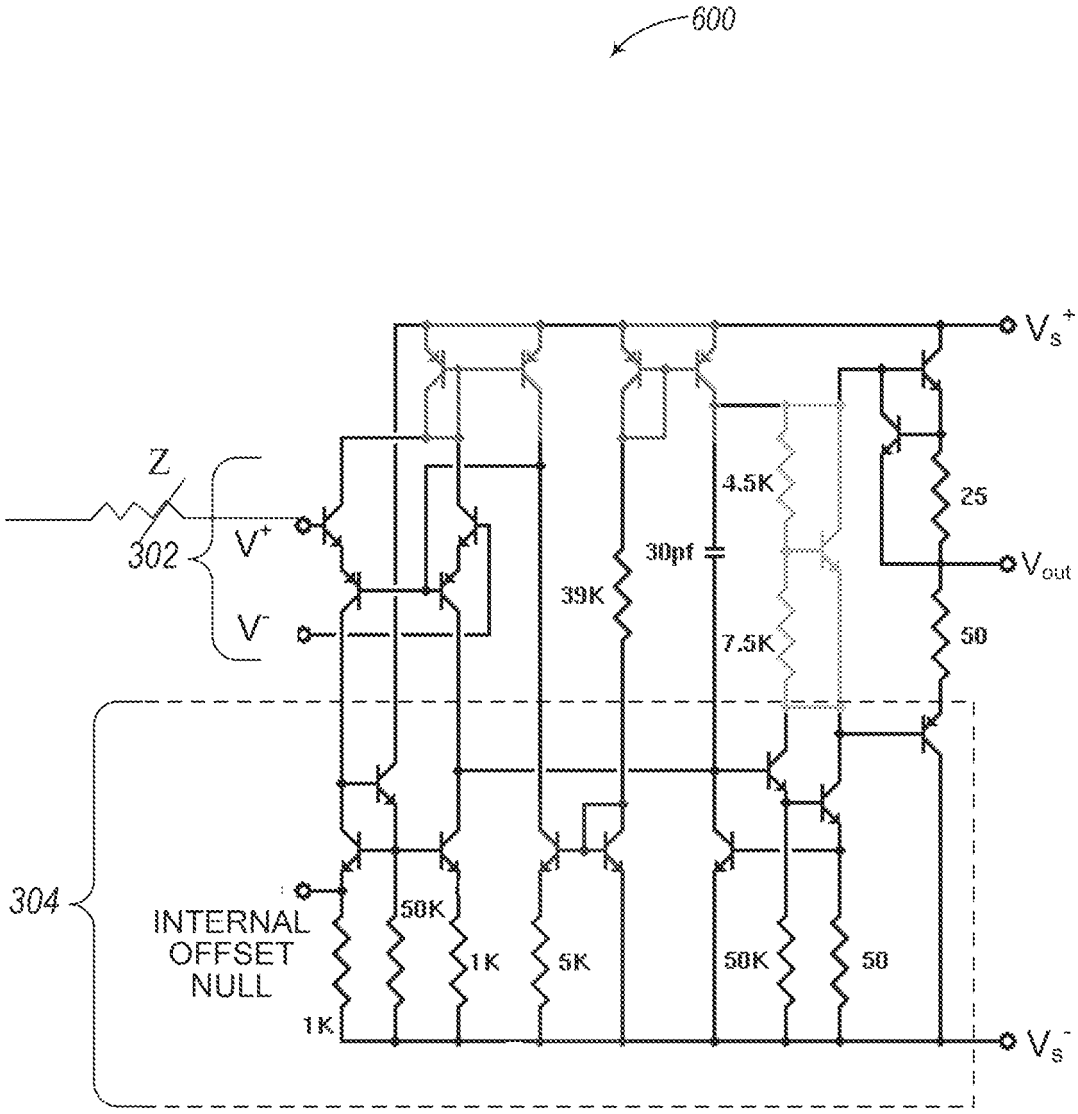
600
Z
302
V+
V-
304
INTERNAL
OFFSET
NULL
50K
1K
1K
5K
39K
30pf
4.5K
7.5K
50K
50
25
50
Vout
Vs+
Vs-

Fig. 6

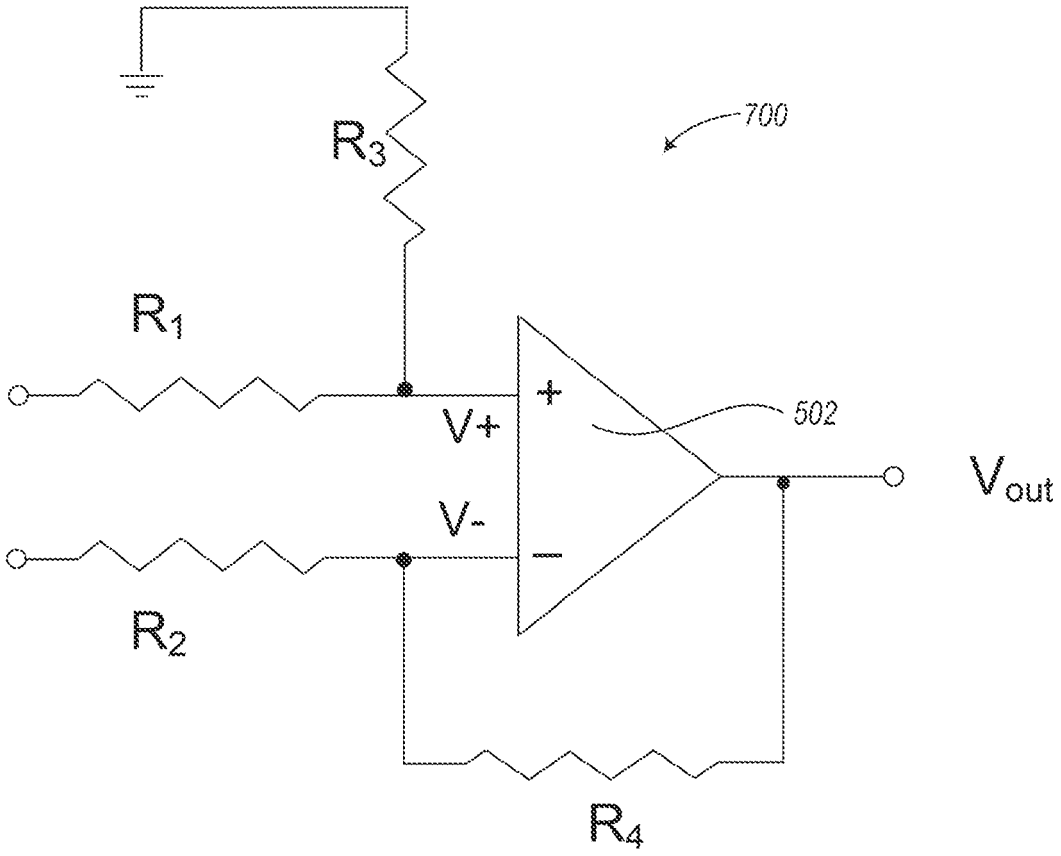

FIG. 7

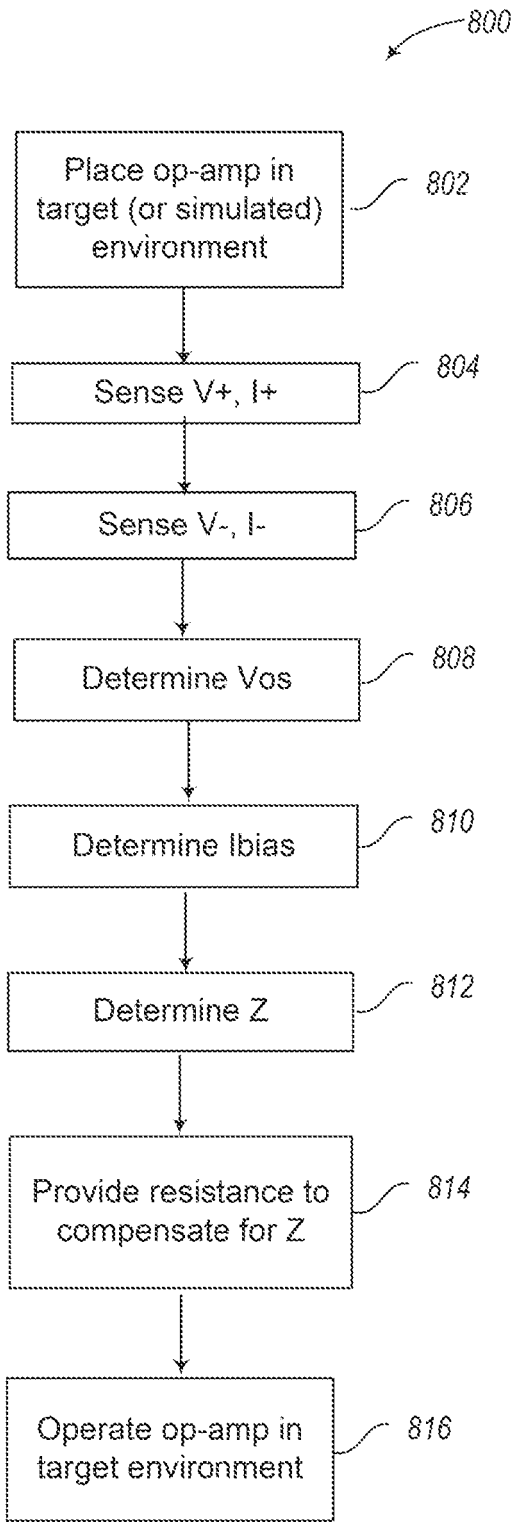
800
Place op-amp in target (or simulated) environment
802
Sense V+, I+
804
Sense V-, I-
806
Determine Vos
808
Determine Ibias
810
Determine Z
812
Provide resistance to compensate for Z
814
Operate op-amp in target environment
816

FIG. 8

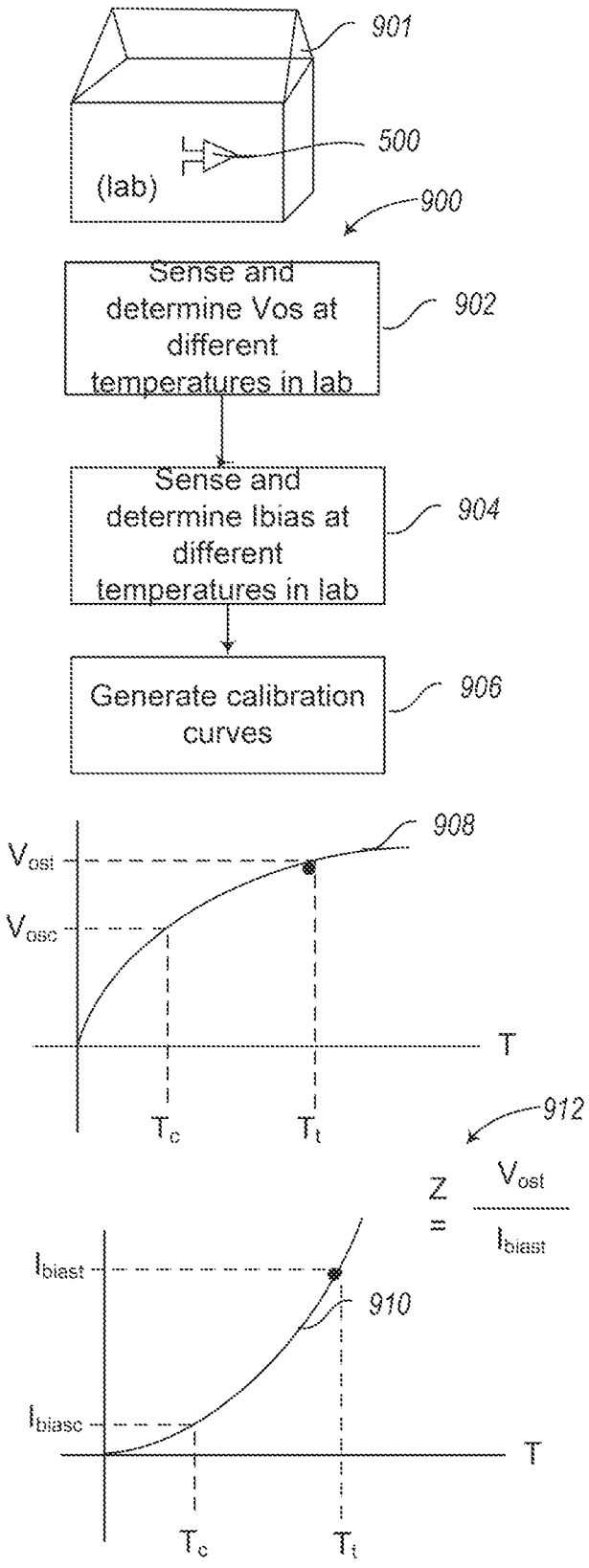
901
500
(lab)
900
Sense and determine Vos at different temperatures in lab
902
Sense and determine Ibias at different temperatures in lab
904
Generate calibration curves
906
908
Vost
Vosc
T
Tc
Tt
912
Z = Vost / Ibiast
Ibiast
910
Ibiasc
T
Tc
Tt

FIG. 9A

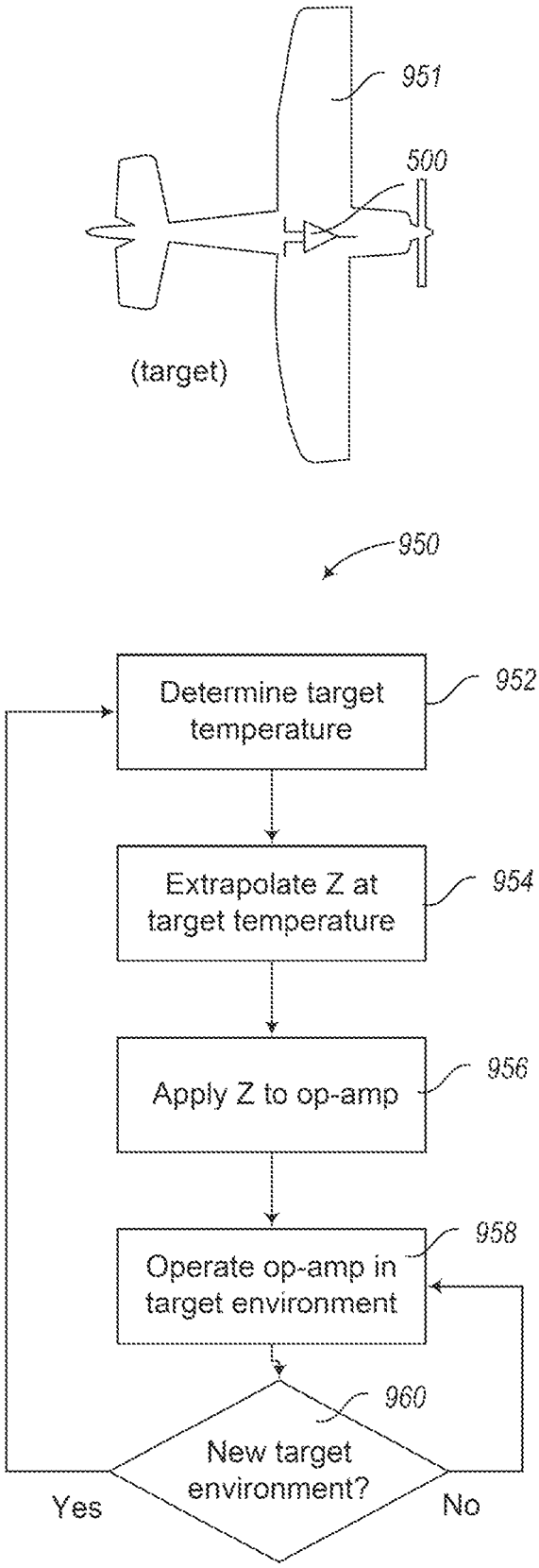
951
500
(target)
950
Determine target temperature
952
Extrapolate Z at target temperature
954
Apply Z to op-amp
956
Operate op-amp in target environment
958
960
New target environment?
Yes
No

FIG. 9B

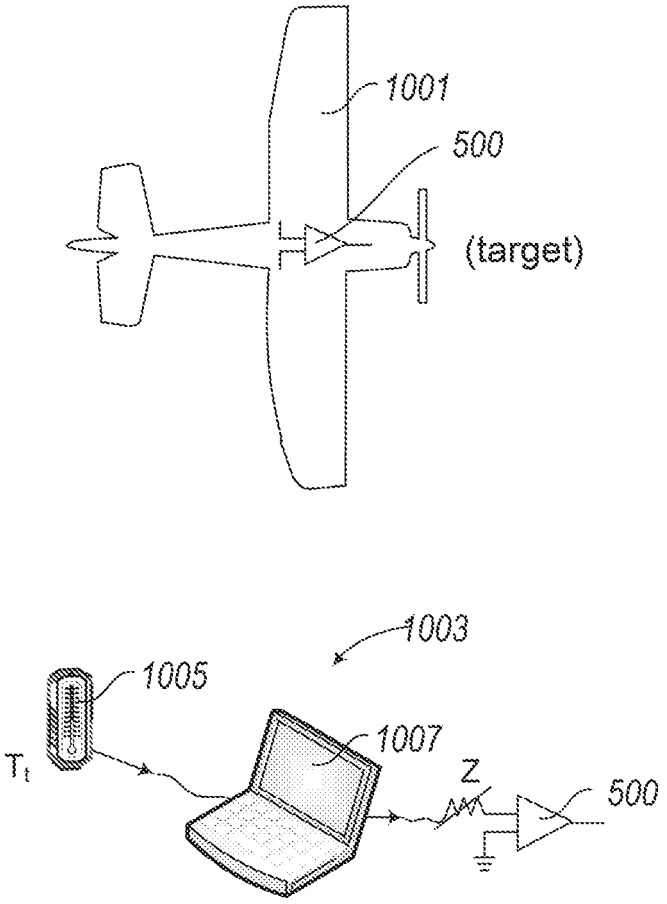

FIG 10A

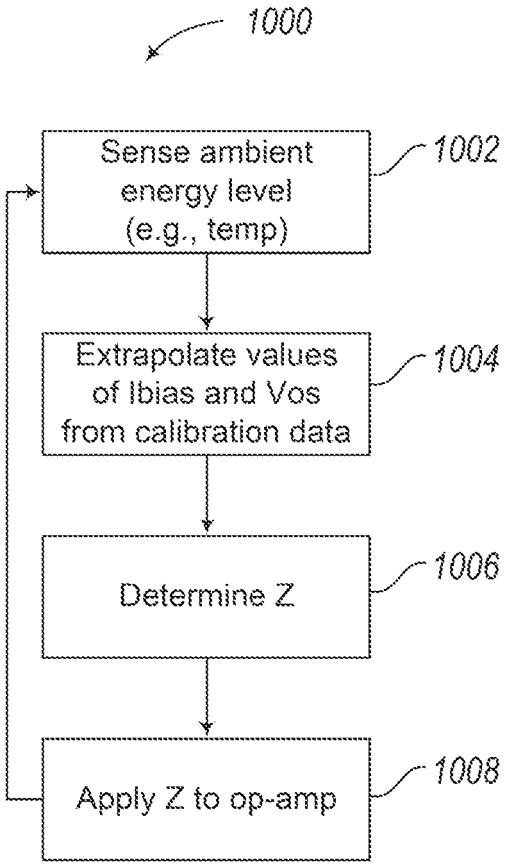

FIG 10B

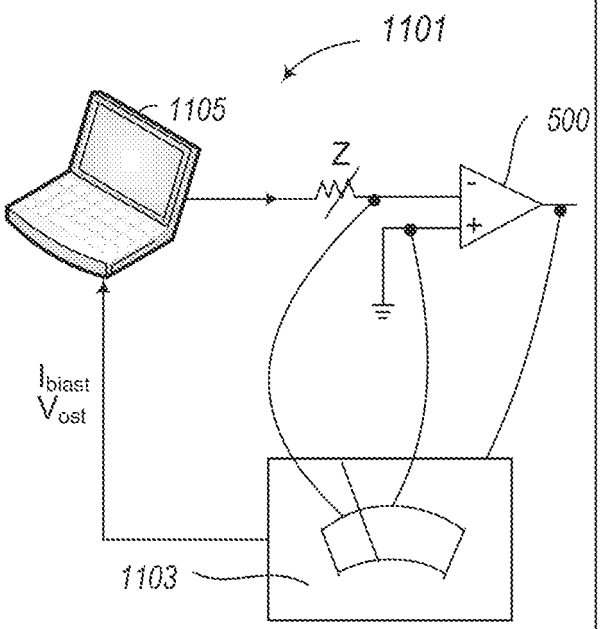

FIG 11A

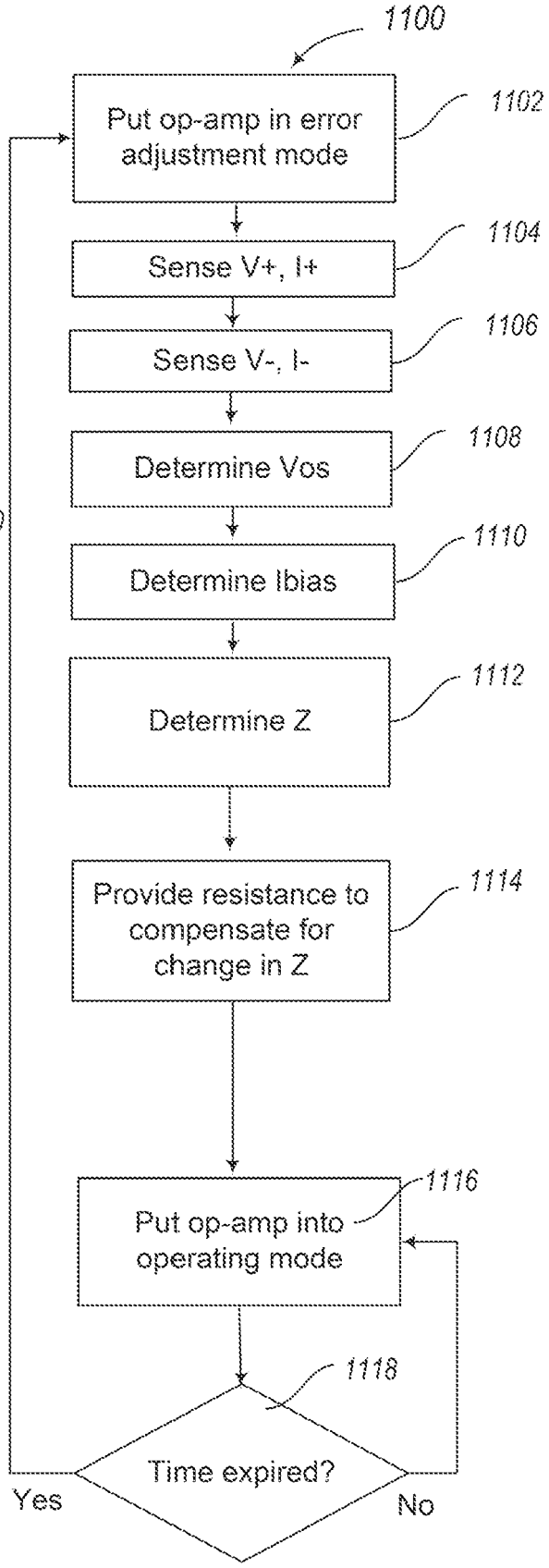

FIG 11B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/058784

A. CLASSIFICATION OF SUBJECT MATTER

H03F 3/45(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F 3/45; H03F 3/34; G01R 31/316; H03F 1/34

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: operational amplifier, compensation, nullify, cancel, impedance, input, offset, voltage, bias, current, resistance, environment, temperature, ambient, fluctuation, change

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2008-0019196 A (ROHM CO., LTD.) 03 March 2008 See paragraphs [0052]-[0054], [0059], [0067]; claim 1 and figure 1.	1-28
A	JP 2007-263944 A (FUJI ELECTRIC DEVICE TECHNOLOGY CO., LTD.) 11 October 2007 See paragraphs [0020]-[0021], [0048], [0050], [0099] and figures 4, 14.	1-28
A	JP 2001-320250 A (NEC CORP.) 16 November 2001 See paragraphs [0031]-[0045]; claim 1 and figures 1, 4.	1-28
A	JP 2002-076799 A (HYNIX SEMICONDUCTOR INC.) 15 March 2002 See paragraphs [0006]-[0009], [0011], [0025] and figures 1-4.	1-28
A	KR 10-2008-0101784 A (NATIONAL SEMICONDUCTOR CORPORATION) 21 November 2008 See paragraphs [0024], [0026]-[0045]; claim 1 and figures 1-3.	1-28

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 December 2013 (19.12.2013)	**20 December 2013 (20.12.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/058784

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 7719351 B2	18/05/2010