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(54) Matrix addressable display and driver having CRT compatibility.

(57) A matrix addressable flat panel display (100) which can be directly interfaced with a conventional CRT graphics controller and which provides both superior display quality and reduced driver complexity as compared with conventional displays. The pixels in each row of the display are formed in every other column, and the pixels in every other row are laterally shifted in both location and colour with respect to adjacent rows such that the pixels in each column are of the same colour. The colour triads, in turn, are defined by first and second laterally adjacent pixels of one row and a third pixel residing in the column intermediate the first and second pixels and in a vertically adjacent row. Since each column contains pixels of only one colour and each row pair contains complete triads, the colour select circuitry of prior art arrangements is substantially eliminated, and the display/driver is compatible with a standard CRT graphics controller. Moreover, the triad aspect ratio is 1:1, resulting in superior image quality.

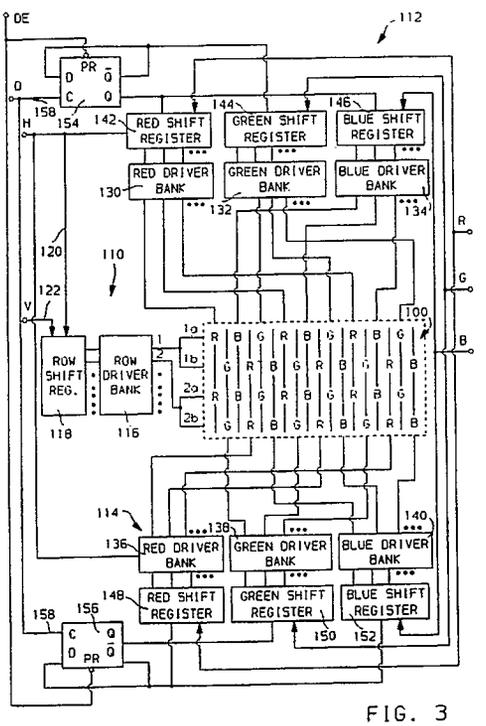

FIG. 3

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MATRIX ADDRESSABLE DISPLAY AND DRIVER HAVING CRT COMPATIBILITY

This invention relates to matrix addressable flat panel display and driver arrangements, and more particularly to a display/driver configuration which may be directly interfaced with a conventional CRT display controller.

Matrix addressable flat panel displays have become increasingly popular as an alternative to the cathode ray tube (CRT), both for television and display applications. This is particularly so in applications where the display depth is limited, such as in automotive and aerospace display panels.

However, the transition to matrix addressable flat panel displays has been slowed by the drive signal incompatibility with CRT's. Whereas, a CRT graphics controller supplies the RGB (red, green and blue) colour information in synchronism, colour element by colour element, matrix addressable display drivers typically require sequential access to the colour information. As a result, the controller must be customized to generate additional information, or the driver must be customized to accept and store synchronously generated data. Either approach adversely affects both cost and performance of the system.

An example of a conventional active matrix liquid crystal display and driver is shown in Figure 1, where the display panel and driver circuit elements are designated by the reference numerals 10 and 12, respectively. The display panel 10 comprises an N x M array of red (R), blue (B) and green (G) pixels formed at the intersections of the N laterally extending rows and the M vertically extending columns. In each row, M pixels are arranged in a predefined and uniform colour sequence, RBGRBG etc. In adjacent rows, the pixels are colour shifted in either direction by one column. Consequently, each row and each column contains pixels of all three colours.

A row-activated thin-film transistor at the intersection of each row and column applies a column-supplied control voltage to the respective pixel to control its intensity whenever the transistor is activated. Thus, the driver 12 includes a row circuit 14 for successively activating the various rows of transistors, and one or more column circuits 16, 18 for storing the appropriate control voltages. In the illustrated embodiment, the column circuit 16 supplies control voltages to the odd numbered columns and the column circuit 18 supplies control voltages to the even numbered columns.

The row circuit 14 comprises a bank 20 of individual driver circuits connected to the various rows of the display panel 10, and a shift register 22 for successively activating the driver circuits of the bank 20 at a shift frequency determined by the horizontal synchronization signal HSYNC on line 42. A vertical synchronization signal VSYNC on line 26 periodically resets the shift register 22 to the first to top row.

The column circuits 16, 18 each comprise a driver bank 28, 30 of individual driver circuits connected to the various columns of the display panel 10, and a shift register 32, 34 for receiving and storing parallel formal digital control voltage data via lines 36, 38. The control voltage data is entered into the shift register 32, 34 under control of the SHIFT CLOCK signal on line 40; when a full row of data has been entered, the HSYNC signal on line 42 signals the driver bank 28, 30 to latch the shift register data.

For display purposes, the pixels are divided into (M X N)/3 groups of colour elements or triads, each comprising a red pixel, a green pixel and a blue pixel. The pixels may be grouped linearly, as indicated by the outlined pixels in row 1, or staggered as indicated by the outlined pixels in rows 3 and 4. The red, blue and green pixel control voltage data is supplied to the driver 12 via lines 44, triad by triad. A colour select circuit designated generally by the reference numeral 45 comprises a demultiplexer (select one-of-three) 46 and a serial to parallel shift register 48 operating under the control of the DOTCLOCK signal on line 50 for suitably applying the pixel control voltage data from lines 44 to lines 36 and 38. The data on lines 44 is in serial format and is applied to the input channels of the demultiplexer 46, which presents individual colour data in succession to serial to parallel shift register 48 on line 54. Since the display columns contain different colour elements and all three pixel colours, the order of the data supplied to serial to parallel shift register 48 varies with the triad grouping and the overall display size.

The triad configuration chosen for a display can also affect the quality of the displayed image and the complexity of the colour select circuit 45. Linear triad configurations, as illustrated in row 1, reduce the complexity of the colour select circuitry, but yield reduced display quality with their 3:1 aspect ratio. Staggered triad configurations, as illustrated in rows 3 and 4, improve the display quality with a 2:1 aspect ratio, but increase the complexity of the colour select circuit 45.

A matrix addressable display in accordance with the present invention is characterised by the features specified in the characterising portion of claim 1.

The present invention is directed to an improved matrix addressable flat panel display which can be directly interfaced with a conventional CRT

graphics controller and which provides both superior display quality and reduced driver complexity.

According to the present invention, the pixels in each row of the display are formed in every other column, and the pixels in every other row are laterally shifted in both location and colour with respect to adjacent rows such that the pixels in each column are of the same colour. The colour elements, in turn, are defined by a triad of first and second horizontally adjacent pixels of one row and a third pixel residing in the column intermediate the first and second pixels and in a vertically adjacent row. Since each column contains pixels of only one colour, the colour select circuitry is greatly simplified or eliminated. Moreover, the aspect ratio of the colour element is 1:1 resulting in drive signal compatibility with CRT graphics controllers.

With the above-described display configuration, the row driver circuits activate two rows at a time, and the colour separation of the control voltage information by the graphics controller is maintained in the display driver. To this end, the column driver circuits are split into individual shift register and driver banks dedicated to processing the red, blue and green control voltage data, and a simple toggle circuit controls the flow of the information.

The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a diagram of a conventional PRIOR ART matrix addressable flat panel display and drive circuit;

Figure 2 is a diagram illustrating the configuration of a matrix addressable flat panel display according to this invention; and

Figure 3 is a diagram of a matrix addressable flat panel display and drive circuit according to this invention.

Referring to Figure 2, the reference numeral 100 generally designates a display panel according to this invention. As with the prior art panels, the display panel 100 comprises a plurality of red (R), blue (B) and green (G) pixels distributed in a row x column matrix array. However, the pixels of display panel 100 are only formed at alternate row/column intersections. In addition, the pixels of every other row (rows 1b, 2b, 3b, etc.) are laterally shifted by one column. In the illustrated embodiment, pixels reside only in the odd numbered columns of rows 1a, 2a, 3a, etc. and in the even numbered columns of rows 1b, 2b, 3b, etc. As a result, the conductor traces for pixels in the even numbered columns run between the pixels of the odd numbered columns, and the conductor traces for pixels in the odd numbered columns run between the pixels of the even numbered columns. Moreover, the colour sequence of the pixels in rows 1b, 2b, 3b, etc. is shifted so that triangular-shaped triads of red, blue and green pixels are formed in each pair of adjacent rows (1a-1b, 2a-2b, 3a-3b, etc.), as indicated by the outlined pixels in rows 1a-1B.

The above-described panel configuration has two important properties: (i) the triads have a 1:1 aspect ratio, and (2) the pixels in each column are all of the same colour. The first property provides the superior image quality of a CRT. The second property permits a reduction in the drive circuit complexity and compatibility with standard CRT graphics controllers, as described below in reference to Figure 3.

Figure 3 illustrates the display panel 100 of Figure 2, a row circuit 110, and upper and lower column circuits 112 and 114. As in the prior art display/driver of Figure 1, the row circuit 110 comprises a bank 116 of individual driver circuits connected to the various rows of the display panel 100, and a shift register 118 for successively activating the driver circuits of the bank 116 at a shift frequency determined by the horizontal sync signal HSYNC on line 120. The vertical sync signal VSYNC on line 122 periodically resets the shift register 118 to row 1. Here, however, the bank 116 activates two rows at a time -- that is, 1a and 1b, 2a and 2b, etc. Due to the triad configuration described above in reference to Figure 2, each output line of bank 116 activates all the pixels of the triads residing in the respective rows. In other words, no partial triads are activated.

The upper and lower column circuits 112, 114 each comprise a driver bank 130, 132, 134; 136, 138, 140 of red, green and blue driver circuits connected to the various columns of the display panel 100. The red driver bank 130 connected to the red pixels residing in odd numbered columns, and the red driver bank 136 is connected to the red pixels residing in even numbered columns. Similarly, the green driver bank 132 is connected to the green pixels residing in odd numbered columns, and the green driver bank 138 is connected to the green pixels residing in even numbered columns. Finally, the blue driver bank 134 is connected to the blue pixels residing in odd numbered columns, and the blue driver bank 140 is connected to the blue pixels residing in even numbered columns.

The red, green and blue driver banks 130 -140 are connected to respective red, green and blue shift registers 142, 144, 146; 148, 150, 152 which receive and store parallel format digital control volta9e data from the red, 9reen and blue serial data lines R, G and B. As with the prior art display/driver of Figure 1, the data is entered into the shift registers 142, 144, 146; 148, 150, 152 one pixel at a time. Here, however, the upper red, green and blue shift registers 142, 144 and 146 only receive control voltage data for the odd numbered panel columns, and the lower red, green and

blue shift registers 148, 150 and 152 only receive control voltage data for the even numbered panel columns.

The control voltage data is distributed between the upper and lower column circuits 112 and 114 by upper and lower flip-flops 154, 156. Both flip-flops 154 and 156 are clocked by the DOTCLOCK (D) signal on line 158, and oscillate at one-half of the DOTCLOCK frequency. Thus, the event triggering logic level transition (rising or falling edge) of upper flip-flop 154's Q output occurs at the same time as that of lower flip-flop 156's Q-bar output. Similarly, the event triggering logic level transition (rising or falling edge) of upper flip-flop 154's Q-bar output occurs at the same time as that of lower flip-flop 156's Q output. The Q output of upper flip-flop 154 enables the upper red and blue shift registers 142 and 146 to receive red and blue control voltage data while the Q-bar output enables the upper green shift register 144. The Q-bar output of lower flip-flop 156 enables the lower red and blue shift registers 148 and 152 to receive red and blue control voltage data while the Q output enables the lower green shift register 150.

A display-enable (DE) signal on line 160 presets the upper and lower flip-flops 154 and 156 to synchronize their operation with the control voltage data stream on lines R, G and B. Thus, when the first triad (rows 1a-1b, columns 1-3) of data is generated on lines R, G and B, the red and blue components are directed to upper red and blue shift registers 142 and 146, respectively, and the green component is directed to the lower green shift register 150. When the second triad (rows 1a-1b, columns 4-6) of data is generated, the red and blue components are directed to lower red and blue shift registers 148 and 152, respectively, and the green component is directed to the upper green shift register 144. When the third triad (rows 1a-1b, columns 7-9) of data is generated, the red and blue components are directed to upper red and blue shift registers 142 and 146, respectively, and the green component is directed to the lower green shift register 150, repeating the pattern of the first triad. When the fourth triad (rows 1a-1b, columns 10-12) of data is generated, the red and flue components are directed to lower red and blue shift registers 148 and 152, respectively, and the green component is directed to the upper green shift register 144, repeating the pattern of the second triad.

The above-described data process is continued until the control voltage data for each triad of rows 1a-1b is stored in the shift registers 142-152. In particular, the upper red shift register 142 will have stored the R1, R3, R5, R7, etc. data (where the numeral indicates the triad number); the upper green shift register 144 will have stored the G2, G4, G6, G8, etc. data; the upper blue shift register 146 will have stored the B_1, B_3, B_5, B_7, etc. data; the lower red shift register 148 will have stored the R2, R4, R6, R8, etc. data; the lower green shift register 150 will have stored the G1, G3, G5, G7, etc. data; and the lower blue shift register 152 will have stored the B_2, B_4, B_6, B_8, etc. data. At such time, the horizontal sync signal HSYNC on line 120 directs the driver banks 130-140 to latch the data from the respective shift registers 142-152, and the vertical sync signal VSYNC signal on line 122 directs the shift register 118 and bank 116 to activate the rows 1a-1b via driver output line 1 to suitably energize the respective pixels of display panel 100. Subsequent horizontal sync pulses HSYNC direct the row shift register 118 to activate successive row pairs as described above.

In the above manner, control voltage data for successive row-pairs of pixels is loaded into the shift registers 142-152, latched into the driver banks 130-140 and applied to the respective control panel pixels. The colour select circuitry 45 of the prior art display/driver is substantially eliminated since colour separation of the control voltage date is maintained by the drive circuitry.

Claims

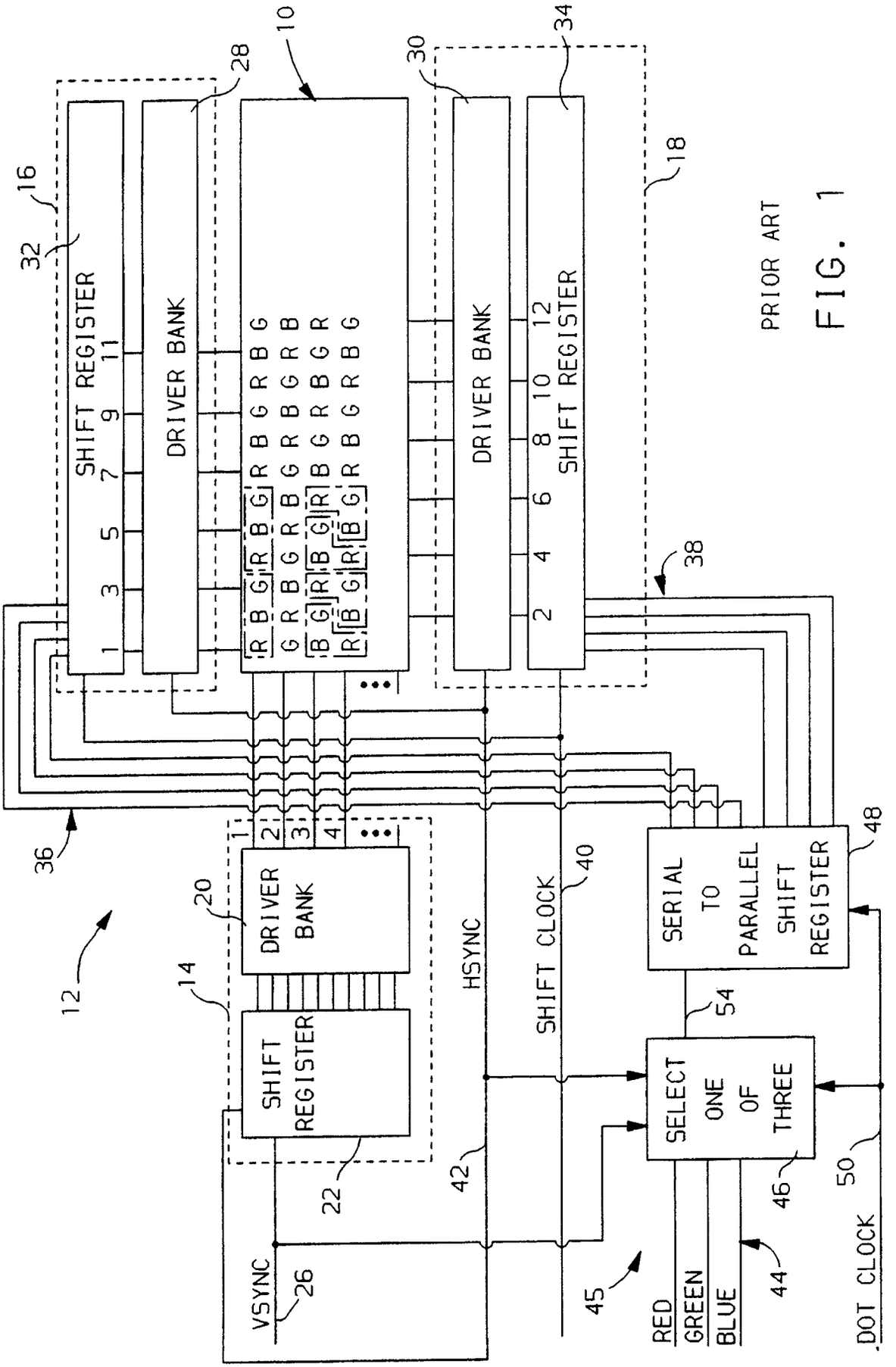
1. A matrix addressable display (100) including N individually controlled red (R), green (G) and blue (B) pixels disposed at the intersections of a matrix array of vertically extending columns and laterally extending rows, grouped to define N/3 triads consisting of a red, blue and green pixel, characterised in that the pixels in each row of the display are disposed in every other column and in a predefined, uniform colour sequence; the pixels in every other row are laterally shifted in both location and colour with respect to adjacent rows such that the pixels in each column are of the same colour; and each of said colour elements is defined by a triad of first and second laterally adjacent pixels of one row and a third pixel disposed in the column intermediate said first and second pixels and in a vertically adjacent row.

2. A matrix addressable flat panel display, comprising a display panel (100) including N individually controllable red, green and blue pixels disposed in a matrix array of vertically extending columns and laterally extending rows; characterised in that the pixels (1) in each row are disposed in every other column in a repetitive colour sequence, and (2) in every other row are laterally shifted in both location and colour with respect to adjacent rows such that the pixels in each column are of the same colour; by column driver means (130-152) for receiving and storing synchronously generated red, green

and blue control voltage information for application to the pixels of a given display panel row; and by row driver means (116-118) for activating the given display panel row to enable application of the stored control voltage information to the pixels disposed therein.

3. A matrix addressable flat panel display as claimed in claim 2, wherein the column driver means comprises red register means (142,148) for receiving and storing the red control voltage information; green register means (144,150) for receiving and storing the green control voltage information; and blue register means (146,152) for receiving and storing the blue control voltage information.

4. A matrix addressable flat panel display as claimed in claim 2, wherein the column driver means comprises first red, green and blue register means (142-146) for receiving and storing red, green and blue control voltage information for pixels disposed in odd columns of the display panel (100); second red, green and blue register means (148-152) for receiving and storing red, green and blue control voltage information for pixels disposed in even columns of the display panel; and means (154,156) for (1) directing red, green and blue control voltage information corresponding to pixels disposed in the odd columns to the first red, green and blue register means, and (2) directing red, green and blue control voltage information corresponding to pixels disposed in the even columns to the second red, green and blue register means.



PRIOR ART

FIG. 1

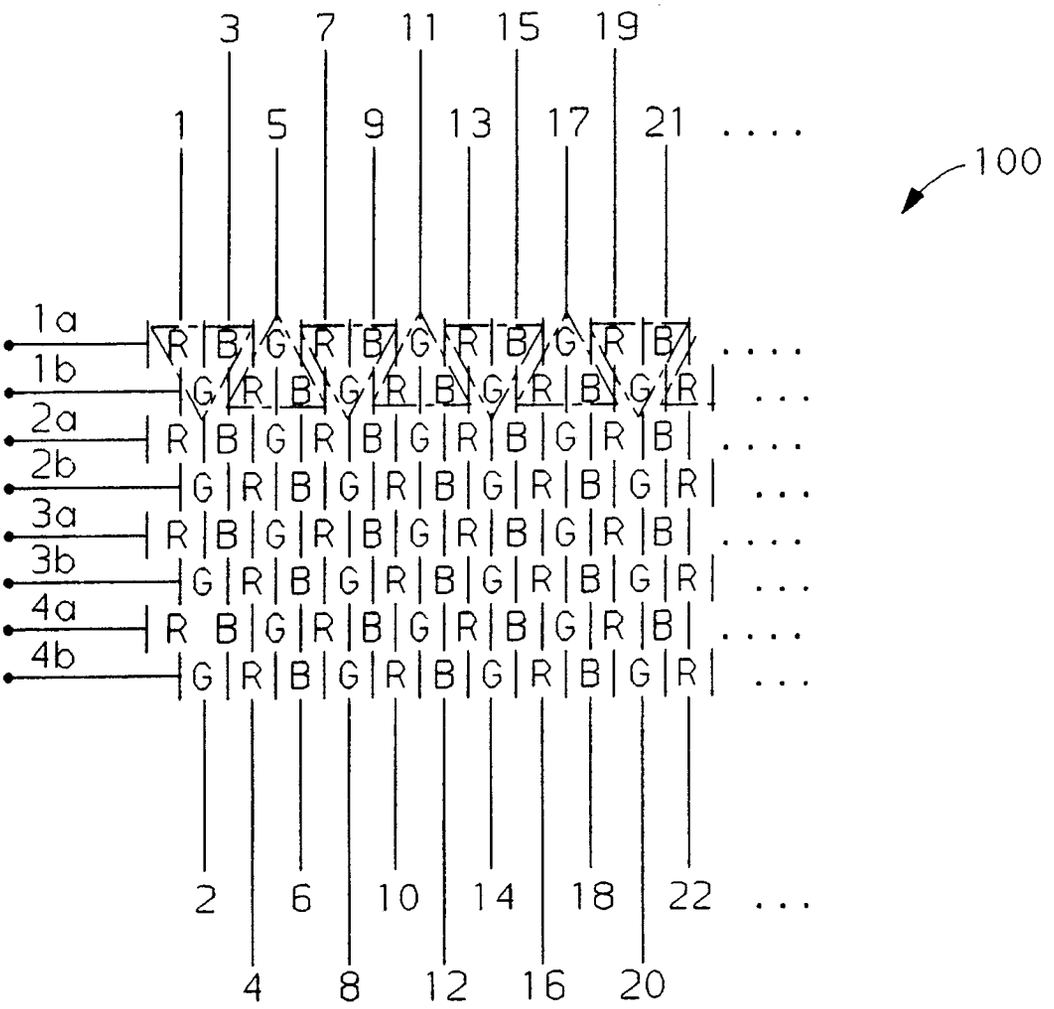

ODD COLUMNS:
3 7 11 15 19
1 5 9 13 17 21 ....
100
1a
1b
2a
2b
3a
3b
4a
4b
R B G R B G R B G R B ....
G R B G R B G R B G R ...
2 6 10 14 18 22 ...
4 8 12 16 20
EVEN COLUMNS:

FIG. 2

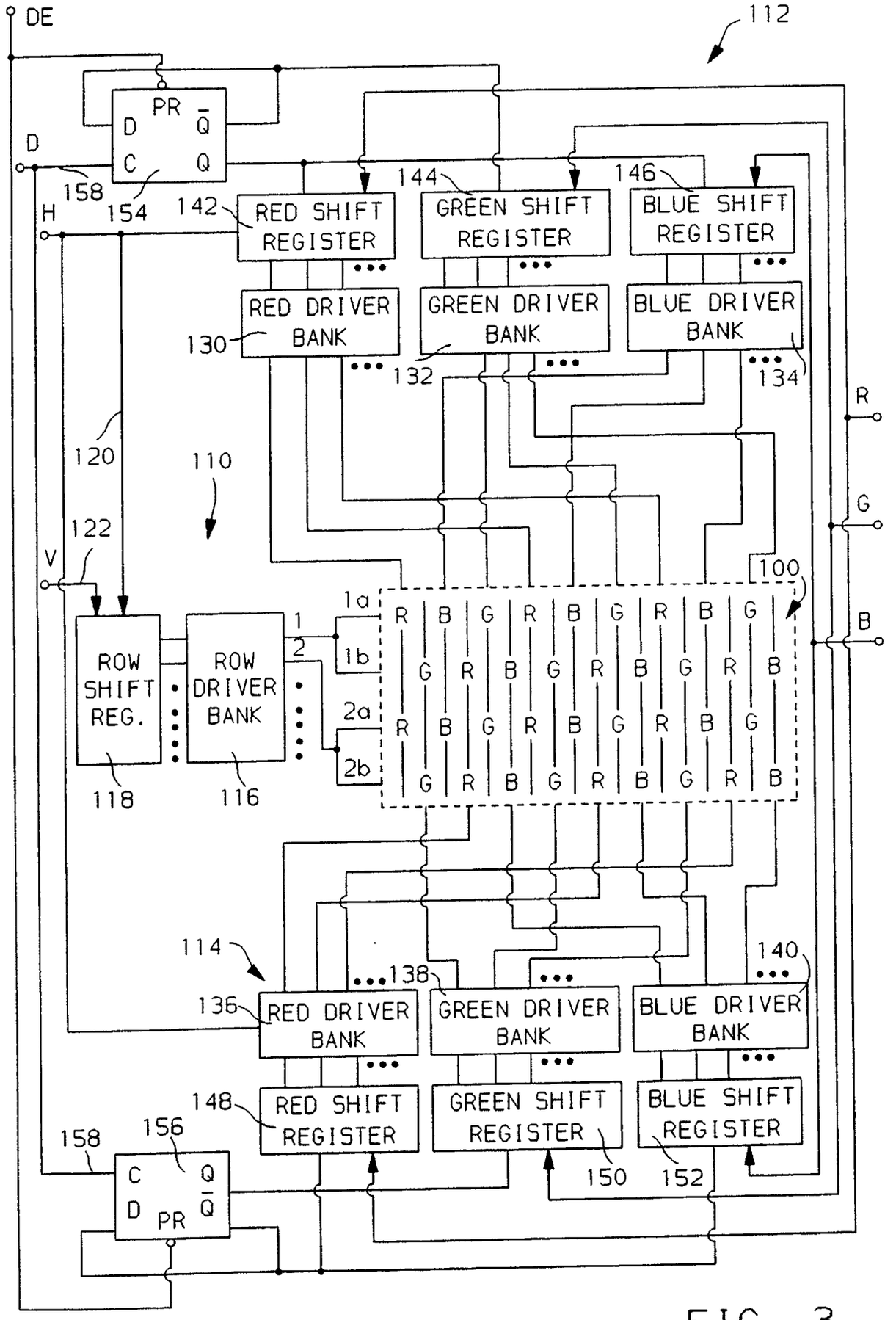

DE
112
PR
D
Q
C
Q
D
158
154
H
142
RED SHIFT REGISTER
144
GREEN SHIFT REGISTER
146
BLUE SHIFT REGISTER
RED DRIVER BANK
130
GREEN DRIVER BANK
132
BLUE DRIVER BANK
134
R
120
110
G
122
V
100
B
1a
1
2
1b
2a
2b
ROW SHIFT REG.
ROW DRIVER BANK
118
116
R B G R B G R B G R B G
114
138
140
136
RED DRIVER BANK
GREEN DRIVER BANK
BLUE DRIVER BANK
148
RED SHIFT REGISTER
GREEN SHIFT REGISTER
BLUE SHIFT REGISTER
158
156
C
Q
D
PR
Q
150
152

FIG. 3