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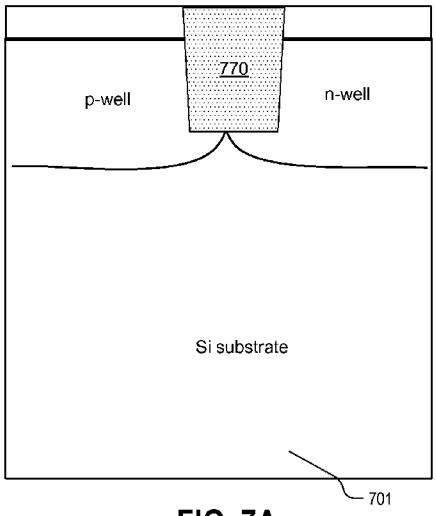


FIG. 7A

(57) Abstract: Methods and apparatuses relate to implanting a surface of a semiconductor substrate with dopants, making undoped semiconductor material directly on the surface implanted with the dopants, and making a transistor with a transistor channel in the undoped semiconductor material, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

METHOD AND APPARATUS WITH CHANNEL STOP DOPED DEVICES

Inventors: Victor Moroz

BACKGROUND

Field

[0001] The present technology relates to methods and apparatuses for channel stop doping, which can decrease the effect of parasitic transistors and improve the current of small dimension transistors.

Description of Related Art

[0002] Small dimension transistors such as finFETs and planar transistors are particularly sensitive to changes in the density of dopants in the transistor channel. Accordingly, a fabrication goal is to decrease or eliminate dopants in the transistor channel.

[0003] One approach is to form shallow trench isolation (STI) oxide regions, and then perform high implant energy implants through the semiconductor surface to form the n-wells and p-wells. However, such an approach has the side effect of undesirable channel doping in the surface of the semiconductor, which runs counter to the original goal of decreasing or eliminating dopants in the transistor channel. Such an approach also fails to have abrupt doping junctions between the lightly doped or undoped channel, and the moderately to heavily doped semiconductor material underlying the channel.

SUMMARY

[0004] Various embodiments are directed to channel stop doping.

[0005] One aspect of the technology is a method of performing channel stop doping in an integrated circuit, comprising:

[0006] implanting a surface of a semiconductor substrate with dopants;

[0007] making undoped semiconductor material directly on the surface implanted with the dopants; and

[0008] making a transistor with a transistor channel in the undoped semiconductor material, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

[0009] Another aspect of the technology is a nontransitory computer readable medium with computer executable instructions determining a layout of an integrated circuit design. The computer executable instructions include:

[0010] first computer executable instructions defining first layout locations for implanting a surface of a semiconductor substrate with dopants; and

[0011] second computer executable instructions defining second layout locations making a transistor with a transistor channel in the undoped semiconductor material, the undoped semiconductor material directly on the surface implanted with the dopants, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

[0012] Another aspect of the technology is a set of lithographic masks determining a layout of an integrated circuit design, including:

[0013] a first lithographic mask defining first layout locations for implanting a surface of a semiconductor substrate with dopants; and

[0014] a second lithographic mask defining second layout locations making a transistor with a transistor channel in the undoped semiconductor material, the undoped semiconductor material directly on the surface implanted with the dopants, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

[0015] Another aspect of the technology is a computer system for laying out an integrated circuit design. The computer system comprises a processor and a memory, and generates a layout of the integrated circuit design that defines a plurality of masks. The computer system is configured to perform computer executable instructions comprising:

[0016] first computer executable instructions defining first layout locations for implanting a surface of a semiconductor substrate with dopants; and

[0017] second computer executable instructions defining second layout locations making a transistor with a transistor channel in the undoped semiconductor material, the undoped semiconductor material directly on the surface implanted with the dopants, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

[0018] The various aspects of the technology have various embodiments.

[0019] In some embodiments, it is unnecessary to define layout locations for making the undoped semiconductor material directly on the surface implanted with the dopants. If both the NMOS and the PMOS channels are built with the same undoped semiconductor, such as Si, then

the undoped semiconductor material can be grown on the entire chip, such that no mask is necessary.

[0020] In other embodiments, third layout locations are defined for making undoped semiconductor material directly on the surface implanted with the dopants. Different undoped semiconductors can be grown for the NMOS and the PMOS transistors, such as InGaAs and Ge. Such locations can be defined via computer executable instructions or a lithographic mask, where the computer executable instructions can be on a nontransitory computer readable medium, or on a computer system configured to perform the instructions.

[0021] In some embodiments, the transistor is a finFET or a planar transistor.

[0022] In some embodiments, the implanted dopants provide latchup protection of the transistor against other structures.

[0023] In some embodiments, the transistor is one of a plurality of transistors with the transistor channel in the undoped semiconductor material. The transistor channels of plurality of transistors share the same number of dopants.

[0024] Other aspects are directed to a computer readable medium storing computer instructions to perform a method of designing an integrated circuit, the method for use by a computer system having a processor and memory. The computer instructions are executable by the computer system to design the integrated circuit as described herein.

[0025] Other aspects are directed to a computer system designing an integrated circuit, comprising a processor and memory, configured to design an integrated circuit as described herein.

[0026] Other aspects are directed to a method of operating an integrated circuit as described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] Figure 1 shows a simplified representation of an illustrative integrated circuit design flow incorporating features of the technology.

[0028] Figure 2A is a simplified block diagram of a computer system that can be used to implement software incorporating aspects of the technology.

[0029] Figure 2B is a memory that can be used to implement aspects of the technology.

[0030] Figure 2C is an integrated circuit created with the described technology.

[0031] Figure 3A shows mid-energy implants of p-type dopants such as boron into the silicon substrate.

[0032] Figure 3B is a doping graph that shows dopant implant depth versus dopant concentration with respect to Figure 3A.

[0033] Figure 4A shows mid-energy implants of n-type dopants such as phosphorus into the silicon substrate.

[0034] Figure 4B is a doping graph that shows dopant implant depth versus dopant concentration with respect to Figure 4A.

[0035] Figure 5A shows the p-well and n-well formed from annealing and implantation of dopants.

[0036] Figure 5B is a doping graph that shows the dopant implant depth versus dopant concentration for the p-well with respect to Figure 5A.

[0037] Figure 5C is a doping graph that shows the dopant implant depth versus dopant concentration for the n-well with respect to Figure 5A.

[0038] Figure 6A shows epitaxial silicon above the p-well and n-well formed from annealing and implantation of dopants.

[0039] Figure 6B is a doping graph that shows the dopant implant depth versus dopant concentration for the p-well with respect to Figure 6A.

[0040] Figure 6C is a doping graph that shows the dopant implant depth versus dopant concentration for the n-well with respect to Figure 6A.

[0041] Figure 7A shows the formation of shallow trench isolation (STI) regions in between the p-well and the n-well.

[0042] Figure 7B is a doping graph that shows the dopant implant depth versus dopant concentration for the p-well with respect to Figure 7A.

[0043] Figure 7C is a doping graph that shows the dopant implant depth versus dopant concentration for the n-well with respect to Figure 7A.

[0044] Figure 8 is a cross-section of finFET transistors, where the fin structures of the finFET transistors have been made according to the process flow of Figures 1-5.

DETAILED DESCRIPTION

[0045] Figure 1 is a simplified representation of an integrated circuit design flow. As with all flowcharts herein, it will be appreciated that many of the steps of Figure 1 can be combined, performed in parallel or performed in a different sequence without affecting the functions achieved. In some cases a rearrangement of steps will achieve the same results only if certain other changes are made as well, and in other cases a rearrangement of steps will achieve the same results only if certain conditions are satisfied.

[0046] At a high level, the process of Figure 1 starts with the product idea (block 100) and is realized in an EDA (Electronic Design Automation) software design process (block 110). When the design is finalized, the fabrication process (block 150) and packaging and assembly processes (block 160) occur, ultimately resulting in finished integrated circuit chips (result 170).

[0047] The EDA software design process (block 110) is actually composed of a number of steps 112-130, shown in linear fashion for simplicity. In an actual integrated circuit design process, the particular design might have to go back through steps until certain tests are passed. Similarly, in any actual design process, these steps may occur in different orders and combinations. This description is therefore provided by way of context and general explanation rather than as a specific, or recommended, design flow for a particular integrated circuit.

[0048] A brief description of the component steps of the EDA software design process (block 110) will now be provided. The following stages reflect the improved device design using channel stop doping.

[0049] System design (block 112): The designers describe the functionality that they want to implement, they can perform what-if planning to refine functionality, check costs, etc. Hardware-software architecture selection can occur at this stage. Example EDA software products that have been available from Synopsys, Inc. that could be used at this step include Model Architect, Saber, System Studio, and DesignWare® products.

[0050] Logic design and functional verification (block 114): At this stage, high level description language (HDL) code, such as VHDL or Verilog code, is written for modules in the system and the design is checked for functional accuracy. More specifically, the design is checked to ensure that it produces the correct outputs in response to particular input stimuli. Example EDA software products that have been available from Synopsys, Inc. that can be used at this step include VCS, VERA, DesignWare®, Magellan, Formality, ESP and LEDA products.

[0051] Synthesis and design for test (block 116): Here, the VHDL/Verilog code is translated to a netlist. The netlist can be optimized for the target technology. Additionally, the design and implementation of tests to permit checking of the finished chip occur. Example EDA software products that have been available from Synopsys, Inc. that could be used at this step include Design Compiler®, Physical Compiler, Test Compiler, Power Compiler, FPGA Compiler, TetraMAX, and DesignWare® products.

[0052] Netlist verification (block 118): At this step, the netlist is checked for compliance with timing constraints and for correspondence with the VHDL/Verilog source code. Example EDA software products that have been available from Synopsys, Inc. that can be used at this step include Formality, PrimeTime, and VCS products.

[0053] Design planning (block 120): Here, an overall floor plan for the chip is constructed and analyzed for timing and top-level routing. Example EDA software products that have been available from Synopsys, Inc. that can be used at this step include Astro and IC Compiler products.

[0054] Physical implementation (block 122): The placement (positioning of circuit elements) and routing (connection of the same) occurs at this step. Example EDA software products that have been available from Synopsys, Inc. that can be used at this step include AstroRail, Primetime, and Star RC/XT products.

[0055] Analysis and extraction (block 124): At this step, the circuit function is verified at a transistor level; this in turn permits what-if refinement. Example EDA software products that have been available from Synopsys, Inc. that can be used at this stage include Custom Designer, AstroRail, PrimeRail, Primetime, and Star RC/XT products.

[0056] Physical verification (block 126): At this stage various checking functions are performed to ensure correctness for: manufacturing, electrical issues, lithographic issues, and circuitry. Example EDA software products that have been available from Synopsys, Inc. that can used at this stage include the Hercules product.

[0057] Tape-out (block 127): This stage provides the "tape-out" data for production of masks for lithographic use to produce finished chips. Example EDA software products that have been available from Synopsys, Inc. that can be used at this stage include the CATS(R) family of products.

[0058] Resolution enhancement (block 128): This stage involves geometric manipulations of the layout to improve manufacturability of the design. Example EDA software products that have been available from Synopsys, Inc. that can be used at this stage include Proteus/Progen, ProteusAF, and PSMGen products.

[0059] Mask preparation (block 130): This stage includes both mask data preparation and the writing of the masks themselves. Example EDA software products that have been available from Synopsys, Inc. that can be used at this stage include CATS(R) family of products.

[0060] The integrated circuit manufacturing flow includes a parallel flow, as follows:

[0061] (1) Develop individual process steps for manufacturing the integrated circuit. This can be modeled with the Synopsys tools "Sentaurus Process", "Sentaurus Topography", and "Sentaurus Lithography". The input information here is the process conditions like temperature, reactor ambient, implant energy, etc. The output information is the change in geometry or doping profiles or stress distribution.

[0062] (2) Integrate the individual process steps into the complete process flow. This can be modeled with the Synopsys tool "Sentaurus Process". The input information here is the collection of the process steps in the appropriate sequence. The output is the geometry, the doping profiles, and the stress distribution for the transistors and the space in between the transistors.

[0063] (3) Analyze performance of the transistor manufactured with this process flow. This can be done with the Synopsys tool "Sentaurus Device". The input information here is the output of step (3) and the biases applied to transistor terminals. The output information is the currents and capacitances for each bias combination.

[0064] (4) If necessary, modify the process steps and the process flow to achieve the desired transistor performance. This can be done iteratively by using the Synopsys tools mentioned above.

[0065] Once the process flow is ready, it can be used for manufacturing multiple circuit designs coming from different fabless companies. The EDA flow can be used by such fabless companies. The parallel flow described here is used at a foundry to develop a process flow that can be used to manufacture designs coming from their fabless customers. A combination of the process flow and the masks are used to manufacture any particular circuit. If the integrated circuit is manufactured at an IDM (integrated device manufacturer) company instead of the combination of a fabless company and a foundry, then both parallel flows described above are done at the same IDM company.

[0066] There is also a bridge between these tools and the EDA tools. The bridge is a Synopsys tool "Seismos" that applies compact proximity models for particular circuit design and layout to obtain netlist with instance parameters for each individual transistor in the circuit as a function of its neighborhood and stress, including material conversion stress. This netlist is used in the analysis step.

[0067] Figure 2A is a simplified block diagram of a computer system 210 suitable for use with embodiments of the technology. Computer system 210 typically includes at least one processor 214 which communicates with a number of peripheral devices via bus subsystem 212. These peripheral devices may include a storage subsystem 224, comprising a memory subsystem 226 and a file storage subsystem 228, user interface input devices 222, user interface output devices 220, and a network interface subsystem 216. The input and output devices allow user interaction with computer system 210. Network interface subsystem 216 provides an interface to outside networks, including an interface to communication network 218, and is coupled via communication network 218 to corresponding interface devices in other computer systems.

Communication network 218 may comprise many interconnected computer systems and communication links. These communication links may be wireline links, optical links, wireless links, or any other mechanisms for communication of information. While in one embodiment, communication network 218 is the Internet, communication network 218 may be any suitable computer network.

[0068] User interface input devices 222 may include a keyboard, pointing devices such as a mouse, trackball, touchpad, or graphics tablet, a scanner, a touchscreen incorporated into the display, audio input devices such as voice recognition systems, microphones, and other types of input devices. In general, use of the term "input device" is intended to include all possible types of devices and ways to input information into computer system 210 or onto communication network 218.

[0069] User interface output devices 220 may include a display subsystem, a printer, a fax machine, or non-visual displays such as audio output devices. The display subsystem may include a cathode ray tube (CRT), a flat-panel device such as a liquid crystal display (LCD), a projection device, or some other mechanism for creating a visible image. The display subsystem may also provide non-visual display such as via audio output devices. In general, use of the term "output device" is intended to include all possible types of devices and ways to output information from computer system 210 to the user or to another machine or computer system.

[0070] Storage subsystem 224 stores the basic programming and data constructs that provide the functionality of some or all of the EDA tools described herein, including cell library devices having channel stop doping and tools applied for development of a layout using the library and corresponding manufacturing. These software modules are generally executed by processor 214.

[0071] Memory subsystem 226 typically includes a number of memories including a main random access memory (RAM) 230 for storage of instructions and data during program execution and a read only memory (ROM) 232 in which fixed instructions are stored. File storage subsystem 228 provides persistent storage for program and data files, and may include a hard disk drive, a floppy disk drive along with associated removable media, a CD-ROM drive, an optical drive, or removable media cartridges. The databases and modules implementing the functionality of certain embodiments may be stored by file storage subsystem 228.

[0072] Bus subsystem 212 provides a mechanism for letting the various components and subsystems of computer system 210 communicate with each other as intended. Although bus subsystem 212 is shown schematically as a single bus, alternative embodiments of the bus subsystem may use multiple busses.

[0073] Computer system 210 itself can be of varying types including a personal computer, a portable computer, a workstation, a computer terminal, a network computer, a television, a mainframe, or any other data processing system or user device. Due to the ever-changing nature of computers and networks, the description of computer system 210 depicted in Figure 2A is intended only as a specific example for purposes of illustrating the preferred embodiments. Many other configurations of computer system 210 are possible having more or less components than the computer system depicted in Figure 2A.

[0074] Figure 2B shows a memory 240 such as a non-transitory, computer readable data storage medium associated with file storage subsystem 228, and/or with network interface subsystem 216 can include a data structure specifying a circuit design that includes cell library devices having channel stop doping. The memory 240 can be a hard disk, a floppy disk, a CD-ROM, an optical medium, removable media cartridge, or other medium that stores computer readable data in a volatile or non-volatile form. The memory 240 is shown storing a circuit design 280 including, for example, an HDL description of a circuit design that includes one or more cell library devices having channel stop doping. Figure 2C is a block representing an integrated circuit 290 created with the described technology that includes one or more cell library devices having channel stop doping.

[0075] Figure 3A shows mid-energy implants of p-type dopants such as boron into the silicon substrate 301. A photolithographically defined pattern of photoresist 303 determines ion implantation windows. The final resting position of the implants is shown as slightly impinging from the volume under the open windows, to the volume covered by the photoresist.

[0076] The doping graph 302 of Figure 3B shows dopant implant depth versus dopant concentration. The implants are "mid-energy" in that neither ultra low energies like below 1 keV nor super high energies like above 500 keV are required. The doping concentration peak of over 10^{19} cm^{-3} is below the surface of the silicon substrate 401, but shallower than 100 nm from the surface of the silicon substrate 301. The target dopant peak concentrations are in the range from 10^{17} cm^{-3} to 10^{21} cm^{-3}. The target dopant peak depths are from zero to 500 nm from the surface.

[0077] Figure 4A shows mid-energy implants of n-type dopants such as phosphorus into the silicon substrate 401. A photolithographically defined pattern of photoresist 403 determines ion implantation windows. The final resting position of the implants is shown as slightly impinging from the volume under the open windows, to the volume covered by the photoresist.

[0078] The doping graph 402 of Figure 4B shows dopant implant depth versus dopant concentration. The implants are "mid-energy" in that neither ultra low energies like below 1

keV nor super high energies like above 500 keV are required. The doping concentration peak of over 10^{19} cm^{-3} is below the surface of the silicon substrate 401, but shallower than 100 nm from the surface of the silicon substrate 401. The target dopant peak concentrations are in the range from 10^{17} cm^{-3} to 10^{21} cm^{-3}. The target dopant peak depths are from zero to 500 nm from the surface.

[0079] Figure 5A shows the p-well formed from the implantation of p-type dopants, and the n-well formed after the implantation of n-type dopants, after annealing to activate the implants and to sharpen the junctions. The doping graphs 502 of Figure 5B and 503 of Figure 5C show the dopant implant depth versus dopant concentration, for the p-well and the n-well respectively. The doping concentration peak of over 10^{19} cm^{-3} has decreased to less than 10^{19} cm^{-3}, and moved to the surface of the silicon substrate 501. The target dopant peak concentrations are in the range from 10^{17} cm^{-3} to 10^{21} cm^{-3}. The target dopant peak depth is zero although it can be conceivably located within several tens or hundreds of nanometers from the surface. Figure 6A shows the growth of epitaxial silicon on the surface of both the p-well and the n-well. The doping graphs 602 of Figure 6B and 603 of Figure 6C show the dopant implant depth versus dopant concentration, for the p-well and the n-well respectively. The preferred thickness range is determined by the height of the fin channel, which is typically 5 nm to 40 nm tall. The doping concentration peak was positioned at the surface of the silicon substrate after the prior step. Accordingly, following the growth of epitaxial silicon, there is an abrupt junction in the doping concentration between the epitaxial layer and the p-well and n-well. At the interface, the doping concentration changes by a decade over a depth of less than 3 nm. The doping concentration profiles from the previous step have shifted downard by a distance corresponding to the thickness of the epitaxial silicon.

[0080] Figure 7A shows the formation of shallow trench isolation (STI) regions in between the p-well and the n-well. The resulting epitaxial surface is used to form the transistor channels in finFETs or planar transistors. The doping graphs 702 of Figure 7B and 703 of Figure 7C show the dopant implant depth versus dopant concentration, for the p-well and the n-well respectively.

[0081] Figure 8 is a simplified illustration showing finFET structures in a typical bulk substrate configuration. In Figure 8, a plurality of fins 811, 812, 813 protrude from a bulk semiconductor body 810, sometimes referred to as body-tied fins. In addition, the individual fins are separated by shallow trench isolation structures 816, 817. A gate dielectric layer 815 overlies the fins 811, 812, 813. A gate conductor 818 extends across the fins and over the gate dielectric layer 815.

[0082] For the embodiment of Figure 8, on either side of the gate conductor 818, source and drain regions (not shown) are implemented in the fins. The FET transistors that result have source, channel and drain regions in the fins, and a gate overlying the fins. Such transistors are often called multi-gate transistors, because the gate conductor overlies two sides of the fins, and as a result increases the effective width of the channel. The fins used to implement the finFET transistors can be quite narrow. For example, fins having widths on the order of 20 nm or less can be utilized. As a result of the multi-gate gate structure and the narrow widths of the fins, finFET transistors have excellent performance characteristics and small layout areas.

[0083] While the present technology is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims. What is claimed is:

CLAIMS

1. A method of performing channel stop doping in an integrated circuit, comprising:

implanting a first part of a surface of a semiconductor substrate with n-type dopants and a second part of the surface with p-type dopants;

making undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants; and

making a transistor with a transistor channel in the undoped semiconductor material, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

2. The method of claim 1, wherein the transistor is a finFET.

3. The method of claim 1, wherein the transistor is a planar transistor.

4. The method of claim 1, wherein the implanted dopants provide latchup protection of the transistor against other structures.

5. The method of claim 1, wherein the transistor is one of a plurality of transistors with the transistor channel in the undoped semiconductor material, and the transistor channels of the plurality of transistors share a same number of dopants.

6. A nontransitory computer readable medium with computer executable instructions determining a layout of an integrated circuit design, the computer executable instructions including:

first computer executable instructions defining first layout locations for implanting a first part of a surface of a semiconductor substrate with n-type dopants and a second part of the surface with p-type dopants; and

second computer executable instructions defining second layout locations making a transistor with a transistor channel in undoped semiconductor material, the undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

7. The medium of claim 6, wherein the transistor is a finFET.

8. The medium of claim 6, wherein the transistor is a planar transistor.

9. The medium of claim 6, wherein the implanted dopants provide latchup protection of the transistor against other structures.

10. The medium of claim 6, wherein the transistor is one of a plurality of transistors with the transistor channel in the undoped seminconductor material, and the transistor channels of the plurality of transistors share a same number of dopants.

11. The medium of claim 6, wherein the computer executable instructions include:

third computer executable instructions defining third layout locations for making the undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants.

12. A set of lithographic masks determining a layout of an integrated circuit design, including:

a first lithographic mask defining first layout locations for implanting a first part of a surface of a semiconductor substrate with dopants and a second part of the surface with p-type dopants; and

a second lithographic mask defining second layout locations making a transistor with a transistor channel in undoped semiconductor material, the undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

13. The masks of claim 12, wherein the transistor is a finFET.

14. The masks of claim 12, wherein the transistor is a planar transistor.

15. The masks of claim 12, wherein the implanted dopants provide latchup protection of the transistor against other structures.

16. The masks of claim 12, wherein the transistor is one of a plurality of transistors with the transistor channel in the undoped seminconductor material, and the transistor channels of the plurality of transistors share a same number of dopants.

17. The masks of claim 12, wherein the set of lithographic masks include:

a third lithographic mask defining third layout locations for making the undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants.

18. A computer system for laying out an integrated circuit design, the computer system comprising a processor and a memory,

the computer system generating a layout of the integrated circuit design, the layout defining a plurality of masks, the computer system configured to perform computer executable instructions comprising:

first computer executable instructions defining first layout locations for implanting a first part of a surface of a semiconductor substrate with n-type dopants and a second part of the surface with p-type dopants; and

second computer executable instructions defining second layout locations making a transistor with a transistor channel in undoped semiconductor material, the undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants, such that the transistor channel of the transistor remains undoped throughout manufacture of the integrated circuit.

19. The system of claim 18, wherein the transistor is a finFET.

20. The system of claim 18, wherein the transistor is a planar transistor.

21. The system of claim 18, wherein the implanted dopants provide latchup protection of the transistor against other structures.

22. The system of claim 18, wherein the transistor is one of a plurality of transistors with the transistor channel in the undoped seminconductor material, and the transistor channels of the plurality of transistors share a same number of dopants.

23. The system of claim 18, wherein the computer executable instructions include:

third computer executable instructions defining third layout locations for making the undoped semiconductor material directly on the first part of the surface implanted with the n-type dopants and on the second part of the surface with the p-type dopants.

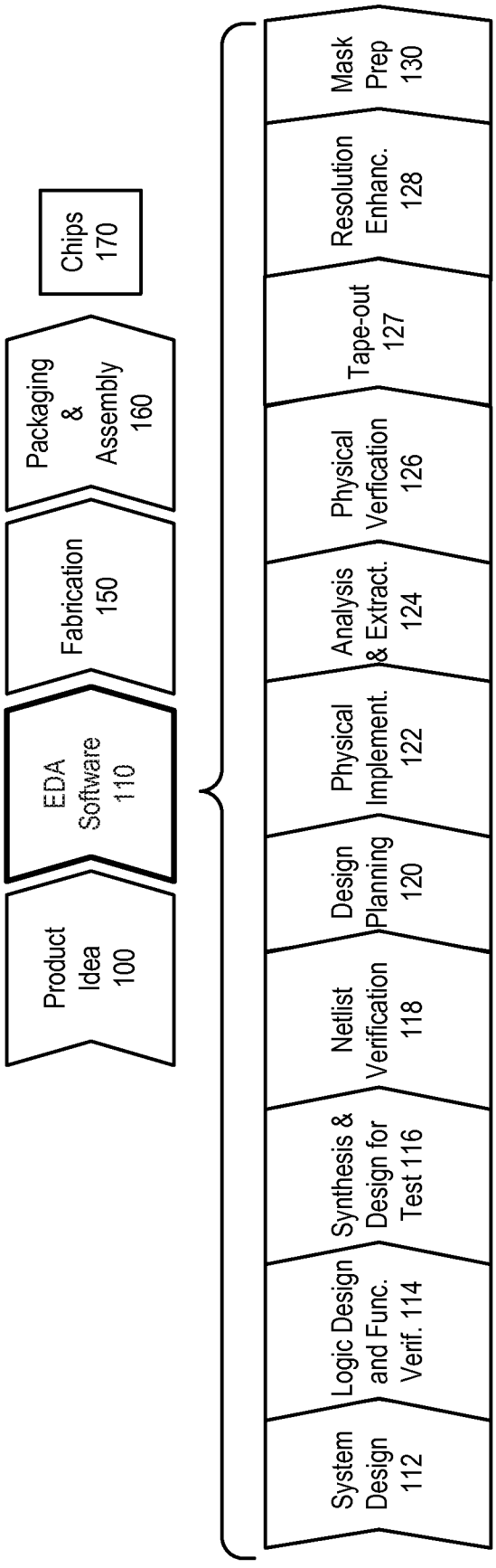

Product Idea 100
EDA Software 110
Fabrication 150
Packaging & Assembly 160
Chips 170
System Design 112
Logic Design and Func. Verif. 114
Synthesis & Design for Test 116
Netlist Verification 118
Design Planning 120
Physical Implement. 122
Analysis & Extract. 124
Physical Verfication 126
Tape-out 127
Resolution Enhanc. 128
Mask Prep 130

FIG. 1

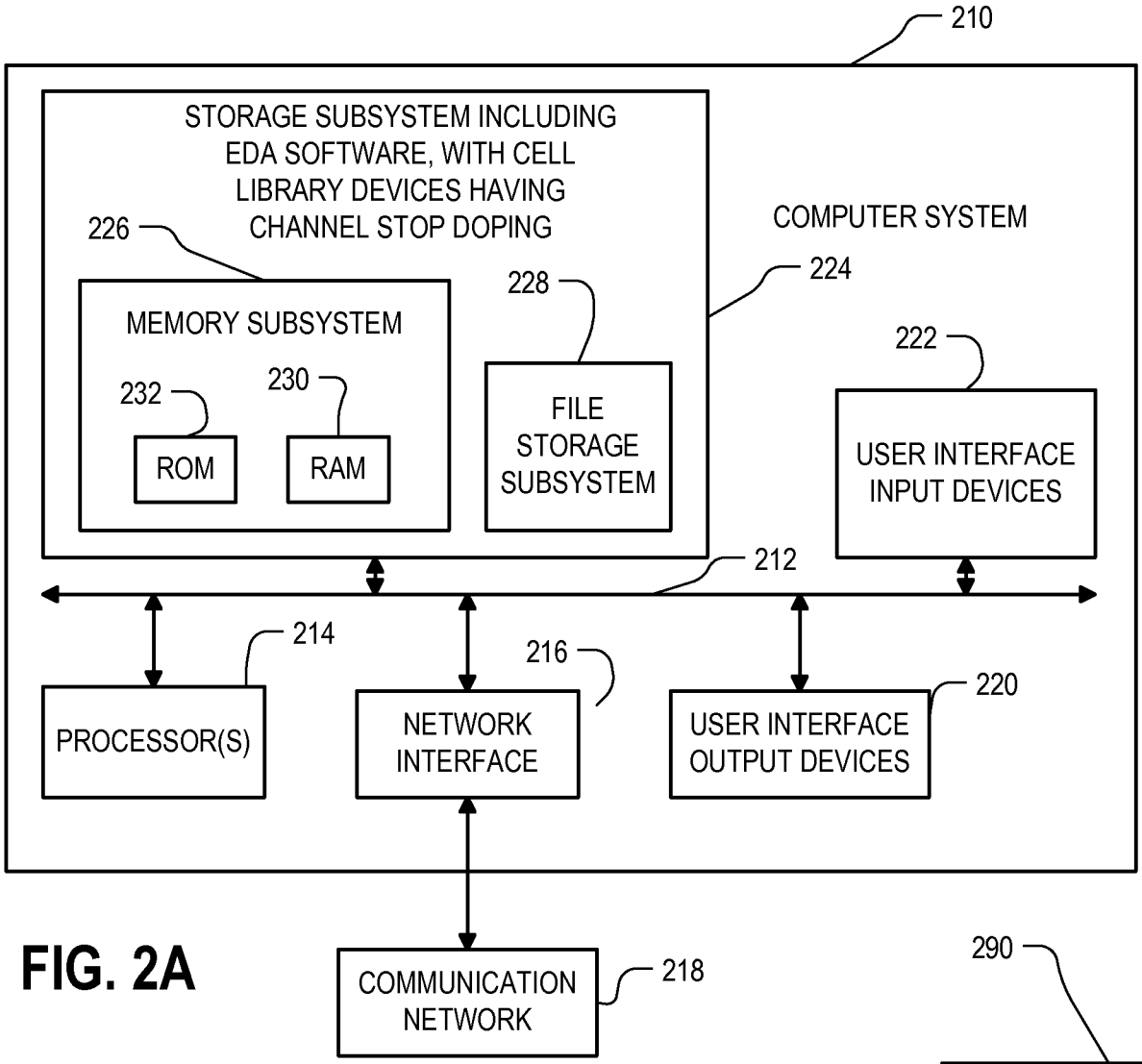


FIG. 2A

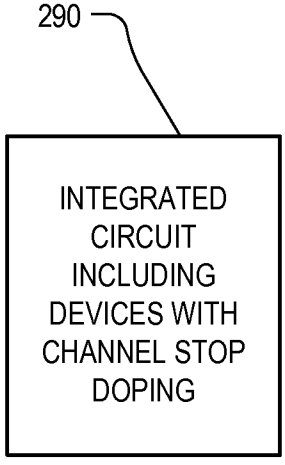


FIG. 2C

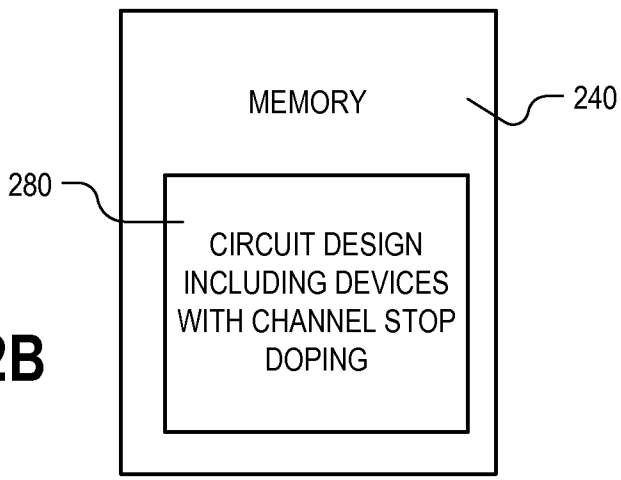


FIG. 2B

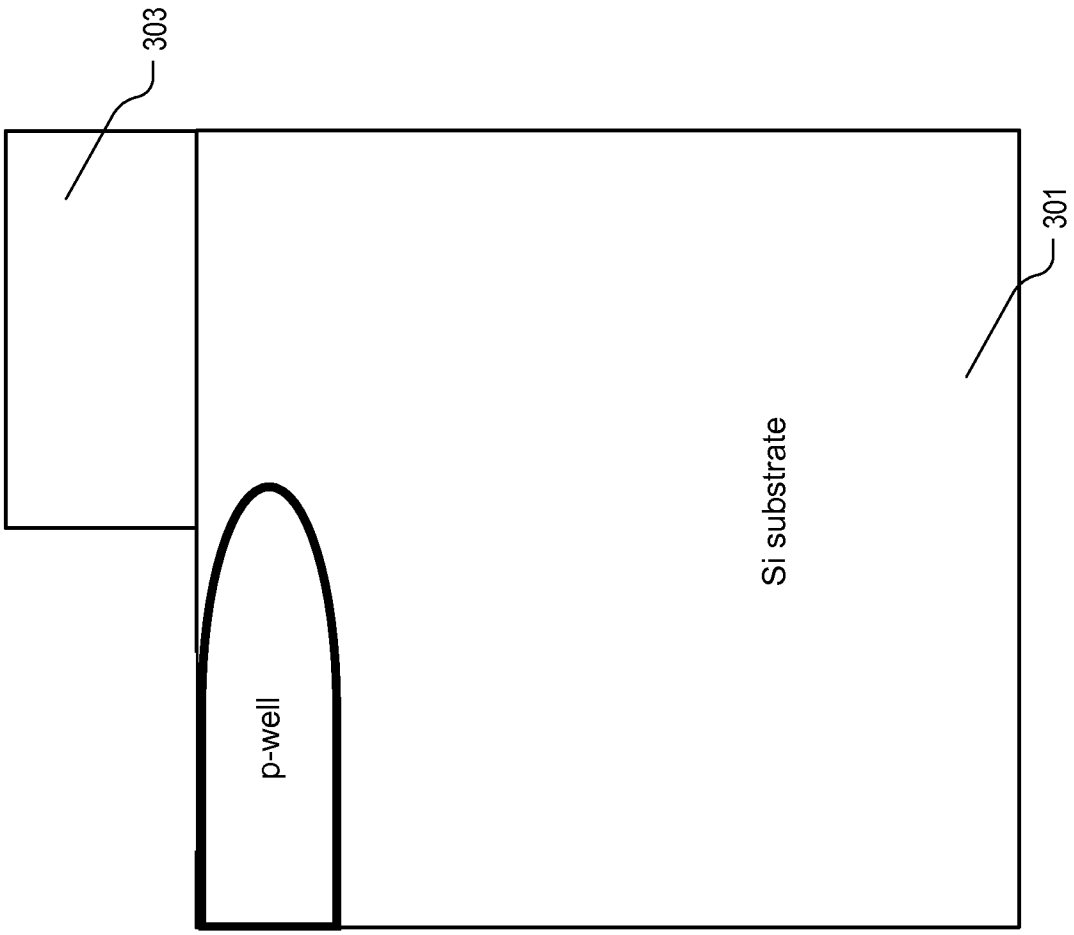
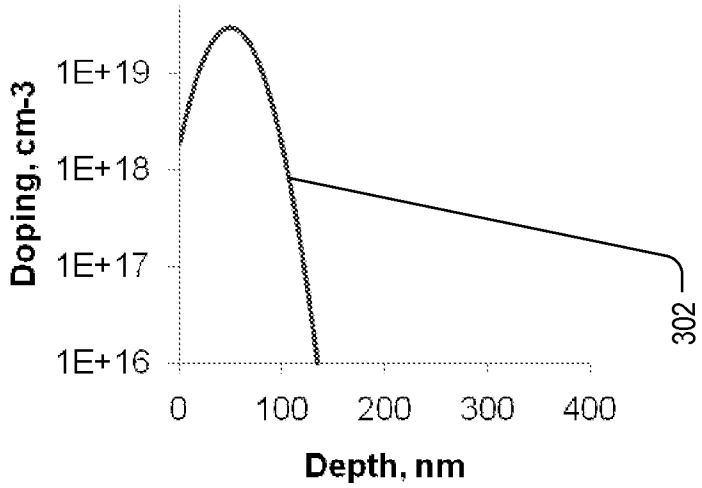

303
301
Si substrate
p-well

FIG. 3A


Doping, cm-3
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1E+18
1E+17
1E+16
0
100
200
300
400
Depth, nm
302

FIG. 3B

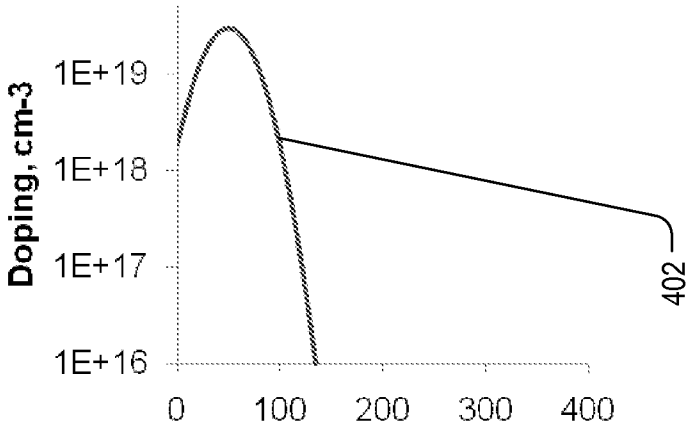
Doping, cm-3
1E+19
1E+18
1E+17
1E+16
0
100
200
300
400
Depth, nm
402

FIG. 4B

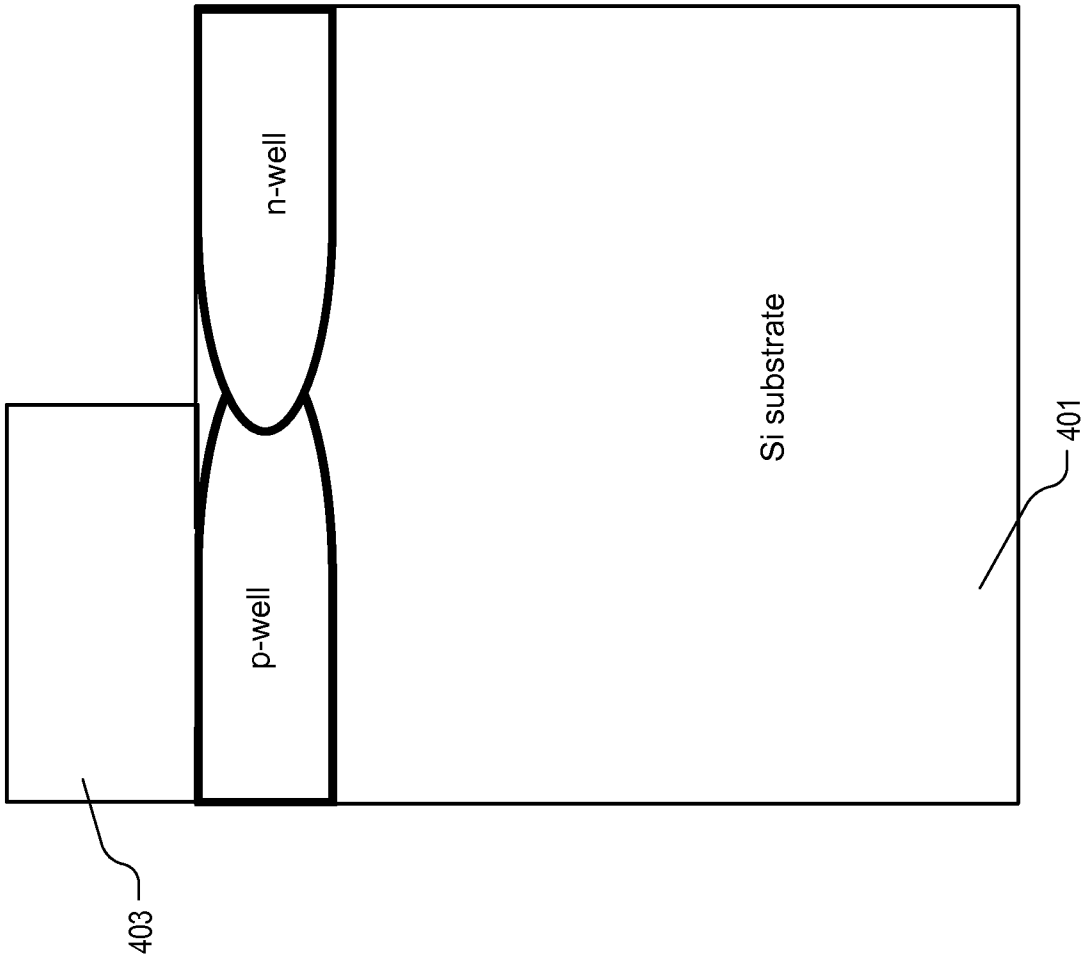
n-well
p-well
Si substrate
401
403

FIG. 4A

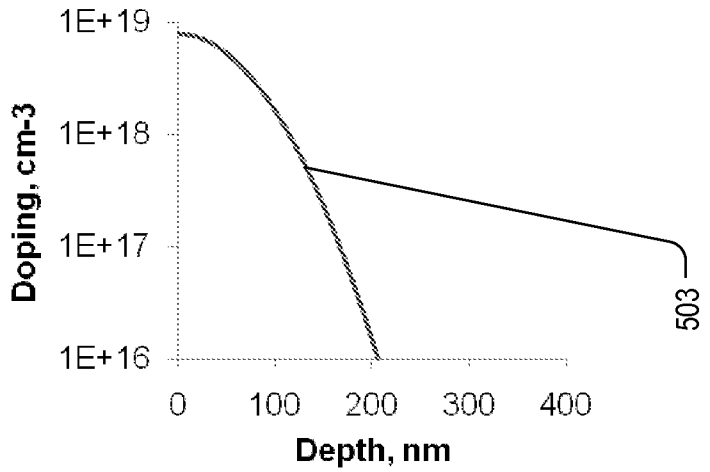

FIG. 5C

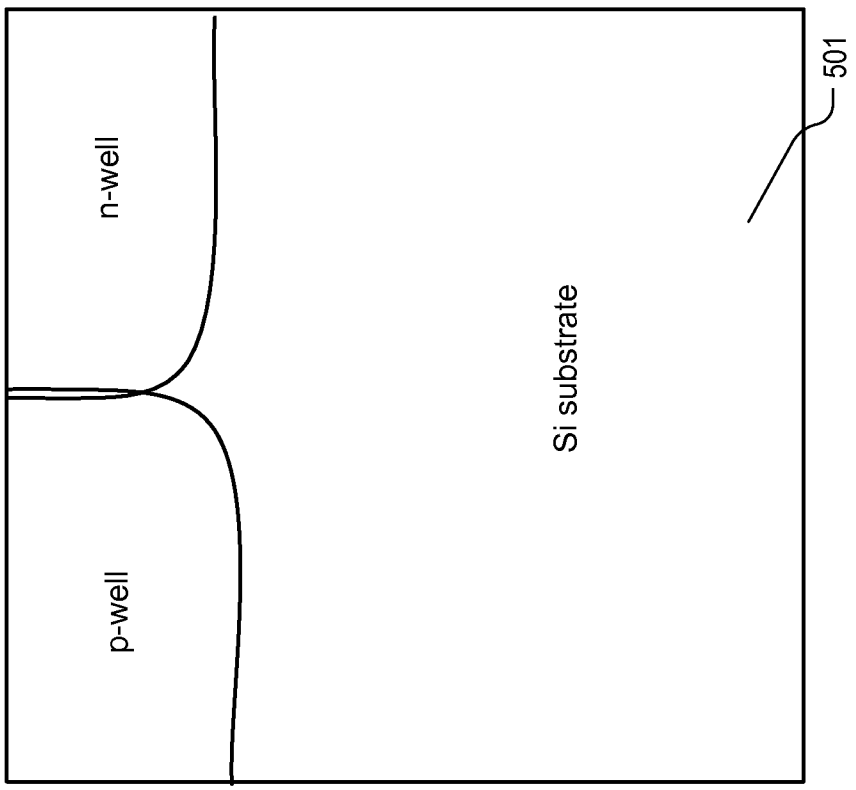

FIG. 5A

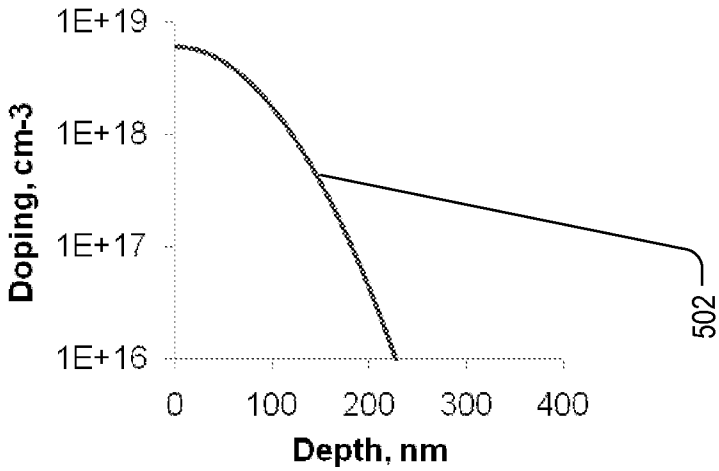

FIG. 5B

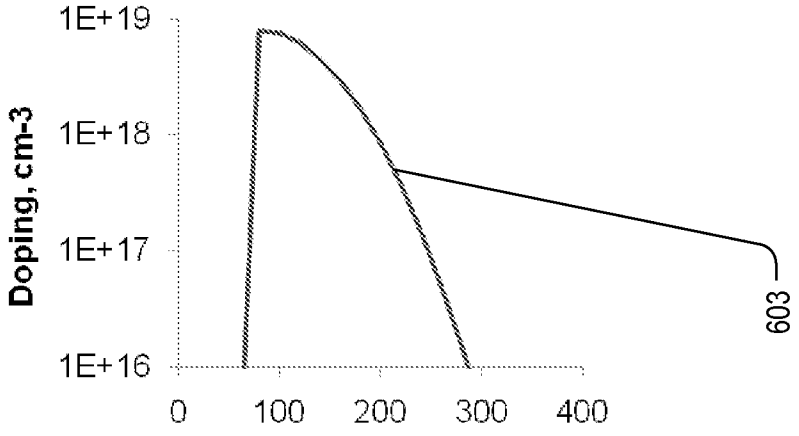

FIG. 6C

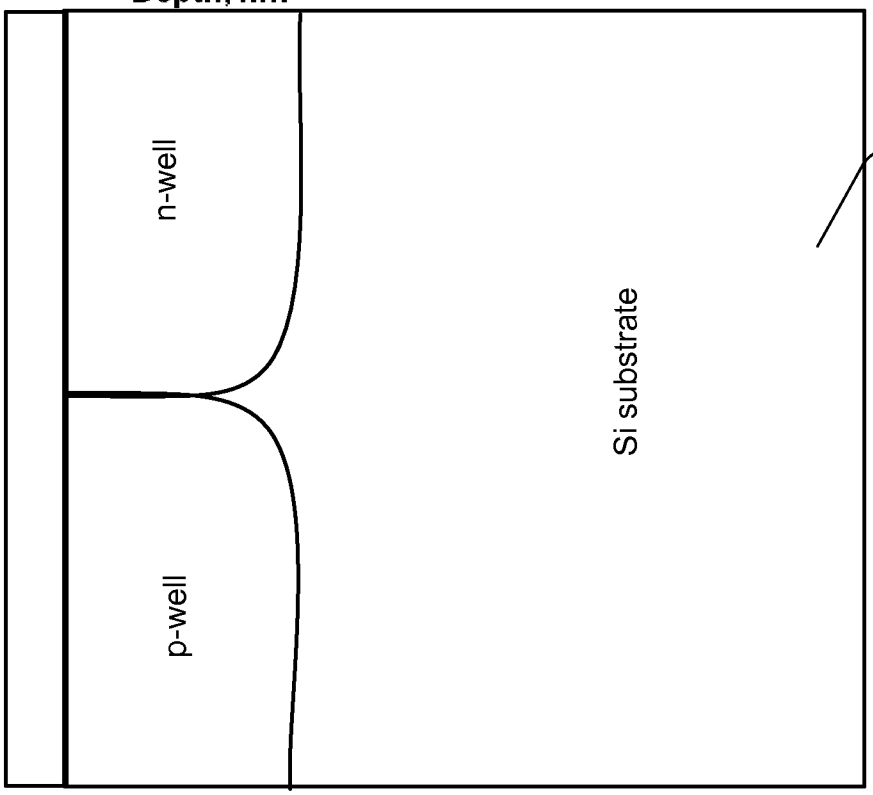

FIG. 6A

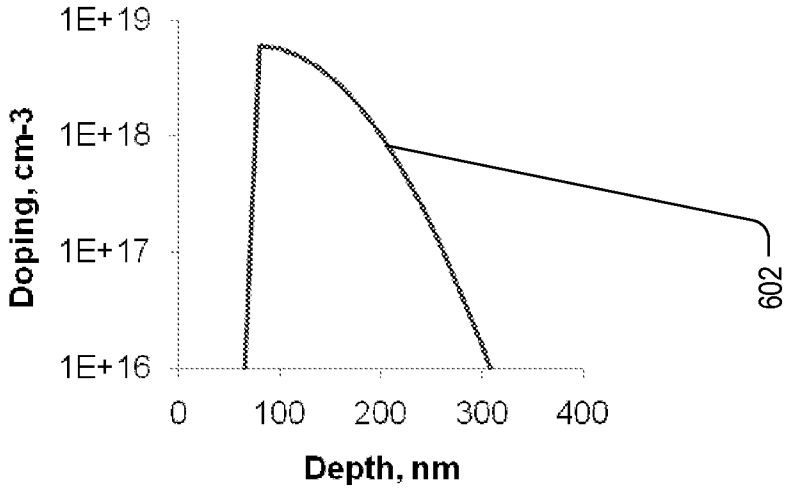

FIG. 6B

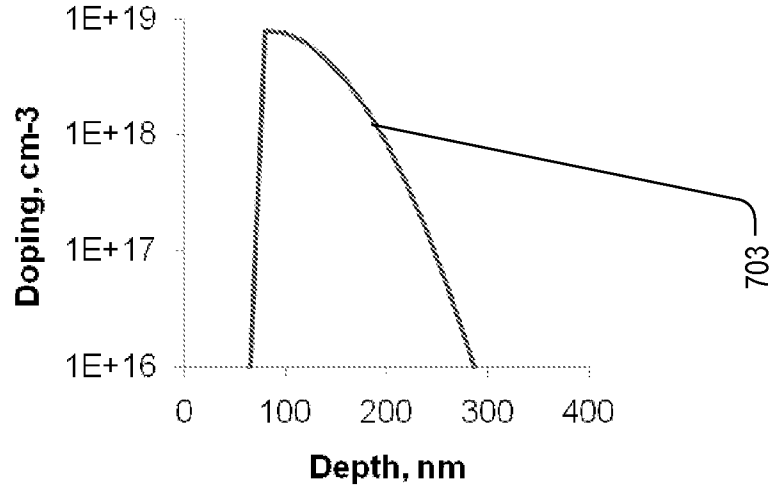

FIG. 7C

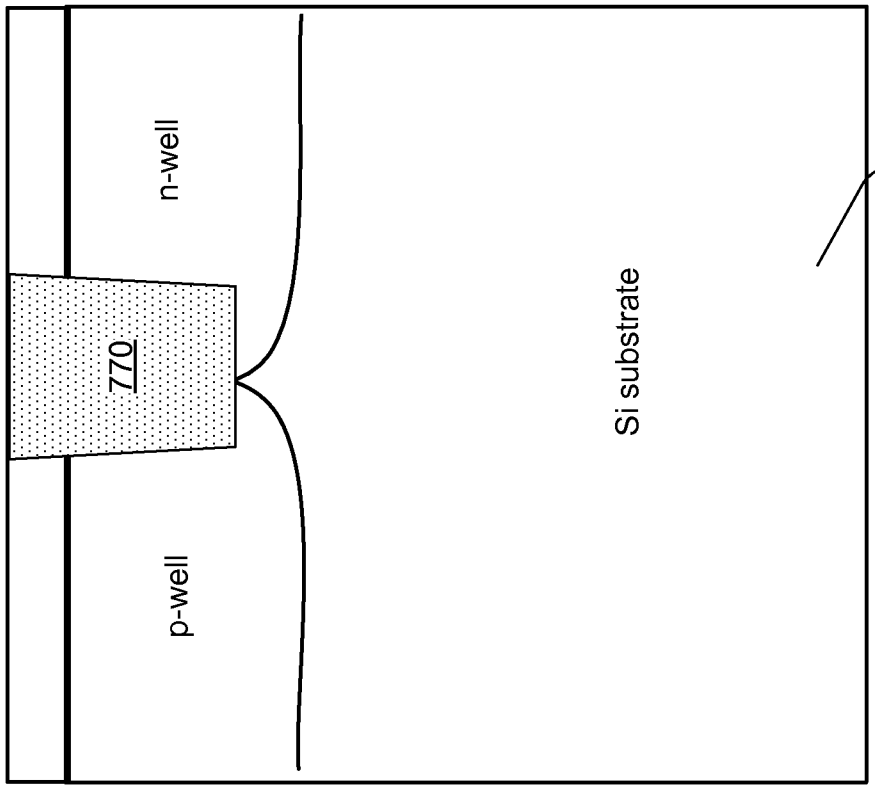

FIG. 7A

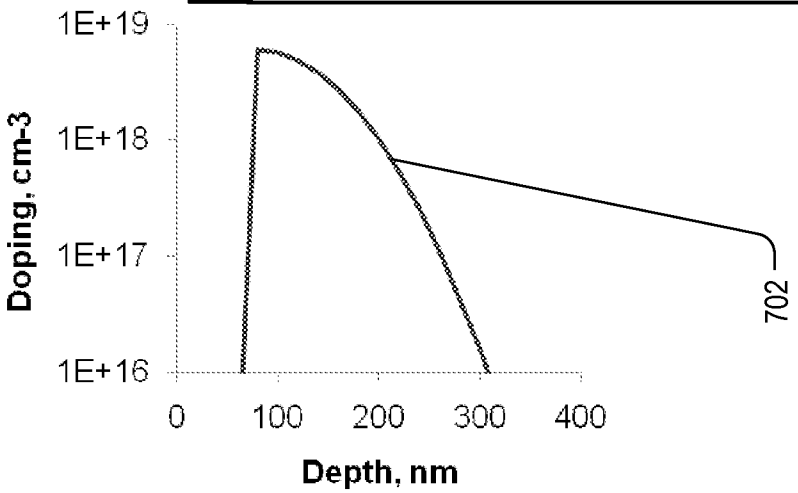

FIG. 7B

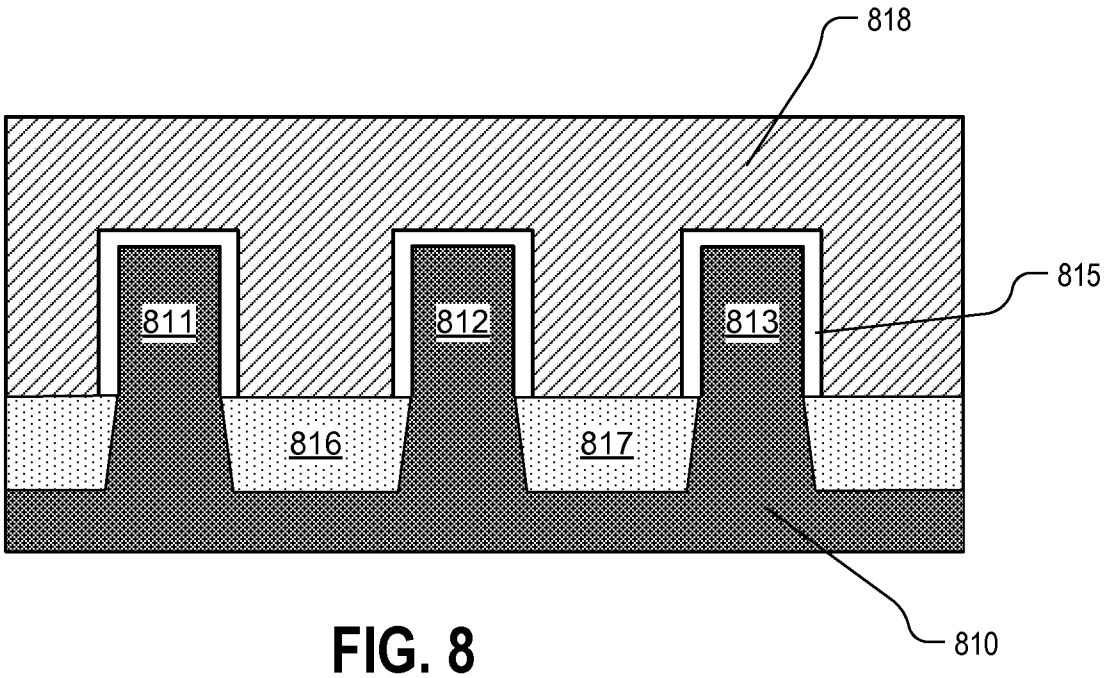

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/073111

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/322(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/322; H01L 21/302; H01L 21/331; H01L 23/62; H01L 21/336; H01L 29/772; H01L 29/78; H01L 27/092

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: dopants, undoped semiconductor material, transistor channel, finFET

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0119309 A1 (KATSUYUKI HORITA) 17 May 2012 See paragraphs [0059], [0072]-[0091]; claim 10; and figures 1-2.	1-23
A	US 2012-0025316 A1 (RICHARD T. SCHULTZ) 02 February 2012 See paragraphs [0046]-[0056]; claims 1-6; and figures 14-23.	1-23
A	US 2003-0201498 A1 (DAVID HU et al.) 30 October 2003 See paragraphs [0067]-[0074]; claims 1-7; and figures 3A-4B.	1-23
A	KR 10-0311498 B1 (HYUNDAI MICRO ELECTRONICS CO., LTD.) 02 November 2001 See pages 3-4; claims 5-7; and figures 1a-3a.	1-23
A	KR 10-2006-0035746 A (INTERNATIONAL BUSINESS MACHINES CORPORATION) 26 April 2006 See pages 3-4; claims 1-7; and figures 4-5f.	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 March 2014 (28.03.2014)	**31 March 2014 (31.03.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/073111

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