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(54) **MOTHER THIN FILM TRANSISTOR ARRAY SUBSTRATE AND THIN FILM TRANSISTOR ARRAY SUBSTRATE FABRICATED THEREFROM**

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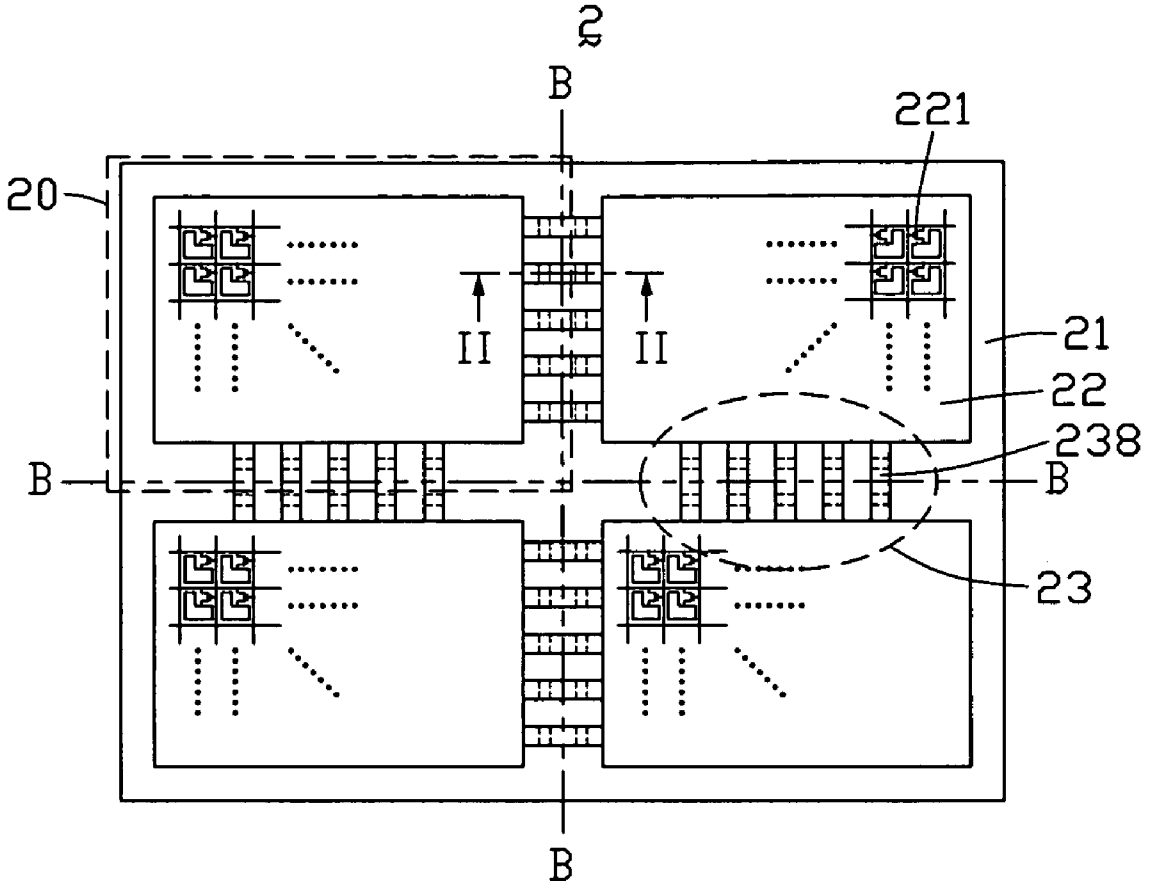
(57) **ABSTRACT**

A mother thin film transistor (TFT) array substrate includes an insulating substrate, at least two TFT arrays and printed wirings. The TFT array includes TFTs formed on the insulating substrate. The printed wirings are connected to the TFT arrays. The printed wiring includes a discontinuous metal layer and at least one bridge layer connecting the discontinuous metal layer. The bridge layer is made from corrosion-resistant material.



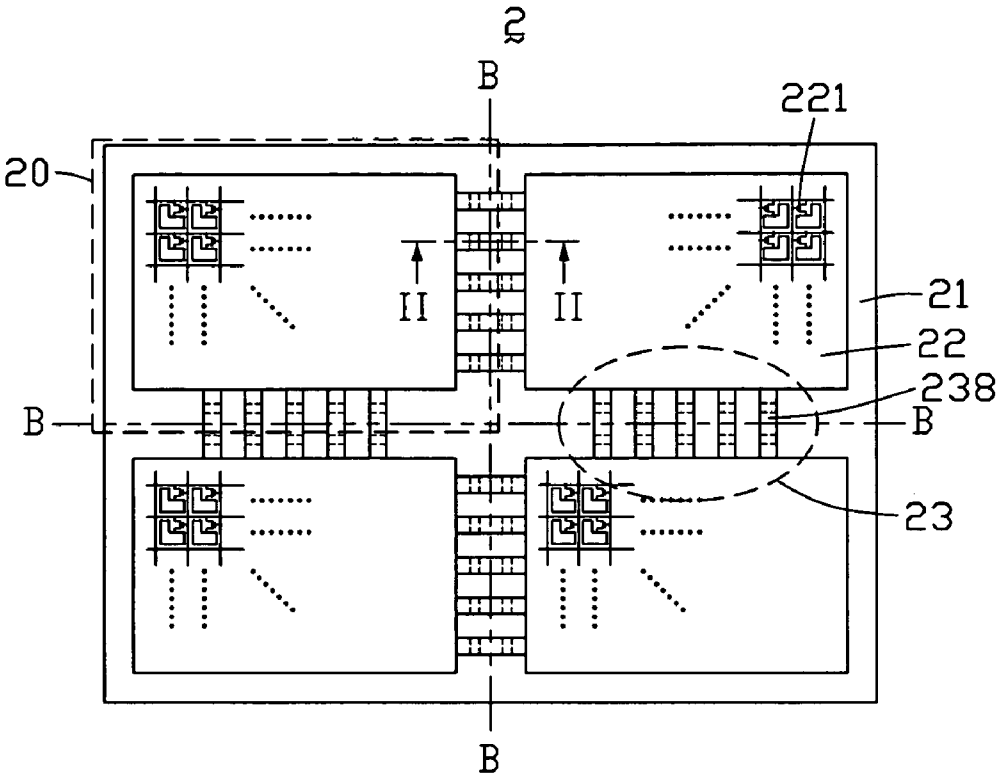


FIG. 1

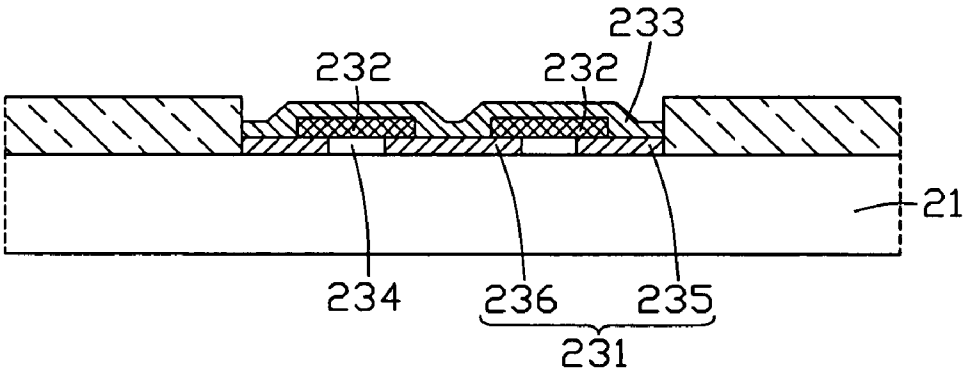


FIG. 2

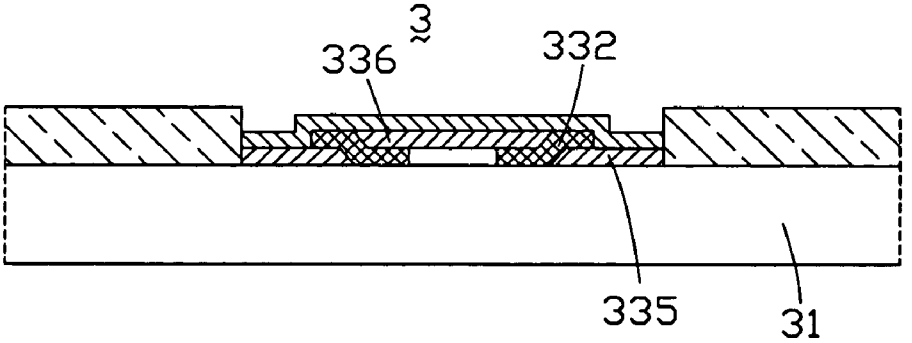


FIG. 3

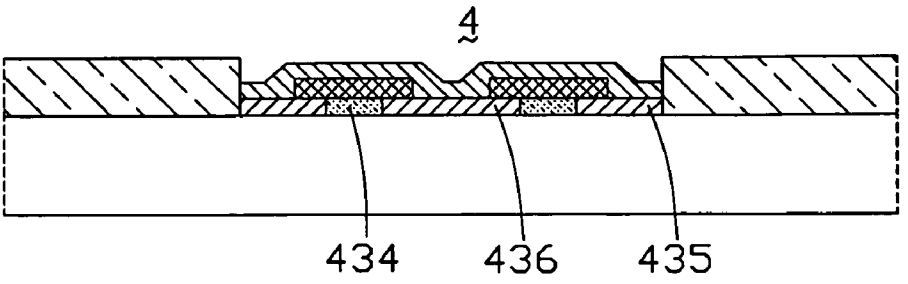


FIG. 4

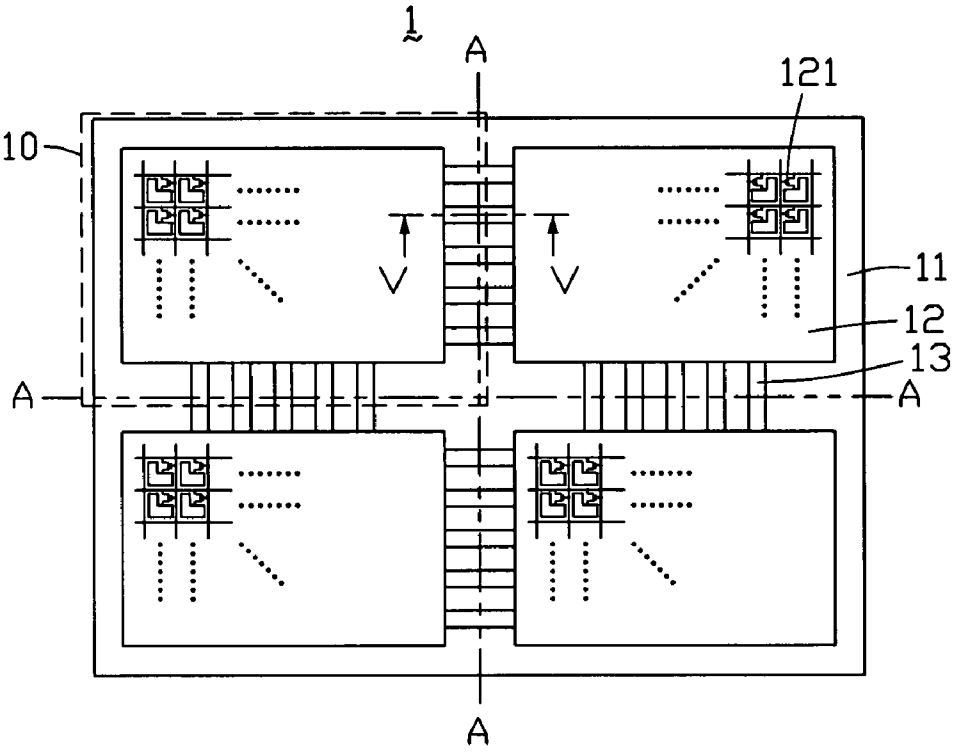


FIG. 5
(RELATED ART)

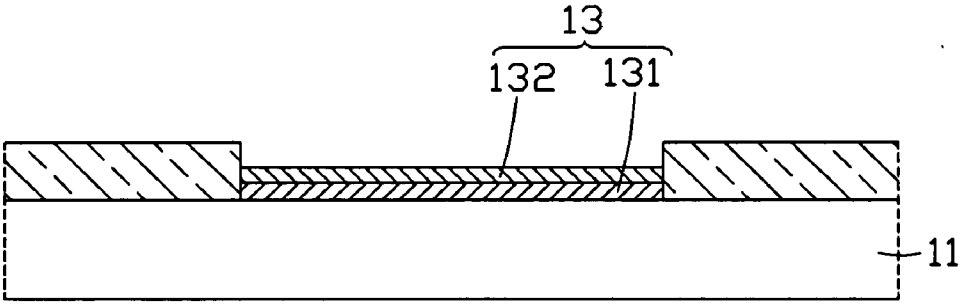


FIG. 6
(RELATED ART)

MOTHER THIN FILM TRANSISTOR ARRAY SUBSTRATE AND THIN FILM TRANSISTOR ARRAY SUBSTRATE FABRICATED THEREFROM

BACKGROUND

[0001] 1. Technical Field

[0002] The present disclosure relates to thin film transistor (TFT) arrays, and particularly to a mother TFT array substrate including printed wirings with bridge layer of corrosion-resistant material, and TFT array substrates fabricated therefrom.

[0003] 2. Description of Related Art

[0004] Liquid crystal displays are commonly used as display devices for compact electronic apparatuses, because they not only provide good quality images but are also very thin. A liquid crystal display generally includes a liquid crystal panel. The liquid crystal panel generally includes a TFT array substrate, a color filter substrate, and a liquid crystal molecule layer disposed therebetween. In mass production of liquid crystal displays, a plurality of individual TFT array substrates may be obtained by cutting a mother TFT array substrate into separate pieces.

[0005] Referring to FIG. **5**, a typical mother TFT array substrate is shown. The mother TFT array substrate **1** includes an insulating substrate **11**, a plurality of TFT arrays **12**, and a plurality of printed wirings **13**. The plurality of TFT arrays **12** and the plurality of printed wirings **13** are formed on the insulating substrate **11**. Each of the TFT arrays **12** defines a TFT array substrate **10** including a plurality of TFTs **121**. The printed wirings **13** are connected between adjacent TFT array substrates **10**. The mother TFT array substrate **1** can be divided into a plurality of TFT array substrates **10** along cutting lines A-A. After that, the printed wirings **13** are generally used to connect the TFTs **121** and an integrated driving circuit (not shown).

[0006] Referring to FIG. **6**, each of the printed wirings **13** includes a metal layer **131** and a protective layer **132**. The metal layer **131** is generally of aluminum printed on a surface of the insulating substrate **11**. The protective layer **132** is generally of insulating material covering the metal layer **131**, such that metal layer **131** is isolated from the environment by the protective layer **132**, preventing damage thereto by moisture.

[0007] However, when the mother TFT array substrate **1** is cut into a plurality of TFT array substrates **10**, each of the printed wirings **13** is broken, exposing a split. Moisture can thus easily erode the metal layer **131** through the split, and the corrosion may spread along the metal layer **131** to affect the TFTs **121**.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** is a top plan view of a first embodiment of a mother TFT array substrate according to the present disclosure.

[0009] FIG. **2** is an enlarged cross-section of the mother TFT array substrate of FIG. **1**, taken along line II-II.

[0010] FIG. **3** is a cross-section of a second embodiment of a mother TFT array substrate according to the present disclosure.

[0011] FIG. **4** is a cross-section of a third embodiment of a mother TFT array substrate according to the present disclosure.

[0012] FIG. **5** is a top plan view of a frequently used mother TFT array substrate.

[0013] FIG. **6** is an enlarged, cross-section of the mother TFT array substrate of FIG. **5**, taken along line V-V.

DETAILED DESCRIPTION

[0014] Reference will now be made to the drawings to describe exemplary embodiments of the present disclosure in detail.

[0015] Referring to FIG. **1**, a first embodiment of a mother TFT array substrate **2** according to the present disclosure is shown. The mother TFT array substrate **2** includes an insulating substrate **21**, a plurality of TFT arrays **22**, and a plurality of printed wiring regions **23**. The insulating substrate **21** is made from transparent insulating material, preferably such as glass. The plurality of TFT arrays **22** and the plurality of printed wiring regions **23** are formed on the insulating substrate **21**. Each of the TFT arrays **22** defines a TFT array substrate **20**. The adjacent TFT arrays **22** are connected by the printed wiring regions **23**.

[0016] Each of the TFT arrays **22** includes a plurality of TFTs **221**, a plurality of pixel electrodes (not labeled), a plurality of gate lines (not labeled), and a plurality of data lines (not labeled) formed during separate photolithographic mask processes. Each of the TFTs **221** is connected to a gate line and a data line. Each of the pixel electrodes is connected to a TFT **221**. Scan voltages are applied via the gate lines to turn on the TFTs **221**, and data voltages are applied via the data lines and the TFTs **221** to the pixel electrodes. The pixel electrodes are generally of indium tin oxide (ITO) or indium zinc oxide (IZO). The gate lines and the data lines are generally of aluminum with thickness of 150 nm to 300 nm, or molybdenum with thickness of 50 nm to 200 nm. However, it should be understood by one of ordinary skill in the art that these materials and component parameters may change depending on various embodiments.

[0017] Referring to FIG. **2**, a plurality of printed wirings **238** and a protective layer **233** are formed on each of the printed wiring regions **23**. The printed wirings **238** are printed directly on a surface of the insulating substrate **21**. The protective layer **233** is deposited to cover the printed wirings **238**. Each of the printed wirings **238** is located between two adjacent TFT arrays **22**.

[0018] Each of the printed wirings **238** includes a discontinuous metal layer **231** and two bridge layers **232**. As shown in FIG. **2**, the metal layer **231** includes two first metal layers **235**, a second metal layer **236** and two disconnected portions **234**. Each of the first metal layers **235** is directly connected to the TFT arrays **22**, and the second metal layer **236** is spaced from the first metal layers **235** by the two disconnected portions **234**. Namely, the metal layer **231** is a discontinuous metal layer with openings. The bridge layers **232** are deposited to cover but not fill the two disconnected portions **234**, respectively. Therefore the first metal layers **235** and the second metal layer **236** are connected by the bridge layers **232**, with an opening remaining between the first metal layer **235** and the second metal layer **236**.

[0019] The metal layer **231** is made from aluminum or molybdenum, preferably formed during the same photolithographic mask process as the gate lines or the data lines. The bridge layers **232** are made from corrosion-resistant material, such as ITO or IZO. Preferably, the bridge layers **232** and the pixel electrode are formed during the same photolithographic mask process.

[0020] When the mother TFT array substrate **2** is cut into a plurality of TFT array substrates **20** along the cutting lines B-B, the second metal layer **236** is divided into two parts. Thus each of the TFT array substrate **20** includes a plurality of second metal layers **236** with a split (not shown) exposed to the environment.

[0021] If moisture in the environment etches the second metal layer **236** through the split, because the first metal layer **235** and the second metal layer **236** are connected by the bridge layer **232** of corrosion-resistant material, the corrosion is contained by the bridge layer **232** and cannot spread to the first metal layer **235**, and integrity of the TFTs **221** is enhanced. In addition, because the bridge layer **232** can be formed with the pixel electrode during a single photolithographic mask process, there is no increase in the number of photolithographic mask processes.

[0022] FIG. **3** shows a second embodiment of a mother TFT array substrate **3** according to the present disclosure. Two discontinuous first metal layers **335** are printed directly on a surface of an insulating substrate **31** with a disconnected portion (not labeled) located therebetween. The two bridge layers **332** are deposited to cover part of the first metal layer **335** respectively, and the bridge layers **332** fill in the disconnected portion to extend to the insulating substrate **31**. A second metal layer **336** is deposited to cover the disconnected portion and connect the two bridge layers **332**. Because the bridge layer **332** covers the first metal layer **335** directly, corrosion is also contained by the bridge layer **332**.

[0023] FIG. **4** shows a third embodiment of a mother TFT array substrate **4** according to the present disclosure. Openings between a first metal layer **435** and a second metal layer **436** can be filled with insulating material layer **434**.

[0024] Further or alternative embodiments of the present mother TFT array substrate can include, for example, the bridge layer **232** being made from high-melting point metal or alloy, such as chromium, titanium, niobium, vanadium, tungsten, tantalum, zirconium, and hafnium.

[0025] It is to be further understood that even though numerous characteristics and advantages of the present embodiments have been set out in the foregoing description, together with details of the structures and functions of the embodiments, the disclosure is illustrative only, and changes may be made in detail, especially in matters of shape, size, and arrangement of parts within the principles of the invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

What is claimed is:

1. A mother thin film transistor (TFT) array substrate, comprising:
- an insulating substrate;
- at least two TFT arrays comprising a plurality of TFTs formed on the insulating substrate; and
- a plurality of printed wirings connected to the TFT arrays, wherein at least one of the plurality of printed wirings comprises a discontinuous metal layer and at least one bridge layer connecting the discontinuous metal layer, the bridge layer being made from corrosion-resistant material.

2. The mother TFT array substrate of claim **1**, wherein the bridge layer is filled in the disconnected portion to connect the discontinuous metal layer.

3. The mother TFT array substrate of claim **2**, wherein the discontinuous metal layer comprises two first metal layers connected to the TFT arrays and partly covered by the bridge layer, a disconnected portion partly filled with the bridge layer, and a second metal layer covering the bridge layer.

4. The mother TFT array substrate of claim **1**, wherein the bridge layer covers the disconnected portion of the metal layer.

5. The mother TFT array substrate of claim **4**, wherein the discontinuous metal layer comprises two first metal layers connected to the TFTs, two disconnected portions, and a second metal layer located between the two disconnected portions.

6. The mother TFT array substrate of claim **4**, wherein the disconnected portion is filled by insulating material.

7. The mother TFT array substrate of claim **1**, wherein the mother TFT array substrate further comprises a protective layer covering the printed wirings.

8. The mother TFT array substrate of claim **1**, wherein the TFT array further comprises a plurality of pixel electrodes formed during the same photolithographic mask process as the bridge layer.

9. The mother TFT array substrate of claim **1**, wherein the bridge layer is made from indium tin oxide, indium zinc oxide, high-melting point metal, or alloy.

10. A thin film transistor (TFT) array substrate, comprising:
- an insulating substrate;
- a TFT array comprising a plurality of TFTs formed on the insulating substrate; and
- a plurality of printed wirings connected to the TFTs, wherein at least one of the plurality of printed wirings comprises a discontinuous metal layer and at least one bridge layer connecting the discontinuous metal layer, the bridge layer being made from corrosion-resistant material.

11. The TFT array substrate of claim **10**, wherein the bridge layer is filled in the disconnected portion to connect the discontinuous metal layer.

12. The TFT array substrate of claim **10**, wherein the bridge layer covers the disconnected portion of the metal layer.

13. The TFT array substrate of claim **12**, wherein the disconnected portion is filled by insulating material.

14. The TFT array substrate of claim **10**, wherein the discontinuous metal layer is made from aluminum or molybdenum.

15. The TFT array substrate of claim **10**, wherein the TFT array further comprises a plurality of pixel electrodes formed during the same photolithographic mask process as the bridge layer.

16. The TFT array substrate of claim **10**, wherein the bridge layer is made from indium tin oxide, indium zinc oxide, high-melting point metal, or alloy.

17. A thin film transistor (TFT) array substrate, comprising:
- a substrate;
- a plurality of TFTs formed on the substrate; and
- a plurality of printed wirings connected to the TFTs, wherein at least one of the plurality of printed wirings comprises at least one corrosion-resistant material layer.

18. The TFT array substrate of claim **17**, wherein at least one of the plurality of printed wirings further comprises a discontinuous metal layer and the corrosion-resistant material layer connects the discontinuous metal layer.

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