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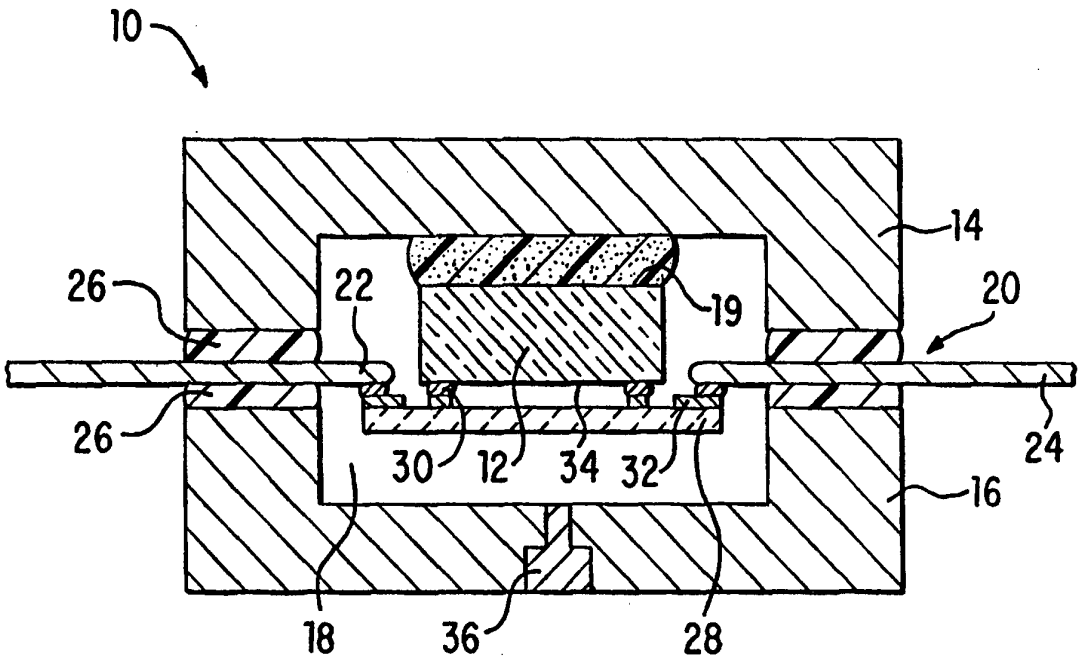
(54) Title: FLIP CHIP IN METAL ELECTRONIC PACKAGES



(57) Abstract

There is provided an electronic package (10) for encapsulating a flip chip bonded integrated circuit device (12). A metallic base component (14) and a cover component (16) define a cavity (18). A substrate (28) is disposed within the cavity (18). The substrate (28) contains a first metallization array (30) and a second metallization array (32). The input/output pads (50) of the integrated circuit device (12) are bonded to the first metallization array (30) and the inner leads (22) of a leadframe (20) are bonded to the second metallization array (32). When the metallic base component (14) and cover component (16) are bonded (26) together with a leadframe (20) disposed therebetween, the substrate (28), inner leads (22) and integrated circuit device (12) are encapsulated within the cavity (18).

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FLIP CHIP IN METAL ELECTRONIC PACKAGES

While the invention is subject to a wide range of applications, it is particularly suited for metal packages to house an electronic device. More particularly, the invention relates to a metal electronic package in which one or more integrated circuit devices are flip chip bonded to a supporting substrate.

Adhesively sealed metal packages for housing electronic devices, such as silicon based semiconductor integrated circuits, are disclosed in U.S. Patent Nos. 4,105,861 to Hascoe; 4,461,924 to Butt and 4,939,316 to Mahulikar et al. The packages have a metallic base and cover. A leadframe is disposed between the base and cover and adhesively bonded to both. The leadframe may include a centrally positioned die attach paddle with the integrated circuit device bonded thereto. Bond wires electrically interconnect the device to the leadframe.

One advantage of metal electronic packages over molded plastic packages such as quad flat packs (QFP's) or ceramic packages such as ceramic dual in line packages (CERDIP's) is improved thermal conduction. Metal packages remove heat generated during operation of the device more efficiently than plastic or ceramic packages. The improved thermal dissipation is due to both improved thermal conduction of the metallic components and the ability of the components to disperse heat laterally along all surfaces of the package. The improved thermal dissipation permits encapsulation of more complex and higher powered integrated circuit devices than is possible with plastic or ceramic packages. Improved thermal dissipation also

facilitates the encapsulation of a plurality of integrated circuit devices within a single package.

As the integrated circuit devices become more complex, more electrical interconnections with external circuitry are required. The leadframe, which electrically interconnects the device to external circuitry, is usually manufactured from a copper base alloy having a thickness of from about 0.13 mm to about 0.51 mm (5-20 mils). Due to stamping and etching constraints, the minimum width of each lead, as well as the spacing between leads, is about equal to the thickness of the leadframe. As a result, there is a limit to the number of leads which may approach the integrated circuit device.

One way to increase the number of leads is to increase the distance between the leadframe and the integrated circuit device. However, the distance over which effective wire bonds are made is limited to about 5.1 mm (200 mils). One method which has been used to electrically interconnect integrated circuit device with a leadframe which does not require the use of thin bond wires is known as controlled collapse chip connection (C4) or flip chip bonding.

In flip chip bonding, as generally described in Section 6.3 of Microelectrocic Packaging Handbook edited by Tummala et al, input/output pads on the electrically active face of a semiconductor device are directly soldered to metallized pads on a substrate. Electrically conductive circuit traces interconnect the input/output pads with terminal pins to electrically interconnect the semiconductor device to external circuitry.

While flip chip bonding has been applied to ceramic and plastic pin grid array packages, it has not been applied to metal electronic packages. Accordingly, it is an object of the invention to provide a metal electronic package having one or more flip chip bonded semiconductor integrated circuits housed therein. It is a feature of the invention that the integrated circuit devices are supported on and electrically interconnected to a substrate by a first array of bond pads. It is another feature of the invention that the inner leads of a leadframe are electrically interconnected to a second array of bond pads on the same substrate. Yet another feature of the invention is that the substrate may be formed from any rigid material having a coefficient of thermal expansion approximately equal to that of the semiconductor device. Among the advantages of the electronic package of the invention are good thermal conductivity and, due to the absence of bond wires, improved electrical characteristics.

In accordance with the invention, there is provided an electronic package. The electronic package has a metallic base component and a cover component. The metallic base component and the cover component define a cavity. A leadframe which has inner and outer lead ends is disposed between the metallic base component and the cover component and bonded to both. The inner lead ends are positioned within the cavity. A substrate is disposed within the cavity. This substrate contains a first metallization array and a second metallization array. The first metallization array

aligns with the input/output pad configuration of a desired integrated circuit device. The second metallization array is electrically interconnected to the leadframe.

The above stated objects, features and advantages will become more apparent from the specification and drawings which follow.

Figure 1 shows in cross-sectional representation a metallic electronic package having a flip chip bonded integrated circuit in accordance with the invention.

Figure 2 shows in top planar view, a substrate for the flip chip bonding of an integrated circuit device in accordance with the present invention.

Figure 3 shows in cross-sectional representation, a first embodiment of the substrate of Figure 2.

Figure 4 shows in cross-sectional representation, a second embodiment of the substrate of Figure 2.

Figures 5-7 show in cross-sectional representation a method for the assembly of the electronic package of the invention.

Figure 8 shows in cross-sectional representation the metal electronic package of the invention incorporating a heat spreader.

Figure 9 shows in cross-sectional representation a ball grid array electronic package in accordance with the invention.

Figure 10 shows in cross-sectional representation a housing for encapsulating an integrated circuit device flip chip bonded to a printed circuit board.

Figure 1 shows in cross-sectional representation an electronic package 10 for encapsulating one or more integrated circuit devices 12 in accordance with the present invention. The electronic package 10 has a metallic base component 14 and a cover component 16. The metallic base component 14 and the cover component 16 define a cavity 18. While the spatial orientation of the metallic base component 14 and cover component 16 depends whether the electronic package 10 is a cavity up or a cavity down configuration, throughout this application the "base component" is that component adjacent the back side 19 of the integrated circuit device 12.

The metallic base component 14 may be formed from any suitable metal, metal alloy or metal compound. To maximize thermal conductivity, the metallic base component 14 is preferably formed from copper, aluminum or alloys thereof. In a most preferred embodiment, the metallic base component 14 is formed from an aluminum alloy and anodized prior to package assembly. Anodization provides corrosion resistance and also electrically insulates the metallic base component. To achieve a uniform gray to black color, useful for infrared soldering, the metallic base component 14 is an aluminum alloy containing manganese and silicon. Preferred aluminum alloys are designated by the ASM (American Society for Metals) as 3xxx and 6xxx series. Alloys of the 3xxx series contain up to about 1.5% by weight manganese along with other alloying elements. Alloys of the 6xxx series contain magnesium and silicon in an approximate proportion to form Mg_2Si.

One preferred aluminum alloy is aluminum alloy 3003 which has the nominal composition of about 0.12% by weight copper, about 1.2% by weight manganese and the balance aluminum.

The light black to black color is achieved by integral color anodization. The metallic base component 14 is immersed in any suitable electrolyte such as a mixture of sulfuric and sulfosalicylic acids in a concentration range of from about 1 to 4 gm/l H_2SO_4 and from about 50 to about 120 gm/l $C_7H_6O_6S$. The amperage is rapidly raised to in excess of 7.5 A/dm^2 (70 amps per square foot) and then allowed to gradually decrease as a function of oxide growth while the voltage is maintained in excess of 70 volts. The integral anodization process is more fully described in U.S. Patent No. 5,066,368 to Pasqualoni et al.

The cover component 16 is formed from any suitable material. To prevent distortion of the electronic package 10 due to coefficient of thermal expansion mismatch, the cover component 16 preferably has a coefficient of thermal expansion approximately equal to that of the metallic base component 14. Any suitable polymer, ceramic or metal may be utilized. A ceramic cover component 16 has the advantage of rigidity and light weight. A metal cover component 16 has the advantage of ease of formability and with aluminum based materials, light weight as well. Preferably, the cover component 16 is formed from the same metal, metal alloy or metal compound as the metallic base component 14, such as an anodized aluminum alloy.

A leadframe 20 having inner lead ends 22 and outer lead ends 24 is disposed between the metallic base component 14 and the cover component 16 and bonded to both. The bond 26 may be any suitable dielectric material such as a low temperature sealing glass or a polymer adhesive. Preferably, the bond 26 is a polymer adhesive such as a thermosetting epoxy resin. Leadframe 20 is positioned such that the inner lead ends 22 are within the cavity 18.

A substrate 28 is disposed within the cavity 18. The substrate 28 contains a first metallization array 30 and a second metallization array 32. The first metallization array 30 aligns with the input/output pad configuration on the electrically active face 34 of the integrated circuit device 12. The second metallization array 32 is electrically interconnected to the inner leads 22 of the leadframe 20.

Vent hole 36, which can be formed either in the metallic base component 14 or, as illustrated in Figure 1, in the cover component 16, facilitates the removal of polymer cure reaction by-products from the package cavity 18 during assembly. The vent hole 36 is subsequently sealed with either a metal plug or a polymer.

The substrate 28 is illustrated in top planar view in Figure 2. The substrate 28 contains a support layer 38 which is preferably rigid or semi-rigid to maintain the integrity of the bonds to the integrated circuit. The support layer 38 may be formed from any suitable metal, ceramic, metal alloy, metal compound or composite. The support

layer 38 preferably has a coefficient of thermal expansion approximately equal to that of the integrated circuit device 12 to prevent stress on the bond between an integrated circuit and the substrate during assembly or operation. Generally, the coefficient of thermal expansion of the support layer 38 is within about 10% of the coefficient of thermal expansion of the integrated circuit device.

Formed on a surface of the support layer 38 is a first metallic array 30 and a second metallic array 32 of any electrically conductive material which may be accurately patterned. Patterning may be by screen printing, photolithography, direct writing or any other means known in the art. Typical materials for the first metallization array 30 and second metallization array 32 are copper, tungsten, palladium/nickel alloys and chromium/copper/chromium laminar structures. Conductive polymers such as a silver filled epoxy can also be used.

The first metallization array 30 is configured to align with the pattern of input/output pads formed on the electrically active face of an integrated circuit device. The second metallization array 32 is configured to align with the inner lead ends of a leadframe. Electrically conductive circuit traces 40 interconnect the first metallization array 30 and the second metallization array 32.

Figure 3 illustrates in cross-sectional representation a substrate 28 in accordance with an embodiment of the invention. The support layer 38 is formed from a rigid or semi-rigid material having

a coefficient of thermal expansion about equal to that of an integrated circuit device. The support layer 38 may be electrically conductive or electrically nonconductive. Typical materials include iron alloys, iron-nickel alloys and iron-nickel-cobalt alloys, as well as ceramic materials such as alumina, aluminum nitride and boron nitride. The thickness is that effective to maintain a rigid to semi-rigid backing layer, typically on the order of from about 0.13mm to about 0.38mm (0.005-0.015 inch). An adhesive layer 42 bonds the support layer 38 to a circuit structure 44. The circuit structure 44 may be a copper foil layer laminated directly to adhesive 42 or, as illustrated in Figure 3, a composite circuit layer. Particularly suitable is a composite flexible circuit. The composite flexible circuit includes a dielectric substrate 46, such as polyimide, laminated to a conductive layer, typically copper or a copper alloy. The conductive layer is patterned, typically by photolithography, to a desired circuit pattern 30, 32, 40. In addition, multiple circuit layers 44 may be laminated one to the other to form a multilayer structure supported by support layer 38.

Figure 4 illustrates in cross-sectional representation, a substrate 28' in accordance with a second embodiment of the invention. The support layer 38 is formed from an electrically insulating material such as alumina, aluminum nitride or boron nitride. A desired circuit pattern 30, 32, 40 is formed on the support layer 38. The circuit pattern can be formed by thick film technology such as

screen printing or direct writing; by thin film technology such as sputtering or vapor deposition followed by selective etching; or by tape automated bonding (TAB) technology such as the selective etching of a laminated copper layer. Typically, the circuit pattern 30, 32 and 40 is deposited as a palladium/nickel alloy paste which is converted to a metallic layer by heating to an elevated temperature in a reducing atmosphere. The metallization layer is then built to a desired thickness by the deposition of an overlying copper layer by electroless or electrolytic means.

The method for the assembly of the electronic package is illustrated in Figures 5-7. With reference to Figure 5, the substrate 28 is bonded to a leadframe 20 electrically interconnecting the inner lead ends 22 with the second metallization array 32. The interconnection 48 may be by any suitable material such as solder, conductive epoxy or a weld. Typical solders include lead-tin and silver-tin alloys, as well as low melting temperature gold alloys such as gold-tin. More preferred, are electrically conductive polymer adhesives such as silver filled thermosetting epoxy.

Referring to Figure 6, the integrated circuit device 12 has a back side 19 which is usually devoid of any electrically active components and is generally a flat plane of silicon dioxide or gold metallized silicon or silicon dioxide. The opposing face 34 of the integrated circuit device 12 contains electrically active features as known from conventional integrated circuit technology. Among these electrically active features are an array 50

of input/output pads arranged in a specific configuration. The first metallization array 30 of the substrate 28 is configured to align with the configuration of the input/output pads 50. Other electronic features 52 may include transistors, resistors, and storage regions. An interconnect 54 bonds the integrated circuit device 12 to the substrate 28. The interconnect 54 electrically interconnects the input/output pads 50 with the first metallization array 30. The interconnect 54 is any suitable electrically conductive material including low melting temperature solders such as tin-lead, tin-silver, gold-tin or gold-silicon alloys. Alternatively, an electrically conductive adhesive such as a silver filled thermosetting epoxy may be used.

The assembly 56 is then assembled into an electronic package housing as illustrated in Figure 7. The assembly 56 is supported by a fixture having a fixture base 58 and a fixture cover 60. The fixture base 58 and fixture cover 60 may be formed from any suitable material which can withstand the assembly temperature of approximately 250°C. Preferred materials include stainless steel and aluminum. Supported on the fixture base 58 is the metallic base component 14. A bond material 26 either stamped as a preform in a window frame shape from a thin sheet of adhesive or deposited in a window frame shape by screen printing or direct writing in the form of an adhesive or sealing glass is deposited on the periphery of the metallic base component 14. A thermally conductive chip attach material 62 is deposited on a central region of the

metallic base component 14. The thermally conductive chip attach material 62 may be any suitable material such as a silver filled thermosetting epoxy. The assembly 56 is then deposited onto the base component 14 with a central portion of the leadframe 20 contacting the bond 26 and the back side 19 of the integrated circuit device 12 contacting the thermally conductive chip attach material 62. The cover component 16 is aligned on the opposing side of the leadframe 20 with a bond material 26 disposed therebetween.

The fixture cover 60 is then positioned on the fixture base 58 and provides a desired amount of pressure on bond 26 and thermally conductive chip attach material 62. When heated, an integral bond is formed between the metallic base component 14 and both the leadframe 20 and back side 19 of the integrated circuit device 12. The vent hole 36 is then sealed, completing assembly of the electronic package.

Figure 8 shows in cross-sectional representation an embodiment in which a heat spreader 64 is disposed between the back side 19 of the integrated circuit device 12 and the metallic base component 14. A first thermally conductive chip attach material 62 and a second thermally conductive chip attach material 66 bond the heat spreader 64. The heat spreader 64 is any thermally conductive material such as copper, aluminum or alloys thereof. Anodized aluminum is particularly suited for multichip applications when it is desirable to electrically isolate the individual integrated circuit devices. The heat spreader 64

laterally diffuses heat away from the integrated circuit device 12. The heat spreader 64 has a cross-sectional area larger than the integrated circuit device 12 to both better dissipate heat and to disperse the thermally conductive chip attach material 62 into a thinner, less thermally resistant, layer and also prevents the chip attach material from running up the sides of the integrated circuit device.

While the invention has been described in terms of a leaded electronic package having a single encapsulated integrated circuit device, the invention is equally applicable to leaded packages having a plurality of encapsulated integrated circuit devices, as well as leadless electronic packages.

Figure 9 shows in cross-sectional representation one such leadless electronic package. The ball grid array package 70 has a metallic base component 14 sealed to a cover component 16. The cover component is either electrically nonconductive or, if electrically conductive, coated with a nonconductive layer. Suitable cover materials include ceramics such as alumina or aluminum nitride as well as polymers. One suitable electrically conductive cover is an aluminum alloy coated with an anodization layer.

A first metallization array 30 is formed on an electrically nonconductive surface of the cover component 16. An interconnection 54 electrically interconnects the first metallization array 30 to the electrically active face 34 of an integrated circuit device 12. A second metallization array 72

is formed on an opposing electrically nonconductive surface of the cover component 16. Conductive vias 74 electrically interconnect the first 30 and second 72 metallization arrays. The second metallization array 72 is electrically interconnected to a third metallization array 78 formed on the substrate 80 of a printed circuit board or other circuit assembly. An interconnect 82, such as a low melting temperature solder or conductive adhesive provides the electrical interconnection.

Figure 10 illustrates in cross-sectional representation an electronic package 90 in which the integrated circuit device 12 is directly bonded to the substrate 80 of a printed circuit board. This package is an improvement over conventional flip chip bonded integrated circuits which are coated with silicone glob top. The package 90 has a metallic base component 14 bonded to the back side of the integrated circuit device 12 to conduct heat from the device. The metallic base component 14 is manufactured from a metal such as copper, aluminum, or alloys thereof or a metal compound or metal composite. The thermally conductive chip attach material 62 and the bond material 26 may be any suitable material such as a thermally or ultra violet curable adhesive.

A first metallization array 30 is formed on the substrate 80 an electrically interconnects to the integrated circuit device 12 by interconnects 54. Circuit traces 92, such as patterned copper foil laminated to the substrate 80 electrically interconnect the integrated circuit device to external circuitry 94.

It is apparent that there has been provided in accordance with this invention an electronic package having a metallic base component and one or more flip chip bonded integrated circuit devices which fully satisfy the objects, features and advantages set forth hereinbefore. While the invention has been described in combination with specific embodiments thereof, it is evident that many alternatives, modifications and variations would be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

IN THE CLAIMS:

1. An electronic package (10) housing one or more integrated circuit devices (12) of the type having an electrically active face (34) containing input/output pads (50) of a desired configuration and an opposing back side (19), characterized by:

a metallic base component (12) bonded to said opposing back side (19);

a cover component (16), said metallic base component (12) and said cover component (16) defining a cavity (18);

a leadframe (20) having inner (22) and outer (24) lead ends disposed between said metallic base component (12) and said cover component (16) and bonded (26) to both, said inner lead ends (22) positioned within said cavity (18); and

a substrate (28) disposed within said cavity (18), said substrate (28) containing a first metallization array (30) and a second metallization array (32), said first metallization array (30) electrically interconnected (54) to the input/output pad (50) configuration of said integrated circuit device (12) and said second metallization array (32) electrically interconnected (48) to said leadframe (20).

2. The electronic package (10) of claim 1 characterized in that said substrate (28) contains a circuit (40) bonded to a backing layer (38).

3. The electronic package (10) of claim 2 characterized in that said backing layer (38) is formed from a material selected from the group consisting iron alloys, iron-nickel alloys, iron-nickel-cobalt alloys, alumina, aluminum nitride and boron nitride and said circuit layer (44) is copper circuit traces (40) supported by a dielectric substrate (46).

4. The electronic package (10) of claim 2 characterized in that said substrate (28') is formed from a material selected from the group consisting of alumina, aluminum nitride and boron nitride and said circuit (40) is a metallized paste fired to said support layer (38).

5. The electronic package (10) of claim 2 characterized in that a heat spreader (64) is disposed between said substrate (28) and said back side face (19).

6. The electronic package (10) of claim 5 characterized in that said heat spreader (64) is copper or a copper alloy.

7. The electronic package (10) of claim 6 characterized in that said metallic base component (14) is a material selected from the group consisting of copper, aluminum and alloys thereof.

8. The electronic package (10) of claim 7 characterized in that said metallic base component (14) is an anodized aluminum alloy, said aluminum alloy selected from the series designated 3xxx and 6xxx as designated by the ASM.

9. An electronic package (70) having one or more integrated circuit devices (12) of the type having an electrically active face (34) containing input/output pads (50) of a desired configuration and an opposing back side face (19), characterized by:

a metallic base component (14) bonded to said back side faces (19);

a cover component (16), said metallic base component (14) and said cover component (16) defining a cavity (18), said cover component (16) containing a first metallization array (30) on a surface within said cavity (18) and a second metallization array (72) on an opposing surface, said first metallization array (30) electrically interconnected (54) to the input/output pad (50) configuration of said integrated circuit devices (12) and said second metallization array (72) aligning with a third metallization array (78) formed on the substrate (80) of a circuit assembly; and

conductive vias (74) electrically interconnecting said first metallization array (30) and said second metallization array (72).

10. The electronic package (70) of claim 9 characterized in that said cover component (16) is formed from a material selected from the group consisting of alumina, aluminum nitride and aluminum alloys.

11. The electronic package (70) of claim 9 characterized in that said cover component (16) is an anodized aluminum alloy, said aluminum alloy selected from the series designated 3xxx and 6xxx as designated by the ASM.

12. An electronic package (90) having one or more integrated circuit devices (12) of the type having an electrically active face (34) containing input/output pads (50) of a desired configuration and an opposing back side face (19), characterized by:

a metallic base component (14) bonded to said opposing back side (19);

a cover component (80), said metallic base component (14) and said cover component (80) defining a cavity (18), said cover component (80) containing a first metallization array (30) on a surface within said cavity (18) electrically interconnected (54) to the input/output pads (50) of said integrated circuit devices (12); and

conductive circuit traces (92) electrically interconnecting said first metallization array (30) to external circuitry (94).

13. The electronic package (90) of claim 12 characterized in that said metallic base component (14) is selected from the group consisting of copper, aluminum and alloys thereof.

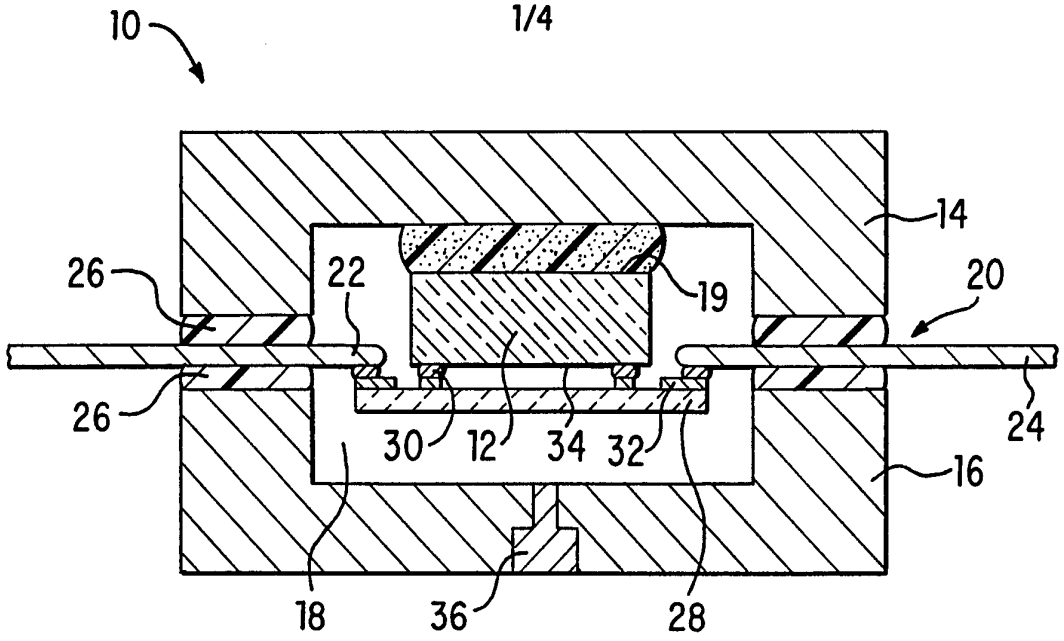


FIG. 1

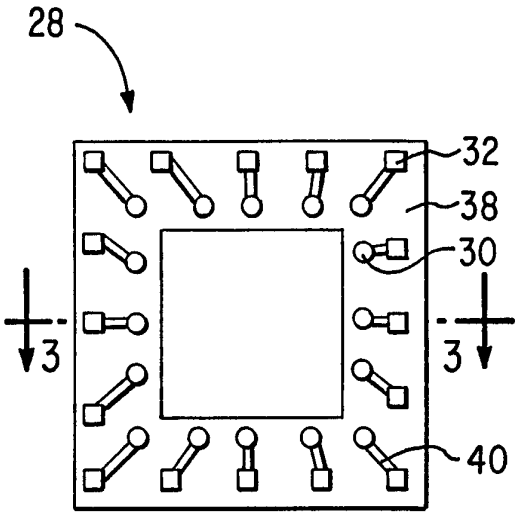
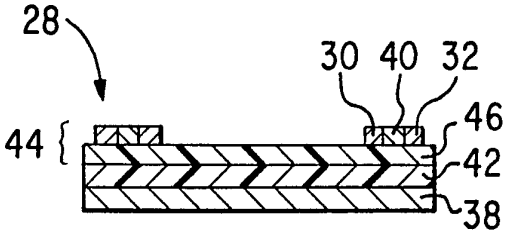


FIG. 2

FIG. 3



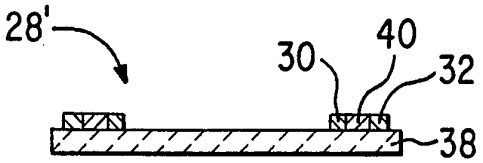


FIG. 4

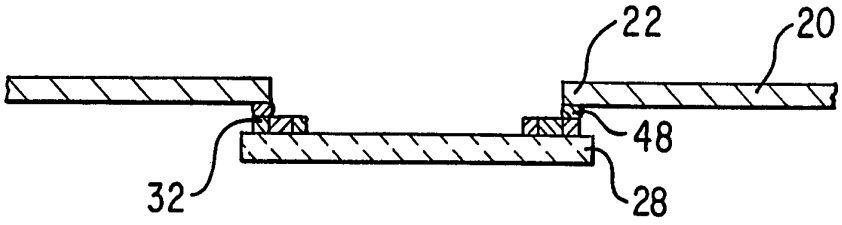


FIG. 5

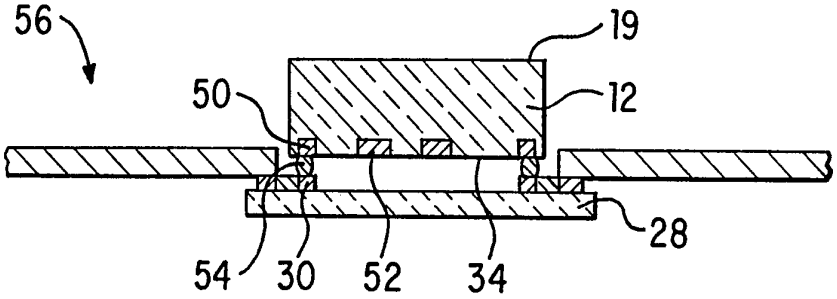


FIG. 6

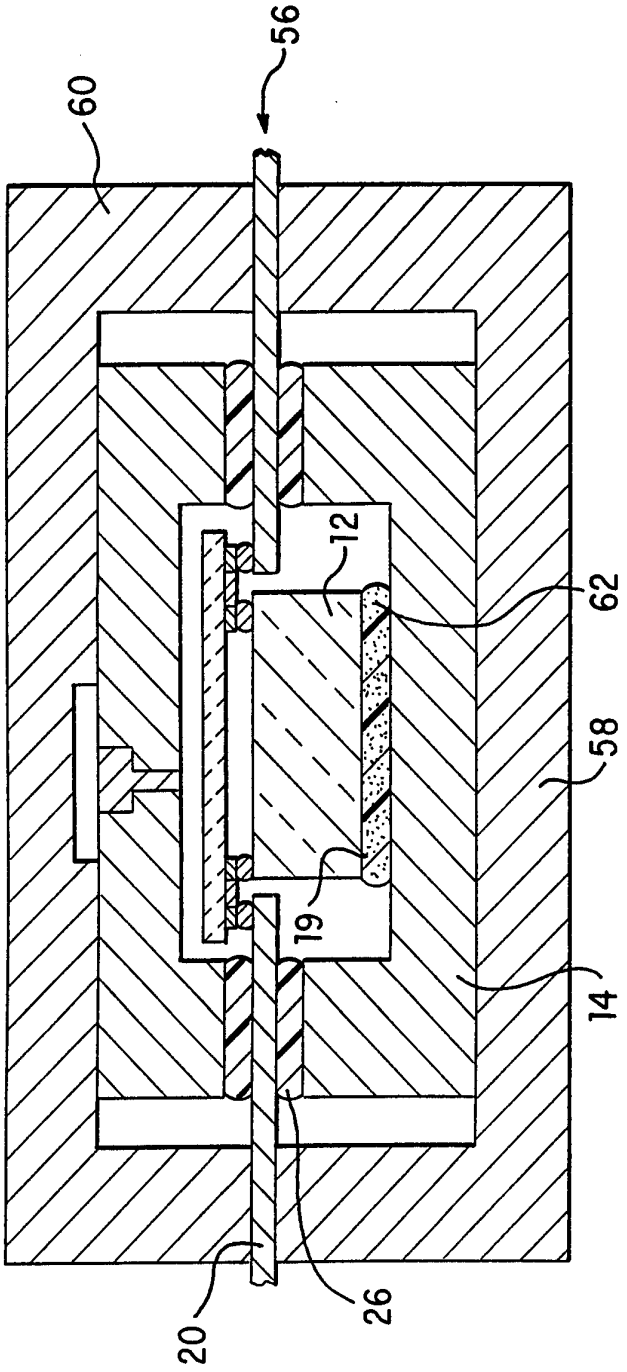
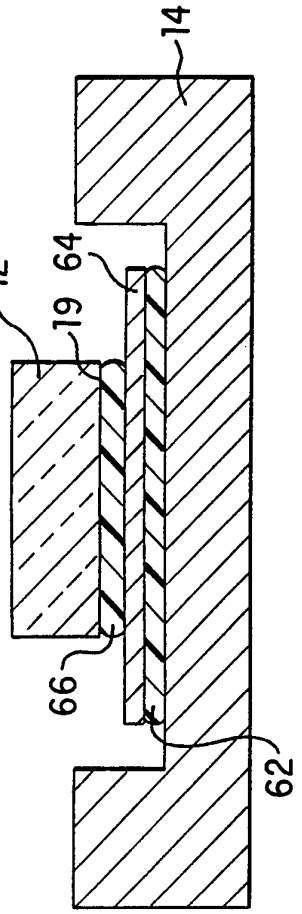


FIG. 7

FIG. 8



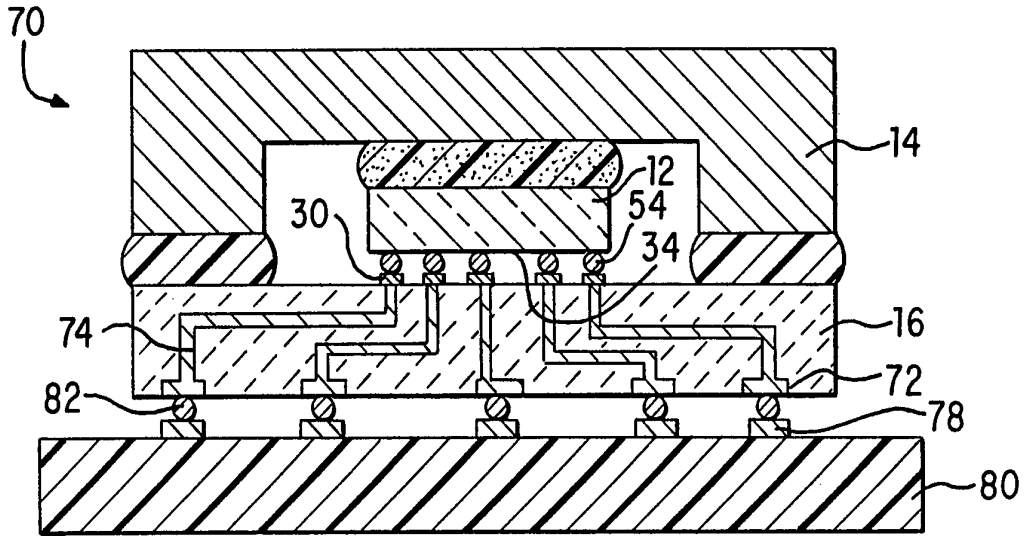


FIG. 9

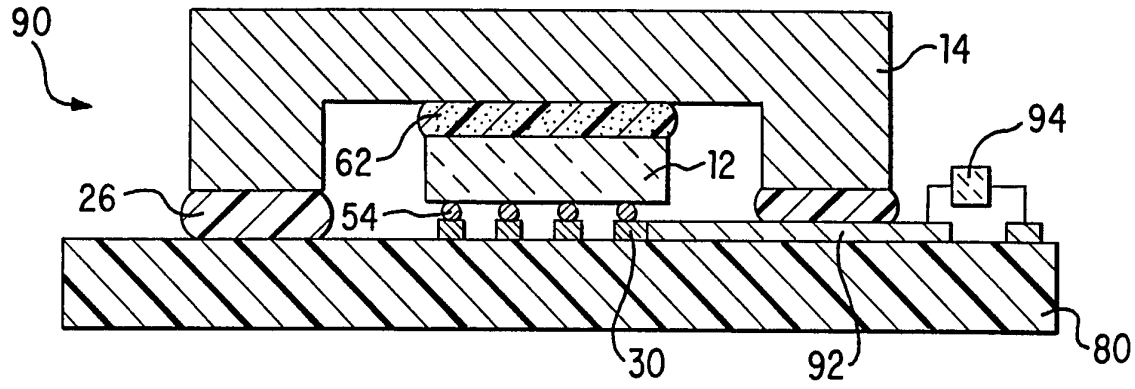


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/09612

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 23/22, 23/48; H05K 7/20
US CL :257/668, 778; 361/704, 813
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/668, 676,688, 777-778, 788; 361/704, 813

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,939,316 (MAHULIKAR ET AL) 03 July 1990, see entire document.	1-8, 9-11
Y	EP, A, 0,210,371 (SATO ET AL) 02 April 1987, see entire document.	1-8
Y	US, A, 4,803,546 (SUGIMOTO ET AL.) 07 February 1989, see entire document.	9-11
Y,P	US, A, 5,311,402 (KOBAYASHI ET ET AL) 10 May 1994, see entire document.	12-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 09 DECEMBER 1994	Date of mailing of the international search report DEC 28 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer THOMPSON GREGORY Telephone No. (703) 308-2249

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