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(54) **Electric circuit arrangement comprising a phase control-circuit.**

(57) A circuit comprises a phase comparator (10) which, when receiving input pulses with which the clock pulses are in phase, produces an output signal having a pulse frequency which is twice the pulse frequency of the input pulses. The ripple on the control voltage for the oscillator (VCO) to be controlled can be compensated for by adding to the output signal of the phase detector a signal which is in anti-phase to the output signal. The result is that only frequency and phase errors produce a ripple on the output signal.

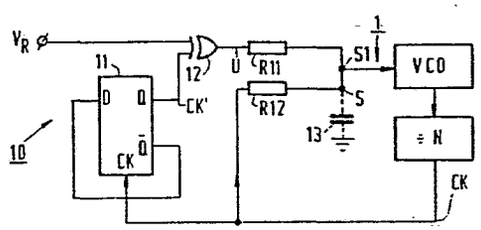

FIG.1a

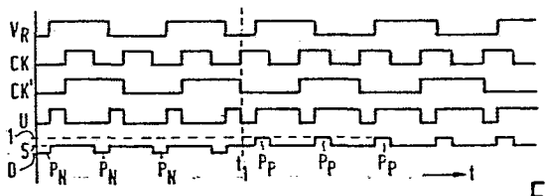

FIG.1b

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Electric circuit arrangement comprising a phase control-circuit.

The invention relates to a phase control-circuit comprising at least one voltage-controlled oscillator and a phase comparator, in which an output of the oscillator is connected at least indirectly to a clock input of the phase comparator for feeding thereto clock pulses produced by the oscillator, said phase comparator being provided with a further input for receiving input pulses, the phase comparator producing from said clock pulses and input pulses a control-signal for the voltage-controlled oscillator.

Such an electric circuit arrangement is known from GB-A 2,089,601 published on June 23, 1982. The electric circuit arrangement shown therein has the property that it does not produce a ripple-free direct voltage even though the clock signal and a data signal to be received are in phase. Consequently, an oscillator controlled by the direct voltage signal will generate a frequency which will always exhibit some undesirable drift.

The invention has for its object to provide a circuit arrangement having a phase control circuit which gives off a ripple-free control-voltage when the lock and the data signals are in phase.

The circuit arrangement having a phase control circuit embodying the invention is characterized in that the phase comparator comprises a D-type flipflop, a pulse delaying element and an exclusive-or gate, said pulse delaying element having a delay time of about half a clock period, whilst a first and a second input respectively of the exclusive-or gate are connected to the output of the pulse delaying element and to the D flipflop respectively and furthermore the clock pulses are applied to the clock input of the D flipflop and the input pulses are applied both to the pulse delaying element and to the D input of

the D flipflop, whilst the output of the exclusive-or gate ic connected to an input of a combinatory network which receives at a further input the clock pulses to form a first and a second output signal, the logical values of which are opposite, when the clock pulses and the input pulses are in phase, whereas when the clock pulses are leading or lagging respectively with respect to the input pulses, the two signals both have the same pulsatory first and second logical values respectively. In such an arrangement, simple means such as a pulse delaying element (not clock controlled), a D flipflop, an exclusive-or gate and a combinatory network provide a phase comparator which supplies a direct voltage, when the clock pulses and the input pulses are in phase (which need not necessarily in regular periods) and which varies it stepwise, under out-of-phase conditions, during the successive clock periods.

A preferred embodiment of a circuit arrangement in accordance with the invention is characterized in that the combinatory network comprises an inverting AND gate, a further AND gate and an inverting gate, in which a first input of the two AND gates is connected to the output of the exclusive-or gate, a second input of the inverting gate and the AND gate respectively receives the clock pulses directly and via the inverting gate respectively, whilst the first and the second output signals are available at the outputs of the AND gates. A phase comparator of this design is very simple and fully satisfies the requirements imposed.

A further embodiment of the circuit arrangement in accordance with the invention, in which the input pulses form a regular periodical signal, is characterized in that the phase comparator comprises a D flipflop and an exclusive-or gate, in which the clock pulses are applied to the clock input of the D flipflop, the output of which is connected for the inverted output signal $\overline{Q}$ to the D input and the output for the output signal Q is connected to a first input of the exclusive-or gate, a further input of which receives the input pulses, whilst at the output of the

exclusive-or gate and the input of the clock pulses a first and a second output signal respectively are available, the logical values of which are opposite, when the clock pulses and the input pulses are in phase, whereas when the clock pulses are leading or lagging respectively with respect to the input pulses, the two signals pulsatorily have the same first and second logical values respectively.

The invention will be described more fully with reference to embodiments shown in a drawing, which shows in

Fig. 1a and 1b an embodiment of a circuit arrangement in accordance with the invention and an associated pulse diagram,

Figs. 2a and 2b a further embodiment of the arrangement with an associated pulse diagram in accordance with the invention,

Fig. 3a and 3b a preferred embodiment of the arrangement with an associated pulse diagram in accordance with the invention and

Fig. 4 a detail of a further embodiment of an arrangement in accordance with the invention.

Fig. 1a shows a first embodiment of a circuit arrangement 1 comprising a phase comparator 10 in accordance with the invention, the circuit arrangement 1 comprising a known voltage controlled oscillator VCO and a frequency divider N which receives the oscillator pulses produced by the oscillator VCO and which produces therefrom clock pulses CK of a lower frequency, which are applied to a clock pulse input of the phase comparator 10. The comparator 10 comprises a D type flipflop 11 which receives the clock pulses CK and the inverted output of which Q is connected to the D input in order to produce a pulse sequence CK' of a pulse frequency amounting to half the pulse frequency of the clock pulses CK. The clock pulses CK and the pulse sequences CK' derived therefrom are represented in Fig. 1b. The output Q of the D flipflop 11 is connected to an input of the exclusive-or gate 12, the second input of which receives input pulses Vr forming a regular periodic signal. By the input pulses the

oscillator VCO is brought to the desired frequency and in the desired phase and maintained therein. The output signal U of the exclusive-or gate 12 is shown in Fig. 1b for two situations as a function of time t. For the instant t_1 the oscillator VCO is leading (the pulses CK are "too early") and after the instant t_1 the oscillator VCO is lagging (the pulses CK are "too late"). The signal U for the instant $t = t_1$ is a "0" level, on which positive peaks "1" are superimposed. After the instant $t = t_1$ the signal U has a "1" level on which negative peaks are superimposed. The pulse frequency of the signal U is twice the frequency of the input pulses Vr. Then a ripple-free control-voltage can be generated (when the oscillator VCO is in phase) by adding the signal CK to the signal U. In the embodiment shown this is performed by applying the two signals U and CK through (preferably equal) resistors R11 and R12 to a junction S1. The resultant signal S is shown in Fig. 1b (as well as the signals Vr and U). The consequence of the combination of the signals U and CK is that only frequency and phase errors can bring about a ripple on the control-voltage. (If the oscillator VCO is leading, the signal S consists of the superimposition of a direct-current signal level midway between the logical "0" and "1" levels and of a plurality of negative pulses P_n having the same pulse frequency as the clock pulses CK and having a logical "0" level. If the oscillator VCO is lagging, the signal S consists of said direct-current signal level on which positive pulses P_p having the logical "1" level and the same pulse frequency as the clock pulses CK are superimposed).It will be obvious that the width of the pulses P_n and P_p depends on the magnitude of the phase difference between the input pulses Vr and the clock pulses CK generated by the oscillator VCO and the clock pulses CK produced by the divider N. As is common practice to do a capacitor 13 can be connected to the junction S1 so that on the junction S1 a mean voltage of the voltage shown in Fig. 1 (S) for controlling the oscillator VCO is formed.

The circuit arrangement shown in Fig. 1a operates only satisfactorily when the input pulses Vr applied thereto form a regular, periodic signal. If the input pulses are not regularly periodical, a phase comparator 2 shown in Fig. 2a can be used in the circuit arrangement embodying the invention or modifications thereof as will be set out hereinafter. The phase comparator 2 shown in Fig. 2a comprises a pulse delaying element 22, a D type flipflop 21, a first and a second exclusive-or gate 23 and 24, an inverting gate 25 and two (identical) resistors R21 and R22. The input pulses A (see Fig. 1b) are applied to the D input of the D type flipflop 21 and to the pulse delaying element 22. The delay of the signal A in the element 22 is substantially equal to half the period of the clock pulse CK applied to the clock input of the D flipflop 21. The output signal B of the element 22 and the output signal C of the D flipflop 21 are applied to the first exclusive-or gate 23, which forms a signal I therefrom (see Fig. 2b). The signal I as well as the clock signal CK are applied to a combinatory network comprising the exclusive-or gate 24 and the inverting gate 25. The clock signal CK is applied to the two gates 24 and 25 and the signal I is applied only to the exclusive-or gate 24. The signals H and CK produced by the gates 24 and 25 with $\overline{CK}$ (see Fig. 2b) constitute the first and the second output signal of the combinatory network. The first and the second output signals H and $\overline{CK}$ are applied through the two resistors R21 and R22 to the junction S as a result of which a control-signal S2 (Fig. 2b) is produced for the voltage-controlled oscillator VCO (not shown in Fig. 2a). When the clock pulses and the input pulses are in phase, the control-signal S2 is again formed by a direct voltage lying midway between the logical "0" and the logical "1" level. By means of the ratio between the values of R21 and R22 the direct voltage level of S2 can be adjusted. When the oscillator is leading (in Fig. 2b at the instant t_2) "negative" pulses (logical "0" level) are formed on the direct voltage level of the signal S2. When the oscillator is lagging (in Fig.2b

after the instant t_2), "positive" pulses (logical "1") are formed on the direct voltage level of S2. The width of the negative or positive pulses is determined by the phase difference between the input pulses A and the clock pulses CK.

As is indicated by a broken line a capacitor 26 can be connected in a conventional manner to the junction S so that across the capacitor 26 a time average of the signal S2 is formed by which said voltage-controlled oscillator is controlled.

Fig. 3a shows a preferred embodiment of a phase comparator 3 for use in a circuit arrangement in accordance with the invention. The input pulses A to be applied to the phase comparator 3 need not necessarily form a regular periodic signal. The phase comparator 3 comprises a D type flipflop 31, a pulse delaying element 32, an exclusive-or gate 33 and a combinatory network itself comprising an AND gate 34, an inverting AND gate 35 and an invertinggate 36. The D flipflop 31, the delaying element 32 and the exclusive-or gate 33 are identical to the components shown in Fig. 2a as well as the clock and input pulses CK and A applied thereto so that the output signal I of the exclusive-or gate 33 (see Fig.3b) is the same as the signal I of Fig. 2b and Fig. 2a. The signal I is applied to the two AND gates 34 and 35 and the clock pulses CK are applied directly to the inverting gate 35 and through the inverting gate 36 to the AND gate 34. The AND gates produce therefrom a first and a second output pulse K and L (see Fig. 3b), which are applied through two (identical) resistors R31 and R32 to the junction S and produce a control-signal S3. It should be noted that the first output signal K has a constant, logical high "1" level, when the oscillator (not shown) is lagging (after the instant t_3, Fig. 3b) and has negative pulses (logical "0" level) when the oscillator is leading (Fig. 3b prior to instant t_3). The second output signal L has a constant logical "0" level when the oscillator is leading (prior to instant t_3 in Fig. 3b) and when the

oscillator is lagging (after t_3), the second output signal has positive pulses (logical "1" level). The control-signal S3 (half the sum of the output signals K and L) produced at the junction is the same as the control-signal S2 (see Figures 2a and 2b). Of course, also in this case a time average of the control-signal S3 is obtained with the aid of a capacitor 37 for controlling the oscillator.

Fig. 4 shows an embodiment of a combinatory network 4 to be used in the phase comparator of Fig. 3. The network 4 receives the signals V and CK (see Figs. 3a and 3b) and comprises three inverting gates 44, 45 and 46. The clock pulses CK are applied to the inverting AND gate 44 as well as to the inverting OR gate 45. The I signal is applied directly to the inverting AND gate 44 and via the inverting gate 46 to the inverting OR gate. From the incoming signals I and CK the gates 44 and 45 produce a first and a second output signal K and L, which are identical to the output signals K and L of Fig. 3a and 3b. The signals K and L of Fig. 4 could, therefore, be joined to form a control-signal in the same manner as is indicated in Fig. 3a. Fig. 4 shows a variant in which the ("negative") and the ("positive") pulses in the signals K and L control switches 42 and 43 respectively. Through the switch 42 or the switch 43 a capacitor 47 is charged or discharged by a current $\underline{i}$ supplied by a current source 48 or a current source 49. The control-signal S4 built up across the capacitor 47 is again the time-mean signal of the control-signal S3 shown in Fig. 3b.

CLAIMS

1. An electric circuit arrangement comprising a phase control circuit having at least one voltage-controlled oscillator and a phase comparator, in which an output of the oscillator is connected at least indirectly to a clock input of the phase comparator for applying thereto clock pulses produced by the oscillator, in which the phase comparator is provided with a further input for receiving input pulses, a control-signal for the voltage-controlled oscillator being formed from said clock pulses and input pulses by the phase comparator, characterized in that the phase comparator comprises a D type flip-flop, a pulse delaying element and an exclusive-or gate, said pulse delaying element having a delay time of about half a clock period, whilst a first and a second input of the exclusive-or gate are connected to the output of the pulse delaying element and to the exclusive-or gate respectively and furthermore the clock pulses are applied to the clock input of the D flipflop and the input pulses are applied both to the pulse delaying element and to the D input of the D flipflop, whilst the output of the exclusive-or gate is connected to an input of a combinatory network, which receives at a further input the clock pulses for forming a first and a second output signal, the logical values of which are opposite, when the clock pulses and the input pulses are in phase, and when the clock pulses are leading or lagging respectively with respect to the input pulses, the two signals have pulsatory the same first and second logical value respectively.

2. A circuit arrangement as claimed in Claim 1, characterized in that the combinatory network comprises a second exclusive-or gate and an inverting gate, an input of the second exclusive-or gate being connected to the output of the first exclusive-or gate and a further input

of the second exclusive-or gate receiving the clock pulses, which are also applied to the invertinggate, whilst a first and a second output signal are available at the outputs of the exclusive-or gate and the inverting gate.

3. A circuit arrangement as claimed in Claim 1, characterized in that the combinatory network comprises an inverting AND gate, a further AND gate and an inverting gate, a first input of the two AND gates being connected to the output of the exclusive-or gate, a second input of the inverting AND gate or of the AND gate respectively receiving the clock pulses directly or via the inverting gate respectively, the first and the second output signal being available at the outputs of the AND gates.

4. A circuit arrangement as claimed in Claim 1, characterized in that the combinatory network comprises an inverting AND gate, an inverting OR gate and an inverting gate in which the output of the exclusive-or gate is connected directly or respectively through the inverting gate to the inverting AND gate and to the inverting OR gate respectively and the further input of the inverting AND or OR gates receive the clock pulses and the first and the second output signal are available at the outputs of the inverting AND or OR gates.

5. A circuit arrangement comprising a phase control-circuit having at least one voltage-controlled oscillator and a phase comparator, in which an output of the oscillator is connected at least indirectly to a clock input of the phase comparator for applying thereto clock pulses produced by the oscillator, in which the phase comparator has a further input for receiving input pulses, a control-signal for the voltage-controlled oscillator being formed from said clock pulses and input pulses by the phase comparator so that the control-signal is a constant voltage at a correct tuning of the voltage-controlled oscillator, whilst the input pulses form a regular periodic signal, characterized in that the phase comparator comprises a D flipflop and an exclusive-or gate, in which the clock pulses are applied to the clock

input of the D flipflop, the output of which is connected for the inverted output signal $\overline{Q}$ to the D input and the output of the output signal Q is connected to a first input of an exclusive-or gate, a further input of which receives the input pulses, whilst a first and a second output signal are available at the output of the exclusive-or gate and the input for the clock pulses respectively, the logical values of said signals being opposite, when the clock pulses and the input pulses are in phase, and when the clock pulses are leading or lagging with respect to the input pulses the two signals have pulsatory the same first and second logical value respectively.

6. A circuit arrangement as claimed in anyone of the preceding Claims, characterized in that the two output signals are applied through two resistors to a junction where the control-signal becomes available.

7. A circuit arrangement as claimed in Claim 3 or 4, characterized in that by the first and the second output signal a first and a second current source respectively is controlled for charging and discharging respectively a capacitor at which the control-voltage becomes available.

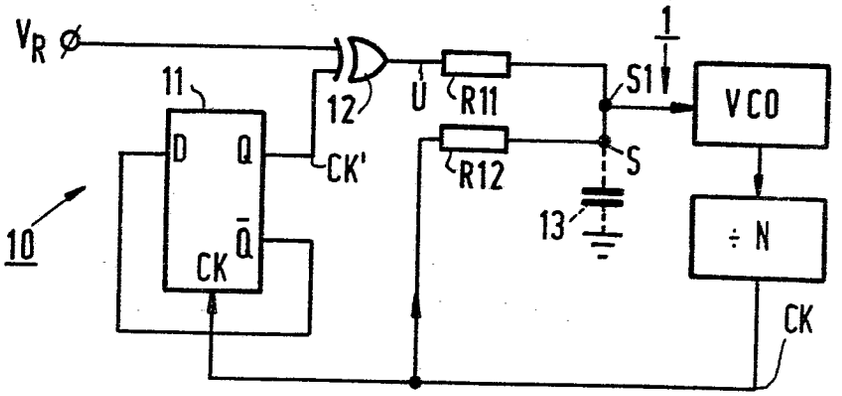

FIG.1a

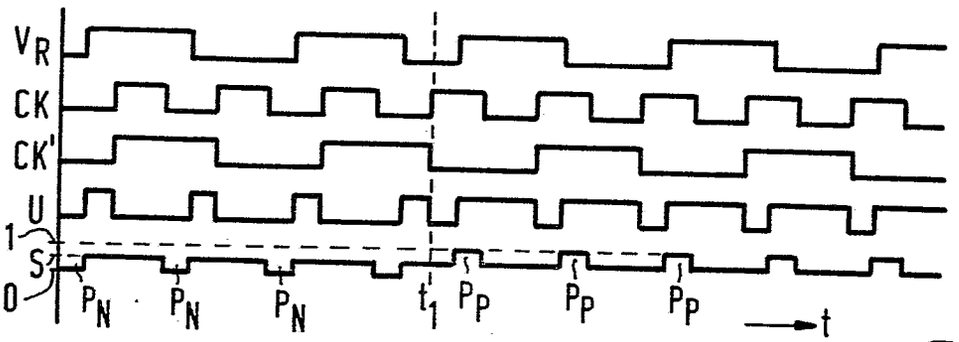

FIG.1b

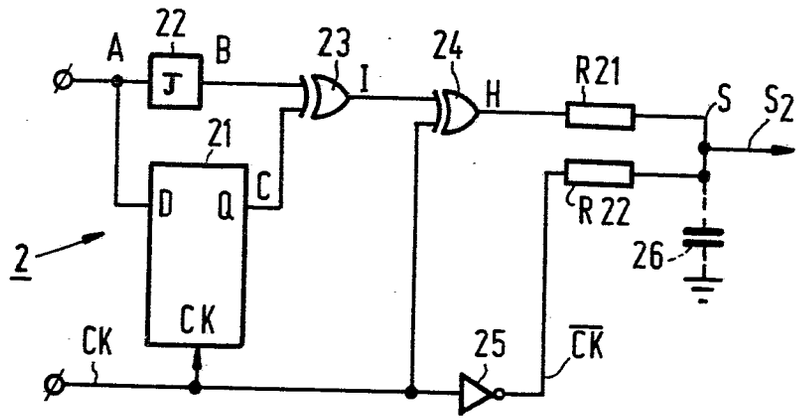

FIG.2a

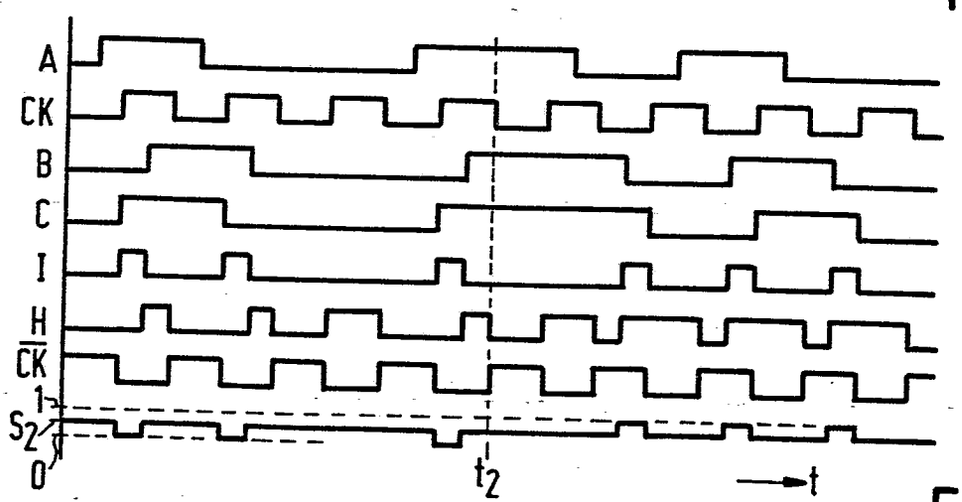

FIG.2b

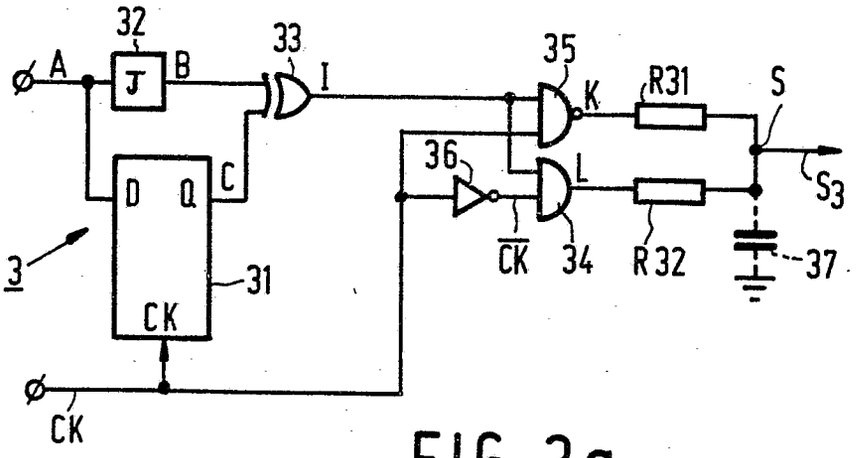

FIG. 3a

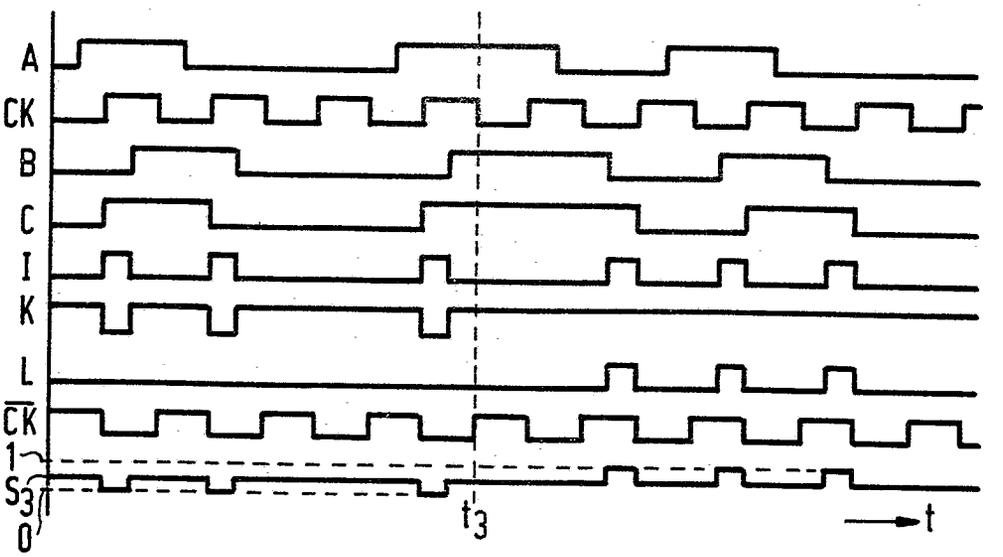

FIG. 3b

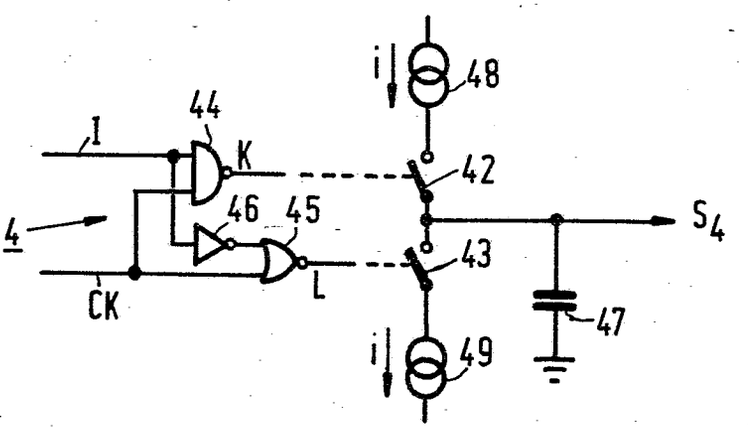

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

0164785 Application number

EP 85 20 0759

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 054 322 (PHILIPS) * Page 9, line 20 - page 11, line 34; figure 7 * & GB - A - 2 089 601 (Cat. D)	1,5	H 03 L 7/08
A	US-A-4 055 814 (ABRAHAM et al.) * Column 2, line 46 - column 5, line 45; figure1 *	1,5	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 03 L
H 03 D
H 04 L
G 01 R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28-08-1985	DHONDT I.E.E.

CATEGORY OF CITED DOCUMENTS

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