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- (71) Applicant (for all designated States except US): **ORACLE INTERNATIONAL CORPORATION** [US/US]; 500 Oracle Parkway, Redwood Shores, CA 94065 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **HARADA, John A.** [US/US]; 531 Church Street, Mountain View, California 94041 (US). **DOUGLAS, David C.** [US/US]; 334 Byron Street, Palo Alto, California 94301 (US). **DROST, Robert J.** [US/US]; 2211 Via Maderas, Los Altos, CA 94024 (US).
- (74) Agent: **SAHASRABUDDHE, Laxman**; 2820 Fifth Street, Davis, California 95618 (US).
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(54) Title: RAMP-STACK CHIP PACKAGE WITH STATIC BENDS

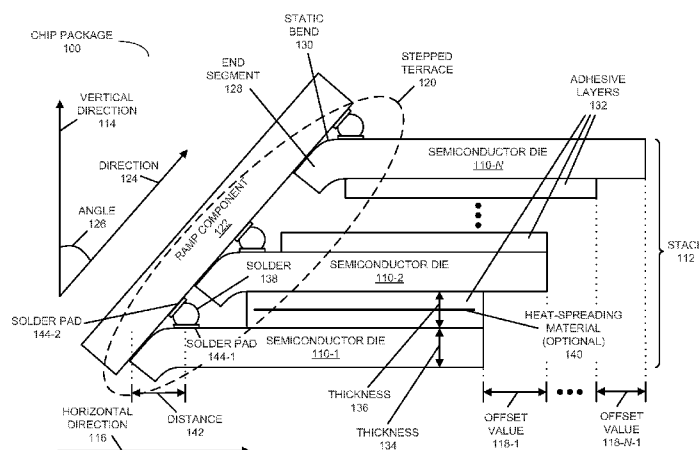


FIG. 1

(57) Abstract: A ramp-stack chip package is described. This chip package includes a vertical stack of semiconductor dies or chips that are offset from each other in a horizontal direction, thereby defining a terrace with exposed pads. A high-bandwidth ramp component, which is positioned approximately parallel to the terrace, is electrically and mechanically coupled to the exposed pads. For example, the ramp component may be coupled to the semiconductor dies using: solder, microsprings and/or an anisotropic conducting film. Furthermore, each of the semiconductor dies includes a static bend so that an end segment of each of the semiconductor dies is parallel to the direction and is mechanically coupled to the ramp component. These end segments may facilitate high-bandwidth communication of signals between the chips and the ramp component, for example, via proximity communication.



INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 376 904 B1 (HABA BELGACEM [US] ET AL) 23 April 2002 (2002-04-23) figures 7A-7D	1-20
A	----- EP 1 028 463 A1 (TOSHIBA KK [JP]) 16 August 2000 (2000-08-16) claim 1; figures 5A-6C -----	1-20



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Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040,
 Fax: (+31-70) 340-3016

Authorized officer

Cortes Rosa, João

INTERNATIONAL SEARCH REPORT

Information on patent family members

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			US 6621155 B1	16-09-2003

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