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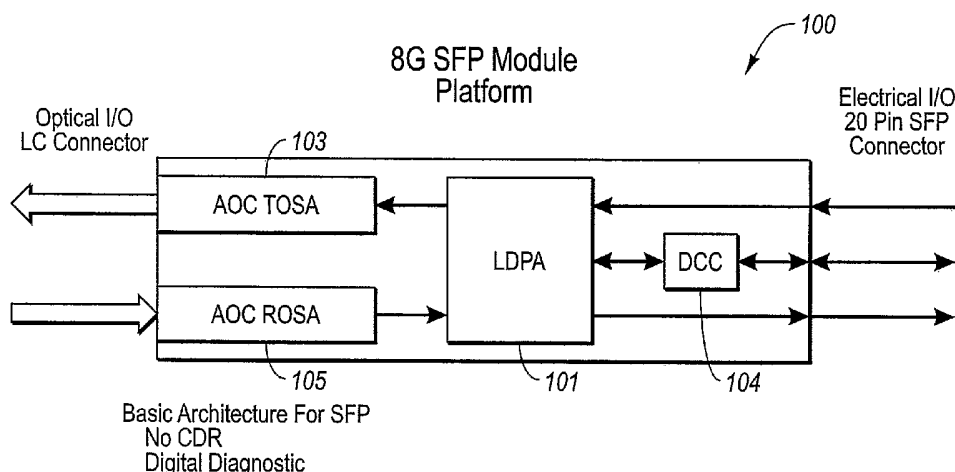
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(54) Title: HIGH SPEED SFP TRANSCEIVER



(57) Abstract: This disclosure concerns optoelectronic transceivers. In one example, a transceiver is implemented as an uncompensated architecture that is substantially compliant with the SFP MSA and is capable of effective operation at a data rate of about 8.5Gb/s. The transceiver includes a TOSA, ROSA, a printed circuit board, an LDPA disposed on the printed circuit board and configured for communication with the TOSA and the ROSA. Finally, the transceiver includes SFP compliant optical and electrical connections.

HIGH SPEED SFP TRANSCEIVER

Field of the Invention

The present invention relates generally to optical communication networks and associated systems, methods and devices. More particularly, embodiments of the invention are concerned with transceivers that achieve relatively high data rates without using CDR signal compensation, while nonetheless maintaining substantial compliance with applicable performance standards.

Related Technology

Data can be efficiently propagated through fiber optic networks and devices by the transmission of optical "1" and "0" digital signals. Maintenance of the integrity of the transmitted data, as well as the speed, or rate, at which the data is transferred relies in large part on the timing of the data. That is, the operation of fiber optic data transmission systems is predicated on the ability to reliably ensure that particular bits of data are transmitted at particular times.

To this end, typical fiber optic data transmission systems incorporate a clock signal that defines the time periods in which data is to be transmitted. The clock may be included in the data stream, or may take the form of a separate signal. The use of clock that is common to the transmitter and the receiver means that the same reference is employed for both data transmission and reception processes throughout the data transmission system. By synchronizing the data transmission system operations in this way, a relatively high degree of data integrity can be achieved.

As line rates move higher however, it becomes increasingly likely that the data will get out of sync with the clock, so that the data bits are not being transmitted precisely during the designated bit periods defined by the clock. This phenomenon is sometimes generally referred to as jitter. Jitter can be caused by environmental factors, circuit design, or by the system components themselves. Because no system performs ideally, typical fiber optic data transmission systems are designed to tolerate a certain amount of jitter without experiencing materially adverse effects in terms of overall system performance. The amount of jitter that can be safely tolerated is sometimes referred to as the jitter budget of the system, or of a component. Significant problems may arise however, when the jitter budget is exceeded.

In particular, excessive jitter can result in data pulse overlap so that a particular data pulse moves forward into the preceding data pulse, or backward into the succeeding data pulse. As a result, the receiver may not be able to detect the presence or absence of a particular pulse, and data integrity is lost.

As technology advances and line rates correspondingly increase, jitter presents an increasingly significant problem. Consequently, various devices and systems have been developed in an attempt to maintain jitter and, accordingly, data integrity, at an acceptable level. One approach that has been employed involves the use of circuits that attempt to compensate for jitter by reshaping and retiming the data stream at various points in the fiber optic communications network so that the jitter budget is not exceeded. The processes of reshaping and retiming the data are sometimes collectively referred to as clock and data recovery ("CDR").

While the CDR approach to jitter compensation has proven useful in some applications, the incorporation of CDR circuits and devices complicates the design, construction, and operation of the transceiver. Correspondingly, the use of CDR circuits and devices also increases the cost of the transceiver. A related problem is that while transceivers exist that do not employ CDR functionality, those transceivers have inherent limitations. In particular, transceivers that do not employ CDR functionality are generally able to avoid the use of CDR circuits and devices because those transceivers operate at relatively low data rates.

ASPECTS OF AN EXEMPLARY EMBODIMENT OF THE INVENTION

In view of the problems in the field that have been identified herein, and other problems not specifically addressed here, it would be useful to provide a transceiver module that employs a simplified architecture without CDR compensation, while also achieving relatively high data rates in a manner that is substantially compliant with various performance and other standards. Accordingly, embodiments of the invention are generally concerned with optoelectronic transceivers that employ a relatively low speed architecture that is nonetheless capable of achieving relatively high data rates without requiring CDR or comparable data signal integrity compensation.

One exemplary embodiment of the invention is concerned with a Fibre Channel compatible transceiver that is generally implemented in the form of a 4G SFP transceiver, although some exceptions may apply with regard to particular

embodiments. Because the transceiver is generally compliant with the SFP MSA, no CDR data signal integrity compensation is implemented in the exemplary transceiver. That is, the SFP architecture, as provided for in the SFP MSA, does not include or implement CDR data signal integrity compensation.

Among other things, the exemplary transceiver includes an integrated post-amplifier and laser driver ("LDPA") in communication with a transmitter optical subassembly ("TOSA") and receiver optical subassembly ("ROSA"), where the ROSA and TOSA are nominally rated for 10 Gb/s operation. The transceiver further includes digital diagnostics systems and functionality, implemented in part by a diagnostics control chip ("DCC") that interfaces with both internal and external devices. In this implementation, the DCC and the LDPA are located on opposing sides of the transceiver circuit board so as to facilitate efficient use of the space in the transceiver housing. Finally, the lengths of one or more traces of the transceiver are minimized to the extent that the exemplary implementation will permit, so as to enhance performance.

In this way, exemplary embodiments provide various useful results. For example, 8G functionality is provided within a 4G SFP architecture and form factor. Particularly, the 8G data rate, and others, are achieved without necessitating the use of any CDR data signal integrity compensation, while maintaining compliance with performance standards for the transceiver.

BRIEF DESCRIPTION OF THE DRAWINGS

To further clarify the above and other aspects of embodiments of the present invention, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. These drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. In addition, the drawings are not drawn to scale. The invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Fig. 1 is a high level schematic of an exemplary embodiment of an 8G SFP module having a 4G SFP architecture;

Figure 2A is a view of a first side of an exemplary 8G SFP board showing the arrangement of a ROSA, TOSA, EEPROM and FCC;

Figure 2B is a view of a second side of an exemplary 8G SFP board showing the arrangement of the ROSA, TOSA, and an LDPA;

Figure 3 indicates electrical and optical eye diagrams corresponding to operation of an exemplary embodiment of the 8G SFP transceiver at about a 2.5Gb/s data rate;

Figure 4 indicates electrical and optical eye diagrams corresponding to operation of an exemplary embodiment of the 8G SFP transceiver at about a 4.25Gb/s data rate; and

Figure 5 indicates electrical and optical eye diagrams corresponding to operation of an exemplary embodiment of the 8G SFP transceiver at about a 8.5Gb/s data rate.

ASPECTS OF EXEMPLARY EMBODIMENTS OF THE INVENTION

Included as part of this disclosure are various figures providing information concerning aspects of some exemplary embodiments of the invention. The figures are illustrative only and should not be construed to limit the scope of the invention in any way.

I. 8G SFP Transceiver Capabilities and General Operation

Exemplary embodiments of the invention are concerned with an 2/4/8Gb/s ("8G") SFP transceiver that substantially comprises a 4G SFP architecture. In this way, nominal rates of 8G are achieved within a desired SFP MSA form factor while meeting performance standards, and without necessitating CDR data signal integrity compensation.

In general, 8G nominal data rates are achieved with the 4G SFP architecture. Such data rates may be achieved in this way for various protocols, one example of which is Fibre Channel. Note that the aforementioned 8G nominal data rate is approximately 8.5G in the Fibre Channel protocol, and may take other values in connection with other protocols. Accordingly, the scope of the invention is not limited simply to 8Gb/s and 8.5Gb/s data rates. In addition to supporting the nominal 8G data rate, at least some embodiments of the invention are also backwards compatible with nominal 1/2/4G data rates for protocols which include Fibre Channel. This is particularly useful since the transceiver can thus operate in connection with 1/2/4G legacy systems.

As noted above, exemplary embodiments of the invention are able to achieve relatively high data rates, with acceptable performance, without requiring data signal integrity compensation. Elimination of data signal integrity compensation circuits

and devices enables relatively low power dissipation to be achieved. In general, power dissipations in the region of about $< 1\text{W}$ can be achieved. In some short wave applications, power dissipation is only about $< 600\text{ mW}$, and in some long wave applications, power dissipation is only about $< 800\text{ mW}$.

II. Exemplary 8.5 Gb/s SFP Transceiver Platform

Attention is directed now to some general aspects of an exemplary SFP transceiver. As noted above, one exemplary embodiment of the invention is concerned with a Fibre Channel compatible transceiver that is generally implemented in the form of a 4G SFP transceiver, such as is employed in Fibre Channel and Ethernet applications. Because the transceiver is generally compliant with the SFP MSA, incorporated herein in its entirety by this reference, no data signal integrity compensation methods or circuitry are implemented in the exemplary transceiver and, as the disclosure herein indicates, no such data signal integrity compensation is necessary to achieve data rates such as 8.5Gb/s.

Consistent with the foregoing, exemplary transceivers that do not require or implement CDR, or comparable, functionality may be referred to herein as comprising or implementing “uncompensated” data signal generation and/or processing components and circuitry. More generally, such transceivers may be referred to as comprising or embodying an “uncompensated” architecture. In similar fashion, operation of such exemplary transceivers may be referred to generally herein as “uncompensated” operation.

At least some embodiments of the invention comprise a 2/4/8G SFP transceiver without CDR. Other embodiments are directed to a 4/8G SFP transceiver without CDR. More generally, embodiments of the invention are concerned with SFP transceivers that are able to support some or all of the 1/2/4/8G nominal data rates, although such transceivers may generally be referred to herein as an “8G SFP transceiver.”

In general, exemplary embodiments of the invention have the same port density as 1/2/4G Fibre Channel and have an optical backward compatibility with 2/4G Fibre Channel. Additionally, embodiments of the invention are electrically and mechanically backward compatible with 2/4G Fibre Channel, that is, the electrical connector and cage of the transceiver are configured to interface with 2/4G Fibre Channel systems and components. Thus, an exemplary embodiment of the 8G

SFP transceiver can be employed in connection with 2/4G legacy systems, and legacy 2/4G modules can be used in 8G systems.

Depending upon the particular system with which the 8G SFP transceiver is to be used, various aspects of the 8G SFP transceiver may be adjusted or modified. As one example, if backward compatibility of the 8G SFP transceiver is only needed for 2/4G Fibre Channel, bandwidth tunability of the receiver may not be required. Correspondingly, some embodiments of the invention employ a receiver with a sensitivity of -19 dBm at 10.7G. The receiver may or may not be a fixed bandwidth receiver.

Sample receiver sensitivity specifications include: -20 dBm (FTRJ8524) at 1.0626G; -18 dBm (FTRJ8524) at 2.125G; and, -15 dBm (FTRJ8524) at 4.25G. One exemplary embodiment of the invention has a measured receiver sensitivity of -20 dBm (FTRJ8524) at 4.25G. Another embodiment of the invention, using the exemplary HFD6x80-41 ROSA and Vitesse post amplifier discussed below, has a measured receiver sensitivity of -16 dBm (FTRJ8524) at 8.5G, with an extinction ratio ("ER") of 3-4dB and 10^{-10} .

With attention now to Figures 1 and 2, various aspects of an exemplary 8G SFP transceiver module 100 are disclosed. In general, Figure 1 is a block diagram illustrating aspects of an exemplary transceiver module 100, and Figure 2 is a photograph of an 8G board 102 that conforms to the SFP MSA.

As indicated, the disclosed embodiment does not employ or incorporate CDR data signal integrity compensation. The illustrated transceiver 100 includes an integrated LDPA 101 configured for communication with a TOSA 103 and a ROSA 105, where the ROSA 103 and TOSA 105 are nominally rated for 10 Gb/s operation. One example of such an LDPA 101 is a 4G laser driver-post amplifier such as those produced by Vitesse Semiconductor Corporation ("Vitesse"). One particular Vitesse model that may be used is the Vitesse VSC7964 laser driver and limiting amplifier. However, other LDPAs of comparable functionality and configuration may alternatively be employed. Separate laser drivers and post-amplifiers may also be used in some embodiments of the invention.

Similarly, the TOSA 103 and ROSA 105 are exemplified by optoelectronic devices produced by Advanced Optical Components ("ADOPCO") of Richardson, TX. In particular, the TOSA 103 may comprise, for example, an ADOPCO HFE6x9x-56 TOSA with an 850nm vertical cavity surface emitting laser

("VCSEL") and having an associated nominal data rate of 10G. The ROSA 105 may comprise, for example, an ADOPCO HFD6x80-41 ROSA with 850nm P-I-N detector and preamp, and having an associated nominal data rate of 10G. In the illustrated implementation, the ROSA 105 and TOSA 103 are hard-connected to the circuit board 102 of the transceiver 100. In alternative embodiments however, the ROSA and/or TOSA employ flex connections.

Any other ROSA and/or TOSA of comparable functionality, performance, and configuration may alternatively be employed however. For example, a ROSA and/or TOSA having a nominal data rate greater or less than 10G may be employed in some cases. Note also that embodiments of the invention are not limited to 850nm devices, and devices operating at other wavelengths may also be employed. As well, optical transmitters other than VCSELs may be employed. Examples of alternative optical transmitters include distributed feedback ("DFB") lasers and Fabry-Perot ("FP") lasers.

The exemplary 8G SFP transceiver 100 further includes digital diagnostics systems and functionality, implemented in part by a diagnostics control chip ("DCC") 104 that interfaces with both internal and external devices. One suitable diagnostics control chip is an Atmel SL828 microcontroller, although other devices of comparable functionality and configuration may alternatively be employed.

As best illustrated in Figure 2, the exemplary 8G SFP transceiver 100 is configured so that the DCC 104 and the LDPA 101 are located on opposing sides of the transceiver circuit board so as to facilitate efficient use of the space in the transceiver housing. The illustrated embodiment further includes, among other things, an EEPROM 106.

Finally, it should be noted that aspects of embodiments of the invention may be modified as necessary to achieve the nominal 8G rate in an SFP form factor. For example, the lengths of one or more traces of the transceiver board may be minimized to the extent that the exemplary implementation will permit, so as to enhance performance. In one particular embodiment, fixed electrical equalization and preemphasis may be implemented in the transceiver if particular traces, such as FR4 traces for example, exceed a certain length, such as about 2 to about 3 inches for example. Suitable trace lengths may vary from one embodiment to another but can be readily determined in various ways, such as through the use of a module demonstrator for example.

III. Examples of Operating Environments and Applications

Exemplary embodiments of the 8G SFP transceiver are well suited for use in connection with the Fibre Channel protocol. However, the scope of the invention is not limited to any particular protocol.

In addition, embodiments of the transceiver represent solutions for a variety of different operating environments. As an example, the 8G SFP transceiver can be used as a short wave solution for 100m multimode fiber ("MMF") (50 μ m 500 MHz km). As another example, the 8G SFP transceiver can be used as a short wave solution for distances up to at least about 10km using single mode fiber ("SMF").

Depending upon considerations such as link length, embodiments of the invention may take various forms. For example, 100m short wave applications are suitable for employing an 850nm VCSEL. Longer link lengths, such as 1-2km long wave applications, may require an FP laser or LW VCSEL. Finally, link lengths of about 10km or greater may necessitate the use of a DFB laser. Aspects of the 8G SFP transceiver other than the optical emitter may additionally or alternatively be modified if necessary.

IV. Performance

Directing attention finally to the optical and electrical eye diagrams designated as Figures 3-5, it can be seen that an exemplary embodiment of the 8G SFP transceiver provides good performance at a variety of data rates. More particularly, Figures 3 through 5 indicate that both optical and electrical masks are maintained at the following data rates: 2.5G (Rx sensitivity of -19 dBm); 4.25G (Rx sensitivity -19 dBm); and, 8.5G (Rx sensitivity -16 dBm). It should be noted with regard to Figure 4 that the distortion in the upper portion of the optical eye diagram is due to a bad connector, and does not reflect any shortcoming in the construction, arrangement or performance of the associated transceiver. Thus, embodiments of the invention are able to employ a 4G SFP architecture to successfully operate at relatively high data rates, such as 8.5Gb/s or higher, without CDR or comparable compensation, while maintaining compliance with operational standards and requirements such as masks and eye diagram requirements.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the

foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

CLAIMS

What is claimed is:

1. A transceiver module, comprising:
an uncompensated architecture capable of a data rate of about 8.5Gb/s,
the uncompensated architecture comprising:
a TOSA;
a ROSA;
a printed circuit board;
an LDPA disposed on the printed circuit board and configured for communication with the TOSA and the ROSA; and
at least one connector in communication with at least one of: the ROSA; and, the TOSA.
2. The transceiver module as recited in claim 1, wherein the uncompensated architecture is substantially compliant with the SFP MSA.
3. The transceiver module as recited in claim 1, wherein the TOSA and the ROSA are each capable of performing at a data rate of about 10Gb/s.
4. The transceiver module as recited in claim 1, wherein the TOSA includes one of: a DFB laser; an 850nm VCSEL; and, an FP laser.
5. The transceiver module as recited in claim 1, wherein the ROSA includes an 850nm P-I-N detector and preamp.
6. A transceiver module, comprising:
an architecture that is substantially compliant with the SFP MSA and that is capable of a data rate of about 8.5Gb/s, wherein the architecture comprises:
a TOSA;
a ROSA;
a printed circuit board;
an LDPA disposed on the printed circuit board and configured for communication with the TOSA and the ROSA; and
at least one connector in communication with at least one of: the ROSA; and, the TOSA.

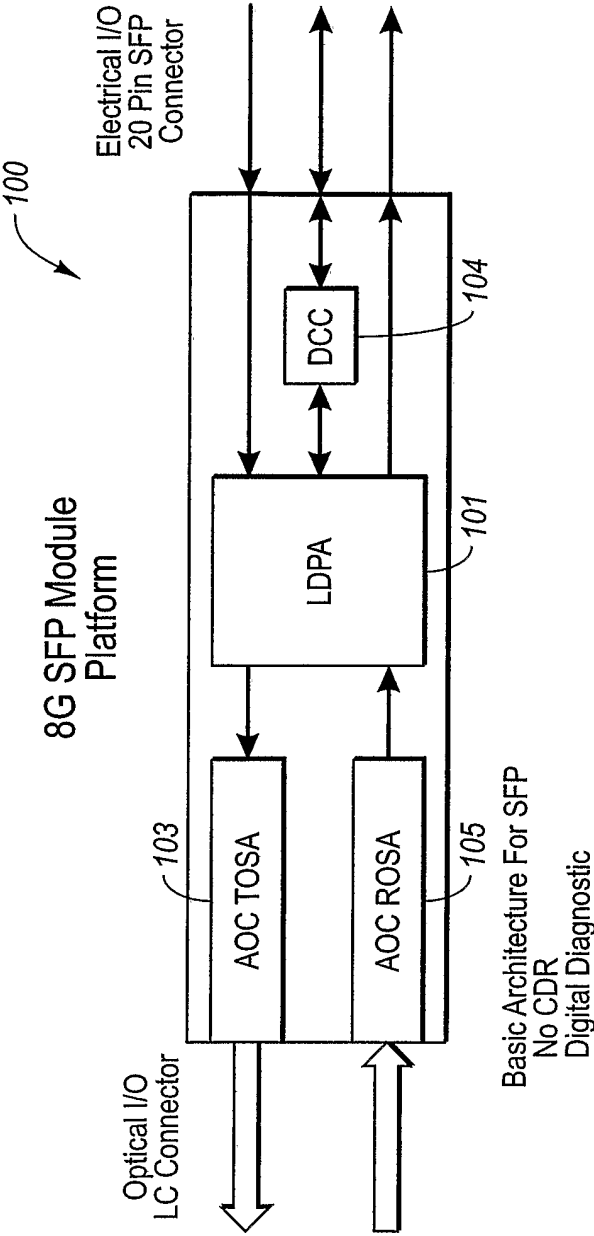


Fig. 1

8G SFP Board Layout

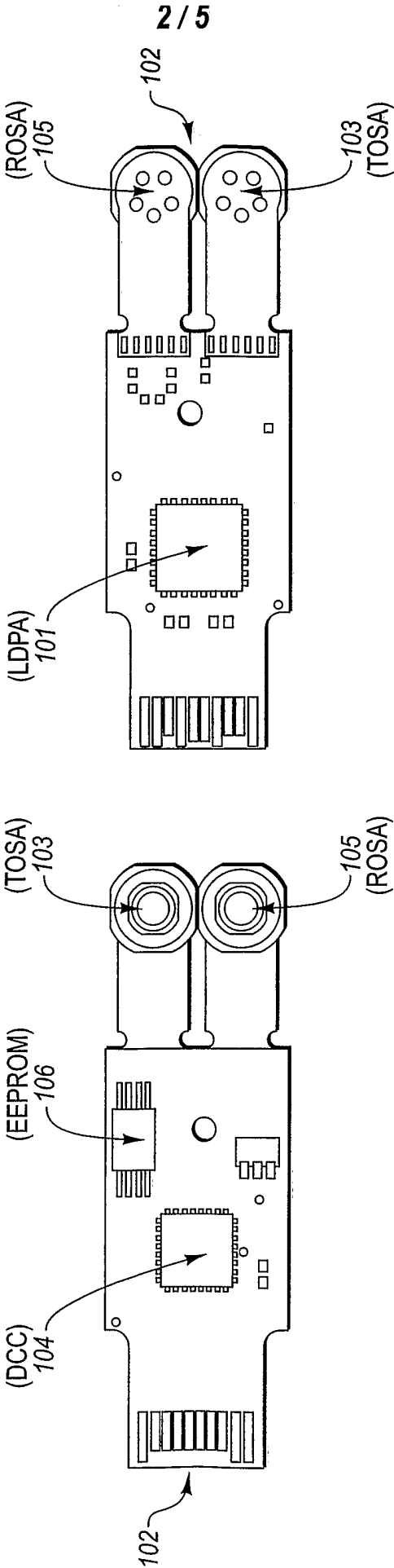


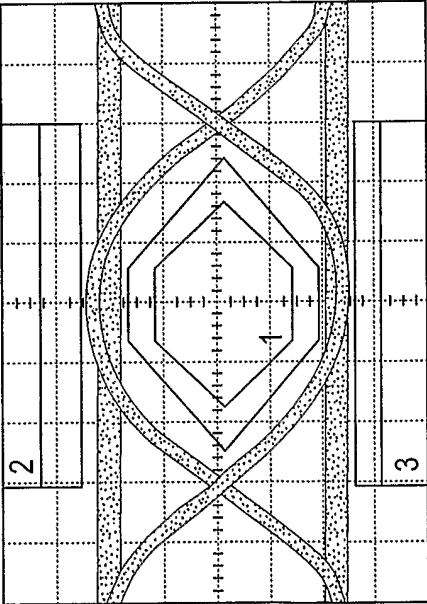
Fig. 2B

Fig. 2A

2.5G Eyes

Optical

(Acq Limit Test) Waveforms: 301
Diff 1-2,125



Mask

FC2125 PI REV13
total wfms 306 margin 59 %
failed smpls 0 mask hits 0
source 3 margin hits 0
Y Align: Full Disp total hits 0

③ 62 μ W/div
77 μ V

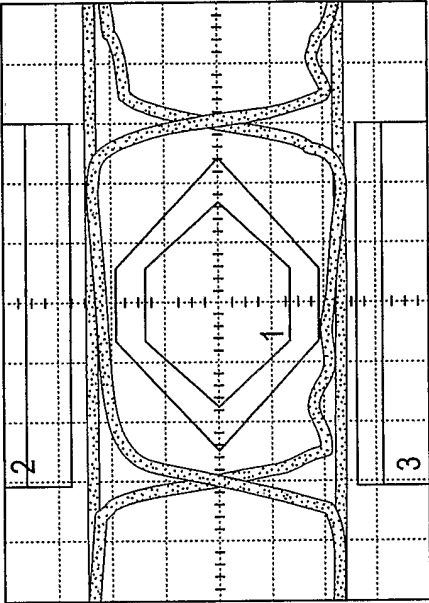
④ 67.8 mV/div
700 μ V

Time: 77.6 ps/div
Delay: 24.0871 ns

Trig: Normal
-208mV

Electrical

(Acq Limit Test) Waveforms: 301
Diff 1-2,125



Mask

FC2125 PI REV13
total wfms 335 margin 64 %
failed smpls 0 mask hits 0
source 4 margin hits 0
Y Align: Full Disp total hits 0

③ 62 μ W/div
77 μ W

④ 68.2 mV/div
400 μ V

Time: 78.9 ps/div
Delay: 24.1352 ns

Trig: Normal
-208mV

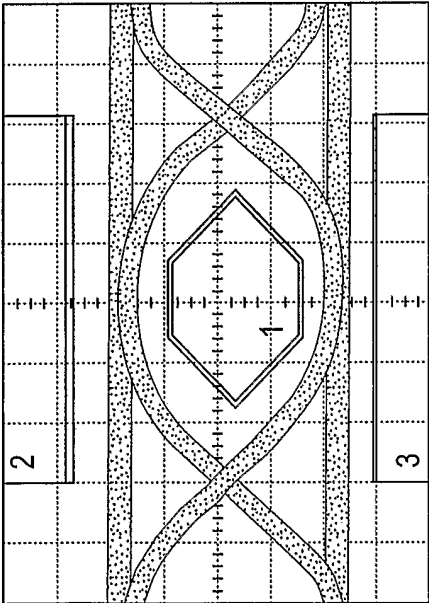
Rx sensitivity = -19dBm

Fig. 3

4.25G Eyes

Optical

(Acq Limit Test) Waveforms: 301
Diff 1-4.25



Mask

FC4250 PI REV13

total wfms 306 margin 11 %
failed smpls 0 mask hits 0
source 3 margin hits 0
Y Align: Full Disp total hits 0

③ 56 μ W/div
④ 68 μ V

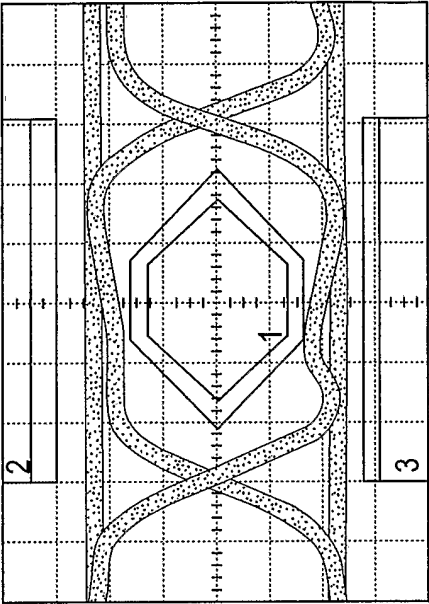
④ 68.2 mV/div
④ 400 μ V

Time: 38.7 ps/div
Delay: 24.2172 ns

Trig: Normal
-207mV

Electrical

(Acq Limit Test) Waveforms: 301
Diff 1-4.25



Mask

FC4250 PI REV13

total wfms 356 margin 37 %
failed smpls 0 mask hits 0
source 4 margin hits 0
Y Align: Full Disp total hits 0

③ 56 μ W/div
④ 68 μ V

④ 68.0 mV/div
④ 700 μ V

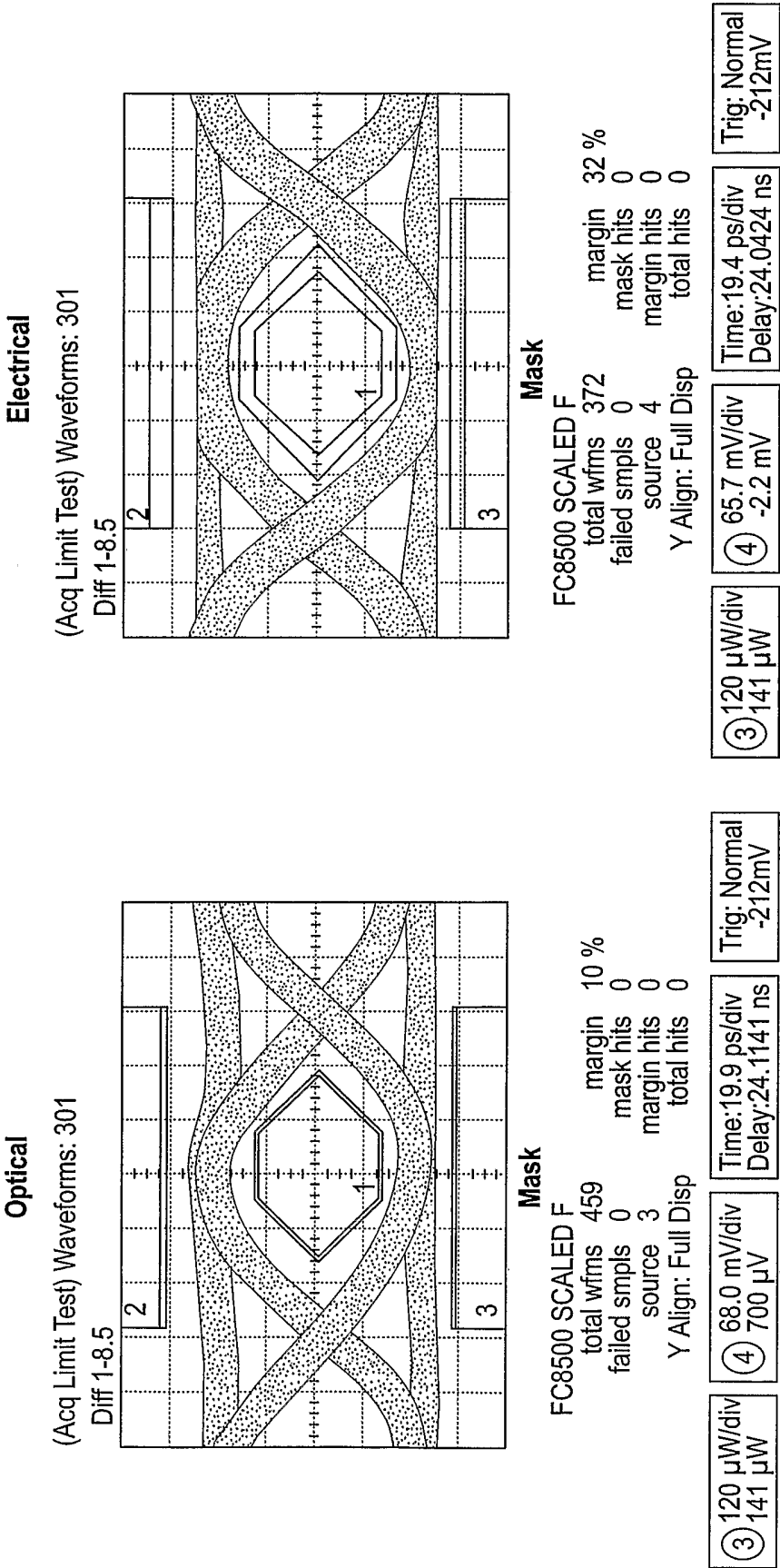
Time: 38.9 ps/div
Delay: 24.2065 ns

Trig: Normal
-207mV

Rx sensitivity = -18dBm

Fig. 4

8.5G Eyes



Rx sensitivity = -16dBm

Fig. 5