FET mixer comprising two switching circuits, each comprising two series connected FET transistors (Q1, Q2; Q3, Q4); a local oscillator balun (T1A, T1B) having a single two terminal input port and two terminal output ports, each output port being connected to the together connected bases of the transistors (Q1, Q2; Q3, Q4) of one of the switching circuits; an RF balun (T2A, T2B) connecting the RF input signal to the drains of the transistors of the switching circuits; an IP balun (T3A, T3B) and a DC bias circuit (45). The mixer needs only a low local oscillator power, provides for a partial cancellation of the nonlinearity distortion imposed on the RF signal and has a reduced intermodulation distortion.
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TRIPLE-BALANCED PASSIVE TRANSMISSION FET MIXER

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates generally to radio frequency communication devices and more specifically to passive transmission FET mixers requiring relatively low local oscillator power levels and having excellent isolation of the local oscillator signal relative to the radio and intermediate frequency signals.

Description of the Prior Art

The dynamic range of many prior art microwave front-ends is controlled by the single and two-tone intermodulation levels of a Schottky diode mixer. (S. Weiner, D. Neuf, S. Spohrer, "2 to 8 GHZ Double Balanced MESFET Mixer With +30 dBm Input 3rd Order Intercept," 1988 IEEE MTT-S Digest, pp.1097-1099.) A typical Schottky mixer obtains third order intercept points approximately equal to the local oscillator (LO) power minus the conversion loss plus 10-Db. The diode-ring double-balanced mixer often requires the LO power to exceed the signal compression level by 6-Db. Trade-offs between LO power levels and third order intercept and one Dbm compression points are inevitable, even in multiple diode schemes attempting to improve isolation, bandwidth, and single-tone intermodulation levels.

Low distortion mixing is known to be possible with small amounts of LO power when an unbiased channel of a GaAs MESFET is used as the mixing element. (See, Stephen A. Maas, "A GaAs MESFET Balanced Mixer With Very Low Intermodulation,"
1987 IEEE MTT-S Digest, pp.895-896.) Weiner, et al., describe both single and double balanced mixers that use GaAs MESFETs instead of diodes. These mixers typically operate over a two to eight Ghz range and obtain third order intercepts greater than +28 Dbm at an LO power input of +23 Dbm, with typical conversion loss of 8-Db, and an LO to radio frequency (RF) isolation greater than 25-Db. Weiner, et al., explain that previous designs using MESFETs had been limited by the LO balun and intermediate frequency (IF) transformer. These limitations were overcome by using a ring of GaAs MESFETs and tapered micro strip baluns in single and double balanced configurations to achieve multi-octave bandwidths. However, the bandwidth of these units is limited by the MESFET package parasitic reactances used in the ring. Weiner, et al., indicate that their future experiments will include a monolithic quad-MESFET with special gate geometry designed to improve the third order distortion, and wire-bonding of the FET to an alumina substrate to minimize parasitic reactances.

The Siliconix Si8901-DBM is a monolithic quad-MOSFET ring demodulator/mixer that is reported to achieve third-order intercepts exceeding +37 Dbm and 2-Db signal overload compression and desensitization of +30 Dbm at a LO drive level of +17 Dbm (50 mW). (Ed Oxner, "High Dynamic Range Mixing With The Si8901," March 1988, pp.10-11.) The Si8901 commutation-mixer relies on the switching action of the quad-MOSFET elements to effect a mixing action. The MOSFETs act, essentially, as a pair of switches reversing the phase of a signal at a rate determined by the LO frequency. The MOSFETs exhibit a finite on-resistance that is expressed as a conversion efficiency loss. The loss results from the $r_{ds(on)}$ of the MOSFETs relative to both the signal and IF impedances and signal conversion to unwanted frequencies.

**SUMMARY OF THIS INVENTION**

Briefly, the present invention comprises a triple balanced passive transmission FET mixer that operates in the LO/RF/IF frequency range of from 10 Mhz to 1000 Mhz with reduced levels of nonlinearity and intermodulation distortion as the result of the topological structure and the application of a dc bias to FET channels used for mixing which is useful for both up- and down-frequency conversion of RF and IF signal frequencies. The RF and IF signal frequencies may overlap.
It is therefore a feature of the present invention to produce a radio frequency mixer that has a wide dynamic range of operation and low overall signal distortion including low intermodulation distortion and partial cancellation of nonlinearity distortion imposed on the radio frequency signal. These and other features and advantages of the present invention will no doubt become clear to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a block diagram of an embodiment of the triple balanced mixer of the present invention.

FIG. 2 is a schematic diagram of a preferred embodiment of the triple balanced mixer of the present invention.

FIG. 3 is a schematic of a pair of back-to-back FETs used as a model to explain how the present invention reduces intermodulation distortion in the preferred embodiment.

FIG. 4 is a schematic diagram of wavefront propagation in a transmission line.

FIG. 5 is a schematic diagram of the embodiment of the invention in FIG. 2 showing the flow of current (neglecting phase shift in the transmission lines) in the RF and IF baluns of the mixer when FETS Q1 and Q2 are conducting (ON) and FETS Q3 and Q4 are not conducting (OFF) for an applied RF input signal.

FIG. 6 is a schematic diagram of the embodiment of the invention in FIG. 2 showing the flow of current (neglecting phase shift in the transmission lines) in the RF and IF baluns in the mixer when FETS Q1 and Q2 are not conducting (OFF) but FETS Q3 and Q4 are conducting (ON) for an applied RF input signal.

FIG. 7 is a schematic diagram of the embodiment of the invention in FIG. 2 showing the flow of current (neglecting phase shift in the transmission lines) in the RF and IF baluns of the mixer when FETS Q1 and Q2 are conducting (ON) and FETS Q3 and Q4 are not conducting (OFF) for an applied IF input signal.

FIG. 8 is a schematic diagram of the embodiment of the invention in FIG. 2 showing the flow of current (neglecting phase shift in the transmission lines) in the RF and IF baluns in the mixer when FETS Q1 and Q2 are not conducting (OFF) but FETS Q3 and Q4 are conducting (ON) for an applied IF input signal.
FIGs. 9 and 10 are schematic diagrams that illustrate the manner in which amplified LO signals of the FET drains are isolated from the RF-port and IF-port.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

FIG. 1 illustrates an embodiment of the triple-balanced mixer 10 of the present invention. Mixer 10 comprises a balanced local oscillator (LO) circuit 11, first and second switching circuits 12 and 13 coupled to local oscillator input circuit 11, a switching circuit control circuit 14 (a bias circuit in the preferred embodiment) coupled to and provided for controlling the switching operation of switching circuits 12, 13, a radio frequency (RF) to intermediate frequency (IF) coupling circuit 16 connected to the switching circuits 12 and 13. A two-terminal local oscillator input port 19 having a pin terminal 20 and a ground terminal 21 is provided for coupling an external local oscillator (LO) signal source 22 to the local oscillator circuit 11 via a LO input filter circuit 23. A two-terminal radio frequency (RF) port 24 having a pin terminal 25 and a ground terminal 26 is provided for coupling an external radio frequency signal sink (or source) 27 to the RF-to-IF coupling circuit 16, and a two-terminal intermediate frequency (IF) port 28 having a pin terminal 29 and a ground terminal 30 is provided for coupling an external intermediate frequency signal source (or sink) 31 to the RF-to-IF coupling circuit 16. Control circuit 14 may optionally be provided with a control circuit input port 32 for coupling the circuit to externally generated signals. For example, in one embodiment of the invention a bias voltage generated by an external bias voltage source 33 is applied to the mixer circuit 10 at input port 32.

Mixer 10 may be operated as either an up-frequency converter in which case the input signal is applied at the intermediate frequency (IF) port 29 and the output signal is extracted at the radio frequency (RF) port 24, or as a down-frequency converter in which case the input signal is applied at the RF port 24 and the output signal is extracted at the IF port 28. The RF and IF ports may be used as stated, or reversed roles, with only minor changes in performance.

When operated as a frequency down conversion circuit, the RF input signal is applied at the RF port 24 and coupled to the switching circuits 12, 13 via RF-to-IF
coupling circuit 16. The LO signal is applied at LO port 19 and coupled to switching circuits 12, 13 in phase complementary manner so that switch 12 is on when switch 13 is off and vice versa. The switches operate at the frequency of the LO input signal, and the rapid transition from a low impedance (ON) to a high impedance (OFF) results in a mixing action between the LO and RF signals within the switch. Control circuit 14 provides an optional control signal for influencing operation of the switching devices 12, 13. Each of the switching circuits 12, 13 are fabricated in such a manner that temporal changes in admittance in each switch (implemented by FETs in one embodiment) resulting from application of the RF signal approximately cancel, thereby reducing intermodulation distortion RF-to-IF. Coupling network 16 is fabricated such that good LO-to-IF, LO-to-IF, and RF-to-IF isolation are realized.

FIG. 2 is an illustration of a preferred embodiment of the triple-balanced mixer shown in functional block diagram form in FIG. 1. In this embodiment, switching devices 12, 13 are realized with a first pair (Q1 and Q2) 38 and a second pair (Q3 and Q4) 39 of interconnected field-effect transistors (FETs), each FET having a control or gate (G) terminal, as well as drain (D) and source (S) terminals. The source terminal of Q1 is connected to the source terminal of Q2, and the source terminal of Q3 is connected to the source terminal of Q4. The FET-pair switching devices 38, 39 are responsible for mixing the local oscillator (LO) signal coupled to the FET switch by the LO input circuit 11 with the radio frequency (RF) signal coupled to the FET switches by the RF-to-IF coupling circuit 16 to generate an intermediate frequency (IF) signal. Because these FET-pairs are at the heart of the signal mixing action and couple to the LO, RF, and IF functional components of the mixer circuit, the structure and operation of mixer 10 are described relative to the FET-pairs 38, 39.

In an embodiment of the triple balanced mixer described, the mixer operates over a LO/RF frequency range of about 1700 MHz to about 2200 MHz, and nominally operates with a LO drive signal of about +21 dBm and a -5 Volt bias voltage. The gate terminals are self biasing at about -2 volts. The circuit is typically useful over the RF bandwidth range of from about 1700 MHZ to about 2200 MHZ, an IF bandwidth of from about 10 MHZ to about 200 MHZ, and LO drives of from about 1700 MHZ to about 2200
MHz; however, in principle there are no absolute frequency limits to the circuit's applicability.

FET pair Q1-Q2 38 provides a single switching operation between circuit nodes 40 and 41. Similarly combined FET-pair Q3-Q4 provides a single switching operation between circuit nodes 42 and 43. Each node 40, 41, 42, and 43 corresponds to a drain terminal of one of the FETs.

In general, signal propagation through a FET junction has a perturbing effect on FET admittance. When FET admittance is perturbed, such perturbation results in output signal distortion, particularly signal intermodulation distortion. Therefore reducing the admittance perturbing effect will reduce distortion and improve overall mixer performance. In the present invention, implementing each signal switching function with FET-pairs rather than with single FETs reduces the perturbing effect as described hereinafter.

When operating as a frequency down-converter where an externally generated RF signal is applied to the RF port, the RF signals are forced to pass through both FETs (Q1 and Q2) of FET-pair 38 in such a way that the RF signal enters the drain of one FET (Q1) emerges from the source terminal of the same FET (Q1), then enters the source terminal of the second FET (Q2) and emerges from the drain of the second FET (Q2). In this circuit, propagation of the RF signal through the first FET (Q1) may perturb the admittance of the FET with the resulting effect on the output signal, but for FETs (Q1 and Q2) of comparable construction, propagation through the second FET (Q2) has an opposite perturbing effect on the admittance of Q2 as compared to the effect on Q1. The same local oscillator signal pumps (switches) both FETs in the FET pair. The net effect of propagation of the signal through both serially connected (source-to-source) FETs Q1 and Q2 is cancellation of some of the distortion, including an appreciable amount of intermodulation distortion. The theoretical basis for this distortion cancellation is now described.
The serially connected FET-pair structure and application of drain bias to the channels of the FET transistors provide structure and method for significantly reducing the intermodulation distortion in the mixer output signal. The manner in which the each pair of back-to-back FETs reduce distortion is now described with reference to FIG. 3, which shows a pair of serially connected FETs (e.g. Q1-Q2 or Q3-Q4). The gate-to-source voltage \( V_{GS} \) is equal to the sum of the gate-to-drain voltage \( V_{GD} \) and the drain-to-source voltage \( V_{DS} \).

\[
V_{GS} = V_{GD} + V_{DS}
\]

Let \( V_{GS} \) be fixed, set by a fixed voltage source for example, then:

\[
0 = \Delta V_{GD} + \Delta V_{DS}
\]

\[
\Delta R_{DS} \propto C \Delta V_{GD}, \text{ where } C \text{ is a constant.}
\]

The change in resistance between the two FET drains \( \Delta R_{D1D2} \) is equal to the change of resistance between the source and drain of the first FET Q1 \( \Delta R_{DIS1} \) and the change of resistance between the source and drain of the second FET Q2 \( \Delta R_{DIS2} \).

\[
\Delta R_{D1D2} = \Delta R_{DIS1} + \Delta R_{DIS2},
\]

\[
= -C (\Delta V_{DIS1} + \Delta V_{DIS2})
\]

To a first approximation, the voltage \( V_{DIS} \) is symmetrically dropped across both FETS Q1 and Q2, so that:

\[
V_{DIS1} = -V_{DIS2} \text{ (approximately)}.
\]

Therefore, it follows that the change in resistance between the two FET drains is approximately zero:

\[
\Delta R_{D1D2} \approx 0.
\]

The small signal shown in FIG. 3 (corresponding to the RF input signal in mixer circuit 10) passes through the FET channel combination Q1 and Q2 without controlling the resistance of the FET channel combination. This condition is equivalent to infinite intermodulation suppression and helps reduce intermodulation distortion in mixer 10.
Infinite intermodulation suppression is achieved only if the approximations assumed here hold, that is for an ideal system. In an actual physical circuit, the approximations do not hold exactly, and intermodulation is suppressed by some finite amount. A comparable derivation showing that the change in resistance between the FET pair Q3-Q4 drain terminals is zero may be made for FET-pair Q3-Q4.

The triple balanced nature of the mixer also reduces mixer distortion. At about the same time that each FET is in transition from "ON" to "OFF" (Q1-Q2 midway from on to off, or Q3-Q4 midway from off to on, for example) the FET transistors are producing nearly maximum distortion. The symmetrical structure of Q1 and Q2 relative to the structure of Q3 and Q4 advantageously results in partial cancellation of the distortion produced by Q1 and Q2 with that distortion produced by Q3 and Q4. The cancellation only obtains for a short period of time, but since cancellation occurs during a period of maximum distortion, and is recursive with respect to every cycle of the LO signal, such cancellation can be significant relative to overall mixer operation.

In reference to FIG. 2, the FETs operate with a gate bias voltage $V_g$ applied by gate bias circuit 44 between the gate and source terminals and a drain bias voltage $V_d$ applied by drain bias circuit 45 between the drain and source terminals. The drain bias voltage $V_d$ acting as a switch control signal source 33 is generated by an external drain bias voltage source 46, while the gate terminals of the FETs are self biased as described hereinafter.

A dc drain bias voltage is generated by dc drain bias circuit 45 and applied to the channels of the mixing FETs (Q1, Q2, Q3, and Q4) at each FET source terminal. This drain bias voltage to the FET pairs significantly reduces intermodulation distortion in the output signal as described. Drain bias circuit 45 is connected to an external dc bias voltage source 46 at drain bias port 47. Scaling resistor R1 94 (50 ohm) serves to scale the bias voltage that appears at the source terminal of each FET transistor (Q1, Q2, Q3, and Q4), and to limit the bias current through each FET. Optional diode D1 95 provides reverse bias protection. Capacitor C1 96 provides ac isolation of the bias port 47 from the other mixer components. The bias voltage is coupled to the FET source
terminals through resistors R4 97 and R5 98, which provide an appropriate impedance for the bias current into each FET pair. For example, in one embodiment of the invention resistors R4 and R5 are selected at about 25 ohms each to provide the desired impedance. The drain bias circuit 45 also comprises RF transmission line balun (T2A, T2B) 73, 76 and IF transmission line balun (T3A, T3B) 80, 81 which provide a dc return path to ground for the drain bias current. For example, drain bias current flows from the point of application at the Q1 source terminal, through FET Q1, out the drain terminal of Q1, and then through IF balun T3A 80 to the ground terminal 79 at IF port 77. Those having ordinary skill in the art in light of this specification will realize that other dc drain bias current paths exist through the baluns.

Application of the drain bias to the FET causes the FET to function as a LO signal amplifier. When a drain bias voltage is applied to the FET source terminals, and the LO signal is applied to the connected gate terminals of the two paired FETs, a LO response signal appearing much like an amplified version of the gate LO signal is generated within the FET structure and appears at each conducting FET drain terminal. The appearance of this drain LO response signal enhances the switching behavior of the FET. The applied LO signal and the response LO signal generated within the FET junction work together in a compound fashion so that, in essence, each FET sees a larger LO driving signal than the LO signal applied at the gate alone. Therefore, the FET switches operate with a lower externally applied LO signal.

The gate self bias is now described with reference to FIG. 2. The gate terminal of each FET is self-biased so that no explicit bias supply is needed. Gate bias voltage provided by Gate bias circuit 44 is generated for FET pair 38 (Q1-Q2) by coupling capacitor C2 58, which functions as a dc current blocking capacitor, between the first LO input circuit 11 output port and joined FET-pair Q1 and Q2 gate terminals. FET pair 38 is pumped by balanced LO circuit 11 comprising first transmission line balun T1A (T1A1 and T1A2) 51 and second transmission line balun T1B (T1B1 and T1B2) 54, first and second termination resistors R2 56 and R3 57, and dc blocking capacitors C2 58 and C3 59. Each of FET Q1 and Q2 attains to a self bias level by the charging of capacitor C2 during Q2, Q2 forward gate conduction. Analogously, gate bias voltage
is generated for FET pair 39 (Q3-Q4) by coupling the second LO input circuit 11 output port with capacitor C3 59 to FET pair 39 (Q3-Q4) gate terminals. Eliminating an explicit bias source for the gate is advantageous because such implementation reduces cost by eliminating some components, and eliminates the inconvenience of having to provide the separate bias source. However, provision of self-biasing circuitry does not preclude application of a separate external gate bias if additional flexibility is desired for tuning the behavior of the mixer circuit 10.

In the exemplary circuit of FIG. 2, where a -5 volt external bias voltage is applied to bias terminal 47, resistor R1 94 is 50 ohms, resistors R4 97 and R5 98 are each 25 ohms, resistors R2 56 and R3 57 are each 100 ohms, capacitor C1 96 is 10K picofarad (pF), capacitors C2 and C3 are each 50 pF, and optional diode D1 95 is a silicon junction diode, the gate terminals of FETs Q1, Q2, Q3, and Q4 self-bias at about -2 volts relative to their source terminals. Nominal circuit component values for the exemplary mixer 10 are indicated parenthetically after the component name.

The two inputs of the balanced LO drive circuits 11 are coupled to external LO source 22 at the LO port 19 through dc blocking capacitors C4 61 and C5 62. The outputs of the two balanced local oscillator drive circuits are connected to the FET pairs 38, 39 in a phase complementary fashion so that Q1 and Q2 are driven 180-degrees out of phase relative to Q3 and Q4. That is, the local oscillator source input connected to pin terminal 20 of the two-terminal LO input port 19 is coupled to the gates of Q1 and Q2 but to the source terminals of Q3 and Q4. And the local oscillator source input connected to the ground terminal 21 of the two-terminal LO input port 19 is coupled to the gate terminals of Q3 and Q4, but to the source terminals of Q1 and Q2.

Within the first part of local oscillator circuit 11, inductor L1 47 (3 nanoHenry (nH)) is connected in serial with inductor L2 48 (3 nH), and the serial combination is connected in parallel with transmission line balun T1A 51 termination resistor R2 56 (100 ohm). Capacitor C6 49 (0.5 pF) is connected between the node common to serially connected inductors L1 and L2 and ground. Analogously within the second part of local oscillator circuit 11, inductor L3 50 (3 nH) is connected in serial with inductor L4 52
(3 nH), and the serial combination is connected in parallel with transmission line balun T1B 54 termination resistor R3 57 (100 ohm). Capacitor C7 53 (0.5 pF) is connected between the node common to serially connected inductors L3 and L4 and ground. Pin terminal 71 and ground terminal 72 of RF input port 70 are coupled to the mixer switching devices 38 and 39 (Q1-Q2 and Q3-Q4) via RF balun T2A (T2A1 and T2A2) 73 and T2B (T2B1 and T2B2) 76. Pin and ground terminals 78, 79 of IF input port 77 are coupled to the mixer switching devices 38 and 39 (Q1-Q2 and Q3-Q4) via IF balun T3A (T3A1 and T3A2) and T3B (T3B1 and T3B2) 80, 81. The RF balun comprises two transformers 73, 76 and IF balun comprises two transformers 80, 81. In one embodiment of the invention, each LO balun, RF balun, and IF balun comprises a pair of 100 ohm transmission line bifilar wires. For example, T2A is a 100 ohm bifilar wire and T2B is a 100 ohm bifilar wire.

The RF balun (73, 76) and IF balun (80, 81) are wired to each other in such a fashion that during frequency down-conversion (for example), and in conjunction with a LO signal applied to switching devices 38, 39 and the action of the switching devices, RF input energy flows unidirectionally from the RF port 70 (source) to IF port 77 (sink). Each of the two RF transmission line transformers 73, 76 making up the RF balun and the two IF transmission line transformers 80, 81 making up the IF balun participate in the conveyance of energy during each and every LO signal half cycle as described in great detail hereinafter. For frequency up-conversion, input energy from the IF port acting as the (source) would flow unidirectionally from the IF port 77 to the RF sink at the RF port 70 in analogous manner.

In a transmission line, the energy in a wave travels in a single direction (before reflection), in this case from left to right as shown in FIG. 4. Upon reflection, it courses back on itself. We can say that the reflected wave travels from right to left as shown in FIG. 4. Associated with the wave, there are local values of voltage and current. A voltage appears at any position Xo as a potential difference across the line. Also, a pair of associated local currents (a local current pair) pair exists in the line at Xo, where the local currents flow in complementary directions, as shown. When the incident wavefront reaches the load, the wave is partially reflected, resulting in both forward and reflected
traveling waves at the load. It is the local current pairs of the forward and reflected waves that flow through the load.

It is therefore ultimately clearer to describe circuit operation by referring to the entire balanced circuit action as a whole. In this context, for a balanced signal that passes simultaneously through both diplexers, the traveling voltage wave reflects from the FETs due to impedance mismatch between the transmission line ($=50\Omega$) and the FETS ($Z_{\text{FETS,ON}} = 8\Omega$, $Z_{\text{FETS,OFF}} \geq 1000\Omega$). When the FETS are conducting the FET impedance is much less than the line impedance ($Z_{\text{FETS}} << 50\Omega$) and when the FETS are not conducting, their impedance is much greater than the line impedance ($Z_{\text{FETS}} >> 50\Omega$). The current associated with the local wavefronts of both the incident and reflected waves must flow through $Q_1$ and $Q_2$, since they form current pairs flowing into the load (e.g. at node A) and out of the load (e.g. at node B); hence they flow through the load.

The energy (current) flow is achieved by providing direct electrical connections between appropriate circuit components (as shown and described hereinafter) and by exciting modes in the transmission line baluns that have appropriate propagation modes. In particular, a first terminal 84 of the RF balun output port is coupled to the first FET Q1 drain and to a second terminal 89 of the first IF balun output port, a second terminal 85 of the first RF balun 73 output port is coupled to the third FET Q3 drain and to a second terminal 91 of second IF balun 81 output port, a first terminal 86 of the RF balun 76 output port is coupled to the fourth FET Q4 drain and to a first terminal 88 of the IF balun 80 output port, and a second terminal 87 of the second RF balun 76 output port is coupled to second FET Q2 drain and to a first terminal 90 of the IF balun 81 output port.

The coupling between local oscillator balun transformers 51, 53 and the gate and source terminals of the first, second, third, and fourth FET transistors is made in pair-wise phase complementary manner such that the first and second FETs Q1 and Q2 are driven about 180 degrees out of phase relative to the third and fourth FETs Q3 and Q4. In this manner, the first and second FETs (Q1-Q2) are driven to ON and OFF conduction states opposite to the conduction states of the third and fourth FETs (Q3-Q4). The conduction
state (ON or OFF) of each FET pair determines the phase angle of transmission, and operation of the FET switches results in commutation of the RF signal to the IF port, for example, during frequency down-conversion.

FIGS. 5 and 6 illustrate the switching action of transistors Q1, Q2, Q3, and Q4 in response to a LO signal input. LO balun 51, 54 will present a 50 Ω impedance to the LO because resistors R2 56 (100 ohms) and R3 57 (100 ohms) are seen in parallel and represent the principal components of the LO input impedance. LO balun 51, 54 is wound such that the LO signal is 180 degrees out of phase between the gates of Q1 and Q2 and the gates of Q3 and Q4. FET transistors Q1, Q2, Q3, and Q4 do not operate in their linear regions for any significant time and will either be fully ON or fully OFF. FIG. 5 illustrates conditions in the mixer when Q1 and Q2 are ON and Q3 and Q4 are OFF. FIG. 6 illustrates the opposite condition when Q1 and Q2 are OFF and Q3 and Q4 are ON. If Q1 and Q2 are ON, then Q3 and Q4 must be OFF, and vice versa.

FETs Q1, Q2, Q3, and Q4 present low impedance of about 2-8 ohms when conducting (ON) and a very high impedance when not conducting (OFF), and either way they do not present an impedance comparable to the impedance of the RF or IF baluns (generally about 50 ohms to about 75 ohms).

From the foregoing description, those having ordinary skill in the art, in light of this description will appreciate that the RF and IF baluns provide at least three benefits. First, the baluns cooperate with other mixer components to provide the primary signal mixing and energy coupling function of the mixer circuit. Secondly, the baluns are an important component of the drain bias circuit. Third, it is desirable that current flow through the baluns in such a way so as to minimize propagation or coupling of any of the LO signal energy that has been amplified in the FETs into the RF or IF ports. Mixer circuit 10 maintains LO-to-RF and LO-to-IF isolation by directing current flow through the baluns in a balanced fashion. The inherent symmetry of mixer 10 results in partial cancellation of nonlinearity distortion imposed on the RF signal. Furthermore, the LO signal excites the RF and IF baluns in a mode that is not capable of propagating to the RF or IF ports. This propagation mode results in about equal LO voltages at the left
hand nodes of T2A1 (node 84), T2A2 (node 85), T2B1 (node 86), T2B2 (node 87), T3A1 (node 88), T3A2 (node 89), T3B1 (node 90), and T3B2 (node 91).

Mixer operation is now described for four cases (Cases I, II, III, and IV) of FET-pair conduction. In Case I, described in reference to FIG. 5, Q1/Q2 are ON, Q3/Q4 OFF, and the RF signal (not shown) is applied to the RF port 71, 72 and the IF port 78, 79 has a load (not shown) connected to it (e.g. the IF port is terminated). Under these conditions, RF-port current flows into T2A1 and emerges at the drain of Q1. Passing through Q1/Q2, it flows through T3B1 in the direction shown in FIG. 5 and emerges out of the IF-port terminal 78. RF-port current also flows from RF lead 71 into T2B1 and then through T3A1 in the direction shown and emerges out of the IF-port terminal 78 into the IF load.

IF port current passes through the IF termination (load) and returns through IF-port ground terminal 79. IF-port ground current flows into T3A2, into the Q1 drain, through Q1/Q2 and through T2B2 in the direction shown in FIG. 5. It then flows out of RF-port ground terminal 72 where it returns to the RF source generator (not shown). IF-port ground current also flows from IF ground terminal 79 into T3B2, through T2A2 in the direction shown and out of RF-port ground terminal 72, where it returns to the RF source generator.

The resulting currents have the following properties: (1) the currents flow through Q1/Q2, which are ON; (2) the currents do not flow through Q3/Q4, which are OFF; and (3) the currents form complementary current pairs in each of T2A, T2B, T3A, T3B, consistent with energy flow through each and every aforementioned transformer.

In Case II, described with reference to FIG. 6, Q1/Q2 are OFF, Q3/Q4 ON, the RF signal is applied to the RF port 71, 72 and the IF port 78, 79 has a load connected to it (e.g. the IF port is terminated). Under these conditions, RF-port current flows from pin terminal 71 into T2A1 and then through T3A2 in the direction shown and out the IF-port ground 79, where it returns to the RF source generator (not shown). RF-port current also flows from pin terminal 71 into T2B1 and emerges at the drain of Q4.
Passing through Q4/Q3, it flows out the Q3 drain and through T3B2 in the direction shown in FIG. 5 and emerges out of the IF-port ground.

IF-port current also flows from pin terminal 78 into T3A1 and emerges at the drain of Q4. Passing through Q4/Q3, it flows through T2A2 in the direction shown in FIG. 6 and emerges out of the RF-port ground terminal 72 (out the Q3 drain and IF-port current also flows from pin terminal 78 into T3B1 and then through T2B2 in the direction shown and emerges out of the RF-port ground terminal 72, where it returns to the RF source generator.

The resulting currents for Case # have the following properties: (1) the currents flow through Q3/Q4, which are ON; (2) the currents do not flow through Q1/Q2, which are OFF; and (3) the currents form complementary current pairs in each of T2A, T2B, T3A, T3B, consistent with energy flow through each and every one of these transformers.

In Case III, described with reference to FIG. 7, Q1/Q2 are ON, Q3/Q4 OFF, and the IF signal is applied to the IF port and the RF port has a load connected to it (e.g. the RF port is terminated). Under these conditions, IF-port current flows from pin terminal 78 into T3B1 and emerges at the drain of Q2. Passing through Q2/Q1, it flows through T2A1 in the direction shown in FIG. 7 and emerges out of the RF-port pin terminal 71. IF-port current also flows into T3A1 and then through T2B1 in the direction shown and emerges out of the RF-port.

RF port current passes through the RF load (not shown) and returns through RF-port ground 72. RF-port ground current flows from good terminal 72 into T2B2, through Q2/Q1 and through T3A2 in the direction shown in FIG. 7. It then flows out of IF-port ground terminal 79 where it returns to the IF source generator (not shown). RF-port ground current also flows from ground level 72 into T2A2, through T3B2 in the direction shown and out of IF-port ground terminal 79, where it returns to the IF source generator.

The resulting currents for Case # III have the following properties: (1) the currents flow through Q1/Q2, which are ON; (2) the currents do not flow through Q3/Q4, which
are OFF; and (3) the currents form complementary current pairs in each of T2A, T2B, T3A, T3B, consistent with energy flow through each and every aforementioned transformer.

In Case IV, described with reference to FIG. 8, Q1/Q2 are OFF, Q3/Q4 ON, and the IF signal is applied to the IF port and the RF port has a load connected to it (e.g. the RF port is terminated). Under these conditions, IF-port current flows from pin terminal 78 into T3B1 and then through T2B2 in the direction shown in FIG. 8, and then out the RF-port ground terminal 72, where it returns to the RF source generator. IF-port current also flows from pin terminal 78 into T3A1 and emerges at the drain of Q4. Passing through Q4/Q3, it flows through T2A2 in the direction shown in FIG. 8 and emerges out of the RF-port ground terminal 72. RF port current then passes through the RF termination (load) and returns through RF-port per terminal 71.

RF-port current also flows into T2B1 and emerges at the drain of Q4. Passing through Q4/Q3, it flows through T3B2 in the direction shown in FIG. 8 and emerges out of the IF-port ground 79. RF-port current also flows into T2A1 and then through T3A2 in the direction shown and emerges out of the IF-port ground terminal, 79 where it returns to the RF source generator.

The resulting currents for Case IV have the following properties: (1) the currents flow through Q3/Q4, which are ON; (2) the currents do not flow through Q1/Q2, which are OFF; and (3) the currents form complementary current pairs in each of T2A, T2B, T3A, T3B, consistent with energy flow through each and every one of these transformers.

From this description, it can now be seen that for Cases I and II, when Q1/Q2 are ON and Q3/Q3 are OFF, current flows into the RF-port pin terminal 71 and out of the IF-port pin terminal 78. When Q1/Q2 are OFF and Q3/Q3 are ON, current still flows into the RF-port pin terminal but it flows into the IF-port pin terminal 78. Hence, the RF signal appears commutated at the IF-port 78, 79 at the LO frequency. This condition is readily recognized as the time domain description of frequency mixing and corresponds to the emergence of LO+RF and LO-RF frequencies from the IF-port.
Furthermore, RF signals do not couple between the RF-port and IF-port, since the commutation is perfectly symmetric.

In an analogous manner, for Cases III and IV, when Q1/Q2 are ON and Q3/Q3 are OFF, current flows into the IF-port pin terminal 78 and out of the RF-port pin terminal 71. When Q1/Q2 are OFF and Q3/Q3 are ON, current again flows into the IF-port pin terminal but it also flows into the RF-port pin terminal 71. Hence, the IF signal appears commutated at the RF-port at the LO frequency. This condition is readily recognized as the time domain description of frequency mixing and corresponds to the emergence of LO+RF and LO-RF frequencies from the RF-port. IF signals do not couple between the RF-port and IF-port, since the commutation is perfectly symmetric.

The manner in which amplified LO signals of the FET drains are isolated from the RF-port and IF-port is now described with reference to FIGS. 9 and 10 which shows current request for alternate LO signal half cycles. As illustrated in FIG. 9 and 10, any current required by RF-port/IF-port during one half cycle of the LO (e.g. Q1/Q2 ON) is the same as that required during alternate LO signal half cycle (e.g. Q3/Q4 ON). Thus, these RF-port and IF-port currents correspond to a symmetrically rectified version of the LO waveform. As such, they do not contain any component at the LO frequency.

Furthermore, since the RF and IF circuits are symmetrical and support frequencies of equal bandwidth, the designations as RF and as IF are somewhat artificial. The input signals are applied at an RF port and output is taken at an IF port. (The labels "RF port" and "IF port" owe their relevance to the mixer application and can alternatively be replaced by the labels "primary port" and "secondary port," respectively.) The higher frequency may be input at either the RF or IF ports and the mixer 10 may be used for either up or down frequency conversion. The input may be applied to either the IF port in which case the output signal is at the RF port, or the input may be applied at the RF port and the output signal extracted at the IF port. Furthermore, the RF and IF frequency bands may be distinct and non-overlapping or alternatively the frequency ranges may overlap broadly.
Those workers having ordinary skill in the art, in light of the description contained herein, will realize that all of the afore-described currents propagate through the baluns and/or FETs simultaneously (depending on the conduction states of the FET pairs) and that is piecewise description is made for the purpose of enhancing understanding of the mixer operation.

Although this invention has been described in terms of the presently preferred embodiments, it is to be understood that the disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those skilled in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.
What is claimed is:

1. A triple balanced mixer comprising:

   a first switching circuit comprising a first and a second FET transistor each having a gate and a drain and a source, the first and second FET transistors having their gates connected to one another and their sources connected together such that the first and second FET transistors are connected in series;

   a second switching circuit comprising a third and a fourth FET transistor each having a gate and a drain and a source, the third and fourth FET transistors having their gates connected to one another and their sources connected together such that the third and fourth FET transistors are connected in series;

   a balanced local oscillator circuit for pumping said first and second switching circuits having a two-terminal input port for connection to an external local oscillator source and first and second two-terminal output ports for connection to said first and second switching devices, said local oscillator circuit further comprising a local oscillator (LO) balun having a two-terminal input port coupled to said external local oscillator, a first two-terminal output port coupled to the gate and the source of said first and second FET transistors, and a second two-terminal output port coupled to the gate and source of said third and fourth FET transistors;

   a first balun termination resistor coupled across a first output port of said local oscillator balun;

   a second balun termination resistor coupled across a second output port of said local oscillator balun;

   a first capacitor connected in series with said first output port of the LO balun and with said gates belonging to the first and second FET transistors;

   a second capacitor connected in series with said second output port of the LO balun and with said gates belonging to the third and fourth FET transistors; and

   an intermediate frequency (IF) balun having a two-terminal input port for coupling to an external intermediate frequency source, and first and second two-terminal output ports;

   a radio frequency (RF) balun having a two-terminal input port for coupling to an external radio frequency source, and first and second two-terminal output ports;
a first terminal of said first RF balun output port coupled to said first FET drain
and to a second terminal of said first IF balun output port;

a second terminal of said first RF balun output port coupled to said third FET
drain and to a second terminal of said second IF balun output port;

a first terminal of said second RF balun output port coupled to said fourth FET
drain and to a first terminal of said first IF balun output port;

a second terminal of said second RF balun output port coupled to said second
FET drain and to a first terminal of said second IF balun output port;

said coupling between said local oscillator balun and said source and drain

5 terminals of said first, second, third, and fourth FET transistors being in pair-wise phase
complementary manner such that said first and second FET transistors are driven about
180 degrees out of phase relative to said third and fourth FET transistors such that said
first and second FET transistors are driven to on and off conduction states opposite to
the conduction states of said third and fourth FET transistors; and

10 dc bias means coupled to each FET transistor source for applying a dc bias voltage
from an eternal bias voltage source to the source terminals of each of said first, second,
third, and fourth FET transistors;

15 whereby the inherent symmetry of the mixer results in partial cancellation of
nonlinearity distortion imposed on the RF signal, and whereby intermodulation distortion
is reduced by the application of the bias voltage to the source terminals of said FET
transistors.

2. The mixer in Claim 1, wherein said bias means comprising a bias voltage
input port for coupling to an external bias voltage source; and a bias scaling resistor and

25 a reverse bias protection diode and a impedance matching resistor serially coupled between
said bias voltage input port and an FET transistor source terminal; and an ac isolation
capacitor coupled between said serially coupled diode and impedance matching resistor;
said RF balun and said IF balun terminals coupled to said FET gate terminals providing
a return path for said bias current introduced at said FET source terminals.

30 3. The mixer in claim 1, wherein said mixer further comprising first and
second dc blocking capacitors connected to said balanced oscillator circuit two-terminal
input port and interposed between said local oscillator circuit and said external local oscillator source for blocking a predetermined range of low frequency signals from said mixer.

4. The mixer of claim 1, wherein said baluns comprises a transmission line baluns.

5. The mixer of claim 4, wherein said transmission line balun comprises bifilar windings on a ferrite core.

6. The mixer of claim 5, wherein said RF transmission line balun has a characteristic impedances of approximately 50 ohms.

7. The mixer of claim 1, further comprising a ceramic substrate.

8. The mixer of claim 1, further comprising an alumina ceramic substrate subjacent first FET, said second FET, said third FET, and said fourth FET.

9. The mixer of claim 7, wherein each said FET transistors comprise a GaAs MESFET MMIC device mounted to the alumina substrate.

10. The mixer of Claim 1, wherein said mixer operates in the frequency range between 10 Mhz and 1000 MHz.

11. A mixer comprising:
    a first switching circuit comprising a first and a second FET transistor each having a gate and a drain and a source, the first and second FET transistors having their gates connected to one another and their sources connected together such that the first and second FET transistors are connected in series;
    a second switching circuit comprising a third and a fourth FET transistor each having a gate and a drain and a source, the third and fourth FET transistors having their
gates connected to one another and their sources connected together such that the third and fourth FET transistors are connected in series;

a balanced local oscillator input port for receiving an external local oscillator signal and for coupling said local oscillator signal to said first and second switching devices,

a local oscillator balun having a two-terminal input port coupled to said external local oscillator and a first two-terminal output port coupled to the gate and the source of said first and second FET transistors, and a second two-terminal output port coupled to the gate and source of said third and fourth FET transistors; and

an intermediate frequency (IF) balun having a two-terminal input port for coupling to an external intermediate frequency source, and first and second two-terminal output ports;

a radio frequency (RF) balun having a two-terminal input port for coupling to an external radio frequency source, and first and second two-terminal output ports;

a first terminal of said first RF balun output port coupled to said first FET drain and to a second terminal of said first IF balun output port, a second terminal of said first RF balun output port coupled to said third FET drain and to a second terminal of said second IF balun output port, a first terminal of said second RF balun output port coupled to said fourth FET drain and to a first terminal of said first IF balun output port, a second terminal of said second RF balun output port coupled to said second FET drain and to a first terminal of said second IF balun output port;

said coupling between said local oscillator balun and said source and drain terminals of said first, second, third, and fourth FET transistors being in pair-wise phase complementary manner such that said first and second FET transistors are driven about 180 degrees out of phase relative to said third and fourth FET transistors such that said first and second FET transistors are driven to on and off conduction states opposite to the conduction states of said third and fourth FET transistors.

12. The mixer of Claim 11, further comprising:

a first balun termination resistor coupled across a first output port of said local oscillator balun;

a second balun termination resistor coupled across a second output port of said local oscillator balun;
a first capacitor connected in series with said first output port of the LO balun and with said gates belonging to the first and second FET transistors; and
a second capacitor connected in series with said second output port of the LO balun and with said gates belonging to the third and fourth FET transistors.

13. The mixer in Claim 11, further comprising dc bias means coupled to each FET transistor source for applying a dc bias voltage from an external bias voltage source to the source terminals of each of said first, second, third, and fourth FET transistors.

14. The mixer in Claim 13, wherein said bias means comprising a bias voltage input port for coupling to an external bias voltage source; and a bias scaling resistor and a reverse bias protection diode and a impedance matching resistor serially coupled between said bias voltage input port and an FET transistor source terminal; and an ac isolation capacitor coupled between said serially coupled diode and impedance matching resistor; said RF balun and said IF balun terminals coupled to said FET gate terminals providing a return path for said bias current introduced at said FET source terminals.

15. The mixer in claim 11, wherein said mixer further comprising first and second dc blocking capacitors connected to said balanced oscillator two-terminal input port and interposed between said local oscillator circuit and said external local oscillator source for blocking a predetermined range of low frequency signals from said mixer.

16. The mixer in claim 15, wherein said predetermined range of low frequency signals include d.c. signals.

17. The mixer of claim 11, wherein said baluns comprise transmission line baluns.

18. The mixer of claim 17, wherein said transmission line balun comprises bifilar windings on a ferrite core.
19. The mixer of claim 17, wherein said RF transmission line balun has a characteristic impedances of approximately 50 ohms.

20. The mixer of claim 11, wherein each said FET transistor comprises a GaAs MESFET.
FIG. 3
FIG. 6B

FROM FIG. 6A

OFF

FROM FIG. 6A

Q1

Q2

FROM FIG. 6A

T2A

T2A1

T2A2

T2B

T2B1

T2B2

FROM FIG. 6A

FROM FIG. 6A

FROM FIG. 6A

Q3

ON

Q4

T3A

T3A1

T3A2

T3B

T3B1

T3B2

FROM FIG. 6A

RF Source (Sink)

RF

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

IF Sink (Source)

IF

31
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC 6 \ H03D9/06

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 \ H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>US 5 280 648 A (DOBROVOLNY PIERRE) 18 January 1994 see column 3, line 48 - column 5, line 7; figures 1,4,5 ---</td>
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<td>A</td>
<td>IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, vol. 38, no. 9, 1 September 1990, pages 1218-1226, XP000142217 TOKUMITSU T ET AL: &quot;DIVIDER AND COMBINER LINE-UNIFIED FET'S AS BASIC CIRCUIT FUNCTION MODULES- PART II&quot; see page 1221, column 1, line 12 - page 1221, column 1; figure 11 ---</td>
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**X** Further documents are listed in the continuation of box C.

**X** Patent family members are listed in annex.

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*"E" document member of the same patent family

Date of the actual completion of the international search

27 March 1997

Date of mailing of the international search report

22.04.97

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Dhondt, I

Form PCT/ISA/210 (second sheet) (July 1992)
<table>
<thead>
<tr>
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<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
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