(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 166 785 B1**

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **04.03.92**

(51) Int. Cl.[5]: **G11B 20/10, G11B 27/10**

(21) Application number: **85900188.5**

(22) Date of filing: **14.12.84**

(86) International application number:
PCT/JP84/00594

(87) International publication number:
WO 85/02707 (20.06.85 85/14)

(54) DISK REPRODUCING APPARATUS.

(30) Priority: **16.12.83 JP 237370/83**
23.12.83 JP 243486/83

(43) Date of publication of application:
08.01.86 Bulletin 86/02

(45) Publication of the grant of the patent:
04.03.92 Bulletin 92/10

(84) Designated Contracting States:
AT CH DE FR GB LI NL SE

(56) References cited:
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EP-A- 0 138 246
JP-A- 578 864
JP-A- 5 750 374
JP-A-52 965 17
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PATENT ABSTRACTS OF JAPAN, vol. 7, no. 212 (P-224)[1357], 20th September 1983; & JP-A-58 105 472 (SONY K.K.) 23-06-1983

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EP 0 166 785 B1

Description

This invention relates to an apparatus for playback discs on which digital data is recorded.

BACKGROUND ART

The system employing an optically encoded digital audio disc (reffered to hereafter as a compact disc) are capable of reproducing stereo music of high quality. In such a disc system, if digital data such as data representing characters, display data, or computer program data other than music can be reproduced in addition to at least one channel of music without significant change in the structure of a player, then a playback apparatus for visual information such as chart or statistics by graphics, or picture books of still images and/or video games apparatus could be achieved merely by adding a display device for example. In this way, the applications of the compact disc system could be extended. The storage capacity of current compact discs is approximately 500 M bytes which is an advantage to be larger than that of conventional flexible discs.

On the other hand, in conventional compact discs, the data is retrieved in relatively large units such as an entire music composition or a passage thereof, since reproduction of audio signals are concerned. It is necessary, however, to read out data in a precise units ranging from 128 bytes to 10 K bytes as a a general data storage device.

In the case of music signals, searching accuracy can afford to be relatively low without noticeably affecting the reproduced sound. Therefore, in the conventional reproducing apparatus, audio data of the main channel separated from the reproduced signal from the compact disc are once written into a buffer memory so as to be subjected to error correction and eliminated jitter in time base. However, since a highly searching accuracy is not required in a subcoding signal as mentioned above, time base jitter is not eliminated in order to reduce manufacturing costs. Accordingly, there is a problem that if the apparatus for playback the compact disc is to be used as a data memory, a read address cannot be specified accurately solely by means of the subcoding signal.

EP-A-0138246, which forms part of the state of the art by virtue of Article 54(3) EPC, discloses an apparatus for playback a disc on which main digital data and subsidiary digital data for selectively reproducing the main digital data area recorded in multiplex fashion, the apparatus comprising: a disc playback device for reproducing said main digital data and subsidiary digital data from the disc so as to generate a reproduced main digital data and subsidiary digital data; an input circuit connected to said disc playback device and for receiving said reproduced main digital data and subsidiary digital data; a decoding circuit including a write clock generating circuit connected to said input circuit for generating a write clock synchronised with said reproduced main digital data, a read clock generating circuit for generating a read clock having a predetermined period, and a memory circuit connected to said input circuit for having said reproduced main digital data written therein and read therefrom in response, respectively, to write address data and read address data corresponding to said write clock and said read clock so that said reproduced main digital data is de-interleaved to be decoded; and a control circuit connected to said disc playback device and for searching a position to be reproduced of said reproduced main digital data on the basis of said reproduced subsidiary digital data. A subsidiary digital data separating circuit is connected to the input circuit for separating out the subsidiary data and writing it to a buffer memory separate from the main memory device in which the main digital data is stored.

An object of this invention is to provide a disc playback apparatus which employs for example conventional digital disc system for audio use and is capable of reading out digital signals, such as computer programs, data and so on instead of digital audio data signals.

Another object of the invention is to provide a disc playback apparatus which can be constructed in low cost by employed a buffer memory used in de-interleaving of the digital data of the main channel.

Still another object of this invention is to provide a disc playback apparatus which is rendered capable of addressing the digital signals of the main channel simply by adding an external circuit without changing reproducing processing circuitry of the convention compact disc.

According to a first aspect of the invention, there is provided an apparatus for reproducing data from a disc on which main digital data and subsidiary digital data for selectively reproducing the main digital data are recorded in multiplex fashion, the apparatus comprising:

a disc playback device for reproducing said main digital data and subsidiary digital data from the disc so as to generate a reproduced main digital data and subsidiary digital data;

an input circuit connected to said disc playback device and for receiving said reproduced main digital data and subsidiary digital data;

a decoding circuit including a write clock generating circuit connected to said input circuit for generating a write clock synchronised with said reproduced main digital data, a read clock generating circuit for generating a read clock having a

predetermined period, and a memory circuit connected to said input circuit for having said reproduced main digital data written therein and read therefrom in response, respectively, to write address data and read address data corresponding to said write clock and said read clock so that said reproduced main digital data is de-interleaved to be decoded; and

a control circuit connected to said disc playback device and for searching a position to be reproduced of said reproduced main digital data on the basis of said reproduced subsidiary digital data; wherein

said memory circuit also has said reproduced subsidiary digital data written therein without said reproduced subsidiary date having been separated from said main digital data in response to said write address data and read address data corresponding to said write clock and said read clock, respectively; and

a decoding circuit is provided connected to said memory circuit for receiving said reproduced subsidiary digital data from said memory circuit and for separating said reproduced subsidiary digital data from said reproduced main digital data.

According to a second aspect of the invention, there is provided an apparatus for reproducing data from a disc on which main digital data and subsidiary digital data for selectively reproducing the main digital data are recorded in multiplex fashion, the apparatus comprising: a disc playback device for reproducing said main digital data and subsidiary digital data from the disc so as to generate a reproduced main digital data and subsidiary digital data; an input circuit connected to said disc playback device and for receiving said reproduced main digital data and subsidiary digital data; a decoding circuit for decoding said reproduced main digital data including a first write clock generating circuit connected to said input circuit for generating a first write clock synchronised with said reproduced main digital data, a first read clock generating circuit for generating a first read clock having a predetermined period, a main memory device for having said reproduced main digital data written therein and read therefrom in response, respectively, to a write address data and read address data corresponding to said first write clock and said first read clock, so that said reproduced main digital data is de-interleaved; a control circuit connected to said disc playback device and for searching a position to be reproduced of said reproduced main digital data on the basis of said reproduced subsidiary digital data; and a subsidiary digital data separating circuit connected to said input circuit for separating said reproduced subsidiary digital data from said reproduced main digital data; a buffer memory circuit for storing said subsidiary digital data from said subsidiary digital data separating circuit; a write address generating circuit arranged to receive a second write clock signal synchronised with said reproduced subsidiary digital data and to generate a second write address signal; a read address generating circuit arranged to receive a second read clock signal and generating a second read address signal; an address monitor adapted to receive the read and write addresses and to monitor the difference therebetween to detect the possibility of under- or over-flow of the buffer memory circuit; and said buffer memory circuit is a FIFO buffer memory device connected to said subsidiary digital data separating circuit, said write address generating circuit and read address generating circuit, respectively, so as to be provided with said second write address signal and said second read address signal independently and so as to write and read out said reproduced subsidiary digital data in response to said second write address signal and said second read address signal, respectively.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings, in which:-

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 are schematic diagrams for use with an explanation of an arrangement of data recorded in a compact disc applied with this invention.

Fig. 3 is a schematic diagram showing one block of digital data when digital data according to one embodiment of this invention is recorded.

Fig. 4 is a block diagram showing a structure of a recording circuit for generating signals to be recorded on a disc.

Fig. 5 is a block diagram showing a reproducing circuit to which the reproduced signals from a disc is supplied.

Figs. 6 and 7A to 7E are a schematic diagram and time charts for use with an explanation of time base jitter cancellation and de-inteleaving in a reproducing circuit.

Fig. 8 is a block diagram showing a buffer circuit according to another embodiment.

Fig. 9 is a block diagram showing the entire structure of another embodiment of this invention.

Fig. 10 is a schematic diagram showing a word format for serial data according to one embodiment of this invention.

BEST MODE FOR CARRYING OUT THE INVENTION

An embodiment of the invention is applied to the compact disc. Referring to Figs. 1 and 2, data

construction of signals stored in the compact disc will be described.

Fig. 1 illustrates a data stream as stored in the compact disc. One frame consists of 588 bits of data to be recorded and includes a frame synchronizing pulse FS of a particular bit pattarn which is followed by the first direct-current component constraint bits group RB consisting of 3 bits. Followingly, 0th to 32nd groups of data bits DB each consisting of 14 bits and groups of direct-current component constraint bits RB each consisting of 3 bits are provided alternately. The 0th data bits DB constitute a subcoding signal or user's bits which serves for controlling disc playback or indicating related informations. The 1st to 12th and 17th to 28th groups of data bits DB are allocated to audio data in a main channel, and the rest, 13th to 16th and 29th to 32nd groups of data bits DB are allocated to parity data for error correction of the main channel. Each group of data bits DB is 14 bits data which has been interleaved and then converted from 8 bits data by an 8-14 modulation technique (EFM) during recording.

The EFM modulation is a method for block-converting 8 bits data into preferable patterns each of 14 bits (namely, to extend the minimum transition interval of the modurated signal and to suppress the low frequency component thereof). A demodulator 22 as mentioned later is constructed to demodulate the EFM.

Fig. 2 shows one reproduced block consisting of parallel arranged successive 98 frames in which direct current component constraint bits RB are excluded, each group of data bits DB is demodulated by 14 to 8 bit demodulation so as to be 8 bits and the parity data is also excluded. The subcoding signals consists of P to W each of 1 bit totalling 8 bits data every one frame. In the first two frames, the subcoding signals P to W constitute synchronizing patterns having paticular bit patterns. With respect to the Q-channel, one block is comprised of 98 frames, that is, 98 bits, the last 16 of the 98 frames constitute an error detection CRC code.

The P-channel is a flag of 1 bit indicating whether the frame is a pause or music, and a high level indicates a pause, a low level indicates music and a 2 Hz pulse indicates a lead-out section, so that detecting and counting the P-channel bits makes the selection of a designated musical piece possible. The Q-channel performs similar but more complicated control. Specifically, the Q-channel information can be supplied to a microprocessor built into the disc playback apparatus to allow such a random music selection as to move to reproduction of the another piece of music immediately in the middle of reproduction of the currently selected music. The remaining channels R through W, as a whole, constitute regions for data indicating the songwriter, composer, text and explanation of a music recorded on the disc with display or voice.

Concerning the Q-channel, the first 2 bits serve as part of the synchronizing signal pattern, the next 4 bits serve as control bits, the following 4 bits serve as address bits, and the subsequent 72 bits serve as data bits, and the final 16 bits serve as a CRC code for error detection.

The 72 data bits include a a track number code TNR and a index code X. The track number code TNR varies from 00 to 99. The index code X varies also from 00 to 99. The data bits of the Q-channel also include a time indication code indicating the duration of the musical selection and pauses and another time indication code indicating the absolute time duration continuously varying from the first of the program area to the outer peripheral end of the compact disc. These time indication codes constitute codes representing each two-digit minutes, seconds, and frames. One second is divided into 75 frames. The another time indication code with respect to the absolute time is used for access digital data in units shorter than an entire musical selection from the compact disc.

In this embodiment, when digital data is recorded as data in a main channel, the data structures of P-channel and Q-channel in the subcoding signal are the same as that of the conventional compact disc.

The detailed data structures of the above-described subcoding signals are disclosed in Japanese Laid-open Patent Publication No. Sho. 58-48279 and EPC Laid-open Patent Application No. 74841.

The Fig. 3 illustrates the recording format of the digital data recorded in the main channel. Each digital data comprises 2352 bytes (=588 X 4 bytes) as an unit which is one block. In Fig. 3, the left channel and right channel as described indicate correspondence to the sampling data of the left and right channels of stereo musical data. In case of stereo musical data, as above described, since 24 (= 6 X 2 X 2) bytes of data is recorded within the period defined by consecutive frame synchronizing signals, if other digital data is recorded in the same format (referring to Fig. 1) as for stereo musical data, the data of one block (2352 bytes) is recorded so as to coincides with the amount of data in frames of from 0th to 97th. Accordingly, the digital data can be recorded without disrupting the 98-frame cycle of the variation of the subcoding signals.

The first byte of the digital data of one block is all zeros and the next ten bytes are all ones, followed finally by another byte of zeros. These 12 bytes constitute a header indicating the beginning of one block of the digital data. The header is

followed by one byte of minutes data, seconds data, sector data and mode data each of one byte.The minute, second and sector byte specify one block address, with the 75 sectors counting one second similar to 75 frames. The mode data indicates the kinds of digital data in the block. The remaining 2340 bytes comprises digital data such as still picture data other than the header, address (minutes, seconds, sector) and mode.

Fig. 4 shows the circuitry of a recording circuit for forming the digital data to be recorded on the compact disc. In Fig. 4, reference numerals 1 and 2 designate input terminals supplied with digital data of 16 bits, respectively. The digital data is converted into an one channel data form by means of a multiplexer 3 and is supplied to an error correction encoder 4. The error correction encoder 4 encodes audio PCM signals by a cross-interleaving process using a Reed-Solomon code to facilitate later error correction. The cross-interleaving process is to rearrange the order of the data so that each symbol is included in two different error correction code systems. The output of the error correction encoder 4 is supplied to a mutiplexer 5.

An encoder 6 for P-channel and Q-channel of the subcoding signals and an encoder 7 for R-through W-channels of the subcoding signals are provided and the output of which are multiplexed by a multiplexer 8 and supplied to the multiplexer 5. the output of the multiplexer 5 is supplied to a modulator 9 and modulated by (8-14) conversion. At this time, a frame sync from a synchronizing signal generator 10 is mixed and supplied to an output terminal 11. The encoder 6 for the Q-channel is designed so as to add a CRC code of 16 bits to the Q-channel subcoding signal. The encoder for R- through W-channels is designed so as to encode an error correction code which employs a Reed-Solomon code and interleaving different from that of the main channel.

The circuits such as the multiplexers 3, 5, 8 are supplied with clock pulses and timing signals generated by a timing generator 12. A reference numeral 13 designates an oscillator for generating a master clock.

Fig. 5 shows a reproducing circuit structure for processing a reproduced signal from the compact disc. An input terminal designated by a reference numeral 20 is supplied with the signal optically reproduced from the disc.

The reproduced signal is supplied to a demodulator 22, clock reproducing circuit 23, and a synchronization detecting circuit 24 through a waveform shaping circuit 21. A bit clock is extracted from the clock reproducing circuit 23 with a PLL structure in synchronism with the reproduced data. The synchronization detecting circuit 24 detects the frame synchronizing signal so as to generate a frame clock in synchronism with the sampling data. The bit clock and frame clock are supplied to each circuit of the reproducing system.

The demodulation of 8-14 modulation by modulator 9, that is 14-8 demodulation is carried out in the demodulator 22, and each output data of 8 bits is subjected to de-interleaving processing corresponding to the interleaving processing carried out by the error correction encoder 4, to error detection, error correction and interpolation processing in the error correcting circuit 25. The error correcting circuit 25 includes a RAM, a RAM controller and an error correction circuit. The RAM has written into it the subcoding signals as well as digital data in the main channel. The write process of the RAM is performed in response to the bit clock and frame clock from the clock reproducing circuit 23 and synchronization detecting circuit 24. Similarly, the digital data of the main channel and subcoding signal are read from the RAM in response to a read clock from a timing generator 31. The read clock is generated from a crystal oscillator 32.

Therefore, the digital data of the main channel and the subcoding signal from which time-base jitter are cancelled, respectively, derive from the error correction circuit 25. The digital data of the main channel from the error correcting circuit 25 is supplied to the demultiplexer 26 so as to be divided into two channels and to derive outputs at corresponding output terminals 27 and 28 respectively. In the case where the main channel signal is general digital data, the data is outputted serially from another output terminal 29. The subcoding signal is supplied to a decoder 30 so as to be subjected to the error detection and error correction processing.

A system controller 35 is supplied with P-channel and Q-channel data of the subcoding signal from the decoder 30. With respect to the system controller 35, a operation device 36 such as a keyboard is attached to and a line display 37 is supplied with a time code for indicating the absolute time encoded in the Q-channel of the subcoding signal so as to display. A key-in operation from the operation device 36 permits digital data of a desired address represented by the time code to be reproduced from the disc. Alternatively, a command from an external computer to which the digital data of the desired address is supplied may be sent to the system controller 35 via an I/O interface. Moreover, the desired P-channel and Q-channel data appear at another output terminal 33, and the R- through W-channel data appear at another output terminal 34. The R- through W-channel data may be still picture data, audio data concerning explanation of the music selection and so on.

Write and read operations of the RAM in the

error correcting circuit 25 of the reproducing system mentioned above will be now described with reference to Fig. 6 and Figs. 7A to 7E. In order to simplify the description, one frame will be assumed to consist of a total of five symbols, four symbols in the main channel and one symbol for the subcoding signals.

Fig. 6 shows the contents of RAM in three successive frames at timings t1, t2 and t3. The numerals in Fig. 6 represent address information. At frame timing t1, reproduced data of one frame is written into the addresses (5, 10, 14, 17, 19) of the RAM. One symbol of the subcoding signal is written into the address 19. At the frame timing t1, the digital data of the main channel written into the addresses (4, 9, 13, 16) at the preceding frame timing are subjected to an error correction as a series of the error correction code C1. At this time, the digital data in the addresses (1, 7, 12, 16) are subjected to an error correction in a series of the error correction code C2. Furthermore, in the frame timing t1, the digital data of 4 symbols W1, W2, W3, W4 in the addresses (0, 6, 11, 15) subjected to an error correction and one subcoding signal of symblol S1 in the address 18 are read out from the RAM.

At the subsequent frame timing t2, the digital data of 4 symbols W5, W6, W7, W8 subjected to an error correction and to the de-interleaving and one subcoding signal of symbol S2 in the in the addresses (1, 7, 12, 16, 19) are read out from the RAM. The digital data in the addresses (5, 10, 14, 17) written at the frame timing t1 are now subjected to an error correction as a series of the error correction code C1 as well as the digital data in the addresses (2, 8, 13, 17) are subjected to an error correction as a series of the error correction code C2. Furthermore, reproduced data of one frame are written into the addresses (6, 11, 15, 18, 20).

Furthermore, at the subsequent frame timing t3, the digital data of 4 symbols W9, W10, W11, W12 subjected to an error correction and to the de-interleaving and one subcoding signal of symblol S3 are written into the addresses (2, 8, 13, 17, 20) as well as reproduced data of one frame are written into the addresses (7, 12, 16, 19, 21).

The write operation of the RAM is performed in response to the clock signal in synchronism with the reproduced data and the read operation of the RAM is performed in response to the clock signal generated from the output of the crystal oscillator, so that the digital data and subcoding signals read out from the RAM are subjected to the same compensation of time base jitter. As shown in Fig. 7A, the read out timing of the digital data from the RAM is carried out at a constant period of l/fs (fs = 44.1 kHz). Simultaneously, as shown in Fig. 7B, the subcoding signal of the symbol S1 is read out at a point of timing offset from the read out timing of the digital data. At this time, the digital data W21, W18, W15 and W12 are written into the addresses (5, 10, 14, 17) of the RAM as shown in Fig. 7C and the subcoding signal of the symbol S2 is written into the address 19 as shown in Fig. 7D. It should be noted that the write timing and the read timing are not overlapped each other. As shown in Fig. 7E, error corrections of series C1 and C2 are executed in the frame t1 except when the RAM is accessed as shown in Figs. 7A to 7D.

In the above described embodiment, the memory area, in which the subcoding signal is stored, as part of the RAM provided in the error correction circuit 25 can be constructed as a separate buffer circuit 40 employing an FIFO buffer memory.

In Fig. 8, the reference numeral 41 designates an FIFO (First-In-First-Out) buffer register 41, to which the reproduced subcoding signals from an input terminal 42, a write address from a write address generator 43 and a read address from a read address generator 44 are supplied, respectively. The FIFO buffer register 41 is such a memory as to sequentially store the input data and derive the output data in the order in which it was inputted and as to be capable of supplying independently with the write address and the read address.

The write address generator 43 is supplied from an input terminal 45 with a write frame clock in synchronism with the reproduced subcoding signals. The read address generator 44 is supplied with a read frame clock formed by frquency division of the output of the crystal oscillator. As described before, the FIFO buffer register 41 outputs the subcoding signal from which the time base jitter is eliminated in the same manner as the digital data of the main channel. The reference numeral 47 designates an address monitor which is supplied with the write address and read address and for monitoring a difference between the write address and read address. The address monitor 47 serves to detect the probability of underflow or overflow of the FIFO buffer register 41, as the time base jitter component included in the reproduced signal exceeds the established range. The address monitor 47 controls the operation of the write and read address generators 43 and 44 so that, for example, change in the write address is temporarily inhibited.

Fig. 9 shows another embodiment of this invention employing the buffer memory constructed as described above, which is the more detailed reproducing circuit of Fig. 5. The reference numerals to those in Fig. 9 designate corresponding elements shown in Fig. 5.

In Fig. 9, the reference numeral 51 designates a compact disc on which digital signals of format

described above are recorded in spiral. The compact disc 51 is rotated by means of a spindle motor 52. A spindle motor 52 is controlled by a spindle servo circuit 53 so as to rotate the compact disc 51 at a constant linear velocity.

The reference numeral 54 designates an optical head which includes a laser source for generating laser beam for reading, a beam splitter, an optical system such as an objective lens, and a light-receiving element for receiving laser beam reflected by the compact disc 51. The optical head 54 is so constructed as to move radially across the compact disc 51 by means of a threading feed motor 55. The threading feed motor 55 is driven by a thread driving circuit 56. The optical head 54 is displaceable in two directions, that is the directions orthogonal to and parallel to the surface on which signal are recorded of the compact disc 51 so as to be controlled to continuously obtain the best focussing and tracking of the laser beam during reproduction. For this purpose, a focussing servo circuit 57 and a tracking servo circuit 58 are provided, respectively.

The reproduced signal from the optical head 54 is supplied to an RF amplifier 59. The optical head 54 is provided with a focussing error detecting part comprising a combination of a cylindrical lens and a square-array optical detectors for instance and a tracking error detecting part using three laser spots. The output signal of the RF amplifier 59 is supplied to a clock extracting circuit 23. The output (data and clock) of the clock extracting circuit 23 is supplied to the frame synchronization detecting circuit 24. The bit clock extracted by the clock extracting circuit 23 and the frame synchronizing signal detected by the frame synchronization detecting circuit 24 are supplied to the demodulator 22 and spindle servo circuit 53.

The subcoding signal is separated in the demodulator 22 and supplied to a system controller 60 through the above described buffer circuit 40 shown in Fig. 8. The system controller 60 is provided with a CPU and so constructed as to control such operation as the rotation of the compact disc 51, threading feed and reading by the optical head 54. The system controller 60 is supplied with control commands through a interface 65 as to be described later. Namely, the system controller 60 carries out control processes using the subcoding signals to read out the desired digital signals from the compact disc 51.

The main digital data outputted from the demodulator 22 is supplied to the RAM 62 and the error correcting circuit 63 through the RAM controller 61. Time base jitter cancellation, error correction, error concealment are performed by the RAM controller 61, RAM 62, and error correcting circuit 63, from which the main digital data is derived. When an compact disc on which an audio data is recorded is reproduced, a D/A converter may be connected to the RAM controller 61. Since digital data is taken out as it is in this system, a D/A converter is not provided and the reproduced data is supplied to the data conversion circuit 64. The data conversion circuit 64 is also supplied with the reproduced subcoding signals from the buffer circuit 40 so that the reproduced data is converted into a serial signal format.

The serial signal is supplied to the interface 65 and the data for the system controller 60 is supplied from the microcomputer system 66 through the interface 65. The microcomputer system 66 specifies an read address and supplys the interface 65 and the system controller 60 with drive controlling signals such as a start signal other than the read address.

Fig. 10 shows an example of the serial signal word format outputted from the data conversion circuit 64. The serial signal is comprised of 32 bits as one word, the first 4 bits serve as a preamble, the next 4 bits as auxiliary bits for audio data, and the following 20 bits as digital audio sampling data.

When an audio digital sample has 16 bits, the sample data of 16 bits is inserted from the least significant bit (LSB), and 4 bits are added subsequent to the audio digital sample. Among these 4 bit, the bit labelled "V" is a flag indicating whether the audio digital sample in that word are effective, the bit labelled "U" is each bit composing the subcoding signal, the bit labelled "C" is a bit for identifying a channel, and the bit labelled "P" is a parity bit. The bits labelled "U" for the subcoding signal are inserted in each word by one bit so as to be transmitted sequentially.

In this embodiment, the buffer circuit 40 eliminates the time base jitter from the subcoding signals. The compensation of time base is the same as that by the RAM controller 61 and the RAM 62 for the digital data of the main channel.

In more detail, the RAM controller 61 generates the write clock synchronized with the reproduced signal from the detected frame synchronizing signal. The digital signal is written into the RAM 62 in response to the write clock, and the read clock formed by the output signal from the crystal socillator is used to read out the digital signal from the RAM 62. The write clock and read clock are used to write and read the subcoding signals into and from the buffer circuit 40. Hence, the subcoding signals read from the buffer circuit 40 include no time base jitter so that it is prevented that the time relationship to the digital signal of the main channel is changed because of the time base jitter.

In this embodiment, the microcomputer system 66 executes a read instruction to read a predetermined address. The address is the code of the Q-

channel for indicating absolute time and is supplied to the system controller 60 through the interface 65. The system controller 60 controls the thread moving circuit 56 and moves the optiacal head 54 to a position near a reading position as target by monitoring the subcoding signals reproduced by the optical head 54. In this example, reproduction of the data starts from a position several blocks away from the reading position as the target in order to prevent malfunction such that an established subcoding signal is not reproducd because of errors included in the reproduced subcoding signals, and the access opreartion is not completed. The target block may be retrieved by either of two methods, namely by making the reprduced subcoding signals coincided with the specifiied address or by starting reproduction from a neighboring, correct subcoding signal and then counting the frame synchronizing signal.

According to the present invention, it is possible to achieve a disc storage device with a considerably larger storage capacity compared with a conventional flexible discs, and to read out digital signal as an unit as an amount suitable for processing.

According to the present invention, it is possible to record digital data other than stereo music signal on the conventional disc for recording stereo music signal such as commercially available compact disc, while the identity of signal forms such as error correction method and data recording format and signal processing is maintained.

Furthermore, according to the present invention since a RAM for de-interleaving is employed for compensation of time base of the subcoding signals, it is possible to use almost all of the conventional reproduction processing circuitry for the compact disc and to achieve a low-cost system structure.

Furthermore, according to the present invention, it is possible to adderss the digital signal of the main channel simply by adding an external circuit without changing the conventional reproduction processing circuitry for the compact disc, therefore, there is the advantage of it being unnecessary to newly design a LSI for the reproduction processing circuitry.

Claims

1. An apparatus for reproducing data from a disc on which main digital data and subsidiary digital data for selectively reproducing the main digital data are recorded in multiplex fashion, the apparatus comprising:

a disc playback device for reproducing said main digital data and subsidiary digital data from the disc so as to generate a reproduced main digital data and subsidiary digital data;

an input circuit (21) connected to said disc playback device and for receiving said reproduced main digital data and subsidiary digital data;

a decoding circuit including a write clock generating circuit (23, 24) connected to said input circuit for generating a write clock synchronised with said reproduced main digital data, a read clock generating circuit (31, 32) for generating a read clock having a predetermined period, and a memory circuit (25) connected to said input circuit (21) for having said reproduced main digital data written therein and read therefrom in response, respectively, to write address data and read address data corresponding to said write clock and said read clock so that said reproduced main digital data is de-interleaved to be decoded; and

a control circuit (35) connected to said disc playback device and for searching a position to be reproduced of said reproduced main digital data on the basis of said reproduced subsidiary digital data; wherein

said memory circuit (25) also has said reproduced subsidiary digital data written therein without said reproduced subsidiary date having been separated from said main digital data in response to said write address data and read address data corresponding to said write clock and said read clock, respectively; and

a decoding circuit (30) is provided connected to said memory circuit (25) for receiving said reproduced subsidiary digital data from said memory circuit (25) and for separating said reproduced subsidiary digital data from said reproduced main digital data.

2. An apparatus according to claim 1, and operative to reproduce data of which one block of said main digital data consists of data of a plurality of frames, each block includes a header signal, an address information signal and a data information signal.

3. An apparatus for reproducing data from a disc on which main digital data and subsidiary digital data for selectively reproducing the main digital data are recorded in multiplex fashion, the apparatus comprising:

a disc playback device for reproducing said main digital data and subsidiary digital data from the disc so as to generate a reproduced main digital data and subsidiary digital data;

an input circuit (21) connected to said disc

playback device and for receiving said reproduced main digital data and subsidiary digital data;

a decoding circuit for decoding said reproduced main digital data including a first write clock generating circuit (23, 24) connected to said input circuit for generating a first write clock synchronised with said reproduced main digital data, a first read clock generating circuit (31, 32) for generating a first read clock having a predetermined period, a main memory device (25) for having said reproduced main digital data written therein and read therefrom in response, respectively, to a write address data and read address data corresponding to said first write clock and said first read clock, so that said reproduced main digital data is de-interleaved;

a control circuit (35) connected to said disc playback device and for searching a position to be reproduced of said reproduced main digital data on the basis of said reproduced subsidiary digital data; and

a subsidiary digital data separating circuit (22) connected to said input circuit (21) for separating said reproduced subsidiary digital data from said reproduced main digital data;

a buffer memory circuit (40) for storing said subsidiary digital data from said subsidiary digital data separating circuit;

a write address generating circuit (43) arranged to receive a second write clock signal synchronised with said reproduced subsidiary digital data and to generate a second write address signal;

a read address generating circuit (44) arranged to receive a second read clock signal and generating a second read address signal;

an address monitor (47) adapted to receive the read and write addresses and to monitor the difference therebetween to detect the possibility of under- or over-flow of the buffer memory circuit; and

said buffer memory circuit (40) is a FIFO buffer memory device (41) connected to said subsidiary digital data separating circuit (22), said write address generating circuit (43) and read address generating circuit (44), respectively, so as to be provided with said second write address signal and said second read address signal independently and so as to write and read out said reproduced subsidiary digital data in response to said second write address signal and said second read address signal, respectively.

4. An apparatus according to claim 3, and operative to reproduce data of which one block of said main digital data consists of data of a plurality of frames, each block includes a header signal, an address information signal and a data information signal.

Revendications

1. Appareil de reproduction de données à partir d'un disque sur lequel des données numériques principales et des données numériques subsidiaires pour reproduire de manière sélective les données numériques principales sont enregistrées selon un procédé de multiplexage, l'appareil comprenant :

un dispositif de lecture de disque pour reproduire lesdites données numériques principales et lesdites données numériques subsidiaires à partir du disque de manière à générer des données numériques principales reproduites et des données numériques subsidiaires reproduites ;

un circuit d'entrée (21) connecté audit dispositif de lecture de disque pour recevoir lesdites données numériques principales reproduites et lesdites données numériques subsidiaires reproduites ;

un circuit de décodage incluant un circuit de génération d'horloge d'écriture (23, 24) connecté audit circuit d'entrée pour générer une horloge d'écriture synchronisée avec lesdites données numériques principales reproduites, un circuit de génération d'horloge de lecture (31, 32) pour générer une horloge de lecture ayant une période prédéterminée et un circuit de mémoire (25) connecté audit circuit d'entrée (21) pour avoir lesdites données numériques principales reproduites écrites dedans et lues-à partir de ce circuit de mémoire en réponse respectivement à des données d'adresse d'écriture et à des données d'adresse de lecture qui correspondent à ladite horloge d'écriture et à ladite horloge de lecture de telle sorte que lesdites données numériques principales reproduites soient dé-entrelacées pour être décodées ; et

un circuit de commande (35) connecté audit dispositif de lecture de disque pour rechercher une position qui doit être reproduite desdites données numériques principales reproduites sur la base desdites données numériques subsidiaires reproduites ; dans lequel :

ledit circuit de mémoire (25) a également lesdites données numériques subsidiaires reproduites écrites dedans sans que lesdites données subsidiaires reproduites aient été séparées desdites données numériques principales en réponse auxdites données d'adresse d'écriture et auxdites données d'adresse de

lecture qui correspondent respectivement à ladite horloge d'écriture et à ladite horloge de lecture ; et

un circuit de décodage (30) est prévu et est connecté audit circuit de mémoire (25) pour recevoir lesdites données numériques subsidiaires reproduites en provenance dudit circuit de mémoire (25) et pour séparer lesdites données numériques subsidiaires reproduites desdites données numériques principales reproduites.

2. Appareil selon la revendication 1, fonctionnant pour reproduire des données dont un bloc desdites données numériques principales est constitué par des données d'une pluralité d'images, chaque bloc incluant un signal d'entête, un signal d'information d'adresse et un signal d'information de données.

3. Appareil de reproduction de données à partir d'un disque sur lequel des données numériques principales et des données numériques subsidiaires pour reproduire de manière sélective les données numériques principales sont enregistrées selon un procédé de multiplexage, l'appareil comprenant :

un dispositif de lecture de disque pour reproduire lesdites données numériques principales et lesdites données numériques subsidiaires à partir du disque de manière à générer des données numériques principales reproduites et des données numériques subsidiaires reproduites ;

un circuit d'entrée (21) connecté audit dispositif de lecture de disque pour recevoir lesdites données numériques principales reproduites et lesdites données numériques subsidiaires reproduites ;

un circuit de décodage pour décoder lesdites données numériques principales reproduites, incluant un premier circuit de génération d'horloge d'écriture (23, 24) connecté audit circuit d'entrée pour générer une première horloge d'écriture synchronisée avec lesdites données numériques principales reproduites, un premier circuit de génération d'horloge de lecture (31, 32) pour générer une première horloge de lecture ayant une période prédéterminée et un circuit de mémoire principal (25) pour avoir lesdites données numériques principales reproduites écrites dedans et lues à partir de ce circuit de mémoire en réponse respectivement à des données d'adresse d'écriture et à des données d'adresse de lecture qui correspondent à ladite première horloge d'écriture et à ladite première horloge de lecture de telle sorte que lesdites données numériques principales reproduites soient dé-entrelacées ;

un circuit de commande (35) connecté audit dispositif de lecture de disque pour rechercher une position qui doit être reproduite desdites données numériques principales reproduites sur la base desdites données numériques subsidiaires reproduites ; et

un circuit de séparation de données numériques subsidiaires (22) connecté audit circuit d'entrée (21) pour séparer lesdites données numériques subsidiaires reproduites desdites données numériques principales reproduites ;

un circuit de mémoire tampon (40) pour stocker lesdites données numériques subsidiaires qui proviennent dudit circuit de séparation de données numériques subsidiaires ;

un circuit de génération d'adresse d'écriture (43) agencé pour recevoir un second signal d'horloge d'écriture synchronisé avec lesdites données numériques subsidiaires reproduites et pour générer un second signal d'adresse d'écriture ;

un circuit de génération d'adresse de lecture (44) agencé pour recevoir un second signal d'horloge de lecture et pour générer un second signal d'adresse de lecture ;

un moniteur d'adresse (47) adapté pour recevoir les adresses de lecture et d'écriture et pour surveiller la différence entre afin de détecter la possibilité d'une sous-charge ou d'une sur-charge du circuit de mémoire tampon ; et

ledit circuit de mémoire tampon (40) est un dispositif de mémoire tampon FIFO (premier entré, premier sorti) (41) qui est respectivement connecté audit circuit de séparation de données numériques subsidiaires (22), audit circuit de génération d'adresse d'écriture (43) et audit circuit de génération d'adresse de lecture (44) de manière à se voir appliquer ledit second signal d'adresse d'écriture et ledit second signal d'adresse de lecture indépendamment et de manière respectivement à écrire et à lire lesdites données numériques subsidiaires reproduites en réponse audit second signal d'adresse d'écriture et audit second signal d'adresse de lecture.

4. Appareil selon la revendication 3, fonctionnant pour reproduire des données dont un bloc desdites données numériques principales est constitué par des données d'une pluralité d'images, chaque bloc incluant un signal d'entête, un signal d'information d'adresse et un signal d'information de données.

Patentansprüche

1. Vorrichtung zum Wiedergeben von Daten von einer Platte, auf der digitale Hauptdaten und digitale Hilfsdaten zum selektiven Wiedergeben der digitalen Hauptdaten in gemultiplexter Form aufgezeichnet sind, mit:

einer Plattenwiedergabeeinrichtung zum Wiedergeben der digitalen Hauptdaten und digitalen Hilfsdaten von der Platte, um wiedergegebene digitale Hauptdaten und digitale Hilfsdaten zu erzeugen;

einem Eingangsschaltkreis (21), der mit der Plattenwiedergabeeinrichtung verbunden ist und die wiedergegebenen digitalen Hauptdaten und digitalen Hilfsdaten empfängt;

einem Decodierschaltkreis mit einem Schreibtaktgenerierungsschaltkreis (23,24), der mit dem Eingangsschaltkreis verbunden ist, zum Generieren eines mit den wiedergegebenen digitalen Hauptdaten synchronisierten Schreibtakts, einem Lesetaktgenerierungsschaltkreis (31,32) zum Generieren eines Lesetakts mit einer vorbestimmten Periode und einem Speicherschaltkreis (25), der mit dem Eingangsschaltkreis (21) verbunden ist, in den die wiedergegebenen digitalen Hauptdaten eingeschrieben bzw. aus dem sie ausgelesen werden abhängig von Schreibadreßdaten und Leseadreßdaten entsprechend dem Schreibtakt bzw. dem Lesetakt, so daß die wiedergegebenen digitalen Hauptdaten entschachtelnd decodiert werden; und

einem Steuerschaltkreis (35), der mit der Plattenwiedergabeeinrichtung verbunden ist und eine wiederzugebende Position der wiedergegebenen digitalen Hauptdaten auf der Basis der wiedergegebenen digitalen Hilfsdaten sucht; wobei

in den Speicherschaltkreis (25) auch die wiedergegebenen digitalen Hilfsdaten, ohne die wiedergegebenen Hilfsdaten von den digitalen Hauptdaten getrennt zu haben, eingeschrieben sind, abhängig von den Schreibadreßdaten und Leseadreßdaten entsprechend dem Schreibtakt bzw. dem Lesetakt; und

ein mit dem Speicherschaltkreis (25) verbundener Decodierschaltkreis (30) vorhanden ist, der die wiedergegebenen digitalen Hilfsdaten vom Speicherschaltkreis (25) empfängt und die wiedergegebenen digitalen Hilfsdaten von den wiedergegebenen digitalen Hauptdaten trennt.

2. Vorrichtung nach Anspruch 1, die Daten wiedergibt, wovon ein Block der digitalen Hauptdaten aus Daten mit mehreren Rahmen besteht, wobei jeder Block ein Kopfsignal, ein Adreßinformationssignal und ein Dateninformationssignal umfaßt.

3. Vorrichtung zum Wiedergeben von Daten von einer Platte, auf der digitale Hauptdaten und digitale Hilfsdaten zum selektiven Wiedergeben der digitalen Hauptdaten in gemultiplexter Form aufgezeichnet sind, umfassend:

eine Plattenwiedergabeeinrichtung zum Wiedergeben der digitalen Hauptdaten und digitalen Hilfsdaten von der Platte, um wiedergegebene digitale Hauptdaten und digitale Hilfsdaten zu generieren;

ein Eingangsschaltkreis (21), der mit der Plattenwiedergabeeinrichtung verbunden ist und die wiedergegebenen digitalen Hauptdaten und digitalen Hilfsdaten empfängt;

ein Decodierschaltkreis zum Decodieren der wiedergegebenen digitalen Hauptdaten mit einem mit dem Eingangsschaltkreis verbundenen ersten Schreibtaktgenerierungsschaltkreis (23,24), zum Generieren eines mit den wiedergegebenen digitalen Hauptdaten synchronisierten ersten Schreibtakts, einem ersten Lesetaktgenerierungsschaltkreis (31,32) zum Generieren eines ersten Lesetakts mit einer vorbestimmten Periode, einer Hauptspeichereinrichtung (25), in die die wiedergegebenen digitalen Hauptdaten eingeschrieben bzw. aus der diese ausgelesen werden abhängig von Schreibadreßdaten und Leseadreßdaten entsprechend dem ersten Schreibtakt und dem ersten Lesetakt, so daß die wiedergegebenen digitalen Hauptdaten entschachtelt werden;

ein Steuerschaltkreis (35), der mit der Plattenwiedergabeeinrichtung verbunden ist und eine wiederzugebende Position der wiedergegebenen digitalen Hauptdaten auf der Basis der wiedergegebenen digitalen Hilfsdaten sucht; und

ein digitale Hilfsdaten trennender Schaltkreis (22), der mit dem Eingangsschaltkreis (21) verbunden ist und die wiedergegebenen digitalen Hilfsdaten von den wiedergegebenen digitalen Hauptdaten trennt;

ein Pufferspeicherschaltkreis (40) zum Speichern der digitalen Hilfsdaten von dem digitale Hilfsdaten trennenden Schaltkreis;

ein Schreibadreßgenerierungsschaltkreis (43) zum Empfangen eines mit den wiedergegebenen digitalen Hilfsdaten synchronisierten zweiten Schreibtakts und zum Generieren eines zweiten Schreibadreßsignals;

ein Leseadreßgenerierungsschaltkreis (44) zum Empfangen eines zweiten Lesetaktsignals und zum Generieren eines zweiten Leseadreßsignals;

eine Adreßkontrollanzeige zum Empfangen der Lese- und Schreibadressen und zum Anzeigen der Differenz zwischen den beiden Adressen, um die Möglichkeit eines Unter-

bzw. Überlaufs des Pufferspeicherschaltkreises festzustellen; wobei

der Pufferspeicherschaltkreis (40) eine FIFO-Pufferspeichereinrichtung (41) ist, die mit dem digitale Hilfsdaten trennenden Schaltkreis (22), dem Schreibadreßgenerierungsschaltkreis (43) und dem Leseadreßgenerierungsschaltkreis (44) verbunden ist, um mit dem zweiten Schreibadreßsignal und dem zweiten Leseadreßsignal unabhängig versorgt zu sein und um die digitalen Hilfsdaten entsprechend dem zweiten Schreibadreßsignal bzw. dem zweiten Leseadreßsignal zu schreiben und zu lesen.

4. Vorrichtung nach Anspruch 3, die Daten wiedergibt, wovon ein Block der digitalen Hauptdaten aus Daten mit mehreren Rahmen besteht, wobei jeder Block ein Kopfsignal, ein Adreßinformationssignal und ein Dateninformationssignal umfaßt.

FIG.1

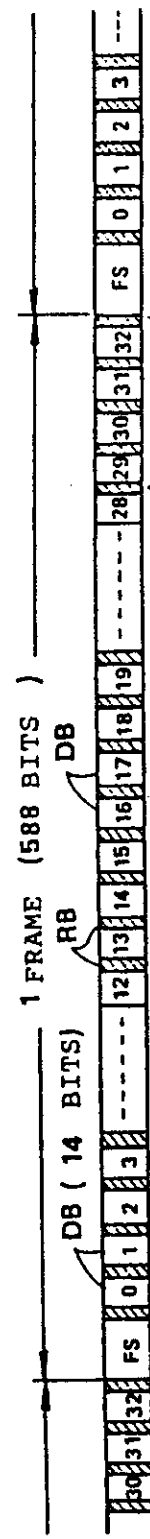

1 FRAME (588 BITS)
DB (14 BITS)
RB
DB
AUDIO DATA
PARITY
AUDIO DATA
PARITY
CONTROL INDICATION
(24 BITS)
RB (3BITS)

FIG.2

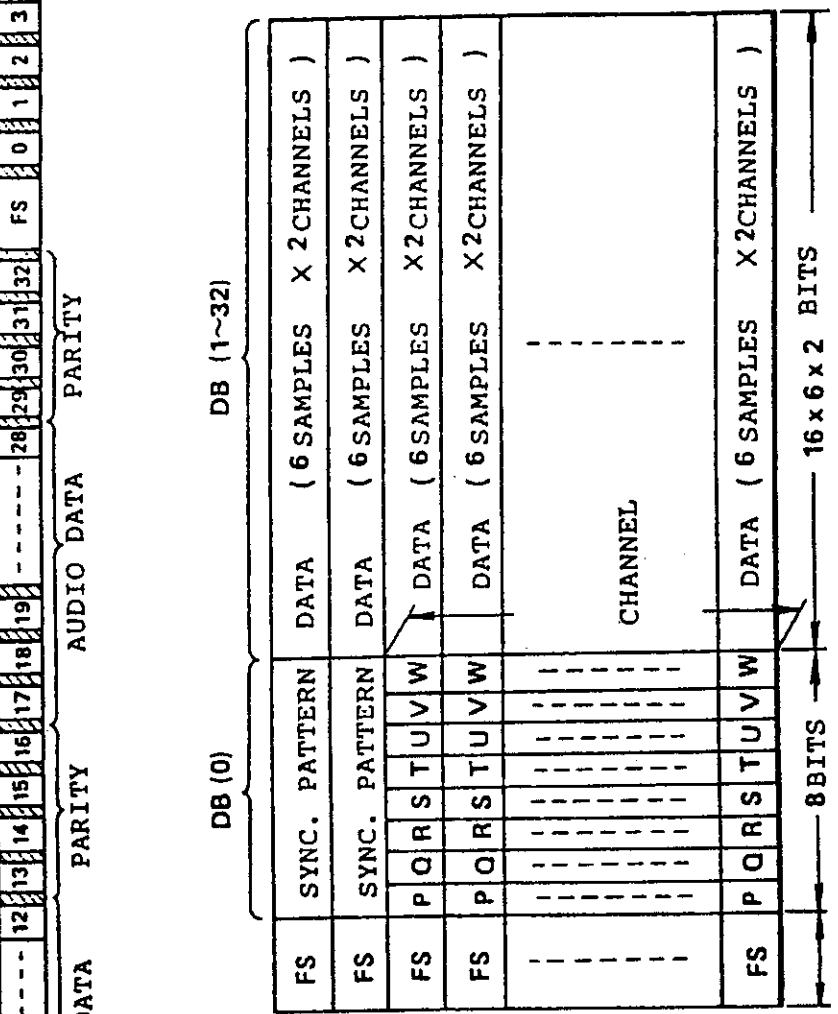

1 BLOCK
DB (0)
DB (1~32)
0 FRAME
1 FRAME
2 FRAME
3 FRAME
97 FRAME
FS
SYNC. PATTERN
DATA (6 SAMPLES X 2 CHANNELS)
P Q R S T U V W
CHANNEL
8BITS
16 x 6 x 2 BITS
24 BITS

FIG.3

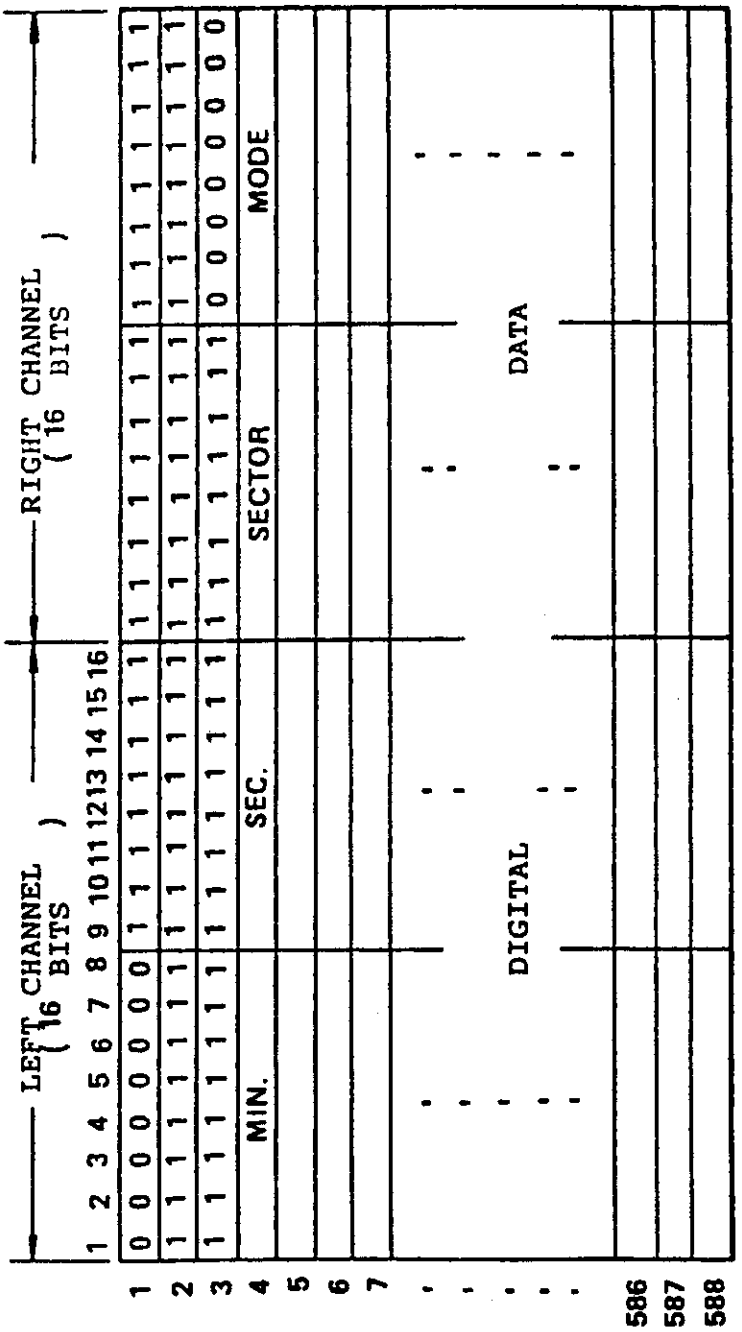

LEFT CHANNEL (16 BITS)
RIGHT CHANNEL (16 BITS)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
MIN.
SEC.
SECTOR
MODE
DIGITAL DATA
1
2
3
4
5
6
7
586
587
588

FIG.4

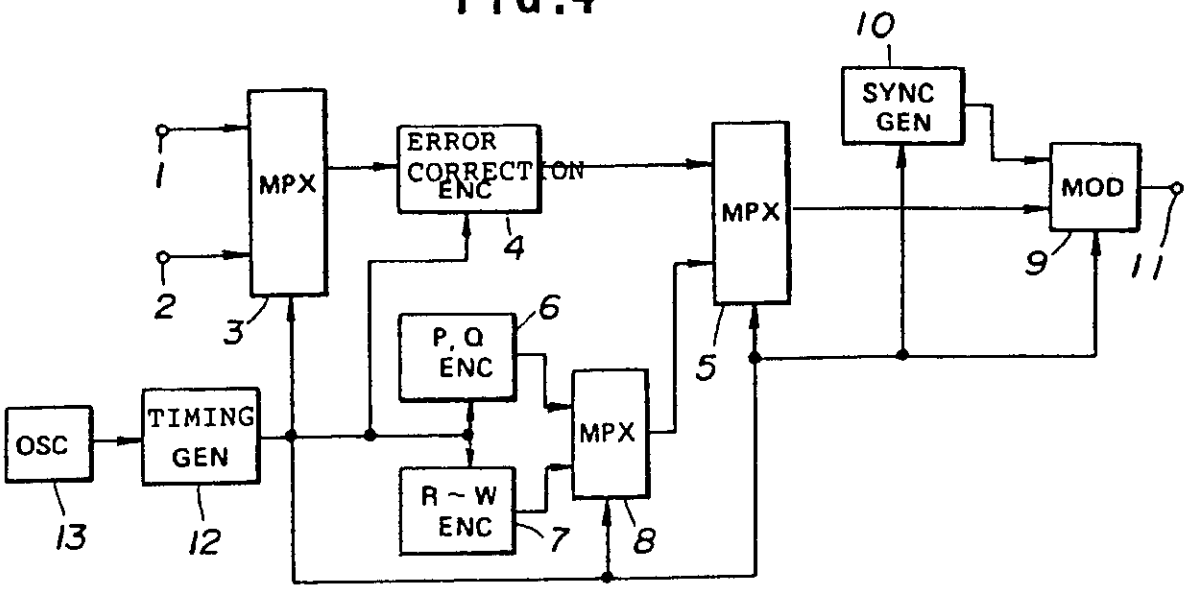

10
SYNC GEN
1
MPX
ERROR CORRECTION ENC
MPX
MOD
2
4
9
11
3
6
P, Q ENC
5
MPX
OSC
TIMING GEN
R ~ W ENC
7
8
13
12

FIG.5

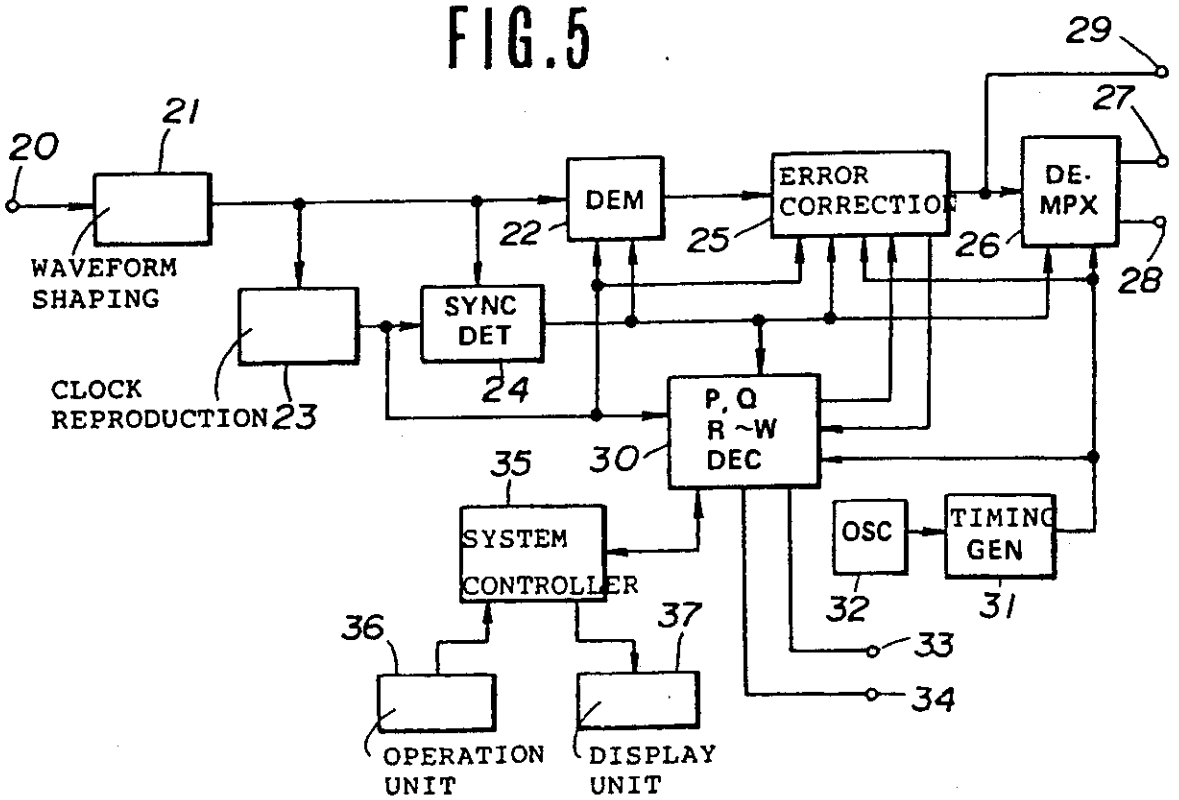
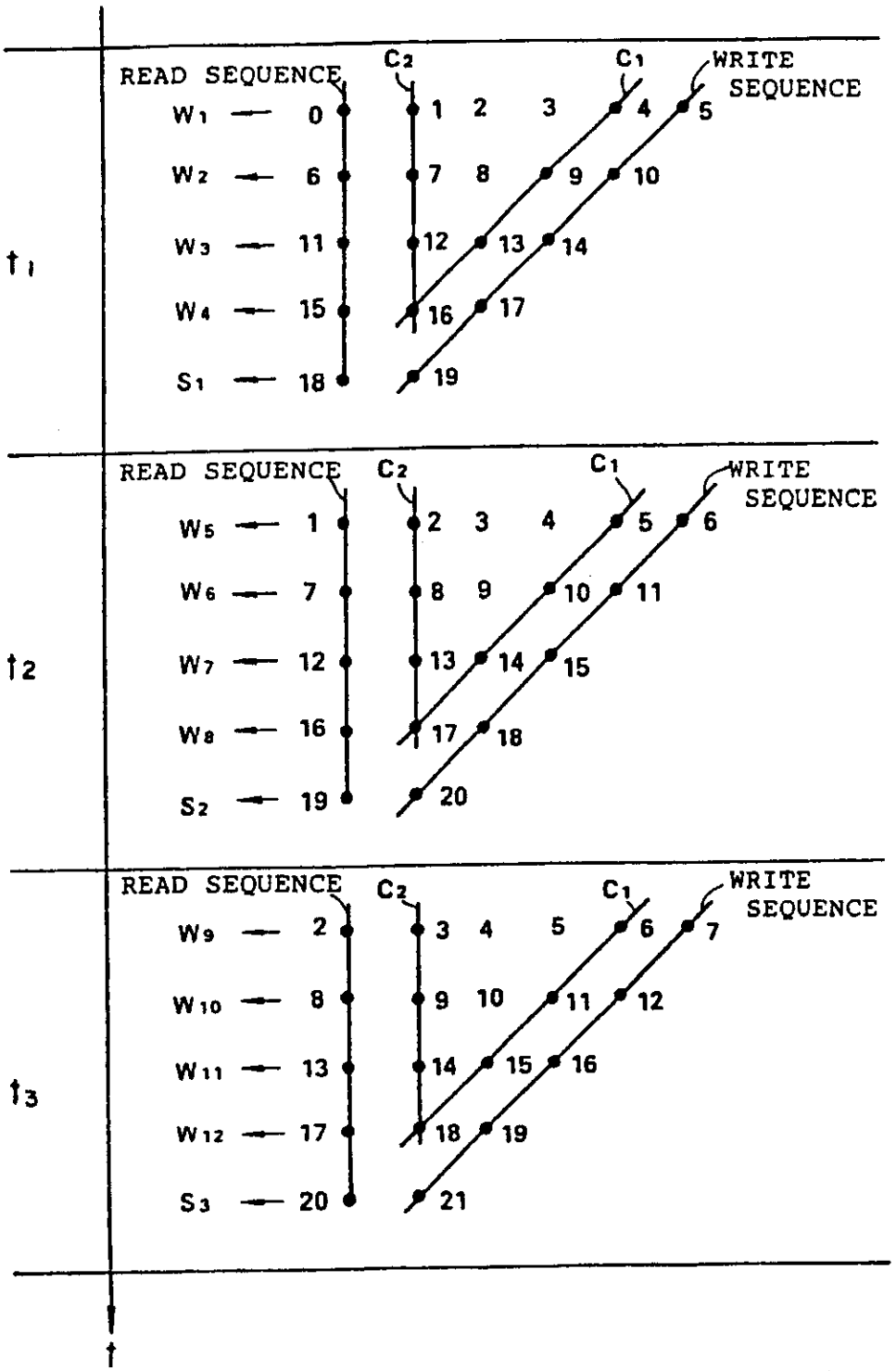

29
27
20
21
DEM
ERROR CORRECTION
DE-MPX
22
25
26
28
WAVEFORM SHAPING
SYNC DET
CLOCK REPRODUCTION
23
24
P, Q R ~W DEC
35
30
SYSTEM CONTROLLER
OSC
TIMING GEN
32
31
33
36
37
34
OPERATION UNIT
DISPLAY UNIT

FIG.6


READ SEQUENCE
C2
C1
WRITE SEQUENCE
W1 — 0
W2 — 6
W3 — 11
W4 — 15
S1 — 18
1 2 3 4 5
7 8 9 10
12 13 14
16 17
19
t1
READ SEQUENCE
C2
C1
WRITE SEQUENCE
W5 — 1
W6 — 7
W7 — 12
W8 — 16
S2 — 19
2 3 4 5 6
8 9 10 11
13 14 15
17 18
20
t2
READ SEQUENCE
C2
C1
WRITE SEQUENCE
W9 — 2
W10 — 8
W11 — 13
W12 — 17
S3 — 20
3 4 5 6 7
9 10 11 12
14 15 16
18 19
21
t3
t

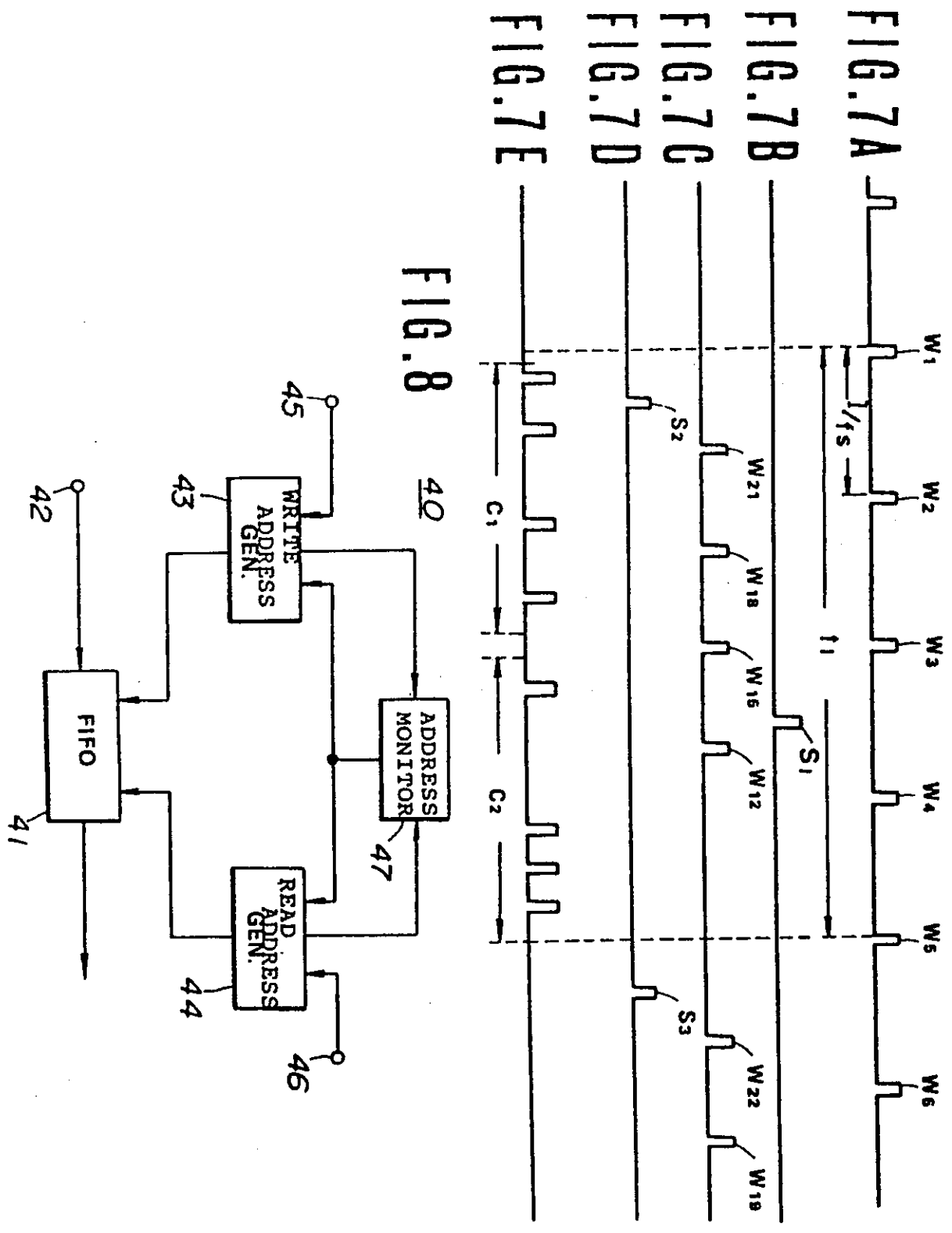


FIG.7A
FIG.7B
FIG.7C
FIG.7D
FIG.7E
W1
W2
W3
W4
W5
W6
1/fs
t1
S1
S2
S3
W21
W18
W16
W12
W22
W19
C1
C2

FIG.8

40
41
42
43
44
45
46
47
FIFO
WRITE ADDRESS GEN.
READ ADDRESS GEN.
ADDRESS MONITOR

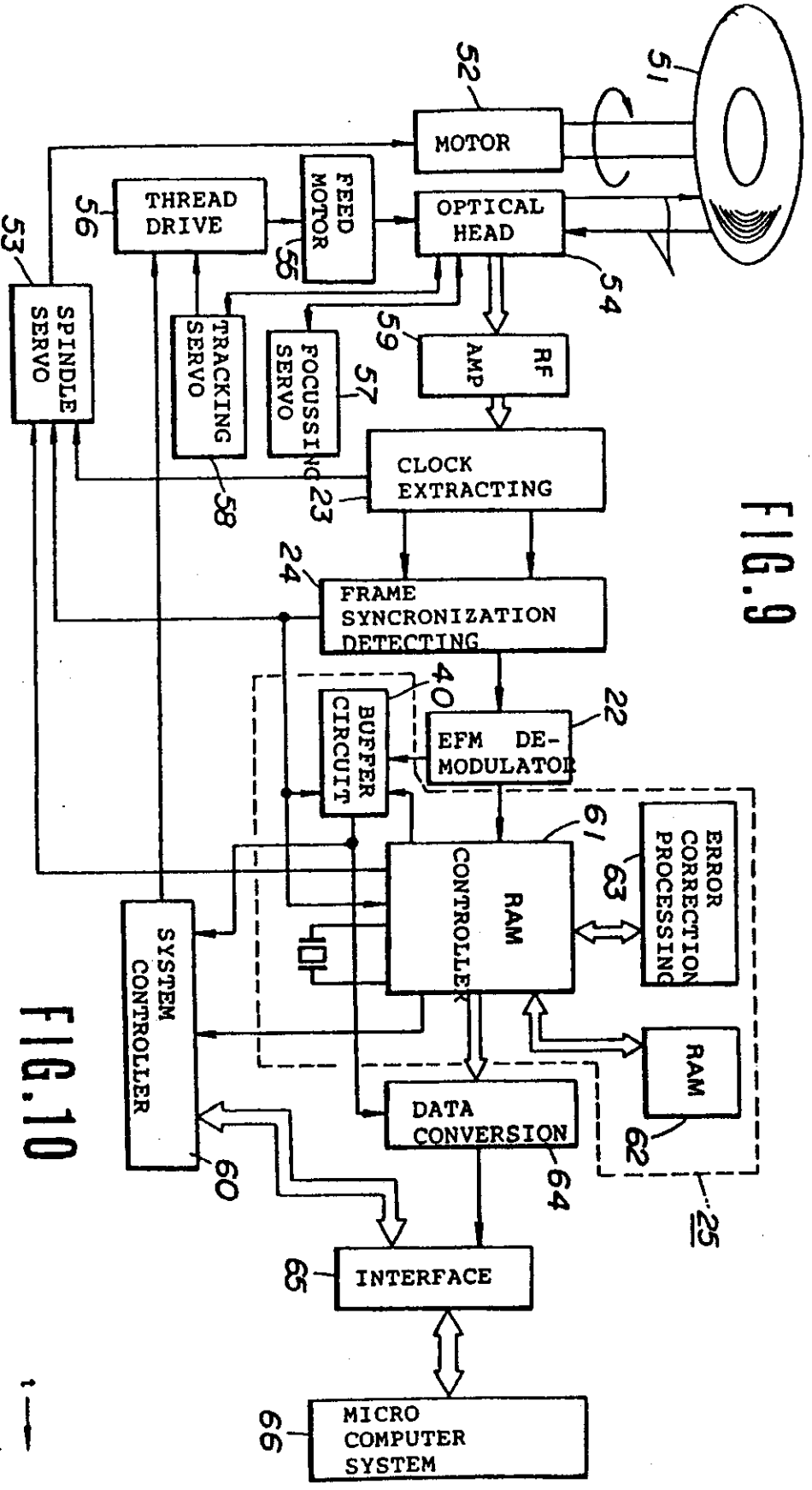

51
52
MOTOR
THREAD DRIVE
56
FEED MOTOR
55
OPTICAL HEAD
54
53
SPINDLE SERVO
TRACKING SERVO
58
FOCUSSING SERVO
57
59
RF AMP
CLOCK EXTRACTING
23
24
FRAME SYNCRONIZATION DETECTING
40
BUFFER CIRCUIT
22
EFM DE-MODULATOR
61
RAM CONTROLLER
63
ERROR CORRECTION PROCESSING
101
SYSTEM CONTROLLER
60
RAM
62
DATA CONVERSION
64
25
65
INTERFACE
66
MICRO COMPUTER SYSTEM

FIG.9

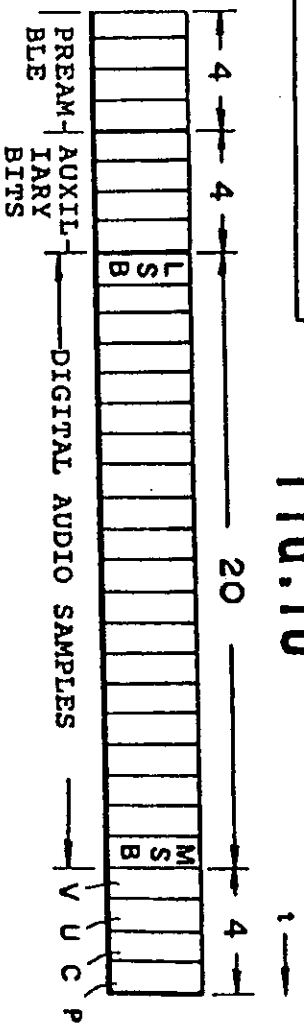

PREAMBLE
AUXILIARY BITS
DIGITAL AUDIO SAMPLES
LSB
MSB
V
U
C
P
4
4
20
4
1

FIG.10

25: error correcting circuit

27, 28: ouput terminal of reproduced data

29: decoder of subcoding signal

40: buffer circuit

41: FIFO buffer register

51: compact disc

52: spindle motor

54: optical head

55: threading feed motor

60: system controller

62: RAM

65: interface

66: microcomputer system

REGISTER ENTRY FOR EP0166785

European Application No EP85900188.5 filing date 14.12.1984

Application in Japanese

Priorities claimed:
16.12.1983 in Japan - doc: 052373708
23.12.1983 in Japan - doc: 052434868

PCT EUROPEAN PHASE
PCT Application PCT/JP84/00594 Publication No WO85/02707 on 20.06.1985

Designated States CH DE FR GB LI NL SE AT

Title DISK REPRODUCING APPARATUS

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Classified to
G4A
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Publication No EP0166785 dated 08.01.1986
Publication in English

Examination requested 14.08.1985

Patent Granted with effect from 04.03.1992 (Section 25(1)) with title DISK REPRODUCING APPARATUS.

**** END OF REGISTER ENTRY ****

RENEWAL DETAILS

PUBLICATION NUMBER	EP0166785

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DATE FILED	14.12.1984
DATE GRANTED	04.03.1992
DATE NEXT RENEWAL DUE	14.12.1995
DATE NOT IN FORCE	
DATE OF LAST RENEWAL	06.12.1994
YEAR OF LAST RENEWAL	11
STATUS	PATENT IN FORCE