



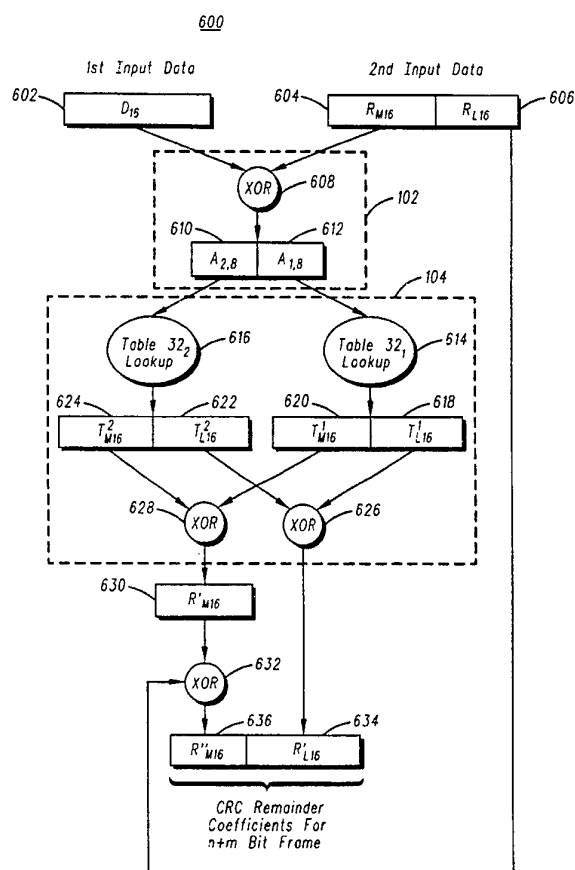
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(54) Title: EFFICIENT CRC REMAINDER COEFFICIENT GENERATION AND CHECKING DEVICE AND METHOD

(57) Abstract

Various parallel CRC remainder coefficient generation devices (100, 200, 300, 400, 500, 600, 700) and methods (1100, 1200) are described for providing efficient error detection in various digital data communication systems (800, 900, 1000). A K-bit CRC remainder is calculated from m bits at a time, where m can be less than, equal to, or greater than K, and where the processing of each of the m bits requires a total of j K-bit table look-ups into a total of j tables (410, 412, 414, 516, 518, 520, 522, 616, 614, 712, 714) of 2^b entries each, where $m = jb$. Also required are one m-bit exclusive-or operation (208, 306, 506, 608, 706), a total of (j-1)K-bit exclusive-or operations (422, 532, 626, 628, 720), and one (K-m)-bit exclusive-or operation (216, 632) if $m < K$. A 16-bit CRC using the new method can be implemented on a 16-bit DSP processor.



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EFFICIENT CRC REMAINDER COEFFICIENT GENERATION AND CHECKING DEVICE AND METHOD

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Field of the Invention

This invention relates generally to digital
communication error detection and, more particularly, to a
10 cyclic redundancy checking (CRC) device and method for error-
detection in a digital data communication system.

Background

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In a digital data communication system a receiver may
receive transmitted data signals that contain errors. A
number of factors, such as attenuation of signals,
transmission line loss, magnetic field changes, and noise may
20 cause such errors. Various error detection methods have been
developed to check received digital data for errors. Linear
systematic cyclic codes, commonly known as cyclic
redundancy (CRC) codes are typically used to provide error
detection capability at various network layers of modern data
25 communications networks.

CRC remainder coefficient generation and checking
devices are implemented both in hardware and in software.
Typical hardware implementations use serial shifter register
30 schemes wherein feedback shift registers perform a long
division of polynomials one bit at a time. To improve
throughput, octet algorithms that handle one 8 bit-byte at a
time have been developed. These octet algorithms are realized
in both hardware and software. However, error processing
35 utilizing CRC computations has a high degree of computational

complexity, and thus can have a significant impact on the performance or cost of a digital data communication system. For example, in one application, 1/3 of the processing available from a DSP56156 processor is consumed by CRC computation. Thus, there is a need for an efficient CRC computation device and method that reduces the complexity and processing requirements for CRC computation in a digital data communication system.

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Summary of the Invention

Described is a cyclic redundancy check (CRC) remainder coefficient generator, and a method for utilizing the generator, in a CRC circuit for generating a plurality of CRC remainder coefficients for an $(n+m)$ bit frame utilizing a first input of data for a plurality of m coefficients representing a last m bits of an $(n+m)$ bit frame (n, m are positive integers, $m > 1$; K is a degree of a CRC generating polynomial) and a second input of data for a plurality of K previously calculated CRC remainder coefficients of a first n bits of the frame. The generator includes at least a CRC circuit combining unit and a CRC circuit conversion unit. The CRC circuit combining unit is operably coupled to receive a preselected portion of the first input data and a preselected portion of the second input data, and substantially performs bitwise modulo-two addition of the preselected portion of the first input data and the preselected portion of second input data to provide adjusted coefficients. The CRC circuit conversion unit is operably coupled at least to the CRC circuit combining unit, and comprises a plurality (more than one) of look-up tables and substantially at least a first EXCLUSIVE-OR circuit, for utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the $(n+m)$ bit frame.

The method of the present invention implements the generator as described above, i.e., utilizing at least the CRC circuit combining unit and the CRC circuit conversion unit, to provide a plurality of CRC remainder coefficients for the (n+m) bit frame.

Brief Descriptions of the Drawings

FIG. 1 is a block diagram of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention.

FIG. 2 is a block diagram of a first embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein K is a length of the CRC.

FIG. 3 is a block diagram of a second embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m = K$.

FIG. 4 is a block diagram of an embodiment of a remainder conversion unit (RCU) in accordance with the present invention, wherein $m = bj$ and where b and j are a positive integers.

FIG. 5 is a block diagram of a fourth embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m = K = 32$, $j = 4$, and $b = 8$.

FIG. 6 is a block diagram of a fifth embodiment of a cyclic redundancy check (CRC) remainder coefficient generator

in a CRC circuit in accordance with the present invention wherein $K = 32$, $m = 16$, $j = 2$, and $b = 8$.

FIG. 7 is a block diagram of a seventh embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m = K = 16$, $j = 2$, and $b = 8$.

FIG. 8 is a block diagram of a point-to-point communication network system utilizing a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention.

FIG. 9 is a block diagram of a multipoint communication network system utilizing a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention.

FIG. 10 is a block diagram of a mixed communication network system utilizing a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention.

FIG. 11 is a flow chart setting forth steps in accordance with a first implementation of the method of the present invention.

FIG. 12 is a flow chart setting forth steps in accordance with a second implementation of the method of the present invention.

FIG. 13 is a block diagram of an embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m > K$.

Detailed Description of a Preferred Embodiment

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The present invention is described below, with a description of its application to a digital transmission system in general. Then, special cases are described. A frame is a
10 block of data that is transmitted or received in a digital data system.

Cyclic code error-detection methods typically divide a data message as a polynomial $d(x)$ by a predetermined
15 generating polynomial $g(x)$ to provide a quotient polynomial $q(x)$ and a remainder polynomial $r(x)$ such that:

$$d(x) = q(x) * g(x) + r(x).$$

The remainder $r(x)$ is the cyclic redundancy check (CRC) and may be, for example, 16 bits in length (two 8 bit bytes). The
20 CRC is appended to the block of data to be transmitted, and the receiving device uses the same predefined generating polynomial to generate its own internally generated CRC based on the received message block, comparing the CRC it has generated with the transmitted CRC. If an error has occurred
25 during transmission, the internally generated CRC does not match the transmitted CRC.

The CRC remainder coefficient generator of the present invention provides CRC remainder coefficients for efficient
30 generation of a frame check sequence for a frame to be transmitted and for efficient cyclic redundancy check (CRC) error detection for a received digital signal frame in a digital communication system, typically by utilizing a system that includes multiple look-up tables having preselected
35 precalculated CRC remainder coefficients. This minimizes

actual computation time during CRC error-checking such that, where the present invention is combined with efficient encoding, the amount of time used for CRC computation is reduced by almost one-half for a software implementation.

- 5 Significant savings can also be achieved with a hardware implementation.

The present invention may be applied to any K-bit CRC with any frame length, but is particularly efficient for 16-bit
10 and 32-bit CRCs with frame length of $8n$ bits (n is a positive integer).

The present invention may be implemented to support a 16-bit CRC as specified in the CCITT (International Telegraph
15 and Telephone Consultative Committee) X.25 recommendation. In addition, the present invention supports the 32-bit CRC specified in the ANSI/IEEE (American National Standards Institute/Institute of Electrical & Electronics Engineers, Inc.)
802.X standard.

20

First, with respect to the 32-bit CRC, the ANSI/IEEE Standard 802.X specifies that the Frame Check Sequence (FCS) is the one's complement of the remainder

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$$r(x) = \text{Rem}_g(x) \{x^i I(x) + x^{32} s_f(x)\}$$

where $g(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ is a generating polynomial, $I(x) = x^{31} + x^{30} + \dots + x + 1$ represents an initial remainder polynomial, i is a
30 number of bits in the frame (not including the FCS), and $s_f(x)$ is a polynomial formed by contents of the frame.

The ANSI/IEEE 802.5 standard specifies that each octet of the frame is transmitted most significant bit first, and that
35 the FCS be transmitted commencing with the coefficient of the

highest term. The coefficient of the highest order term is the most significant bit of the first octet of the frame.

- 5 The basis for the present invention may be understood as follows:

Let $g(x)$ be any CRC generating polynomial of degree K , $s(x)$ be a polynomial of $(n-1)$ th degree formed by the first n bits of the frame, and $I(x)$ be a polynomial of $(K-1)$ th degree formed by an initial remainder. Throughout the description of this invention, m , n and K are defined to be positive integers. Upon processing a first n bits of the frame, a remainder polynomial for the n bits is

15

$$\begin{aligned} r(x) &= \text{Rem}_{g(x)}\{x^n I(x) + x^K s(x)\} \\ &= r_{K-1}x^{K-1} + r_{K-2}x^{K-2} + \dots + r_1x + r_0. \end{aligned}$$

where $r_{K-1}, r_{K-2}, \dots, r_1, r_0$ are remainder coefficients.

- 20 To find a remainder $r'(x)$ for a first $(n+m)$ bits of the frame, where $0 < m \leq K$, the polynomial $s'(x)$ formed by the first $(n+m)$ bits may be written as

$$s'(x) = s(x)x^m + d(x)$$

25

where $d(x) = d_{m-1}x^{m-1} + d_{m-2}x^{m-2} + \dots + d_1x + d_0$ is a polynomial whose coefficients are from an m additional bits of the frame. Thus, the new remainder $r'(x)$ is given by:

30

$$\begin{aligned} r'(x) &= \text{Rem}_{g(x)}\{x^{n+m} I(x) + x^K s'(x)\} \\ &= \text{Rem}_{g(x)}\{x^{n+m} I(x) + x^K [s(x)x^m + d(x)]\} \\ &= \text{Rem}_{g(x)}\{x^m [x^n I(x) + x^K s(x)] + x^K d(x)\}. \end{aligned}$$

Since $r(x) = \text{Rem}_g(x)\{x^n l(x) + x^K s(x)\}$, which means that $x^n l(x) + x^K s(x) = q(x)g(x) + r(x)$, where $q(x)$ is the quotient polynomial, the above equations may be rewritten:

$$\begin{aligned}
 5 \quad r'(x) &= \text{Rem}_g(x)\{x^m[q(x)g(x) + r(x)] + x^K d(x)\} \\
 &= \text{Rem}_g(x)\{x^m q(x)g(x) + x^m r(x) + x^K d(x)\} \\
 &= \text{Rem}_g(x)\{x^m q(x)g(x)\} + \text{Rem}_g(x)\{x^m r(x) + x^K d(x)\} \\
 &= \text{Rem}_g(x)\{x^m r(x) + x^K d(x)\} \\
 &= \text{Rem}_g(x)\{[r_{K-1} + d_{m-1}]x^{K+m-1} + \dots + [r_{K-m} + d_0]x^K \\
 10 \quad &\quad + r_{K-m-1}x^{K-1} + \dots + r_1x^m + r_0x^{m-1}\} \\
 &= \text{Rem}_g(x)\{[r_{K-1} + d_{m-1}]x^{K+m-1} + \dots + [r_{K-m} + d_0]x^K \\
 &\quad + r_{K-m-1}x^{K-1} + \dots + r_1x^m + r_0x^{m-1}\}.
 \end{aligned}$$

Thus, utilizing the above relationship for $0 < m \leq K$, the present invention provides for obtaining the new remainder coefficients for the first $(n+m)$ bits from the previous remainder coefficients for the first n bits by:

1) bitwise modulo-two addition of the m new bits to the m coefficients of the m highest order terms of the previous remainder polynomial (i.e., $r_{K-1} + d_{m-1}$, $r_{K-2} + d_{m-2}$, ..., $r_{K-m} + d_0$);

2) determining coefficients of an intermediate remainder

25 $\text{Rem}_g(x)\{[r_{K-1} + d_{m-1}]x^{K+m-1} + \dots + [r_{K-m} + d_0]x^K\}$; and

3) obtaining the new remainder coefficients by adding the $(K-m)$ lowest order term coefficients of the previous remainder $r_{K-m-1}x^{K-1} + \dots + r_1x^m + r_0x^{m-1}$ to the $(K-m)$ highest order term coefficients of the intermediate remainder.

For $m > K$, $r'(x)$ becomes:
 $r'(x) = \text{Rem}_g(x)\{x^m r(x) + x^K d(x)\}$

$$= \text{Rem}_g(x) \{ [r_{K-1} + d_{m-1}] x^{K+m-1} + \dots + [r_0 + d_{m-K}] x^m + d_{m-K-1} x^{m-1} + \dots + d_0 x^K \}$$

Hence, for the case of $m > K$, a new remainder for the first $(n+m)$ bits can be obtained from the m additional bits and a previous remainder of the first n bits by:

1. bitwise adding (modulo 2) the K bit previous remainder to the K coefficients of the K highest order terms of $d(x)$; i.e., $r'_{K-1} + d_{m-2}$, $r_{K-2} + d_{m-2}$, $\dots$, $r_0 + d_{m-K}$; and

2. the new remainder $r'(x)$ is then:
 $\text{Rem}_g(x) \{ [r_{K-1} + d_{m-1}] x^{K+m-1} + \dots + [r_0 + d_{m-K}] x^m + d_{m-K-1} x^{m-1} + \dots + d_0 x^K \}$

FIG. 1, numeral 100, is a block diagram of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention. The invention comprises two elements: a CRC circuit combining unit (102) and a CRC circuit conversion unit (104). The CRC circuit combining unit (102) combines data of a first input, a preselected portion of a last m coefficients of an $(n+m)$ bit frame, with a preselected portion of the second input data that represents a preselected portion of previously calculated CRC remainder coefficients of a first n bits of the $(n+m)$ bit frame to provide a plurality of adjusted coefficients. The CRC circuit combining unit (102) typically is an EXCLUSIVE-OR circuit (see FIG. 2, 208) that performs bitwise modulo-two addition on said inputs. The CRC circuit conversion unit (104) is operably coupled at least to the CRC circuit combining unit (102), and comprises at least one of A) a first look-up table, and B) a plurality (more than one) of look-up tables and substantially at least a first EXCLUSIVE-OR circuit, for

utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the (n+m) bit frame. An EXCLUSIVE-OR circuit performs bitwise modulo-two addition. Selected implementations of the present invention are set forth below.

For example, FIG. 2, numeral 200, is a block diagram of a first embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein K is a length of the CRC. Here $D_m = [d_{m-1}, d_{m-2}, \dots, d_1, d_0]$ (202) represents m coefficients of an (n+m) bit frame (i.e., m bits after the first n bits), $R_{Mm} = [r_{K-1}, r_{K-2}, \dots, r_{K-m}]$ (204) represents a preselected portion of previously calculated CRC remainder coefficients of n bits of the (n+m) bit frame (here, m highest order remainder coefficients of the second input data, where m is greater than zero and less than or equal to K), and $R_{L(K-m)} = [r_{K-m-1}, r_{K-m-2}, \dots, r_0]$ ((206) represents a second preselected portion of previously calculated CRC remainder coefficients of n bits of the (n+m) bit frame (here, (K-m) lowest order remainder coefficients of the second input data). In this implementation, the CRC circuit combining unit (102) includes an EXCLUSIVE-OR circuit (208) that performs bitwise modulo-two addition of D_m (202) and R_{Mm} (204) (m highest order coefficients of the previous remainder polynomial, where $1 < m \leq K$) to provide (output) adjusted coefficients. The CRC conversion unit (104) in this implementation includes a Remainder Conversion Unit 1 (210) that typically includes one of A-B:

A) one memory look-up table of size 2^m by K, operably coupled to the CRC circuit combining unit (102), for utilizing the adjusted coefficients to output one of:

A1) all coefficients (FIG. 3 (310)) of the CRC intermediate remainder for the (n+m) bit frame, wherein each

coefficient has been precomputed and stored in the memory look-up table; and

A2) K coefficients (212, 214) of a CRC intermediate remainder (212, 214) comprising K-m highest order coefficients (212) of the CRC intermediate remainder and m lowest order coefficients (214) of the CRC intermediate remainder that are m lowest order coefficients of the CRC remainder for the (n+m) bit frame, wherein each coefficient has been precomputed and stored in the memory look-up table; and

B) j memory look-up tables ($1 < j < m$; j is a positive integer) of size 2^b by K (where $jb = m$), operably coupled to the CRC circuit combining unit (102), for utilizing the adjusted coefficients to output all coefficients (212, 214) of the CRC intermediate remainder for the (n+m) bit frame, wherein each coefficient has been precomputed and stored in one of the j memory look-up tables.

The Remainder Conversion Unit 1 (210) utilizes adjusted coefficients to provide intermediate remainder coefficients ($T_{M(K-m)}$, (K-m) highest order coefficients of the intermediate remainder (212); R'_{Lm} , m lowest order coefficients of the intermediate remainder (214)). The adjusted coefficients are $[r_{K-1} + d_{m-1}]$, $[r_{K-2} + d_{m-2}]$, ..., $[r_{K-m} + d_0]$ for the remainder terms x^{K+m-1} , x^{K+m-2} , ..., x^K , respectively. The CRC conversion unit (104) further includes an EXCLUSIVE-OR circuit (216) that performs bitwise modulo-two addition of $T_{M(K-m)}$ (212) (the highest order coefficients of the intermediate remainder) and $R_{L(K-m)}$ (214) (the lowest order coefficients of the previous remainder (for n bits) $r_{K-m-1}x^{K-1} + \dots + r_1x^m + r_0x^{m-1}$) to provide $R'_{M(K-m)}$ (218) (the highest order coefficients of the CRC remainder for the (n+m) bit frame), typically to a memory register. The Remainder Conversion Unit 1 (210) also provides R'_{Lm} (220) (the lowest order coefficients of the CRC remainder for the (n+m) bit frame), typically to a memory register.

These two outputs, $R'_{M(K-m)}$ (218) and R'_{Lm} (220), represent all the coefficients of the CRC remainder for the $(n+m)$ bit frame. Where selected, the CRC remainder coefficients for the $(n+m)$ frame may be stored as a set of bits in a memory register.

FIG. 3, numeral 300, is a block diagram of a second embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m = K$. Here, the remainder for an $(n + m)$ bit frame, where $m = K$, is calculated K bits at a time, significantly saving in CRC remainder generation time. In this implementation, $D_m = D_K = [d_{K-1}, d_{K-2}, \dots, d_1, d_0]$ (302) represents $m = K$ coefficients of an $(n+m)$ bit frame (i.e., m bits after the first n bits), $R_K = [r_{K-1}, r_{K-2}, \dots, r_0]$ (304) represents all of the previously calculated CRC remainder coefficients of n bits of the $(n+m)$ bit frame or, identically, all of the remainder coefficients of the second input data. In this implementation, the CRC circuit combining unit (102) includes an EXCLUSIVE-OR circuit (306) that performs bitwise modulo-two addition of D_K (302) and R_K (304) to provide adjusted coefficients to the CRC conversion unit (104). The CRC conversion unit (104) in this implementation includes a Remainder Conversion Unit 2 (308) that typically includes one of:

- one memory look-up table of size 2^K by K , operably coupled to the CRC circuit combining unit (102), for utilizing the adjusted coefficients to output all coefficients (R'_K , 310) of the CRC intermediate remainder for the $(n+m)$ bit frame, wherein each coefficient has been precomputed and stored in the memory look-up table; and
- j memory look-up tables ($j < K$; j is a positive integer) of size 2^b by K (where $jb = K$), operably coupled to the CRC circuit combining unit (102), for utilizing the adjusted coefficients to output all coefficients (R'_K , 310) of the CRC intermediate

remainder for the $(n+m)$ bit frame, wherein each coefficient has been precomputed and stored in one of the j memory look-up tables.

5 In the special case of the second implementation, the coefficients of the CRC intermediate remainder are simply the coefficients of the CRC remainder for the $(n + K)$ bit frame. Thus, the Remainder Conversion Unit 2 (308) provides intermediate remainder coefficients $R'_K = [r_{K-1} + d_{K-1}]$, $[r_{K-2} + d_{K-2}]$, ... , $[r_0 + d_0]$ that represent all of the coefficients for the
 10 CRC remainder for the $n + K$ bit frame. Note that this implementation does not require a second EXCLUSIVE-OR circuit, as was utilized in the first implementation, thus saving on circuit complexity or computation time.

15 Thus, it is clear that the remainder conversion unit (RCU) may be implemented in a number of ways. Where the remainder conversion unit utilizes only one memory look-up table of size 2^m by K to store precomputed intermediate remainder
 20 coefficients, a fastest implementation is achieved. However, where m is large (for example, $m = K$), such a look-up table would require a large memory space consumption. On the other extreme, the RCU can be implemented by using m precomputed tables of size 1 by K , which will require $(m-1)$ additional K -bit
 25 EXCLUSIVE-OR operations, significantly lowering conversion speed of the RCU. Generally, it is possible to trade-off some speed with memory space consumption in an implementation that utilizes j memory look-up tables of size 2^b by K , where $jb = m$, as is set forth in FIG. 4.

30 FIG. 4, numeral 400, is a block diagram of an embodiment of a remainder conversion unit (RCU) in accordance with the present invention, wherein $m = bj$ and where b is a positive integer, typically 8, and j is a positive integer. In this
 35 implementation, the RCU includes j memory look-up tables

(Table K_1 Lookup (410), Table K_2 Lookup (412), ... , Table K_j Lookup (414)) of size 2^b by K that are operably coupled to the CRC circuit combining unit (102), and an EXCLUSIVE-OR circuit (422) that is operably coupled to the memory look-up tables.

- 5 The adjusted coefficients from the CRC circuit combining unit (102) are utilized by the j memory look-up tables (Table K_1 Lookup (410), Table K_2 Lookup (412), ... , Table K_j Lookup (414)), to output, typically to memory registers, j sets T_{K^1} (416), T_{K^2} (418), ..., T_{K^j} (420), each having K bits, of precomputed
 10 intermediate remainder coefficients, which, bitwise modulo-two summed (i.e., EXCLUSIVE-ORed) together $(j-1)$ times, are all coefficients of the CRC intermediate remainder for the $(n + m)$ bit frame, wherein each coefficient has been precomputed and stored in one of the j memory look-up tables.

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Hence, in the FIG. 4 RCU implementation, the intermediate CRC remainder may be rewritten as (i.e., the formula for generating the tables of coefficients):

$$\begin{aligned}
 & \text{Rem}_{g(x)}\{[r_{K-1} + d_{m-1}]x^{K+m-1} + \dots + [r_{K-m} + d_0]x^K\} = \\
 20 \quad & \text{Rem}_{g(x)}\{[r_{K-1} + d_{m-1}]x^{K+m-1} + \dots + [r_{K-b} + d_{m-b}]x^{K+m-b}\} \\
 & \text{Rem}_{g(x)}\{[r_{K-b-1} + d_{m-b-1}]x^{K+m-b-1} + \dots \\
 & \quad + [r_{K-2b-m} + d_{m-2b}]x^{K+m-2b}\} \\
 & + \dots + \text{Rem}_{g(x)}\{[r_{K-(j-1)b-1} + d_{m-(j-1)-1}]x^{K+m-(j-1)-1} + \dots \\
 & \quad + [r_{K-jb} + d_0]x^K\}
 \end{aligned}$$

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- Thus, in general, each of j terms of the the above equation calculates a remainder of a polynomial of degree $[K + m - (j - 1)b - 1]$ whose all but b highest order terms are zeros. Thus, where $m = jb$, the m bits are partitioned into j segments A_{1b} (408), A_{2b} (406), ... (404), A_{jb} (402), of b bits each, and each
 30 segment is used as an address for a memory look-up table of coefficients. Each table of coefficients is precomputed and prestored for each of the j intermediate remainder terms, each table containing 2^b entries, and each entry consisting of K
 35 coefficients of the intermediate remainder of such polynomial

of degree $[K + m - (j - 1)b - 1]$ with a particular combination of b highest order coefficient terms (all other terms must be zero by definition).

5 For applications where the word lengths are shorter than K , each entry of the table occupies more than one memory location. For example, for a 32-bit CRC determination, if the word length of the device is 16, then each table entry requires 2 memory locations and 2^{b+1} memory words for each lookup
10 table. Depending on the architecture and addressing mode of the device, each lookup table may be organized as 2^b entries with each entry occupying two consecutive 16-bit words. Alternatively, each lookup table may be organized as two halves, where the upper half table contains the 2^b upper word
15 of every entry and the lower half table contains the 2^b lower word of every table entry.

In this implementation, the CRC circuit combining unit (102) includes an EXCLUSIVE-OR circuit (422), operably
20 coupled to receive the j memory register (416, 418, ..., 420) outputs, that performs bitwise modulo-two addition of all j look-up table coefficients, $T_K^1(416)$, $T_K^2(418)$, ..., $T_K^j(420)$ to provide all $(T_K, 424)$ of the the coefficients of the intermediate remainder.

25 FIG. 5, numeral 500, is a block diagram of a fourth embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m = K = 32$, $j = 4$, and $b = 8$. This
30 implementation is well-suited to a 32-bit device. Where $D_{32} = [d_{31}, d_{30}, \dots, d_1, d_0]$ (502) represents 32 coefficients of an $(n+32)$ bit frame (i.e., 32 bits after the first n bits), $R_{32} = [r_{31}, r_{K-2}, \dots, r_0]$ (504) represents a preselected portion of previously calculated CRC remainder coefficients of 32 bits of
35 the n bit frame (here, 32 highest order remainder coefficients

(i.e., all) of the second input data). In this implementation, the CRC circuit combining unit (102) includes an EXCLUSIVE-OR circuit (506) that performs bitwise modulo-two addition of D_{32} (502) and R_{32} (504) to provide (output) adjusted coefficients, which, in this implementation, are partitioned into four segments $A_{1,8}$ (514), $A_{2,8}$ (512), $A_{3,8}$ (510), $A_{4,8}$ (508), of 8 bits each, and each segment is used as an address for a memory look-up table of coefficients of the CRC circuit conversion unit (104): Table 32₁ Lookup (516), Table 32₂ Lookup (518), Table 32₃ Lookup (520), and Table 32₄ Lookup (522), respectively. Each table of coefficients is precomputed and prestored for each of the 4 intermediate remainder terms, each table containing 2^8 entries, and each entry consisting of 32 adjusted coefficients of the intermediate remainder of such polynomial of degree $[K + m - (j - 1)b - 1]$ with a particular combination of 8 highest order coefficient terms (all other terms must be zero by definition). Each look-up table (Table 32₁ Lookup (516), Table 32₂ Lookup (518), Table 32₃ Lookup (520), and Table 32₄ Lookup (522)) of the RCU (104) is operably coupled to a memory register (T_{32}^1 , (524); T_{32}^2 , (526); T_{32}^3 , (528); T_{32}^4 , (530)) (102) for storing the entries in the memory registers.

The CRC conversion unit (104) further includes an EXCLUSIVE-OR circuit (532) that performs bitwise modulo-two addition of T_{32}^1 (524), T_{32}^2 (526), T_{32}^3 (528), T_{32}^4 (530) to provide R'_{32} (534), all the coefficients of the CRC remainder for the $(n+m)$ bit frame. Where selected, the CRC remainder coefficients for the $(n+m)$ frame may be stored as a set of bits in a memory register.

FIG. 6, numeral 600, is a block diagram of a fifth embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the

present invention wherein $K = 32$, $m = 16$, $j = 2$, and $b = 8$. This implementation is well-suited to a 16-bit processing device. Here $D_m = D_{16} = [d_{15}, d_{14}, \dots, d_1, d_0]$ (602) represents 16 coefficients of an $(n+16)$ bit frame (i.e., 16 bits after the first
 5 n bits), $R_{M16} = [r_{31}, r_{30}, \dots, r_{16}]$ (604) represents a preselected portion of previously calculated CRC remainder coefficients of n bits of the $(n+16)$ bit frame (here, 16 highest order remainder coefficients of the second input data), and $R_{L16} = [r_{K15}, r_{14}, \dots, r_0]$ ((606) represents a second preselected
 10 portion of previously calculated CRC remainder coefficients of n bits of the $(n+16)$ bit frame (here, a (16) lowest order remainder coefficients of the second input data).

In this implementation, the CRC circuit combining unit
 15 (102) includes an EXCLUSIVE-OR circuit (608) that performs bitwise modulo-two addition of D_{16} (602) and R_{M16} (604) to provide (output) adjusted coefficients, which, in this implementation, are partitioned into two segments, $A_{1,8}$ (612) and $A_{2,8}$ (610), of 8 bits each, and each segment is used as an
 20 address for a memory look-up table of coefficients of the CRC circuit conversion unit (104): Table 32₁ Lookup (614) and Table 32₂ Lookup (616), respectively. Each table (of which there are two) of coefficients is precomputed and prestored for each of the 2 intermediate remainder terms, each table containing 2⁸
 25 entries, each entry consisting of 32 adjusted coefficients of the intermediate remainder. Each table (Table 32₁ Lookup (614) and Table 32₂ Lookup (616)) provides 32 bit intermediate remainder coefficients for a separate intermediate remainder, wherein the coefficients from each
 30 table are partitioned into two segments, one segment having 16 highest order remainder coefficients (T^1_{M16} (620); T^2_{M16} (624)) and the other segment having 16 lowest order remainder coefficients (T^1_{L16} (618); T^2_{L16} (622)). Thus, each look-up table (Table 32₁ Lookup (614) and Table 32₂ Lookup (616)) of
 35 the RCU (104) is operably coupled to a memory register that is

partitioned to provide two 16 bit entries (T^1_{L16} (618) and T^1_{M16} (620), and T^2_{L16} (622) and T^2_{M16} (624)) for storing the entries in the memory registers.

5 In FIG. 6, the CRC conversion unit (104) includes a second EXCLUSIVE-OR circuit that includes a first (626) and a second (628) intermediate EXCLUSIVE-OR circuit, the first (626) being operably coupled to memory registers for T^1_{L16} (618) and T^2_{L16} (622), and the second (628) being operably coupled to
 10 memory registers for T^1_{M16} (620) and T^2_{M16} (624), respectively, that perform bitwise modulo-two addition of $\{T^1_{L16}$ (618) and T^2_{L16} (622)}, and on $\{T^1_{M16}$ (620), T^2_{M16} (624)} respectively to provide two 16 bit coefficient (highest (630) and lowest (634)) sets to a memory register unit (R'_{L16} (634); R'_{M16} (630)). A third intermediate EXCLUSIVE-OR
 15 circuit (632), operably coupled to memory register unit having the 16 highest order coefficients (630) of the second EXCLUSIVE-OR circuit and to the memory register for R_{L16} (606), performs bitwise modulo-two addition on R'_{M16} (630) and R_{L16} (606) to provide coefficients R''_{M16} (636) (higher coefficients) that together with R'_{L16} (634) (lower coefficients) represent CRC remainder coefficients for the (n+m) bit frame. Where selected, the CRC remainder coefficients for the (n+m) frame may be stored in a memory
 20 register.
 25

 According to the definition of the ANSI/IEEE 802.3/Ethernet, the frame check sequence is based on the same CRC generating polynomial as that of IEEE/ANSI 802.5, but the
 30 order of transmission and bits arrangement are different. However, utilizing a similar derivation, it is clear that for the ANSI/IEEE 802.3/Ethernet CRC, FIGs. 1 through 6 stay the same if m is restricted to be 8, 16, 24, or 32, with slightly different definitions for D_8 , D_{16} , D_{24} , D_{32} , R_{32} , R'_{32} , and T_{j32} 's etc.:

$$\begin{aligned}
D_8 &= [d_7, d_6, \dots, d_0] \\
D_{16} &= [d_7, d_6, \dots, d_0, d_{15}, d_{14}, \dots, d_8] \\
D_{24} &= [d_7, d_6, \dots, d_0, d_{15}, d_{14}, \dots, d_8, d_{23}, d_{22}, \dots, d_{16}] \\
D_{32} &= [d_7, d_6, \dots, d_0, d_{15}, d_{14}, \dots, d_8, d_{23}, d_{22}, \dots, d_{16}, d_{31}, \\
5 \quad &d_{30}, \dots, d_{24}] \\
R_{32} &= [r_7, r_6, \dots, r_0, r_{15}, r_{14}, \dots, r_8, r_{23}, r_{22}, \dots, r_{16}, r_{31}, \\
&r_{30}, \dots, r_{24}] \\
R'_{32} &= [r'_7, r'_6, \dots, r'_0, r'_{15}, r'_{14}, \dots, r'_8, r'_{23}, r'_{22}, \dots, r'_{16}, \\
&r'_{31}, r'_{30}, \dots, r'_{24}] \\
10 \quad T_{j32} &= [t_{j7}, t_{j6}, \dots, t_{j0}, t_{j15}, t_{j14}, \dots, t_{j8}, t_{j23}, t_{j22}, \dots, t_{j16}, t_{j31}, \\
&t_{j30}, \dots, t_{j24}]
\end{aligned}$$

where $1 \leq j \leq 4$ and the d_i 's, r_i 's, r'_i 's, t_{j_i} 's are the coefficients of

$$\begin{aligned}
15 \quad d(x) &= d_{m-1} + d_{m-2}x + d_{m-3}x^2 + \dots + d_1x^{m-2} + d_0x^{m-1} \\
r(x) &= r_{31} + r_{30}x + r_{29}x^2 + \dots + r_1x^{30} + r_0x^{31} \\
r'(x) &= r'_{31} + r'_{30}x + r'_{29}x^2 + \dots + r'_1x^{30} + r'_0x^{31} \\
t_j(x) &= \text{Rem}_{g(x)} \{ [a_7 + a_6x + \dots + a_0x^7] x^{32+(j-1)8} \} \\
&= t_{j32} + t_{j30}x + t_{j29}x^2 + \dots + t_{j1}x^{30} + t_{j0}x^{31}
\end{aligned}$$

20

and $a_0, a_1, \dots, a_7$ are any combination of 1's and 0's.

FIG. 7, numeral 700, is a block diagram of a seventh embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention wherein $m = K = 16$, $j = 2$, and $b = 8$. This implementation is similar to that in FIG. 5. The order of bits is similar to that of ANSI/IEEE 802.3/Ethernet. Here $D_m = D_{16} = [d_7, d_6, \dots, d_1, d_0, d_{15}, d_{14}, \dots, d_8]$ (702), $R_{16} = [r_7, r_6, \dots, r_0, r_{15}, r_{14}, \dots, r_8]$ (704), and $R'_{16} = [r'_7, r'_6, \dots, r'_0, r'_{15}, r'_{14}, \dots, r'_8]$ (722). That is, the two octets of D_{16} , R_{16} , and R'_{16} are swapped. Actually, for memory organized as 16-bit word units, an X.25 frame is stored in exactly the same order shown given by D_{16} . The bit ordering reversal is solved utilizing the

following equations to generate the two look-up tables, Table 16₁(712) and Table 16₂(714):

$$t_1(x) = \text{Rem}_{g(x)} \{x^{16}[(r_{15} + d_{15}) + (r_{14} + d_{14})x^1 + \dots + (r_8 + d_8)x^7]\} \\ = t_{1,15} + t_{1,14}x + \dots + t_{1,8}x^7 + t_{1,7}x^8 + t_{1,6}x^9 + \dots + t_{1,0}x^{15}$$

5

$$t_2(x) = \text{Rem}_{g(x)} \{x^{16}[(r_7 + d_7)x^8 + (r_6 + d_6)x^9 + \dots + (r_0 + d_0)x^{15}]\} \\ = t_{2,15} + t_{2,14}x + \dots + t_{2,8}x^7 + t_{2,7}x^8 + t_{2,6}x^9 + \dots + t_{2,0}x^{15}$$

10 $t_1(x)$ is utilized to generate the coefficients of Table 16₁(712), $t_2(x)$ is utilized to generate the coefficients of Table 16₂(714), and the coefficients are stored in the following order:

$$[t_{1,7}, t_{1,6}, \dots, t_{1,0}, t_{1,15}, t_{1,14}, \dots, t_{1,8}] \text{ and} \\ [t_{2,7}, t_{2,6}, \dots, t_{2,0}, t_{2,15}, t_{2,14}, \dots, t_{2,8}].$$

15

Thus, in real-time remainder calculation, no additional time is required.

20 For frames containing an odd integer number of octets, the last octet of the frame has to be treated differently for CRC remainder generation if the rest of the frames are processed 16 bits at a time. Calculation of the CRC remainder 8 bits at a time is a known technique and may be implemented together with the present invention for processing a last byte 25 of a frame where the frame has an odd number of bytes. However, for completeness, it is shown here. Letting $m=8$ and $d(x) = d_7 + d_6x + \dots + r_0x^7$:

$$r'(x) = \text{Rem}_{g(x)} \{x^{n+8}I(x) + x^{16}s'(x)\} \\ = \text{Rem}_{g(x)} \{x^{n+8}I(x) + x^{16}[s(x)x^8 + d(x)]\} \\ 30 \quad = \text{Rem}_{g(x)} \{x^8[I(x)x^n + x^{16}s(x)] + x^{16}d(x)\} \\ = \text{Rem}_{g(x)} \{x^8r(x) + x^{16}d(x)\} \\ = \text{Rem}_{g(x)} \{(r_7 + d_7)x^{16} + (r_6 + d_6)x^{17} + \dots + (r_0 + d_0)x^{23}\} \\ + r_{15}x^8 + r_{14}x^9 + \dots + r_8x^{15}.$$

In this implementation, the CRC circuit combining unit (102) includes an EXCLUSIVE-OR circuit (706) that performs bitwise modulo-two addition of D_{16} (702) and R_{16} (704) to provide (output) adjusted coefficients, which, in this
5 implementation, are partitioned into two segments, $A_{1,8}$ (710) and $A_{2,8}$ (708), of 8 bits each, and each segment is used as an address for a memory look-up table of coefficients of the CRC circuit conversion unit (104): Table 16₁ Lookup (712) and Table 16₂ Lookup (714), respectively. Each table (of which there are
10 two) of coefficients is precomputed and prestored for each of the 2 intermediate remainder terms, each table containing 2^8 entries, each entry consisting of 16 adjusted coefficients of the intermediate remainder. Each table (Table 16₁ Lookup (712) and Table 16₂ Lookup (714)) provides 16 bit
15 intermediate remainder coefficients (T^1_{16} (716) and T^2_{16} (718)) for a separate intermediate remainder. Each look-up table (Table 16₁ Lookup (712) and Table 16₂ Lookup (718)) of the CRC circuit conversion unit (104) is operably coupled to a memory register that is partitioned to provide two 16 bit
20 entries (T^1_{16} (716) and T^2_{16} (718)) for storing the entries in the memory registers.

In FIG. 7, the CRC circuit conversion unit (104) further includes an EXCLUSIVE-OR circuit (720) that performs bitwise
25 modulo-two addition of T^1_{16} (716) and T^2_{16} (718) to provide a 16 bit set (R'_{16} (722)) of coefficients that together represent CRC remainder coefficients for the $(n+16)$ bit frame. Where selected, the CRC remainder coefficients for the $(n+16)$ frame may be stored in a memory register.

30

Thus, FIG. 7 illustrates a very fast generation for the FCS of a frame based on a 16-bit CRC on a 16-bit device, while utilized a reasonable amount of memory (for two 256-by-16 look-up tables). Similarly, FIG. 6 illustrates a very fast
35 generation of a FCS of a frame for a 32-bit CRC on a 16 bit

device with reasonable amount of memory (for two 256-by-32 look-up tables). Of course, the fastest way to generate the 32-bit CRC remainder is to use a 32 bit device with 1024-by-32 bit memory with the implementation shown in FIG. 5.

5

FIG. 8, numeral 800, is a block diagram of a point-to-point communication network system utilizing a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention. The point-to-point communication network system includes a computer (802), operably coupled to selected modems (804,...), wherein at least one modem is further coupled to another modem that is coupled to a terminal (806), and at least one modem is coupled to a switched network (806) that is coupled to an acoustic device (such as a telephone) (808). The acoustic device is coupled to an acoustic coupler (810) that is coupled to a further terminal. Any of: the computer (802), modems (804, ...), switched network (806), and terminals (812,...) in this system may be selected to include the cyclic redundancy check remainder coefficient generator of the present invention (100). Since the point-to-point communication network system, not including the present invention, is known in the art, it will not be further described here.

25

FIG. 9, numeral 900, is a block diagram of a multipoint communication network system utilizing a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention. The multipoint communication network system includes a computer (902), operably coupled to selected modems (904,...), wherein at least one modem is further coupled to a plurality of other modems, each further modem being further coupled to a terminal (906). Any of: the computer (902), modems (904, ...), and terminals (912,...) in this system may be selected to include the cyclic redundancy check remainder coefficient generator of the

35

present invention (100). Since the multipoint communication network system, not including the present invention, is known in the art, it will not be further described here.

5 FIG. 10, numeral 1000, is a block diagram of a mixed communication network system utilizing a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the present invention. The mixed (i.e., including point-to-point and multipoint) communication
10 network system includes a computer (1002), operably coupled to selected modems (1004,...), wherein at least one modem is further coupled to another modem that is coupled to a terminal (1006), wherein at least one modem is further coupled to a plurality of other modems, each further modem being further
15 coupled to a terminal (1006) and at least one modem is coupled to a switched network (1006) that is coupled to an acoustic device (such as a telephone) (1010). The acoustic device is coupled to an acoustic coupler (1012) that is coupled to a further terminal. Any of: the computer (1002), modems (1004,
20 ...), switched network (1008), and terminals (1006,...) in this system may be selected to include the cyclic redundancy check remainder coefficient generator of the present invention (100). Since the mixed communication network system, not including the present invention, is known in the art, it will not be
25 further described here.

 FIG. 11, numeral 1100, is a flow chart setting forth steps in accordance with a first implementation of the method of the present invention, a method for generating cyclic
30 redundancy check (CRC) remainder coefficients in a CRC circuit having a first input of data for a plurality of m coefficients representing m bits of an $(n+m)$ bit frame (n, m are positive integers, $m > 1$; K is a positive integer representing a degree of a CRC generating polynomial) and a second input of data for a
35 plurality of K previously calculated CRC remainder

coefficients of n bits of the frame. The method includes the steps of: (1) substantially performing, in a CRC circuit combining unit, bitwise modulo-two addition of a preselected portion of the first input data and the preselected portion of the second input data to provide a plurality of adjusted coefficients (1102); and (2) in a CRC circuit conversion unit, utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the $(n+m)$ bit frame (1104).

10

In the method set forth in FIG. 11, the CRC circuit combining unit may be selected to include at least an EXCLUSIVE-OR circuit, as described above. The preselected portion of the first input data comprises one of: (1) where
15 $m \leq K$, all remainder coefficients of the first input data; and (2) where $m > K$, K highest-order remainder coefficients of the first input data. Also, the preselected portion of the second input data typically comprises one of: (1) where $m \geq K$, all remainder coefficients of the second input data; and (2) where
20 $1 < m < K$, m highest-order remainder coefficients of the second input data. The CRC circuit conversion unit generally includes at least a remainder conversion unit that includes one of: (1) one memory look-up table of size 2^m by K , operably coupled to the CRC circuit combining means, for utilizing the plurality of adjusted coefficients to output all coefficients of the CRC intermediate remainder for the $(n+m)$ bit frame, wherein each coefficient has been precomputed and stored in the memory look-up table; and (2) j memory look-up tables ($1 < j < m$) of size 2^b by K (where $jb = m$; $1 < b < m$), operably
25 coupled to the CRC circuit combining means, for utilizing the plurality of adjusted coefficients to output all coefficients of the CRC intermediate remainder for the $(n+m)$ bit frame, wherein each coefficient has been precomputed and stored in one of the j memory look-up tables, wherein, where selected,
30 the coefficients of the CRC intermediate remainder for the
35

(n+m) bit frame are stored in memory registers for output to an EXCLUSIVE-OR circuit.

Further, in the method set forth in FIG. 11, the CRC circuit conversion unit may be selected to include one of: (1) at least a first memory register unit for receiving and storing the coefficients output by the included set of table(s) (above) and a second EXCLUSIVE-OR circuit for performing bitwise modulo two addition on K-m coefficients for highest order terms of the CRC intermediate remainder for the (n+m) bit frame, and K-m coefficients of lowest order remainder terms of the second input to provide K-m CRC remainder coefficients for a K-m highest order term coefficients for the (n+m) bit frame and for outputting the K-m highest order remainder coefficients with m lowest order remainder coefficients output by the included set of table(s) to provide the CRC remainder coefficients for the (n+m) bit frame; (2) where $m=bj$, j memory register units for each receiving and storing K coefficients output by the included set of table(s), and a second EXCLUSIVE-OR circuit for performing bitwise modulo two addition on the K coefficients of the j memory register units to provide the CRC remainder coefficients for the (n+m) bit frame; and (3) wherein $K=32$, $m=16$, $j=2$, and $b=8$, and two 32 bit look-up tables are utilized, further being characterized by: (3a) the second EXCLUSIVE-OR circuit being utilized for receiving and processing by bitwise modulo-two addition, 16 coefficients for highest order terms from each of the two 32 bit look-up tables to provide 16 highest order remainder coefficients for the CRC remainder coefficients for the (n+m) bit frame, and (3b) a third EXCLUSIVE-OR circuit being utilized for receiving and processing by bitwise modulo-two addition, 16 coefficients for lowest order terms from each of the two 32 bit look-up tables to provide 16 lowest order remainder coefficients for the CRC remainder coefficients for the (n+m)

bit frame, such that the plurality (32) of CRC remainder coefficients are provided for the (n+m) bit frame.

Similarly, where $K=32$, $m=8$, $j=1$, and $b=8$, the method set forth in FIG. 11 typically provides that (1) the preselected remainder coefficients of the second input data are 8 coefficients for highest order terms of the second input data, (2) the CRC circuit combining unit includes at least a first EXCLUSIVE-OR circuit for receiving and performing bitwise modulo two addition on the preselected remainder coefficients and the first input data to provide 8 intermediate coefficients; and (3) the CRC circuit conversion unit includes: (3a) a 32 bit memory look-up table for utilizing the 8 intermediate coefficients to output 32 coefficients of an intermediate 32 bit CRC remainder for the (n+m) bit frame, wherein each coefficient has been precomputed and stored in the memory look-up tables; (3b) a first storage register (1st SR) unit for receiving and storing, for 1st SR output, the 32 coefficients of the intermediate 32 bit CRC remainder, (3c) a shifting unit for receiving and shifting left by 8 bits (and inserting 8 zeros as lowest order term coefficients), 24 coefficients for lowest order terms of the second input data to provide a shift unit output, (3d) a second storage register (2nd SR) unit for receiving and storing, for 2nd SR output, the shifting unit output (data for 32 coefficients), and (3e) a second EXCLUSIVE-OR circuit, for receiving the 1st SR output and the 2nd SR output, for performing bitwise modulo-two addition on the 1st SR output and 2nd SR output to provide the plurality (32) of CRC remainder coefficients for the (n+m) bit frame.

FIG. 12, numeral 1200, is a flow chart setting forth steps in accordance with a second implementation of the method of the present invention, a method for generating cyclic redundancy check (CRC) remainder coefficients in a CRC circuit. The method includes the steps of: (1) storing data for

a plurality of m coefficients representing m bits of an $(n+m)$ bit frame (n, m are positive integers, $1 < m \leq K$; K is a positive integer representing a degree of a CRC generating polynomial) in a first memory register unit (1202), (2) storing data for a plurality of K previously calculated cyclic division polynomial remainder coefficients of a remaining portion of n bits of the frame in a second memory register unit (1204), (3) in a CRC circuit combining unit, substantially performing bitwise modulo-two addition on data from the first memory register storage unit and on a preselected portion of data from the second memory register unit to provide a plurality of adjusted coefficients (1206); and (4) in a CRC circuit conversion unit, utilizing at least the plurality of adjusted coefficients for providing a plurality of CRC remainder coefficients for the $(n+m)$ bit frame (1208), wherein the CRC circuit is in a modem. This implementation may also include the additional elements described above for FIG. 11. Thus, those further descriptions for the method in FIG. 12 are not repeated here.

It is clear, for example, that the present invention may be implemented in a LAN (local area network), a WAN (wide area network), or a MAN (metropolitan area network).

Clearly, the implementation where $1 < m \leq K$ may be extended to the case where $m > K$, as is illustrated in FIG. 13, where $D_{MK} = [d_{m-1}, d_{m-2}, \dots, d_{m-K}]$, $D_{L(m-K)} = [d_{m-K-1}, \dots, d_0]$, and $R_K = [r_{K-1}, r_{K-2}, \dots, r_0]$. Note that it is very similar to the special case of $m = K$ except that R_K is XORed with D_{MK} only. This case is useful where K is small relative to a word length of a processor/device, as in header checking for asynchronous transfer mode cells.

FIG. 13, numeral 1300, is a block diagram of an embodiment of a cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit in accordance with the

present invention wherein $m > K$. Here R_K represents a K-bit previously calculated CRC remainder $[r_0, r_1, \dots, r_{K-1}]$ (1302), D_{MK} (1304) represents K most significant bits of the m data bits, and $D_{L(m-K)}$ (1306) represents (m-K) bits of a least significant portion of the m data bits. In this implementation, the CRC circuit combining unit (102) includes an EXCLUSIVE-OR circuit (1308) that performs bitwise modulo-two addition of R_K (1302) and D_{MK} (1304), outputting K adjusted coefficients (A_{MK}) (1310) that represent K most significant coefficients of an intermediate result, typically to a register (1310) of the CRC circuit conversion unit (104). The (m-K) bits of the least significant portion of the m data bits ($D_{L(m-K)}$ (1306)), may be implemented, for example, by utilizing an (m-K) least significant bit portion of a register (1312) and inputting A_{MK} (1310) and $D_{L(m-K)}$ (1306) into a Remainder Conversion Unit (1314). Thus, the CRC circuit conversion unit (104) in this implementation includes a Remainder Conversion Unit (1314), implemented as described above for Remainder Conversion Unit 2 (308), that outputs a K-bit remainder R'_K (1316), representing all the coefficients of the CRC remainder. Where selected, the CRC remainder coefficients for the (n+m) frame may be stored as a set of bits in a memory register. It is clear to one skilled in the art that, in one implementation, a register 1304/1306 may be the same register as register 1310/1312.

25 A 16-bit CRC may be implemented using the method (700) in a 16-bit DSP processor, for example a DSP56156 processor, with $m=16$, $j=2$ and $b=8$, thereby reducing processor loading by 43% relative to the fastest prior art method which uses $m=8$, $j=1$, and $b=8$. A 32-bit CRC may be implemented using the method (600) in a 16-bit DSP processor with $m=16$, $j=2$, and $b=8$, thereby reducing the processor loading by 41% relative to the fastest prior art method which uses $m=8$, $j=1$, and $b=8$. Hardware implementation of the new method provides similar benefits with respect to throughput and area.

Although exemplary embodiments are described above, it will be obvious to those skilled in the art that many alterations and modifications may be made without departing
5 from the invention. Accordingly, it is intended that all such alternations and modifications be included within the spirit and scope of the invention as defined in the appended claims.

We claim:

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Claims:

1. A cyclic redundancy check (CRC) remainder coefficient generator in a CRC circuit having a first input of data for a plurality of m coefficients representing a last m bits of an $(n+m)$ bit frame (n, m are positive integers, $m > 1$; K is a positive integer representing a degree of a CRC generating polynomial) and a second input of data for a plurality of K previously calculated CRC remainder coefficients of a first n bits of the frame, comprising:
- 5
- 10
- 15
- 20
- 1A) CRC circuit combining means, operably coupled to receive a preselected portion of the first input data and a preselected portion of the second input data, for substantially performing bitwise modulo-two addition of the preselected portion of the first input data and the preselected portion of second input data to provide a plurality of adjusted coefficients; and
- 1B) CRC circuit conversion means, operably coupled at least to the CRC circuit combining means, comprising a plurality (more than one) of look-up tables and substantially at least a first EXCLUSIVE-OR circuit, for utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the $(n+m)$ bit frame.

2. The generator of claim 1 wherein the CRC circuit combining means includes at least an EXCLUSIVE-OR circuit, and, where selected, one of 2A-2B:

5 2A) the preselected portion of first input data that the EXCLUSIVE-OR circuit is coupled to receive comprises one of 2A1-2A2:

2A1) where $m > K$,
K most significant coefficients of m first input
10 data; and

2A2) where $1 < m \leq K$,
all coefficients of the first input data,
and

2B) the preselected portion of second input data that
15 the EXCLUSIVE-OR circuit is coupled to receive comprises one of 2B1-2B2:

2B1)) where $m \geq K$,
all remainder coefficients of the second input data;
and

20 2B2) where $1 < m < K$,
m highest-order remainder coefficients of the
second input data.

25 3. The generator of claim 1 wherein the CRC circuit conversion means includes at least a remainder conversion unit that includes j memory look-up tables ($1 < j < m$) of size 2^b by K (where $jb = m$; $1 < b < m$), operably coupled to the CRC circuit combining means, for utilizing at least the plurality of
30 adjusted coefficients to output all coefficients of the CRC intermediate remainder for the (n+m) bit frame, and wherein each coefficient has been precomputed and stored in one of the j memory look-up tables, wherein, where selected, the coefficients of the CRC intermediate remainder for the (n+m)

bit frame are stored in memory registers for output to an EXCLUSIVE-OR circuit, and, where selected, one of 3A-3B:

3A) one of: $b = 8$ and $b = 16$,

3B) the CRC circuit conversion means further includes
5 a second EXCLUSIVE-OR circuit, operably coupled to j register means, each of which is operably coupled to a separate one of the j memory look-up tables such that the circuit receives j sets of K coefficients for the CRC intermediate remainder, for performing bitwise modulo-two addition ($j-1$ times) on said
10 coefficients to provide the CRC remainder coefficients for the $(n+m)$ bit frame, and where selected, wherein $K = 32$, $m = 16$, $j = 2$, and $b = 8$, and two 32 bit look-up tables are utilized, wherein the second EXCLUSIVE-OR circuit includes one of 3B1-3B4:

15 3B1) a first intermediate EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for lowest order terms from each of the two 32 bit look-up tables;

20 3B2) a second intermediate EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for highest order terms from each of the two 32 bit look-up tables;

25 3B3) remainder means, operably coupled to the first intermediate EXCLUSIVE-OR circuit and to the second intermediate EXCLUSIVE-OR circuit, for storing 16 coefficients for highest order terms of an intermediate remainder and 16 coefficients for lowest order coefficients of a CRC remainder for the $(n+m)$ bit frame; and

30 3B4) a third intermediate EXCLUSIVE-OR circuit, operably coupled to the second EXCLUSIVE-OR circuit and to receive 16 lowest order coefficients of the second input of data for the plurality of K previously calculated CRC remainder coefficients of n bits, for performing bitwise modulo-two addition on the 16 coefficients for highest order
35 terms of an intermediate remainder and the 16 lowest order

coefficients of the second input of data to provide 16 highest order term coefficients that, together with the 16 lowest order coefficients (from the remainder means) of the CRC remainder coefficients for the $(n+m)$ bit frame, represent all
5 (32) CRC remainder coefficients for the $(n+m)$ bit frame.

4. The cyclic redundancy check (CRC) remainder coefficient generator of claim 1, wherein the generator is a component of
10 a communication network system that comprises at least a computer, a plurality of modems, and a plurality of terminals, and, where selected, a switched network.

5. A cyclic redundancy check (CRC) remainder coefficient generator in a communication network system comprising:
- 5A) first storage means for storing data for a plurality of m coefficients representing a last m bits of an $(n+m)$ bit frame (n, m are positive integers, $m > 1$; K is a positive integer representing a degree of a CRC generating polynomial);
- 5B) second storage means for storing data for a plurality of previously calculated CRC remainder coefficients of a precomputed CRC remainder for a first n bits of the frame;
- 5C) an EXCLUSIVE-OR circuit, operably coupled to the first storage means and to the second storage means, for substantially performing bitwise modulo-two addition on a preselected portion of first storage means data and on a preselected portion of second storage means data to provide a plurality of adjusted coefficients;
- 5D) CRC circuit conversion means, operably coupled at least to the EXCLUSIVE-OR circuit, comprising a plurality (more than one) of look-up tables and substantially at least a first EXCLUSIVE-OR circuit, for utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the $(n+m)$ bit frame.

6. The generator of claim 5 wherein at least one of 6A-6B:
 6A) wherein the CRC circuit combining means includes at least an EXCLUSIVE-OR circuit, and, where selected,

5 one of 6A1-6A3:

6A1) wherein the preselected portion of first input data that the EXCLUSIVE-OR circuit is coupled to receive comprises one of 6A1a-6A1b:

6A1a) where $m > K$,
 10 K most significant coefficients of m first input data; and

1 6A1b) where $1 < m \leq K$,
 all coefficients of the first input data,

6A2) wherein the preselected portion of second storage means data that the EXCLUSIVE-OR circuit is coupled to receive comprises one of 6A2a-6A2b:

6A2a) where $m \geq K$,
 all remainder coefficients of the second input data;
 and

20 6A2b) where $1 < m < K$,
 m highest-order remainder coefficients of the second input data,
 and

6A3) wherein the CRC circuit conversion means
 25 includes at least a remainder conversion unit that includes j memory look-up tables ($1 < j < m$) of size 2^b by K (where $jb = m$; $1 < b < m$), operably coupled to the CRC circuit combining means, for utilizing at least the plurality of adjusted coefficients to output all coefficients of the CRC intermediate remainder for the (n+m) bit frame, and wherein each
 30 coefficient has been precomputed and stored in one of the j memory look-up tables, wherein, where selected, the coefficients of the CRC intermediate remainder for the (n+m) bit frame are stored in memory registers for output to an
 35 EXCLUSIVE-OR circuit, and, where selected, one of 6A3a-6A3b:

- 6A3a) wherein one of: $b = 8$ and $b = 16$, and
6A3b) wherein the CRC circuit conversion means further includes a second EXCLUSIVE-OR circuit, operably coupled to j register means, each of which is operably coupled to a separate one of the j memory look-up tables of claim 12B such that the circuit receives j sets of K coefficients for a CRC intermediate remainder, for performing bitwise modulo-two addition ($j-1$ times) on said coefficients to provide the CRC remainder coefficients for the $(n+m)$ bit frame, and where selected, wherein $K = 32$, $m=16$, $j=2$, and $b=8$, and two 32 bit look-up tables are utilized in claim 16, wherein the second EXCLUSIVE-OR circuit includes 6A3b1-6A3b4:
- 6A3b1) a first intermediate EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for lowest order remainder terms from each of the two 32 bit look-up tables;
- 6A3b2) a second intermediate EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for highest order remainder terms from each of the two 32 bit look-up tables;
- 6A3b3) remainder means, operably coupled to the first intermediate EXCLUSIVE-OR circuit and to the second intermediate EXCLUSIVE-OR circuit, for storing 16 coefficients for highest order terms of an intermediate remainder and 16 lowest order coefficients of a CRC remainder for the $(n+m)$ bit frame; and
- 6A3b4) a third intermediate EXCLUSIVE-OR circuit, operably coupled to the second EXCLUSIVE-OR circuit and to receive 16 lowest order coefficients of the second input of data for the plurality of K previously calculated CRC remainder coefficients of n bits, for performing bitwise modulo-two addition on the 16 highest order coefficients of an intermediate remainder and the 16

lowest order coefficients of the second input of data to provide 16 highest order coefficients that, together with the 16 lowest order coefficients (from the remainder means) of the CRC remainder coefficients for the $(n+m)$ bit frame,

- 5 represent all (32) CRC remainder coefficients for the $(n+m)$ bit frame,
and

- 6B) wherein the communication network system comprises at least a computer, a plurality of modems, and a
10 plurality of terminals, and, where selected, a switched network.

7. A method for generating cyclic redundancy check (CRC) remainder coefficients in a CRC circuit having a first input of data for a plurality of m coefficients representing a last m bits of an $(n+m)$ bit frame (n, m are positive integers, $m > 1$; K is a positive integer representing a degree of a CRC generating polynomial) and a second input of data for a plurality of K previously calculated CRC remainder coefficients of a first n bits of the frame, comprising the steps of:
- 5 7A) substantially performing, in a CRC circuit
- 10 combining unit, bitwise modulo-two addition of a preselected portion of the first input data and a preselected portion of the second input data to provide a plurality of adjusted coefficients; and
- 15 7B) in a CRC circuit conversion unit comprising a plurality (more than one) of look-up tables and substantially at least a first EXCLUSIVE-OR circuit, utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the $(n+m)$ bit frame.

8. The method of claim 7 wherein the CRC circuit combining unit includes at least an EXCLUSIVE-OR circuit, and, where selected, at least one of 8A-8C:

5 8A) wherein the preselected portion of first input data that the EXCLUSIVE-OR circuit is coupled to receive comprises one of 8A1-8A2:

8A1) where $m > K$,
K most significant coefficients of m first input
10 data; and

8A2) where $1 < m \leq K$,
all coefficients of the first input data,

8B) wherein preselected portion of the second input data comprises one of 8B1-8B2:

15 8B1) where $m \geq K$,
all remainder coefficients of the second input data; and

8B2) where $1 < m < K$,
m highest-order remainder coefficients of the
20 second input data,

8C) wherein the CRC circuit conversion unit includes at least a remainder conversion unit that includes j memory look-up tables ($1 < j < m$) of size 2^b by K (where $jb = m$; $1 < b < m$), operably coupled to the CRC circuit combining means, for
25 utilizing at least the plurality of adjusted coefficients to output all coefficients of the CRC intermediate remainder for the (n+m) bit frame, and wherein each coefficient has been precomputed and stored in one of the j memory look-up tables, wherein, where selected, the coefficients of the CRC
30 intermediate remainder for the (n+m) bit frame are stored in memory registers for output to an EXCLUSIVE-OR circuit, and where selected, one of 8C1-8C2:

8C1) wherein one of: $b = 8$ and $b = 16$, and

8C2) wherein the CRC circuit conversion means of
35 claim 23 further includes a second EXCLUSIVE-OR circuit,

operably coupled to j register means, each of which is operably coupled to a separate one of the j memory look-up tables of claim 23 such that the circuit receives j sets of K coefficients of a CRC intermediate remainder, for performing
5 bitwise modulo-two addition ($j-1$ times) on said coefficients to provide the CRC remainder coefficients for the $(n+m)$ bit frame, and where selected,

wherein $K=32$, $m=16$, $j=2$, and $b=8$, and two 32 bit look-up tables are utilized in claim 25, wherein the
10 second EXCLUSIVE-OR circuit includes 8C2a-8C2d:

8C2a) a first intermediate EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for lowest order remainder terms from each of the two 32 bit look-up tables;

15 8C2b) a second intermediate EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for highest order remainder terms from each of the two 32 bit look-up tables;

8C2c) remainder means, operably coupled to
20 the first intermediate EXCLUSIVE-OR circuit and to the second intermediate EXCLUSIVE-OR circuit, for storing 16 coefficients for highest order remainder terms of an intermediate remainder and 16 lowest order coefficients of a CRC remainder for the $(n+m)$ bit frame; and

25 8C2d) a third intermediate EXCLUSIVE-OR circuit, operably coupled to the second EXCLUSIVE-OR circuit and to receive 16 lowest order coefficients of the second input of data for the plurality of K previously calculated CRC remainder coefficients of n bits, for performing bitwise
30 modulo-two addition on the 16 coefficients for highest order terms of an intermediate remainder and the 16 lowest order coefficients of the second input of data to provide 16 highest order coefficients that, together with the 16 lowest order coefficients (from the remainder means) of the CRC remainder

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coefficients for the $(n+m)$ bit frame, represent all (32) CRC remainder coefficients for the $(n+m)$ bit frame.

9. A method for generating cyclic redundancy check (CRC) remainder coefficients in a CRC circuit in a communication network system, comprising the steps of:

- 5 9A) storing data for a plurality of m coefficients representing a last m bits of an $(n+m)$ bit frame (n , m are positive integers, $m > 1$; K is a positive integer representing a degree of a CRC generating polynomial) in a first memory register unit;
- 10 9B) storing data for a plurality of K previously calculated cyclic division polynomial remainder coefficients of a remaining portion of a first n bits of the frame in a second memory register unit;
- 15 9C) in a CRC circuit combining unit, substantially performing bitwise modulo-two addition on data from a preselected portion of the first memory register storage unit and on a preselected portion of the data from the second memory register unit to provide a plurality of adjusted coefficients;
- 20 9D) in a CRC circuit conversion unit comprising a plurality (more than one) of look-up tables and substantially at least a first EXCLUSIVE-OR circuit, utilizing at least the plurality of adjusted coefficients to provide a plurality of CRC remainder coefficients for the $(n+m)$ bit frame.

10. The method of claim 9 wherein at least one of 10A-10C:
 10A) the CRC circuit combining unit includes at least an
 EXCLUSIVE-OR circuit, and where selected at least one of

5 10A1-10A3:

10A1) wherein the preselected portion of first
 input data that the EXCLUSIVE-OR circuit is coupled to receive
 comprises one of 10A1a-10A1b:

10A1a) where $m > K$,
 10 K most significant coefficients of m first input
 data; and

10A1b) where $1 < m \leq K$,
 all coefficients of the first input data,
 10A2) wherein the preselected portion of the data
 15 from the second memory register unit that the EXCLUSIVE-OR
 circuit is coupled to receive comprises one of 10A2a-10A2b:

10A2a) where $m \geq K$,
 all remainder coefficients of the second input data;
 and

20 10A2b) where $1 < m < K$,
 m highest-order remainder coefficients of the
 second input data,

10A3) wherein the CRC circuit conversion unit
 includes at least a remainder conversion unit that includes j
 25 memory look-up tables ($1 < j < m$) of size 2^b by K (where $jb =$
 m ; $1 < b < m$), operably coupled to the CRC circuit combining
 means, for utilizing at least the plurality of adjusted
 coefficients to output all coefficients of the CRC intermediate
 remainder for the (n+m) bit frame, and wherein each
 30 coefficient has been precomputed and stored in one of the j
 memory look-up tables, wherein, where selected, the
 coefficients of the CRC intermediate remainder for the (n+m)
 bit frame are stored in memory registers for output to an
 EXCLUSIVE-OR circuit, and where selected, at least one of

35 10A3a-10A3b:

- 10A3a) wherein one of: $b = 8$ and $b = 16$, and
10A3b) wherein the CRC circuit conversion means of claim 31 further includes a second EXCLUSIVE-OR circuit, operably coupled to j register means, each of which is
5 operably coupled to a separate one of the j memory look-up tables of claim 31 such that the circuit receives j sets of K coefficients a CRC intermediate remainder, for performing bitwise modulo-two addition ($j-1$ times) on said coefficients to provide the CRC remainder coefficients for the $(n+m)$ bit
10 frame, and where selected,
wherein $K = 32$, $m = 16$, $j = 2$, and $b = 8$, and two 32 bit look-up tables are utilized in claim 33, wherein the second EXCLUSIVE-OR circuit includes 103b1-103b4:
103b1) a first intermediate
15 EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for lowest order remainder terms from each of the two 32 bit look-up tables;
103b2) a second intermediate
20 EXCLUSIVE-OR circuit, operably coupled to receive and process by bitwise modulo-two addition, 16 coefficients for highest order remainder terms from each of the two 32 bit look-up tables;
103b3) remainder means, operably
25 coupled to the first intermediate EXCLUSIVE-OR circuit and to the second intermediate EXCLUSIVE-OR circuit, for storing 16 coefficients for highest order remainder terms of an intermediate remainder and 16 lowest order coefficients of a CRC remainder for the $(n+m)$ bit frame; and
103b4) a third intermediate
30 EXCLUSIVE-OR circuit, operably coupled to the second EXCLUSIVE-OR circuit and to receive 16 lowest order coefficients of the second input of data for the plurality of K previously calculated CRC remainder coefficients of n bits,
35 for performing bitwise modulo-two addition on the 16

coefficients for highest order remainder terms of an intermediate remainder and the 16 lowest order coefficients of the second input of data to provide 16 highest order coefficients that, together with the 16 lowest order coefficients (from the remainder means) of the CRC remainder coefficients for the $(n+m)$ bit frame, represent all (32) CRC remainder coefficients for the $(n+m)$ bit frame,

10B) wherein the communication network system comprises at least a computer, a plurality of modems, and a plurality of terminals, and, where selected, a switched network, and where selected,

wherein the communication network system is one of 10B1-10B3:

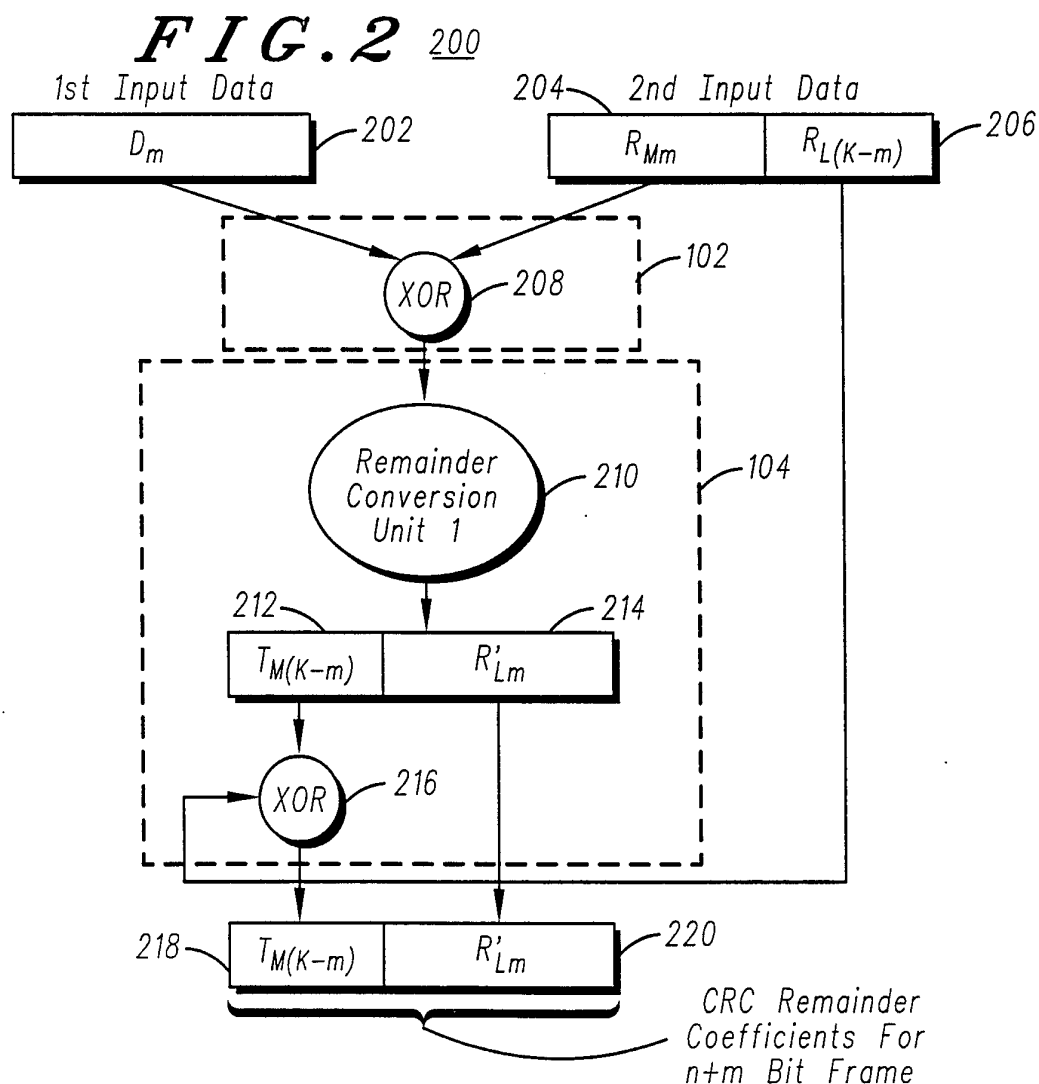
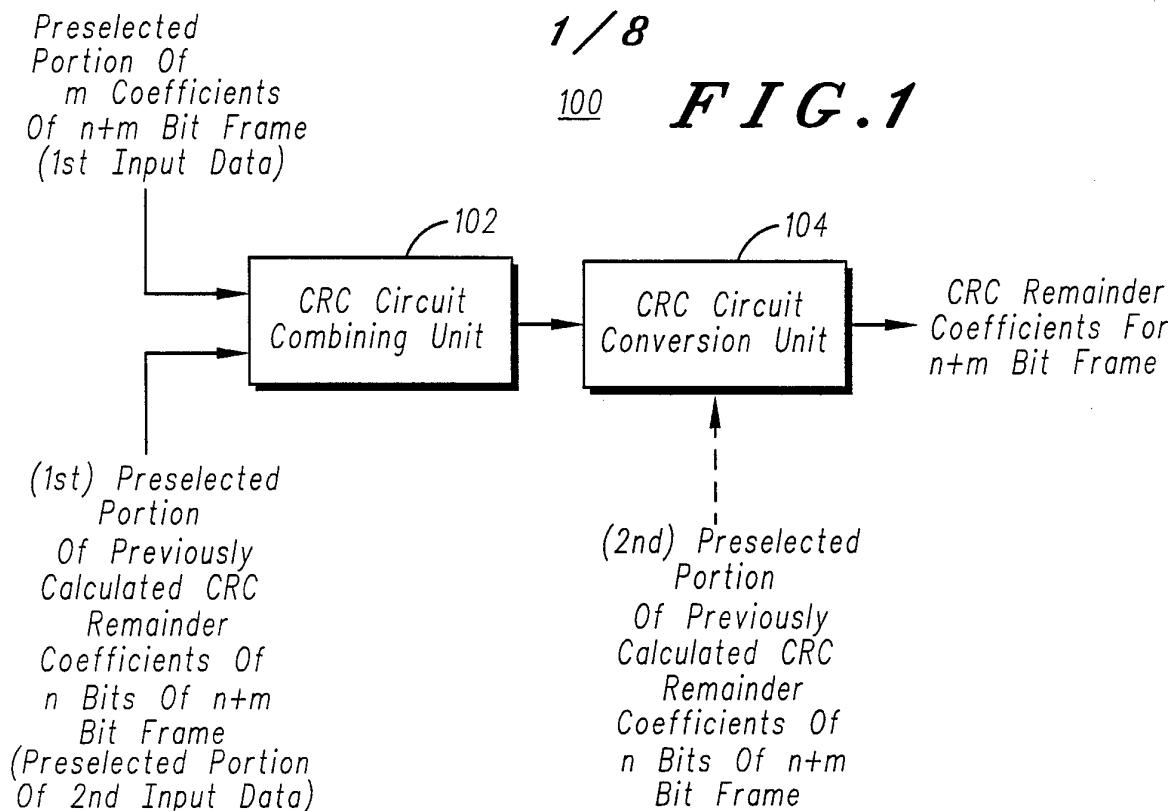
10B1) a point-to-point communication network line structure system;

10B2) a multipoint communication network line structure system; and

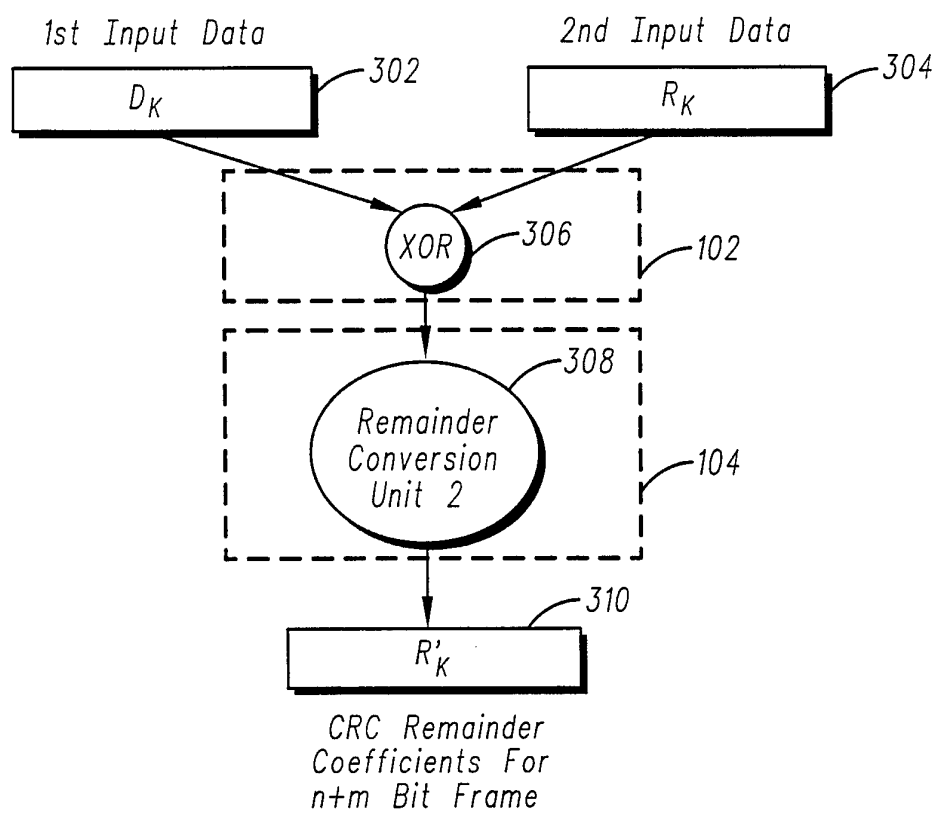
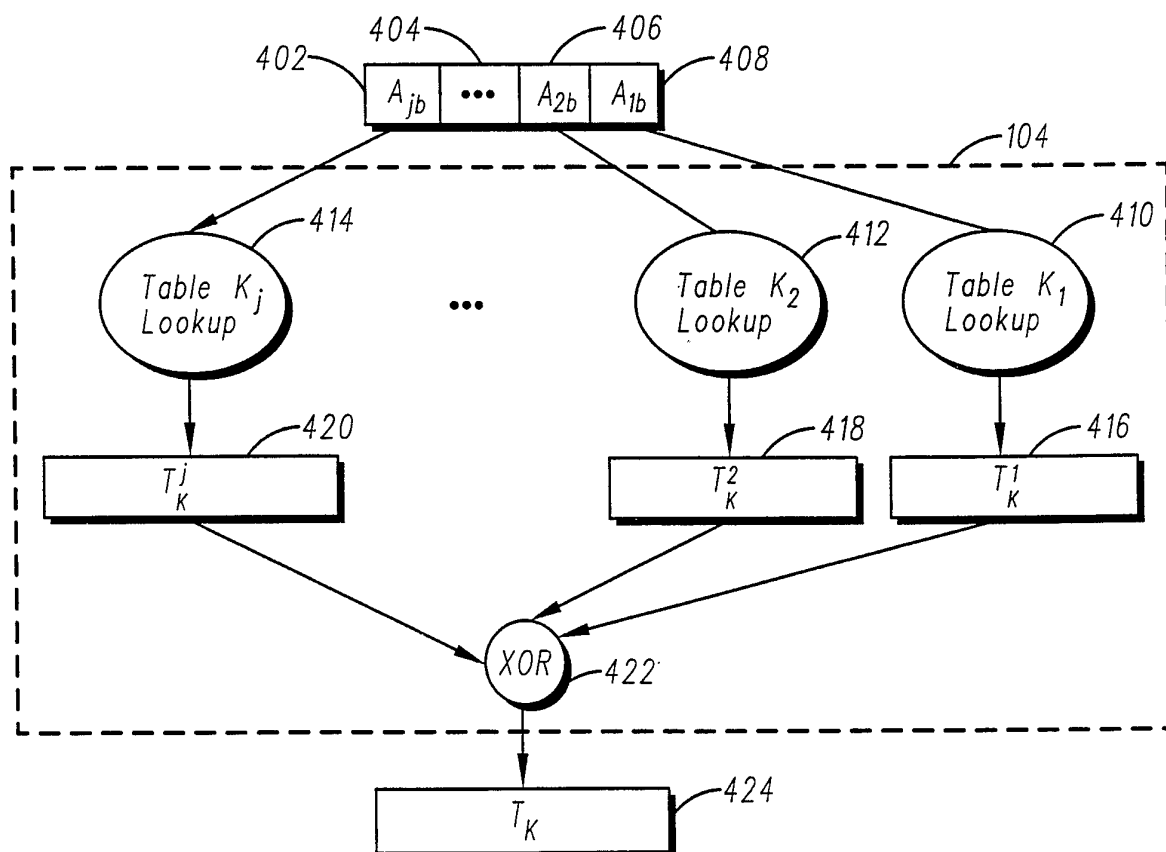
10B3) a mixed communication network line structure system,

20 and

10C) wherein the steps of the method for generating the cyclic redundancy check (CRC) remainder coefficients in the CRC circuit are implemented in a digital signal processor.



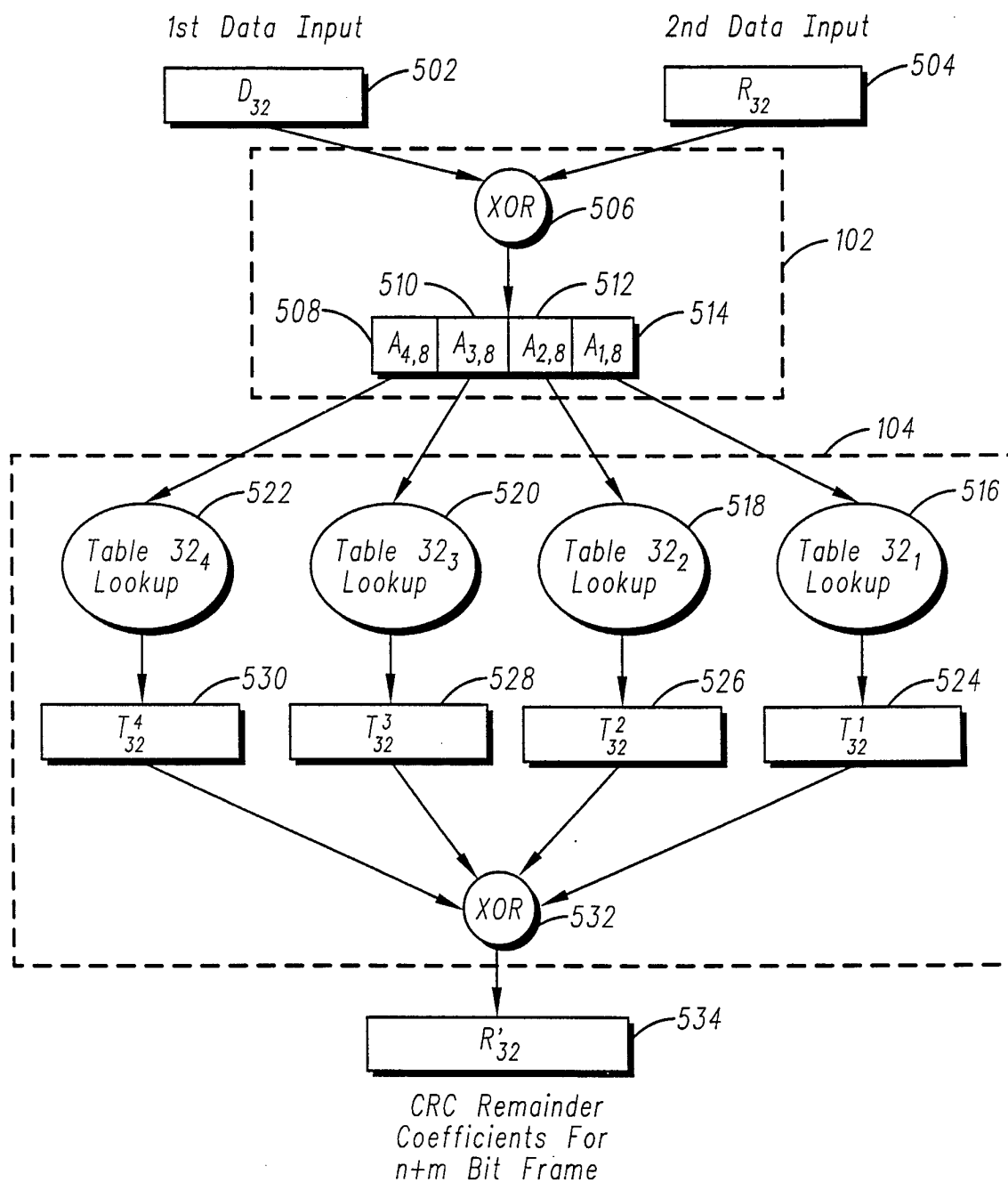
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FIG. 3300**FIG. 4**400

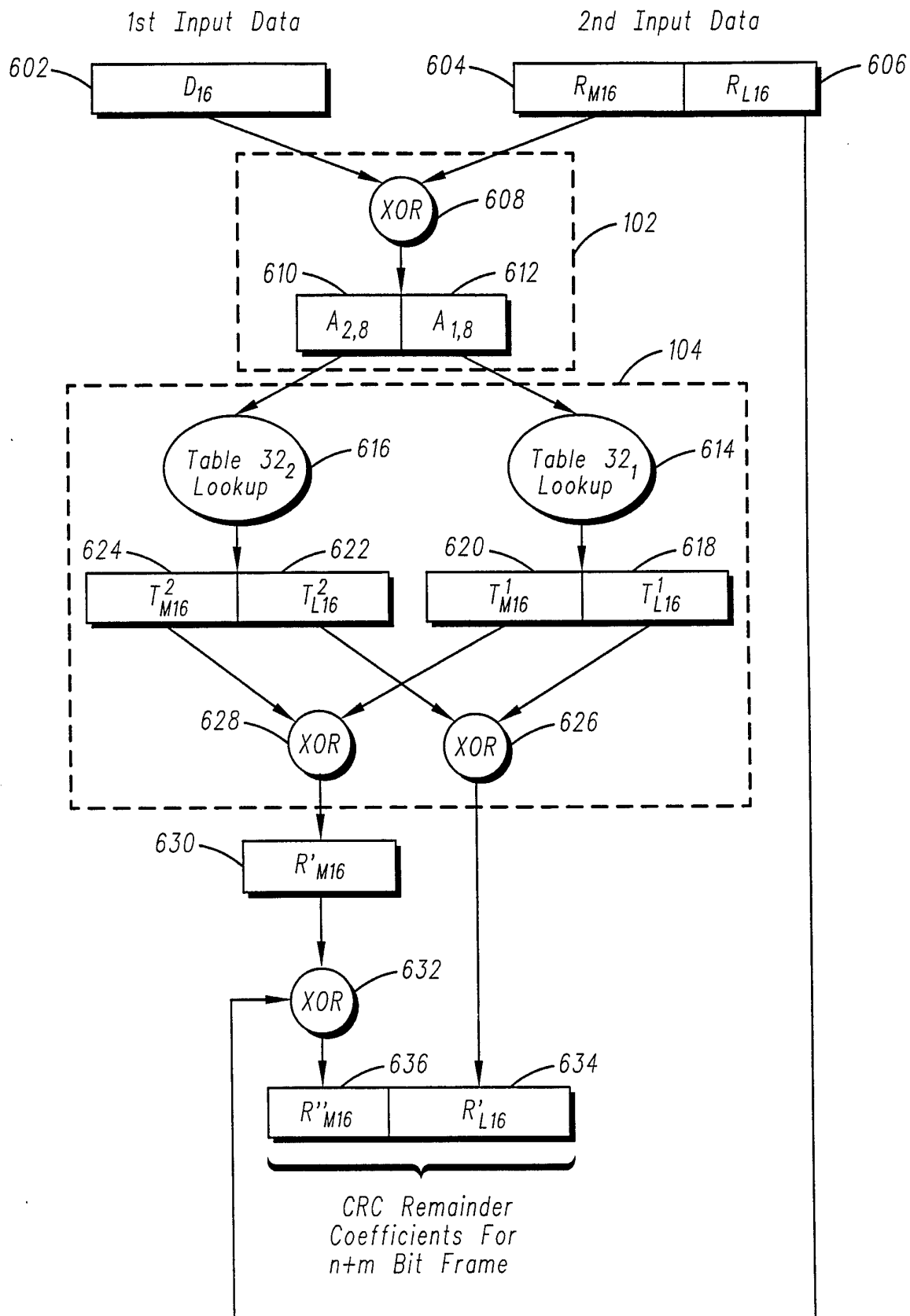
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FIG. 5

500

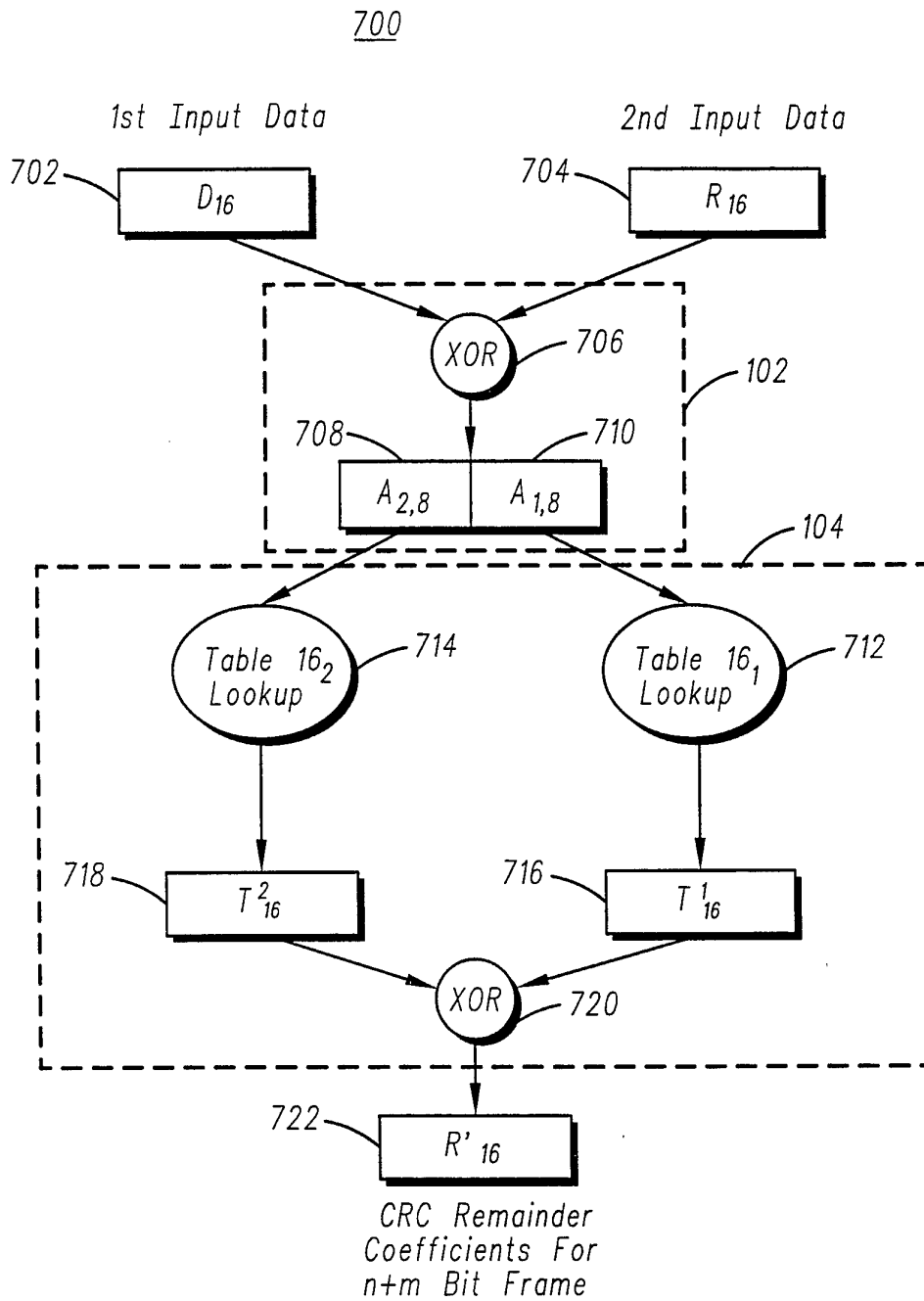


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FIG. 6 600

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FIG. 7



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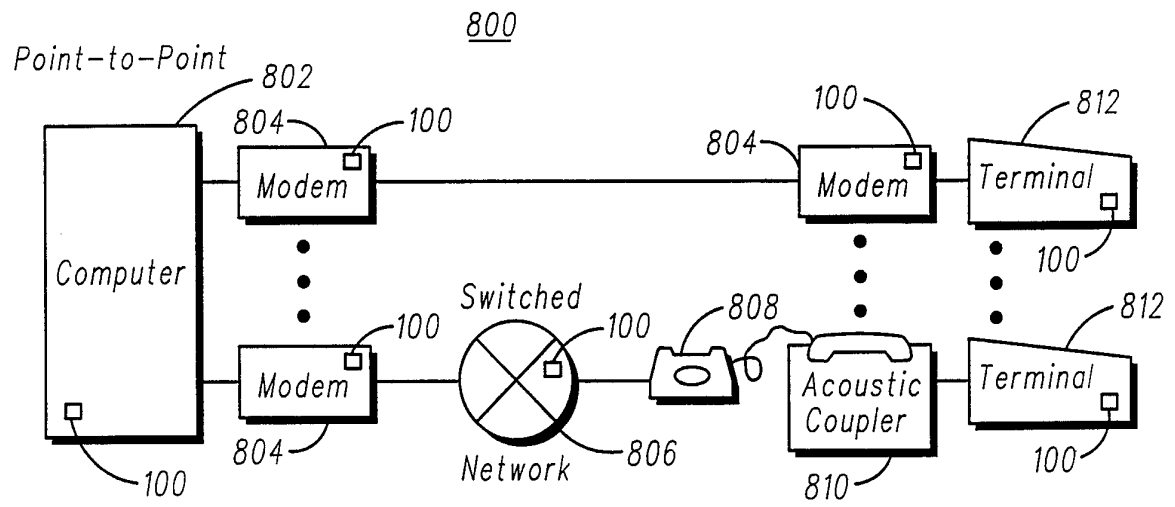
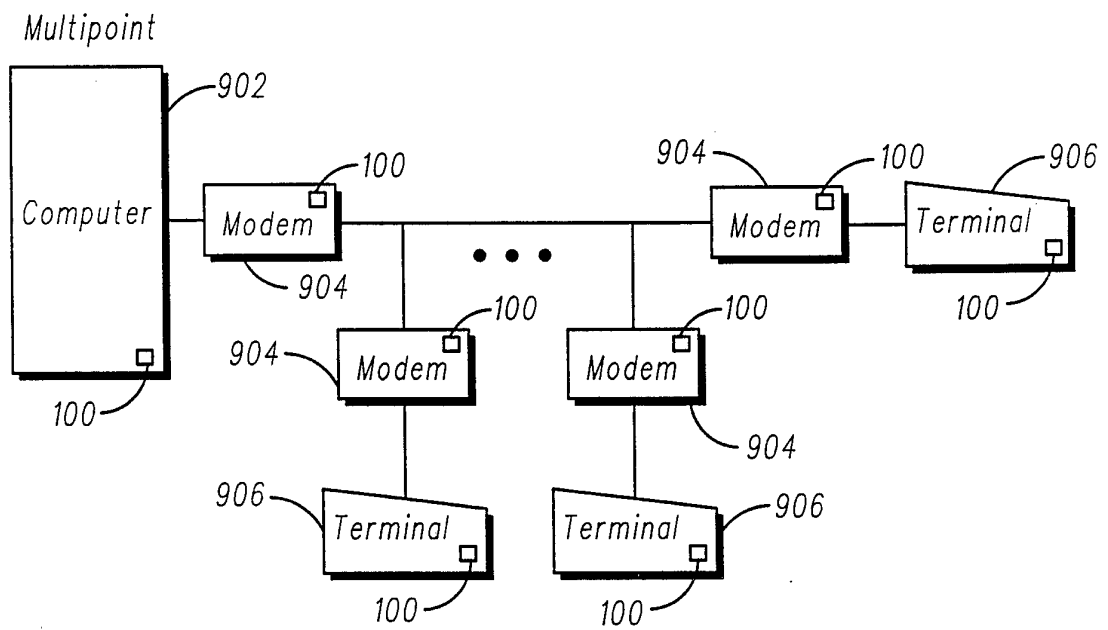
FIG. 8**FIG. 9**900

FIG. 10 1000 7/8

1000

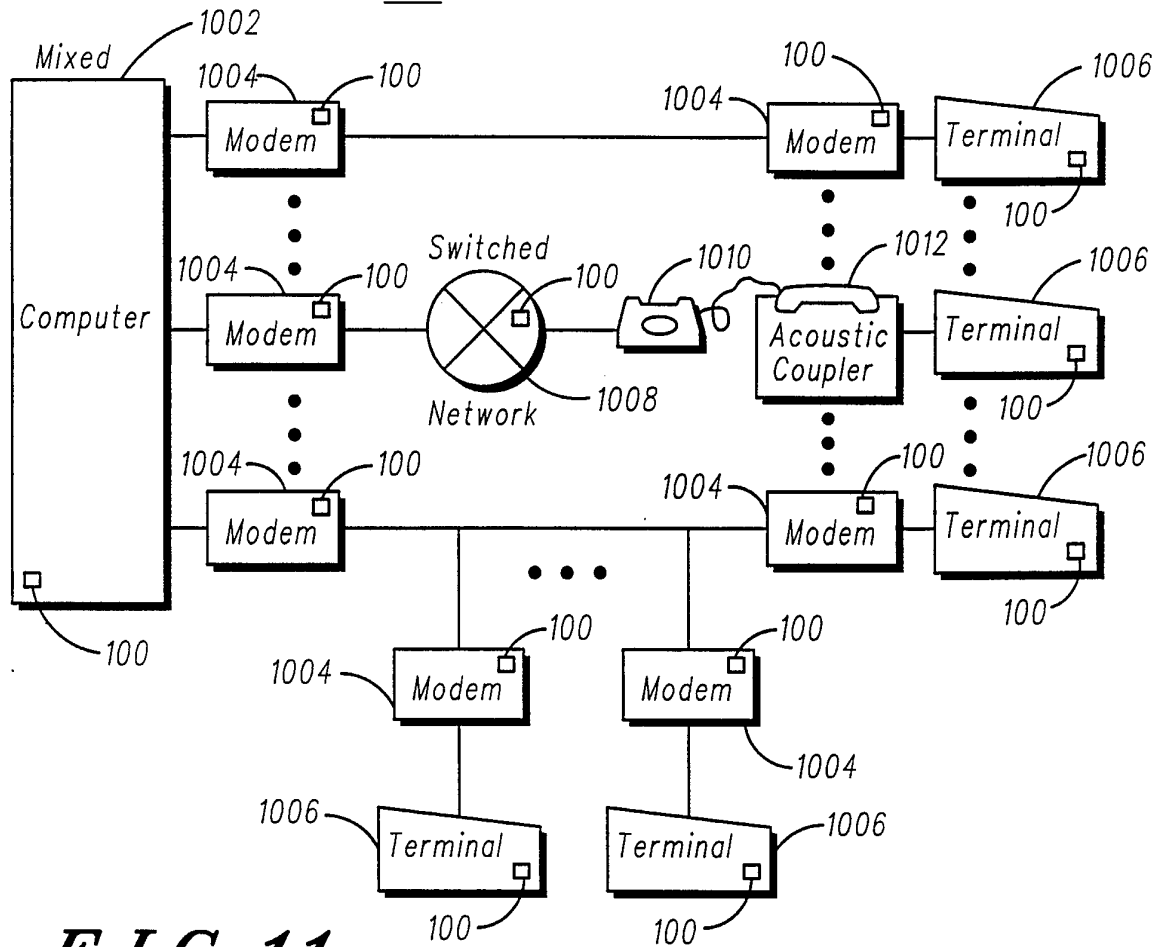


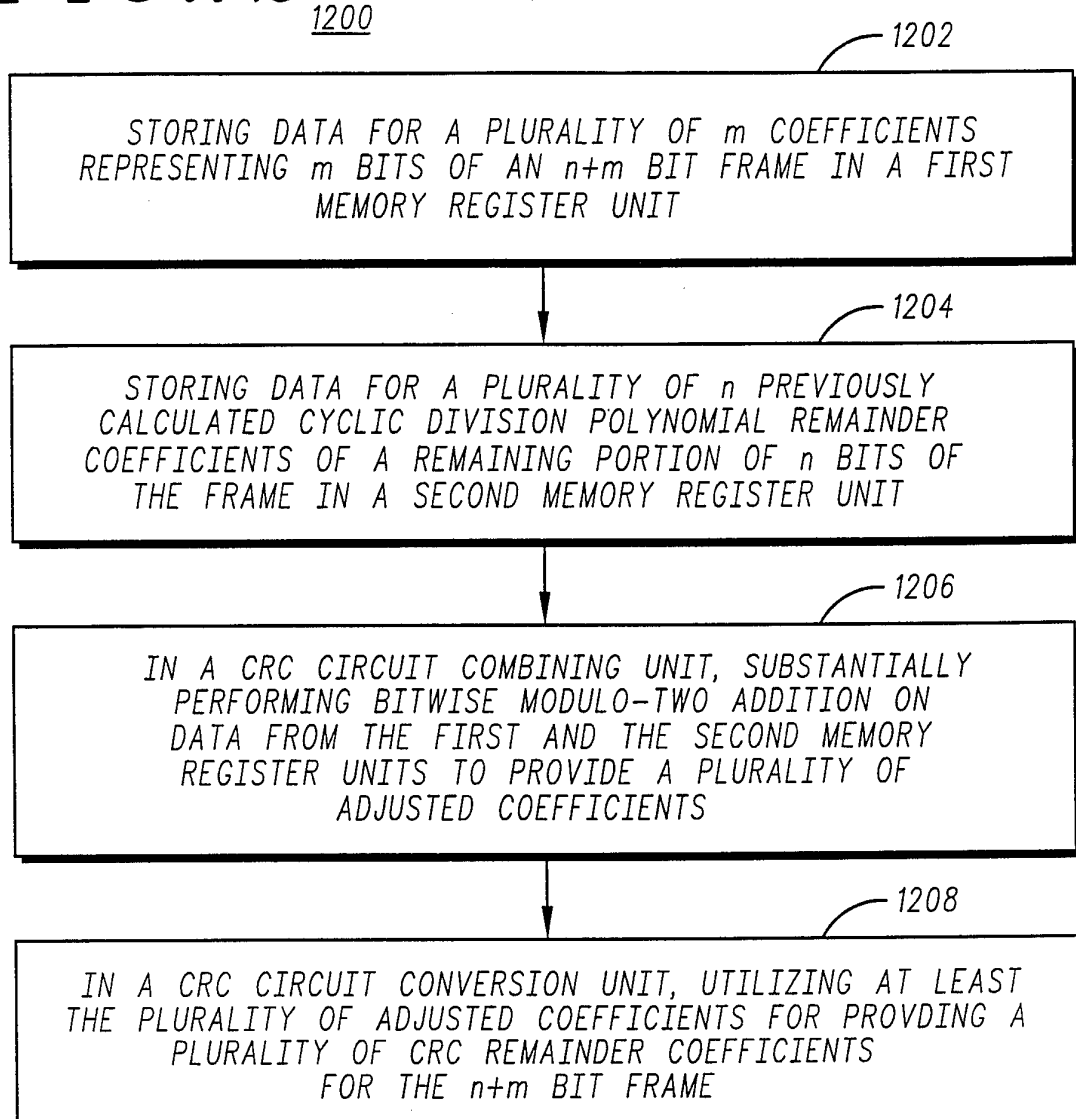
FIG. 11

1100

IN A CRC CIRCUIT COMBINING UNIT, PERFORMING
BITWISE MODULO-TWO ADDITION ON:
A PLURALITY OF m COEFFICIENTS REPRESENTING
 m BITS OF AN $n+m$ BIT FRAME (n, m POSITIVE
INTEGERS; $m > 1$; K IS A DEGREE OF A CRC
GENERATING POLYNOMIAL (1st ELECTRICAL INPUT
DATA) AND
A PLURALITY OF PREVIOUSLY CALCULATED CRC
REMAINDER COEFFICIENTS OF A FIRST n BITS OF THE FRAME,
TO PROVIDE A PLURALITY OF ADJUSTED COEFFICIENTS

IN A CRC CIRCUIT CONVERSION UNIT, UTILIZING AT
LEAST THE PLURALITY OF ADJUSTED COEFFICIENTS TO
PROVIDE A PLURALITY OF CRC REMAINDER
COEFFICIENTS FOR THE
 $n+m$ BIT FRAME

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FIG. 12

INTERNATIONAL SEARCH REPORT

Int. onal application No.

PCT/US93/11790

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H 03 M 13/00

US CL :371/37.6, 37.8, 53

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 364/739, 746.1, 764, 766; 371/37.6, 37.8, 53

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,473,902 (CHEN) 25 September 1984, column 1 lines 7-12, column 2 lines 44-61, column 3 lines 16-26 and lines 42-49, figures 1-3.	1-10
A	Electronics, 27 March 1980, A. J. Weissberger, "Control Chip Handles Error Checking and Character-Based Protocols Easily", pages 151-155, see especially page 151 lines 1-14, page 155 inset lines 13-16, figure 1.	1-10
A	IEEE Micro, August 1988, T.V. Ramabadran et al., "A Tutorial on CRC Computations", pages 62-74, see especially the sections entitled "Table lookup algorithm" and "Reduced table lookup algorithm" on pages 67-68.	1-10

☐ Further documents are listed in the continuation of Box C
 ☐ See patent family annex.

* Special categories of cited documents:	* I* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
* A* document defining the general state of the art which is not considered to be part of particular relevance	* X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
* E* earlier document published on or after the international filing date	* Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
* L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	* Z* document member of the same patent family
* O* document referring to an oral disclosure, use, exhibition or other means	
* P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

27 January 1994

Date of mailing of the international search report

APR 13 1994

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