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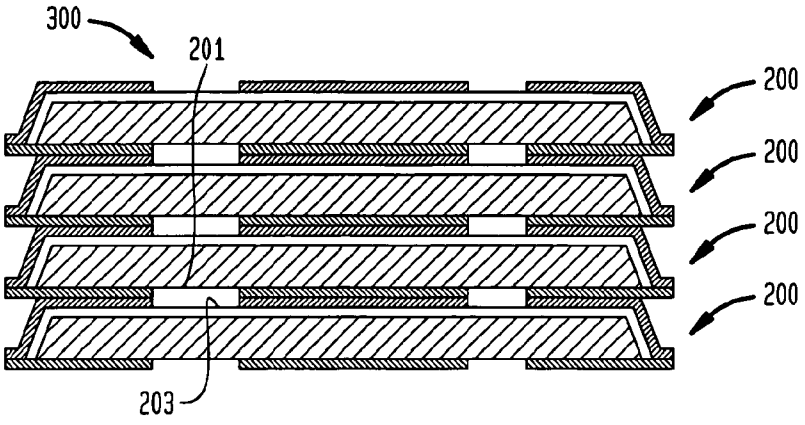
(54) **Title**: STACKING OF WAFER-LEVEL CHIP SCALE PACKAGES HAVING EDGE CONTACTS

FIG. 3



(57) **Abstract**: A microelectronic assembly (300) can include a' first microelectronic device (200) and a second microelectronic device (200). Each microelectronic device has a die structure including at least one semiconductor die (104) and each of the microelectronic devices has a first surface (201), a second surface (203) remote from the first surface and at least one edge surface (134) extending at angles other than a right angle away from the first and second surfaces (201, 203). At least one electrically conductive element (which may include portions 110, 124, 122, 126) extends along the first surface onto at least one of the edge surfaces and onto the second surface (203). At least one conductive element of the first microelectronic device can be conductively bonded to the at least one conductive element of the second microelectronic device to provide an electrically conductive path therebetween.

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STACKING OF WAFER-LEVEL CHIP SCALE PACKAGES HAVING EDGE CONTACTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the filing date of United States Provisional Patent Application No. 61/061,953 filed June 16, 2008, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to packaged microelectronic elements and methods of fabricating them, and more particularly, to a stackable packaged microelectronic die assembly.

[0003] Microelectronic chips are typically flat bodies with oppositely facing, generally planar front and rear surfaces and with edges extending between these surfaces. Chips generally have contacts, sometimes also referred to as pads or bond pads, on the front surface which are electrically connected to the circuits within the chip. Chips are typically packaged by enclosing them with a suitable material to form microelectronic packages having terminals that are electrically connected to the chip contacts. The package may then be connected to test equipment to determine whether the packaged device conforms to a desired performance standard. Once tested, the package may be connected to a larger circuit, e.g., a circuit in an electronic product such as a computer or a cell phone, by connecting the package terminals to matching lands on a printed circuit board (PCB) by a suitable connection method such as soldering.

[0004] Microelectronic packages may be fabricated at the wafer level; that is, the enclosure, terminations and other features that constitute the package, are fabricated while the chips, or die, are still in a wafer form. After the die have been formed, the wafer is subject to a number of additional process steps to form the package structure on the wafer, and the wafer is then diced to free the individually packaged die. Wafer level processing may be a preferred fabrication method because it may provide a cost savings advantage, and because

the footprint of each die package may be made identical, or nearly identical, to the size of the die itself, resulting in very efficient utilization of area on the printed circuit board to which the packaged die is attached. A die packaged in this manner is commonly referred to as wafer-level chip scale package or wafer-level chip sized package (WLCSP).

[0005] In order to save additional space on the substrate to which a packaged die is mounted, multiple chips may be combined in a single package by vertically stacking them. Each die in the stack must typically provide an electrical connection mechanism to either one or more other die in the stack, or to the substrate on which the stack is mounted, or to both. This allows the vertically stacked multiple die package to occupy a surface area on a substrate that is less than the total surface area of all the chips in the package added together. Because there are in general far more electrical connections when using a die stack than when packaging a single die, the electrical connections between the various dies of the stack must be extremely robust and reliable.

BRIEF SUMMARY OF THE INVENTION

[0006] A microelectronic assembly can include a first microelectronic device and a second microelectronic device. Each microelectronic device has a die structure including at least one semiconductor die and each of the microelectronic devices has a first surface, a second surface remote from the first surface and at least one edge surface extending at angles other than a right angle away from the first and second surfaces. At least one electrically conductive element extends along the first surface onto at least one of the edge surfaces and onto the second surface. At least one conductive element of the first microelectronic device can be conductively bonded to the at least one conductive element of the second microelectronic device to provide an electrically conductive path therebetween.

[0007] In accordance with one embodiment, the electrically conductive elements of each microelectronic device can include

first elements formed by plating onto one of the first and second surfaces and second elements formed by plating onto another one of the first and second surfaces and the at least one edge surface. In one embodiment, the second elements can be plated onto portions of the first elements. For example, the second elements extend along the portions of the first elements on which the second elements are plated.

[0008] The second elements can extend along edges of the first elements so as to be conductively joined with the first elements at such edges.

[0009] The conductive elements of the first and second microelectronic devices can be bonded using a fusible metal or using conductive paste, for example. In one embodiment, one of the first and second surfaces of the first microelectronic device can confront one of the first and second surfaces of the second microelectronic device and portions of the conductive elements exposed at the confronting surfaces are bonded together. For example, the conductive elements may include conductive pads exposed at at least one of the first or second surfaces of each microelectronic device and the conductive pads can be bonded together.

[0010] The conductive elements may include traces and conductive pads, wherein the at least one conductive pad is disposed a spaced distance from the at least one edge surface. In a particular embodiment, a conductive element of each microelectronic device includes a conductive pad which is proximate the at least one edge surface or which can extend to the at least one edge surface.

[0011] In a particular embodiment, one or more of the microelectronic devices can include a plurality of dies. In such case, the bond pad-bearing surfaces of at least two of the semiconductor dies included in the at least one microelectronic device may face in the same direction, or they may face in different directions.

[0012] The at least one edge surface along which the at least one conductive element extends can be disposed at an

angle of between 50 degrees and 89 degrees with respect to at least one of the first and second surfaces.

[0013] In the microelectronic assembly, the first and second microelectronic devices can be stacked in a vertical direction and the at least one edge surfaces of the first and second microelectronic devices can be offset from each other.

[0014] The first surfaces of the first and second microelectronic devices can extend in lateral directions and have first dimensions in the lateral directions. In one embodiment, the lateral dimensions of the first surfaces of the first and second microelectronic devices can be different.

[0015] In one embodiment, a microelectronic assembly is provided which includes first and second microelectronic devices. Each of the microelectronic devices can include a die structure having at least one semiconductor die. Each of the microelectronic devices can have a first surface, a second surface remote from the first surface and at least one edge surface extending away from the first surface. An electrically conductive element can extend along the first surface and onto at least one of the edge surfaces. The at least one conductive element of the first microelectronic device can be conductively bonded to the at least one conductive element of the second microelectronic device to provide an electrically conductive path therebetween.

[0016] In one embodiment, the at least one edge surface extends at an angle other than a right angle away from the first and second surfaces. Edge portions of the electrically conductive elements exposed at the at least one edge surfaces can be conductively bonded to provide the electrically conductive path. Such edge portions can be bonded using a fusible metal or can be bonded using conductive paste.

[0017] A method of fabricating a stacked microelectronic assembly is provided according to one embodiment. In such embodiment a major surface of a first microelectronic device can be arranged to confront a major surface of a second microelectronic device. An electrically conductive element

exposed at the major surface of the first microelectronic device can be conductively bonded with an electrically conductive element exposed at the major surface of the second microelectronic device to provide an electrically conductive path therebetween. Each microelectronic device can include a die structure including at least one semiconductor die and each of the microelectronic devices can have a first major surface, a second major surface remote from the first surface, at least one edge surface and at least one electrically conductive element extending along the first surface onto at least one of the edge surfaces and onto the second major surface.

[0018] In accordance with one embodiment, a stacked microelectronic assembly can be fabricated. A stack can be formed which includes a first microelectronic device stacked with a second microelectronic device. Each of the microelectronic devices can include a die structure including at least one semiconductor die. Each of the microelectronic devices can have a first surface, a second surface remote from the first surface and at least one edge surface extending away from the first surface. At least one electrically conductive element can extend along the first surface and onto at least one of the edge surfaces. Portions of the conductive elements exposed at the edge surfaces can be conductively bonded to provide an electrically conductive path therebetween.

[0019] In such embodiment, a first microelectronic device can be disposed above the second microelectronic device, and the step of bonding can be performed by heating a fusible metal proximate the conductive element exposed at the at least one edge surface of the first microelectronic device. In such way, the fusible metal may flow onto the conductive element exposed at the at least one edge surface of the second microelectronic device. In such embodiment, the fusible metal may bridge a gap between the conductive elements of the first and second microelectronic devices.

[0020] In such embodiment, the first microelectronic device can be disposed above the second microelectronic device and the

step of bonding can be performed by dispensing a flowable conductive material onto the conductive element exposed at the at least one edge surface of the first microelectronic device. The conductive material may then flow onto the conductive element exposed at the at least one edge surface of the second microelectronic device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The devices and methods described herein are best understood when the following description of several illustrated embodiments is read in connection with the accompanying drawings wherein the same reference numbers are used throughout the drawings to refer to the same or like parts. The drawings are not necessarily to scale; emphasis has instead been placed upon illustrating the principles of the described embodiments.

[0022] FIG. 1A displays a perspective view of a wafer containing a number of microelectronic chips;

[0023] FIG. 1B shows a cross-section of a portion of the wafer.

[0024] FIG. 1C illustrates a perspective view of a single die of the wafer that has a first metallization layer disposed over the bond pads, in accordance with one embodiment.

[0025] FIGS. 1D-1I show a cross-section of a portion of the wafer similar to that of FIG. 1B undergoing additional processing steps.

[0026] FIG. 2A shows a cross-section view of a separated microelectronic device according to one embodiment.

[0027] FIGS. 2B and 2C show a detail view of variants of join structures of FIG. 2A, in accordance with one embodiment.

[0028] FIG. 2D is a perspective view showing the microelectronic device of FIG. 2A.

[0029] FIG. 2E outlines a process flow used to create a finished microelectronic device according to one embodiment.

[0030] FIG. 3 shows a cross-section view of several dies forming a die stack structure, in accordance with one embodiment.

[0031] FIGS. 4A and 4B show cross-section views of two variants of joining methods to form the device of FIG. 3, in accordance with one embodiment.

[0032] FIG. 5A shows a cross-section view of a die stack structure comprising heterogeneous elements, in accordance with one embodiment.

[0033] FIG. 5B shows a cross-section view of a die stack structure comprising heterogeneous elements with dies of various sizes, in accordance with one embodiment.

[0034] FIG. 6A illustrates a perspective view of a single die of the wafer that has a first metallization layer disposed over the bond pads, in accordance with one embodiment.

[0035] FIG. 6B shows perspective view of a single die of a wafer with bond pads extended to the edge, in accordance with one embodiment.

[0036] FIG. 6C-6I show a cross-section view of a portion of the wafer with dies similar to that of FIG. 6A undergoing additional processing steps, in accordance with one embodiment.

[0037] FIG. 7 shows a cross-section view of a die stack structure formed according to one embodiment.

[0038] FIG. 8A shows a cross-section view of a die structure according to one embodiment.

[0039] FIG. 8B shows a cross-section view of a die stack with additional reflowable material added, in accordance with one embodiment.

[0040] FIG. 8C shows a cross-section view of a die stack structure according to one embodiment.

[0041] FIG. 9 outlines a process flow used to create a finished device die according to one embodiment.

[0042] FIG. 10A-10E show a cross-section view of process steps leading to the creation of a die stack comprising two or more dies, in accordance with one embodiment.

[0043] FIG. 10F shows a cross-section view of a die structure comprising two or more dies, in accordance with one embodiment.

[0044] FIG. 10G shows a cross-section view of a die stack structure comprising multiple die structures of FIG. 10F, in accordance with one embodiment.

[0045] FIG. 10H shows a cross-section view of a variant of a portion of the process flow starting in FIG. 10A, in accordance with one embodiment.

[0046] FIG. 11A-11E show a cross-section view of process steps leading to the creation of a die stack, in accordance with one embodiment.

[0047] FIG. 11F shows a cross-section view of a die structure comprising two or more dies, in accordance with one embodiment.

[0048] FIG. 11G shows a cross-section view of a die stack structure comprising multiple die structures of FIG. 11F, in accordance with one embodiment.

DETAILED DESCRIPTION

[0049] As used in this disclosure, a statement that an electrically conductive structure is "exposed at" a surface of a dielectric structure indicates that the electrically conductive structure is available for contact with a theoretical point moving in a direction perpendicular to the surface of the dielectric structure toward the surface of the dielectric structure from outside the dielectric structure. Thus, a terminal or other conductive structure which is exposed at a surface of a dielectric structure may project from such surface; may be flush with such surface; or may be recessed relative to such surface and exposed through a hole or depression in the dielectric.

[0050] FIG. 1A displays a perspective view of a wafer 100 containing a number of microelectronic chips. The wafer substrate 102 is commonly a semiconductor material such as silicon but may be made of other materials or be a composite of

some type. The wafer is divided up into individual dies 104 that comprise part, or all, of the working portion of a microelectronic chip; after additional processing the dies are separated from one another at the dotted lines 103. Each chip may have one or more functions and is created on or under the surface of the substrate using techniques well known to those with skill in semiconductor processing. These examples are not intended to be limiting-the processed wafer 100 could represent any number of types of devices, including memory, processor, image sensor, or other possibilities. Bond pads 106 are electrically connected to circuitry on or in the substrate. FIG. 1B shows a cross-section of a portion of a wafer, such as wafer 100 illustrated in FIG. 1A. For clarity, the bond pads 106 are exposed at a "front" or contact-bearing surface 101 of the substrate 102. The bond pads 106 may protrude above the surface 101, may be flush with the surface or may be recessed with respect to the surface. Dotted lines 103 indicate the dicing lanes between each die. Although the wafer as described herein may be a semiconductor material with working portions formed therein, in other cases the wafer may be a reconstituted wafer wherein the wafer is created from a number of components placed to form individual dies and held together by an adhesive, for example an epoxy. Alternatively, instead of a wafer 100, the structure may be a plurality of dies which are connected together at edges of the dies shown at dotted lines 103, which structure may be rectangular in form, such as a panel. The edges of the dies may meet at the dotted lines and the semiconductor material may be a continuous uncut structure, or the edges of the dies may be spaced from each other and joined in a reconstituted structure with an adhesive.

[0051] FIG. 1C-1I show steps for processing the wafer in accordance with one embodiment. Note that the steps illustrated may be performed in the order described, or, alternatively, in a different order. In some implementations, two or more of the described steps may be combined into a single step. In other implementations, a described step may be excluded completely

from the process. In yet other variants, additional processing steps may be required.

[0052] FIG. 1C is a perspective view of a single die 108 of the wafer 100 that has a first metallization layer 110 contacting the bond pads. A metal film can be deposited on a surface 101 of the wafer in some manner such as deposition or plating, and then the film can be patterned to form the metallization layer. In a particular embodiment, a seed layer can be formed on the surface, then patterned and subsequently plated to form the metallization layer. Part of the metallization layer is configured to create connection pads 112 that will be used to connect stacked components. The metallization layer may be configured to be a redistribution layer. Additionally, portions of the metallization layer extend as conductive, e.g., metal traces from the bond pads 106 to the edge of the die. FIG. 1D is a cross-section view of a wafer, such as wafer 100 shown in FIG. 1A, but with the metallization layer 110 added. For simplicity, this figure shows only one connection pad area 112 in contact with each set of bond pads 106 on each die. Note that a particular cross-section may include one or more separate connection areas depending on the desired layout.

[0053] FIG. 1E shows a next step in processing the wafer. In FIG. 1E, the assembly displayed in FIG. 1D is flipped so that the metallization layer 110 is facing down and attached to a separate temporary carrier substrate 114. The temporary substrate 114 is held to the primary substrate 102 using an adhesive layer 116. Thereafter, the primary substrate 102 can be thinned using techniques such as grinding or polishing down to a desired thickness, the result of which is displayed as structure 117 in FIG. 1F.

[0054] A subsequent step in processing the wafer is shown in FIG. 1G. In FIG. 1G, a channel 118 is cut or etched into the substrate 102 to open up a hole to expose a portion of the first metallization layer 110. In one embodiment, such etch can be performed by a process controlled to stop on an

intermediate layer between the semiconductor substrate and the metallization layer, and then proceeding to remove a portion of the intermediate layer to expose the metallization layer 110. The intermediate layer can be a dielectric layer. The channels 118 can be trenches that serve to expose metallization layer portions connected to a plurality of bond pads of one or more dies. FIG. 1H shows the step of forming a dielectric layer 120 on the surface of the substrate 102. The dielectric layer, among other purposes, serves to protect the newly exposed surface of the substrate 102. The dielectric layer insulates the substrate 102 from subsequently formed conductive structure. The bottom of the channels 118 is either left clear by a patterned deposition of the passivation layer, or material left covering the metal traces of the first metallization layer might be exposed in a further step. In either case, the structure of FIG. 1H is formed with a portion of the first metallization layer exposed.

[0055] FIG. 1I illustrates the step of forming a second metallization layer 122 to extend along the rear edge surfaces 134 and the rear surface 132 of substrate 102. Again, dotted lines show where the dies 104 may be separated from one another. The second metallization layer 122, like the first metallization layer, can include connection pads 126 and other traces. The connection pads 126 can be a spaced distance 107 from the edge surface of the die 104, as also shown in FIG. 1C. That is, the connection pads themselves do not reach the edge surface. Of particular notice are conducting elements 124 extending along edges of the die structures which electrically connect portions of the first and second metallization layers to one another. In one embodiment, conducting elements 124 are formed as part of the second metallization layer 122 and are formed simultaneously with the connection pads 126 and associated traces of the second metallization layer. Alternatively, the metallization layer 122 and the conducting elements 124 may be formed in separate steps. After forming the conductive elements and metallization layer, the substrate

can be severed into a plurality of individual die structures 200 as described below and illustrated relative to FIGS. 2A-2D A process flow summarizing the steps outlined above to create device 200 can be seen in FIG. 2E.

[0056] The sizes, shapes and positions of the connection pads of the second metallization layer can be the same as or similar to that of the connection pads of the first metallization layer 110, although other configurations are possible. Alignment of connection pads on the various layers can facilitate later stacking of individual die structures to form a stacked microelectronic assembly such as described below with reference to FIG. 3, for example.

[0057] FIG. 2A is a sectional viewing showing one embodiment of a final structure of a microelectronic device 200 after it has been separated from neighboring elements. FIG. 2D is a corresponding perspective view looking towards a surface 203 of the device opposite the surface 201 on which the bond pads 106 originally were exposed. FIG. 2B illustrates a detail view of an example connection between a conducting element 124 and the first metallization layer 110. FIG. 2B shows the structure of the joint between the layers if the process has been completed as previously outlined for the embodiment. Processes for forming similar metallization layers and joints between them are described in U.S. Patents 6,972,480 and 7,192,796, the disclosures of which are incorporated by reference herein. The conducting element 124 in this example extends in a direction in which the first metallization layer extends horizontally along surface 201. The conducting element may be plated onto the metallization layer. The portion of the conducting element that extends beyond the edge surface 134 can vary in length depending on how the singulation cut is performed or other factors. In a variation, the joint between the conducting element 124' and the metallization layer 110' can be as shown in FIG. 2C in which the conducting element 124' extends along an edge 208 of the metallization layer 110', the edge 208 extending in a direction of a thickness 214 of the layer 110'

away from surface 201. Processes for forming similar structure with similar joints between conductive elements are described in U.S. Patents 6,646,289 and 6,777,767, the disclosures of which are incorporated by reference herein. Such structure can result if the channels 118 are etched deeper and create a gap entirely through the portion of the first metallization layer that they intersect. In one embodiment, microelectronic devices, like those shown in FIG. 2A, may be stacked and connected to form a stacked die device. One example of this can be seen in FIG. 3. In this example, a die stack assembly 300 is composed of four substantially identical microelectronic devices 200. The various devices 200 in the stack may be taken from a single wafer, or they may come from different wafers. To improve reliability and yield, each die device may be tested before stacking to ensure that it is fully functional before assembly. By using known good devices to make up the stack, the problem of compound yield problems with the die stack can be mitigated. As described, this method of stacking can be perceived as a die-level process where the dies are stacked after being separated from the wafer.

[0058] In one embodiment, die stack 300 is functionally complete, but may require additional steps to package it into its final form. Any additional packaging steps involve techniques that are well-known to those with skill in the art.

[0059] In an alternative embodiment, the joining may be done at the wafer level. After joining the wafers together into a stack, the completed die stacks could then be separated.

[0060] The actual joining of one die to the next layer may be accomplished in a variety of ways. FIGS. 4A and 4B illustrate two exemplary approaches. In FIG. 4A, a microelectronic device, like those illustrated in FIG. 2A, is shown. In FIG. 4B a layer of conductive bonding material 402, which can be a fusible metallurgical joining metal, for example, has been placed on the upper connection pad 126. The joining metal, which may be solder, tin, indium, a eutectic or alloy of such metal or other such combination of metals, may be

plated on or deposited in a different manner. As shown, the joining metal may be applied only to the connection pads 402 exposed at the rear surface 403, but it is conceivable that the process may place metal on one or more of the exposed metal surfaces including the side conductive elements or other pads at surface of the die. In either case, the dies with joining metal are then aligned and stacked. The stack may then be heated to complete the face-to-face joining. Alternatively, a conductive paste, e.g., silver-filled paste, gold paste, solder paste, etc. can be used as the conductive bonding material to form an electrically conductive path between conductive elements of microelectronic devices in the stack. As illustrated in FIG. 3, the front surfaces 201 of some microelectronic devices confront rear surfaces 203 of other microelectronic devices. Electrically, conductive elements at front surfaces 201 of some microelectronic devices 200 are conductively bonded to electrically conductive elements at rear surfaces 203 of the other microelectronic devices 200. In a particular embodiment, two microelectronic devices can be arranged such that their front surfaces 401 (FIG. 4A) confront each other. Then, connection pads exposed at a front surface 401 of a microelectronic device 400 can be joined with connection pads exposed at a front surface 401 of another microelectronic device. In another embodiment, the rear faces of two microelectronic devices can confront each other and the connection pads on such rear faces be joined by the above-described methods. In a particular embodiment, the bonding of conductive elements can be made at the surfaces confronting each other while the microelectronic devices 200 remain attached in wafer form, as shown in FIG 1I, for example.

[0061] In another die stack embodiment, the die stack may be composed of a heterogeneous assortment of dies with different functionalities. FIG. 5A shows one such die stack structure 500. The die stack structure 500 is similar to that of FIG. 3; however, the individual devices in the stack are different. In this example, the top two dies 502 in the stack are the same,

but the bottom two dies (504 and 506) are different. For example, die 502 may be a memory element, die 504 may be a memory controller, and die 506 may be a processing unit. In this stack configuration, the lateral size of the individual dies is substantially the same, and the connection pads between the various dies overlap is essentially the same position. Although the die stack 500 can be assembled at a die level, in alternative embodiments, it can also be assembled at the wafer level with little waste in wafer area on any given wafer. The constraint in die size is not necessary. In fact, FIG. 5B shows an embodiment in which the die stack structure 510 is composed of dies that are heterogeneous in both function and size. In one embodiment, the only constraint to stacking dies is that adjacent faces should have connection pads in the same locations. In the example shown in FIG. 5B, die 514 has connection pads on both the top and bottom surfaces that do not match with each other, but are configured to match with those on dies 512 and 516 respectively.

[0062] In one embodiment, the connection pads of a microelectronic device are positioned at or near the bond pads of a chip. For certain configurations, this may provide enough usable area of metal surface to form a connection with a second microelectronic device in a die stack. FIG. 6A shows a perspective view of a die 600 having bond pads 606 exposed at a front, i.e., contact-bearing surface 601. This view is similar to that of FIG. 1C. The die is part of a wafer with one or more dies that may be equivalent to the wafer of FIG. 1A. The metallization layer can include connection pads 604 that are formed over or in contact with the bond pads of the chip. In many cases, the spacing of the bond pads of the chip may be so close already as to prevent the width of the metallization layer over the bond pads from being substantially wider than the bond pads themselves. In a variation of this embodiment, no metallization layer is provided over the bond pads, which can be seen in FIG. 6B. In FIG. 6B, the bond pads are proximate edges and may extend to the edge of the die area so that a

second metallization step can connect each bond pad via a conductive element to the other surface of the chip. In other respects, the subsequent steps of the process are similar as for the structure of FIG. 6A.

[0063] Referring again to FIG. 6A, a substrate 602, e.g., a wafer is processed in a manner similar to the process outlined in FIG. 2E. FIG. 6C shows a cross-section view of an example substrate 602 containing several dies 600 with a metallization layer 604 covering bond pads 606 underneath, although in the case (FIG. 6B) where there is no metallization over the bond pads, the first metallization step may be bypassed. In FIG. 6D, in accordance with one embodiment, the substrate is flipped and bonded to a temporary substrate 610 with an adhesive layer 608. FIG. 6E shows the substrate 602 after the rear face of the die has been thinned. FIG. 6F shows the substrate 602 after it is cut or etched to expose the first metallization layer 604 (or the bond pads in the variant). Then, in accordance with one embodiment, the substrate is covered with a dielectric passivation layer 614 on the thinned and etched substrate, leaving a portion of the first metallization layer exposed, as illustrated in FIG. 6G. In accordance with one embodiment, a second metallization layer is deposited, forming both connection pads 616 and conductive elements 618 connecting the first and second metallization layers. The resulting structure is shown in FIG. 6H. After dicing along the dotted lines, the final structure of the microelectronic device 620 can be seen in FIG. 6I.

[0064] Microelectronic devices 620 can be joined to provide a die stack similarly to previous embodiments. FIG. 7 shows an exemplary die stack assembly 700. Individual devices in the die stack may be joined by methods such as shown in FIGS. 4A and 4B to join connection pads 604 at a front face of one microelectronic device with connection pads 604 exposed at a rear face of the microelectronic device adjacent to such device. Alternatively, the microelectronic devices can be arranged with front faces confronting each other and the pads

on the front faces being joined by such methods. In another variation, the microelectronic devices can be arranged so that the rear faces confront each other and the pads thereon be joined. Because the joining area at connection pads of device 620 is typically smaller than one such device 200 (FIG. 2), additional care may be necessary for proper alignment of each device with one another. The die stack 700 is shown here using homogenous elements, but it may also be formed from devices with different size and/or functionality.

[0065] In yet another embodiment, connections between dies in a stack may be made after the joining step. FIG. 8A shows a single microelectronic device 800. Device 800 is formed similarly to that of the device of FIG.2 and FIG. 7. Conductive elements 812 exposed at edges 804 are not used to provide a wraparound bridge to the other surface of the die, but instead are connection elements (e.g., bond ribbons, traces or pads) to provide surface area for later conductive bonding. FIG. 8B displays one embodiment of a die stack formed from devices 800. Each device in the stack is attached to the next using an adhesive layer 802. At this point, the devices may not be in electrical contact with each other. To conductively join the devices, a ball of solder or other reflowable material 806 can be deposited on the top of the stack near the side edge. Upon application of heat, the reflowable material 806 flows downward to wet and join together the connection elements exposed at the edge surfaces of the microelectronic devices in the stack. The result may be seen as die stack assembly 810 in FIG. 8B.

[0066] In another embodiment, the above fabrication method (FIGS. 1A-1I) can be applied simultaneously to two or more substrates joined together to form microelectronic devices having internally stacked dies. An example process flow is provided in FIG. 9. In this embodiment, two or more substrates can be joined at rear surfaces before adding side conductive elements. To do so, a substrate is patterned with a first metallization layer and attached to a temporary carrier wafer. The substrate is thinned by grinding, polishing, or some other

method. The result of this process is shown in FIG. 10A, which is similar to the structure 117 of FIG. 1F. In FIG. 10B, a second structure 117 is flipped upside-down and attached with an adhesive layer 1002 to the first structure 117. FIG. 10C shows intermediate wafer stack 1000 after the upper temporary carrier wafer and an upper adhesive layer have been removed. Next, as FIG. 10D shows, channels 1004 are cut or etched through both substrates and the central adhesive layer 1002 to expose the first metallization layer of the lower substrate.

[0067] In this embodiment, a separate passivation step may not be necessary since the thinned surfaces of the substrates are facing inward toward the central adhesive layer. However, this may be added as an optional step after creation of the channels since there may be some unprotected areas of the substrate within the channels depending on how they were created. FIG. 10E shows wafer structure 1010 after a metallization layer is deposited and patterned to form side conductive elements 1012 at edge surfaces which connect conductors, e.g., traces, connection pads on a first surface 1001 of each device 1020 with conductive elements on a second surface 1003 of the device. Note that while the third metallization layer creates the side conductive elements 1012 connecting the top of the stack to the bottom, it also overlaps with the patterned metallization layer of the upper substrate to form electrically conductive paths between the metallization layers. Although there is some overlap of these metal layers, the entire process may be simplified and cost savings achieved with this method since identical structures may be used as part of the process. After separation at the dotted lines, intermediate die stack device 1020 is created and is shown in FIG. 10F. Similarly to previous embodiments, die stack device 1020 may be joined to other similar devices in a composite stack 1030 using methods such as described above with respect to FIGS. 4B, 7 OR 8A-C. Although device 1020 is referred to as an intermediate die stack device, it is contemplated that this

device could be packaged and used on its own without subsequent stacking.

[0068] In a variant, the first metallization layer on the upper substrate may be omitted. An example of such is structure 1040 shown in FIG. 10H. In this variant, structure 1040 is joined to the lower substrate with an adhesive layer and then channels 1004 created. Deposition of a metallization layer and subsequent patterning will lead to a structure substantially the same in appearance and function to structure 1010 of FIG. 10E, which may then be processed and stacked further in an equivalent manner. The two wafer substrates in this variant may be created somewhat differently, eliminating one of the required metallization steps in the process.

[0069] In a further variant to this embodiment, not pictured here, a second wafer stack 1000 might be flipped and attached to a first wafer stack 1000 with another adhesive layer, and then the upper carrier wafer removed again. This assembly can then be cut and metalized to create a four-level connected stacked device.

[0070] In yet another embodiment, both of the substrates may be processed in a face-down manner before connecting them electrically. FIG. 11A shows two wafer structures to be joined that are essentially the same as structure 111 of FIG. 1C and structure 117 of FIG. 1F. Rather than attaching structure 111 to a temporary carrier wafer to be thinned (as shown in FIG. 1E), it is instead attached directly to the back face of structure 117. This is illustrated in FIG. 11B, where the two structures are attached with a layer of adhesive 1102. FIG. 11C shows the result of thinning the upper substrate. After this, channels are created through both substrates and the central metallization layer as depicted in FIG. 11D. In FIG. 11E, a third metallization layer is deposited and patterned to create structure 1110. Note here that the edge conductive element portions 1112 of the third metallization layer make contact with both of the other metallization layers. Finally, the lower carrier is removed and the devices 1120 are separated as seen

in FIG. 11F. These devices may be stacked in a die stack assembly 1130 as shown in FIG. 11G or in some other manner.

[0071] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

CLAIMS

1. A microelectronic assembly, comprising:

a first microelectronic device and a second microelectronic device, each of the microelectronic devices including a die structure including at least one semiconductor die and each of the microelectronic devices having a first surface, a second surface remote from the first surface and at least one edge surface extending at angles other than a right angle away from the first and second surfaces, and at least one electrically conductive element extending along the first surface onto at least one of the edge surfaces and onto the second surface, the at least one conductive element of the first microelectronic device being conductively bonded to the at least one conductive element of the second microelectronic device to provide an electrically conductive path therebetween.

2. A microelectronic assembly as claimed in claim 1, wherein the electrically conductive elements of each microelectronic device include first elements formed by plating onto one of the first and second surfaces and second elements formed by plating onto another one of the first and second surfaces and the at least one edge surface, wherein the second elements are plated onto portions of the first elements.

3. A microelectronic assembly as claimed in claim 2, wherein the second elements extend along the portions of the first elements on which the second elements are plated.

4. A microelectronic assembly as claimed in claim 2, wherein the second elements extend along edges of the first elements.

5. A microelectronic assembly as claimed in claim 1, wherein the conductive elements are bonded using a fusible metal.

6. A microelectronic assembly as claimed in claim 1, wherein the conductive elements are bonded using conductive paste.

7. A microelectronic assembly as claimed in claim 1, wherein one of the first and second surfaces of the first microelectronic device confronts one of the first and second surfaces of the second microelectronic device and portions of the conductive elements exposed at the confronting surfaces are bonded together.

8. A microelectronic assembly as claimed in claim 7, wherein the conductive elements include conductive pads exposed at at least one of the first or second surfaces of each microelectronic device, the conductive pads being bonded together.

9. A microelectronic assembly as claimed in claim 7, wherein the conductive elements include traces and conductive pads, wherein the at least one conductive pad is disposed a spaced distance from the at least one edge surface.

10. A microelectronic assembly as claimed in claim 7, wherein the conductive element of each microelectronic device includes a conductive pad proximate the at least one edge surface.

11. A microelectronic assembly as claimed in claim 10, wherein the conductive pad extends to the at least one edge surface.

12. A microelectronic assembly as claimed in claim 1, wherein at least one of the die structures includes a plurality of semiconductor dies.

13. A microelectronic assembly as claimed in claim 12, wherein the bond pad-bearing surfaces of at least two of the semiconductor dies included in the at least one die structure face in the same direction.

14. A microelectronic assembly as claimed in claim 12, wherein the bond pad-bearing surfaces of at least two of the semiconductor dies included in the at least one die structure face in different directions.

15. A microelectronic assembly as claimed in claim 1, wherein the edge surface extends at an angle of between 50

degrees and 89 degrees with respect to at least one of the first and second surfaces.

16. A microelectronic assembly as claimed in claim 1, wherein the first and second microelectronic devices are stacked in a vertical direction and the at least one edge surfaces of the first and second microelectronic devices are offset from each other in a direction away from the vertical direction.

17. A microelectronic assembly as claimed in claim 1, wherein the first surfaces of the first and second microelectronic devices extend in lateral directions and have first dimensions in the lateral directions, wherein the lateral dimensions of the first surfaces of the first and second microelectronic devices are different.

18. A microelectronic assembly, comprising:

a first microelectronic device and a second microelectronic device, each of the microelectronic devices including a die structure including at least one semiconductor die and each of the microelectronic devices having a first surface, a second surface remote from the first surface and at least one edge surface extending away from the first surface, and at least one electrically conductive element extending along the first surface and onto at least one of the edge surfaces, the at least one conductive element of the first microelectronic device being conductively bonded to the at least one conductive element of the second microelectronic device to provide an electrically conductive path therebetween.

19. A microelectronic assembly as claimed in claim 18, wherein the at least one edge surface extends at an angle other than a right angle away from the first and second surfaces.

20. A microelectronic assembly as claimed in claim 18, wherein at least edge portions of the electrically conductive elements exposed at the at least one edge surfaces are conductively bonded to provide the electrically conductive path.

21. A microelectronic assembly as claimed in claim 20, wherein the at least edge portions of the conductive elements are bonded using a fusible metal.

22. A microelectronic assembly as claimed in claim 20, wherein the at least edge portions of the conductive elements are bonded using conductive paste.

23. A method of fabricating a stacked microelectronic assembly, comprising:

arranging a major surface of a first microelectronic device to confront a major surface of a second microelectronic device and conductively bonding an electrically conductive element exposed at the major surface of a first microelectronic device with an electrically conductive element exposed at the major surface of the second microelectronic device to provide an electrically conductive path therebetween, wherein each of the microelectronic devices includes a die structure including at least one semiconductor die and each of the microelectronic devices has a first major surface, a second major surface remote from the first surface, at least one edge surface and at least one electrically conductive element extending along the first surface onto at least one of the edge surfaces and onto the second major surface.

24. A method of fabricating a stacked microelectronic assembly, comprising:

forming a stack including a first microelectronic device with a second microelectronic device, each of the microelectronic devices including a die structure including at least one semiconductor die and each of the microelectronic devices having a first surface, a second surface remote from the first surface and at least one edge surface extending away from the first surface, and at least one electrically conductive element extending along the first surface and onto at least one of the edge surfaces; and

conductively bonding portions of the conductive elements exposed at the edge surfaces to provide an electrically conductive path therebetween.

25. A method as claimed in claim 24, wherein the first microelectronic device is disposed above the second microelectronic device, and the step of bonding is performed by heating a fusible metal proximate the conductive element exposed at the at least one edge surface of the first microelectronic device such that the fusible metal flows onto the conductive element exposed at the at least one edge surface of the second microelectronic device.

26. A method as claimed in claim 25, wherein the fusible metal bridges a gap between the conductive elements of the first and second microelectronic devices.

27. A method as claimed in claim 24, wherein the first microelectronic device is disposed above the second microelectronic device, and the step of bonding is performed by dispensing a flowable conductive material onto the conductive element exposed at the at least one edge surface of the first microelectronic device such that the conductive material flows onto the conductive element exposed at the at least one edge surface of the second microelectronic device.

FIG. 1A

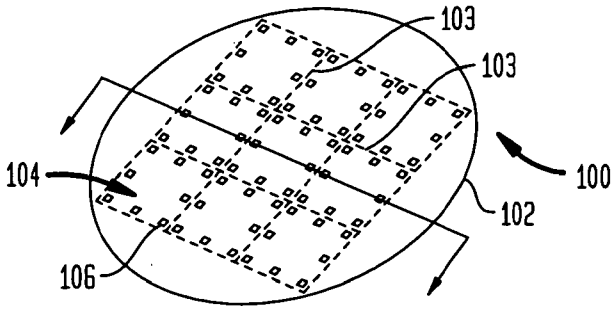


FIG. 1B

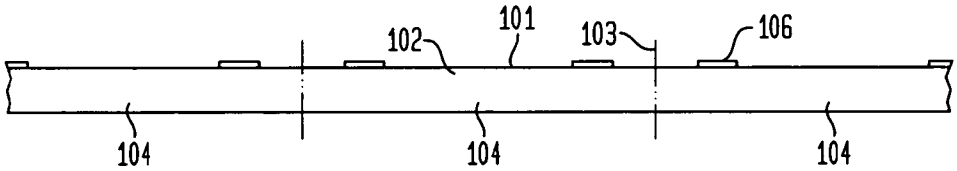


FIG. 1C

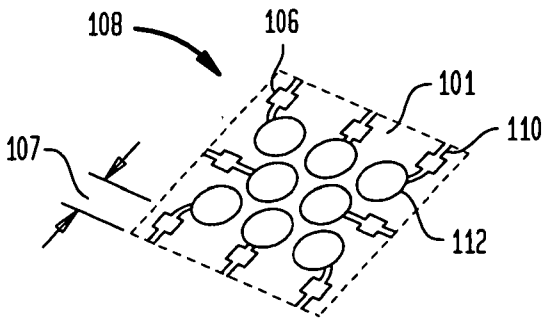


FIG. 1D

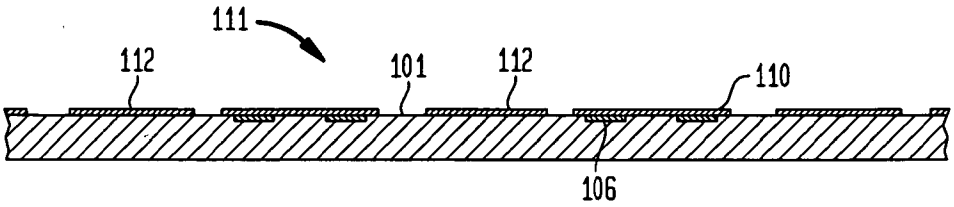


FIG. 1E

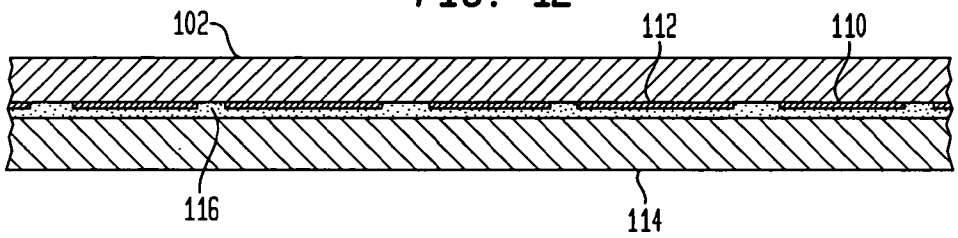


FIG. 1F

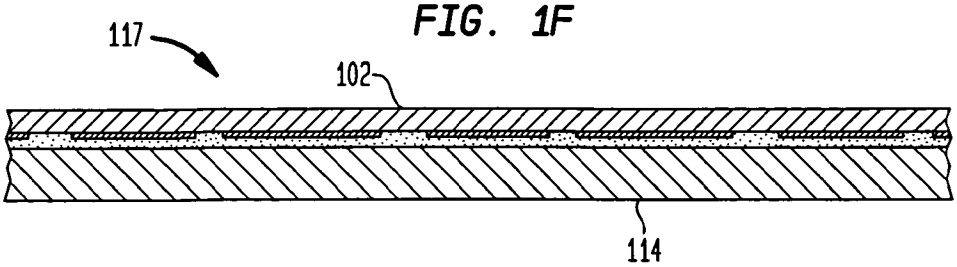


FIG. 1G

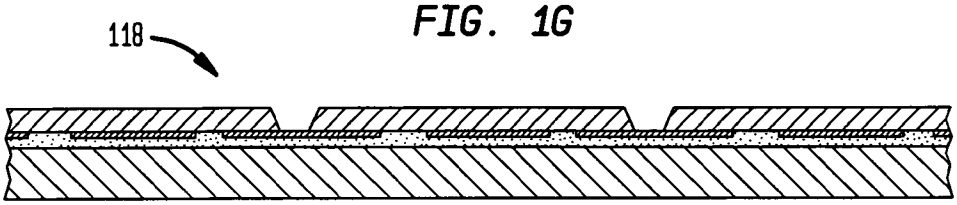


FIG. 1H

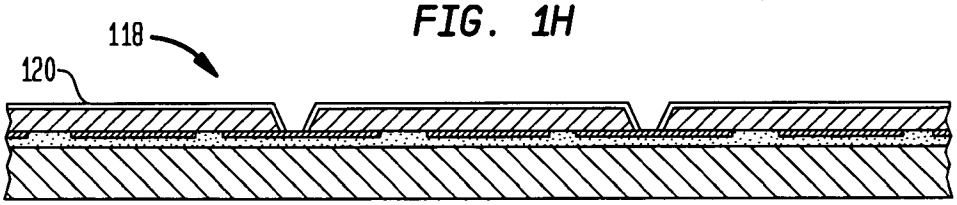


FIG. 1I

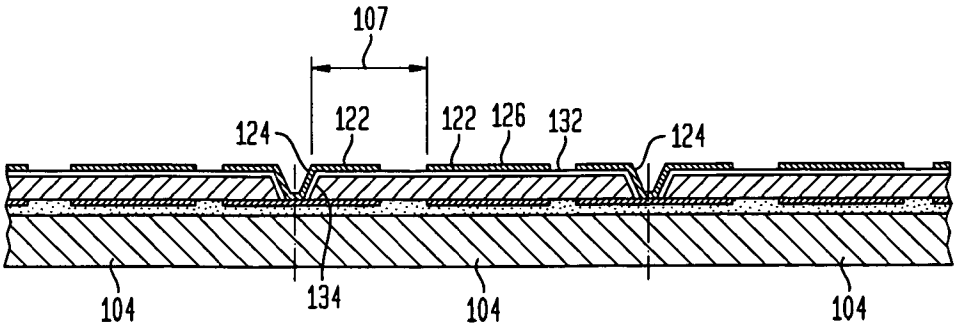


FIG. 2A

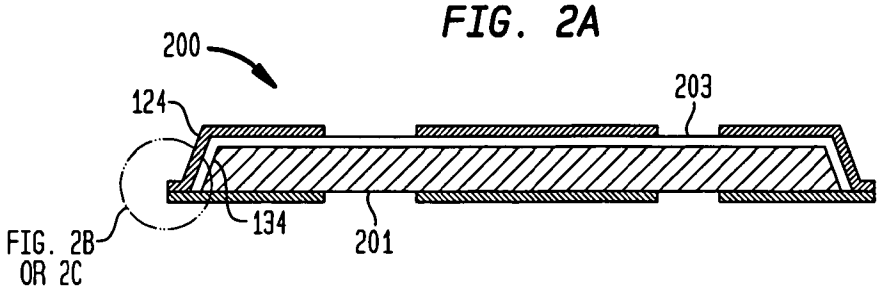


FIG. 2B

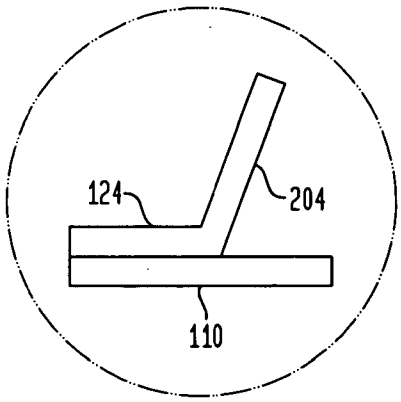


FIG. 2C

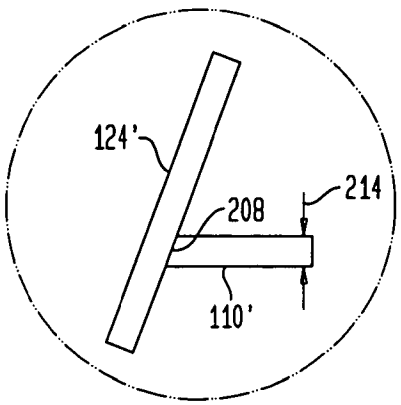


FIG. 2D

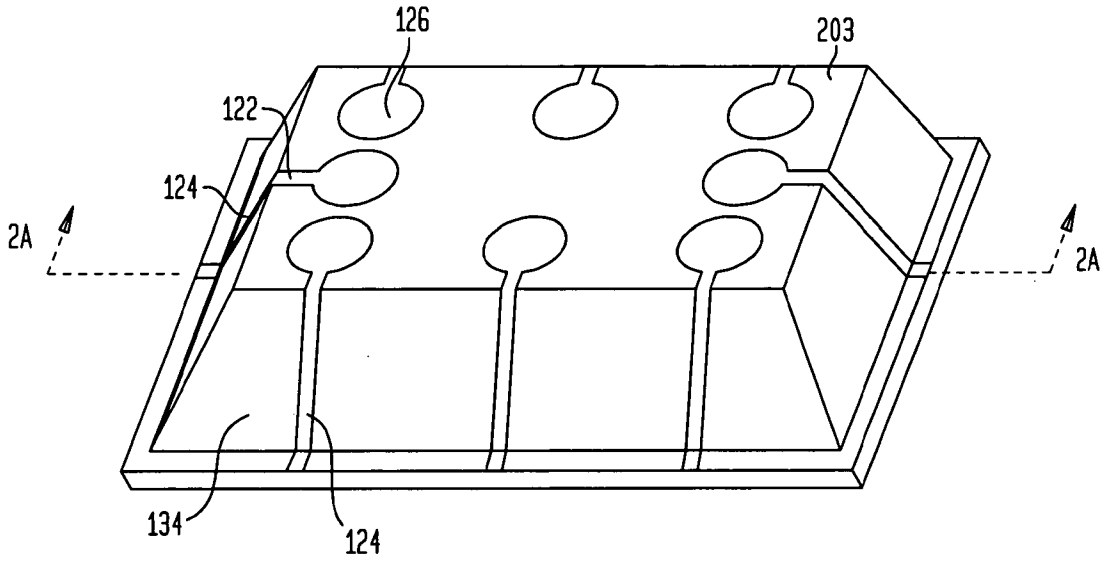


FIG. 2E

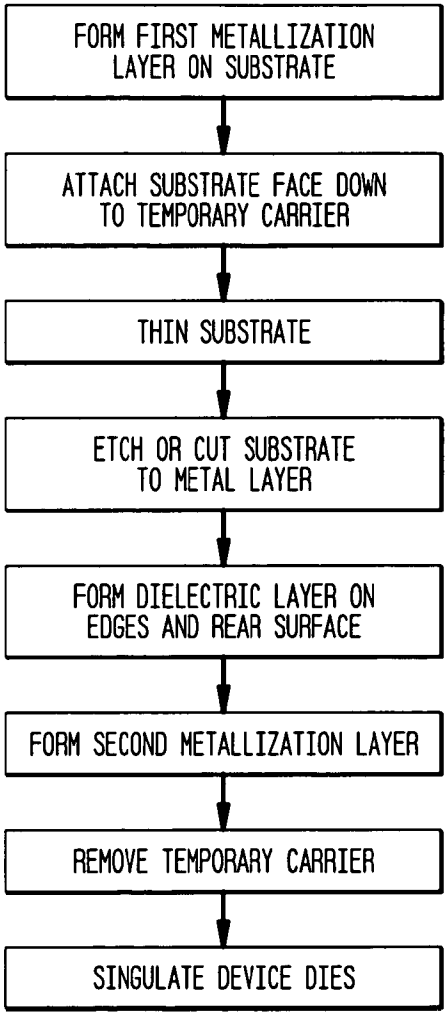

FORM FIRST METALLIZATION LAYER ON SUBSTRATE
ATTACH SUBSTRATE FACE DOWN TO TEMPORARY CARRIER
THIN SUBSTRATE
ETCH OR CUT SUBSTRATE TO METAL LAYER
FORM DIELECTRIC LAYER ON EDGES AND REAR SURFACE
FORM SECOND METALLIZATION LAYER
REMOVE TEMPORARY CARRIER
SINGULATE DEVICE DIES

FIG. 3

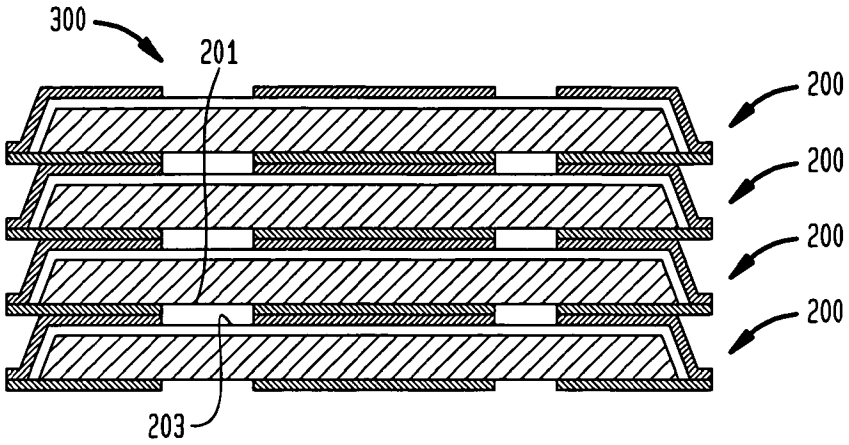


FIG. 4A

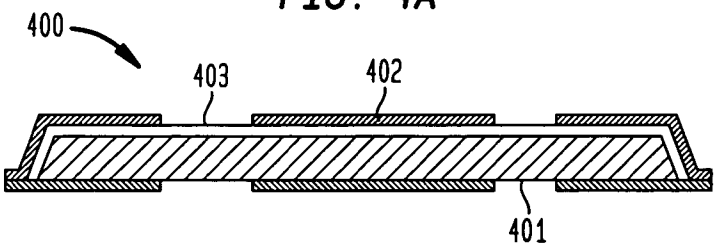


FIG. 4B

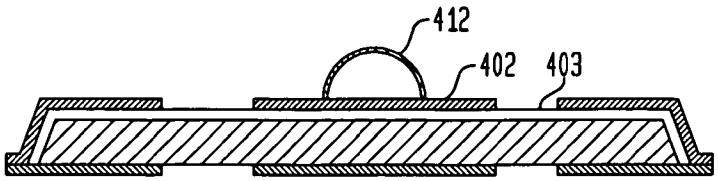


FIG. 5A

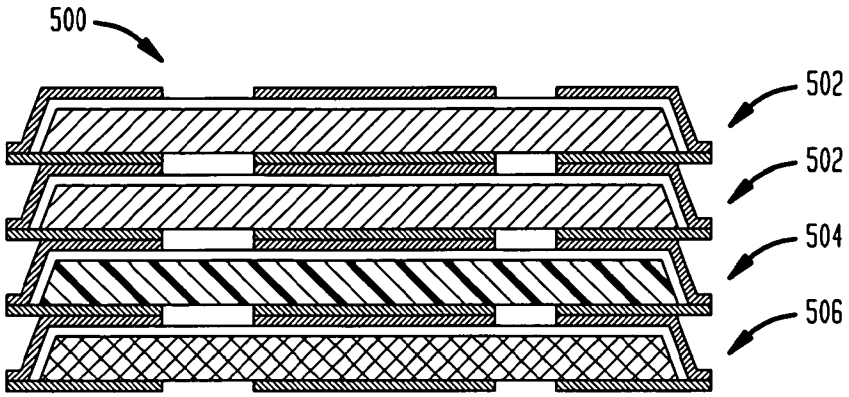


FIG. 5B

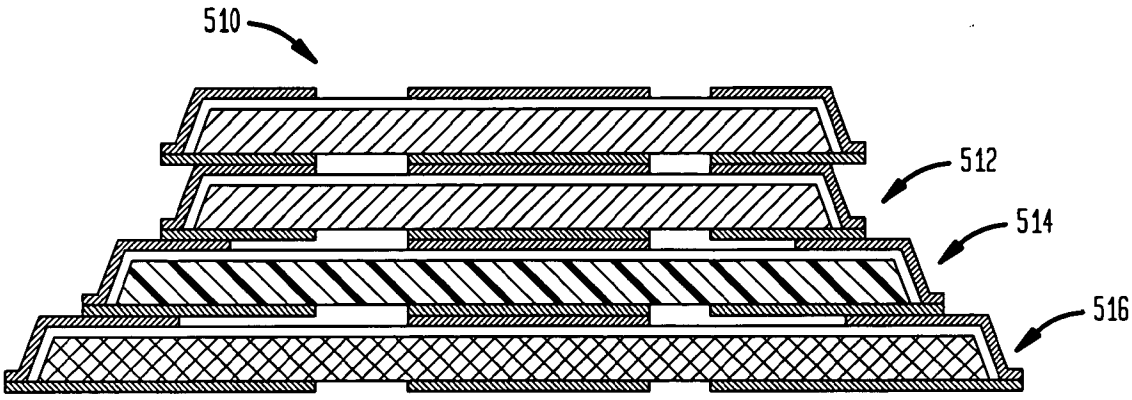


FIG. 6A

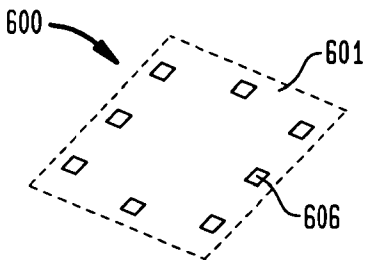


FIG. 6B

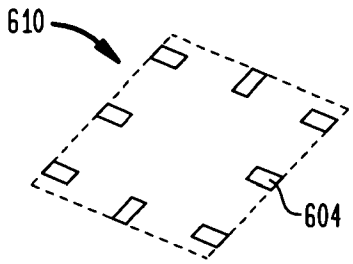


FIG. 6C

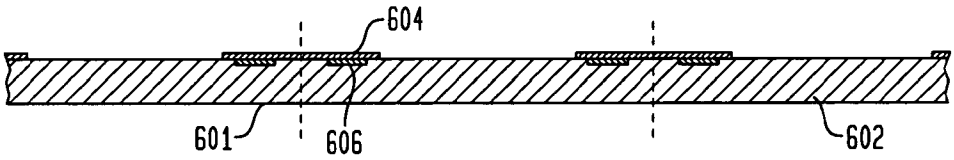


FIG. 6D

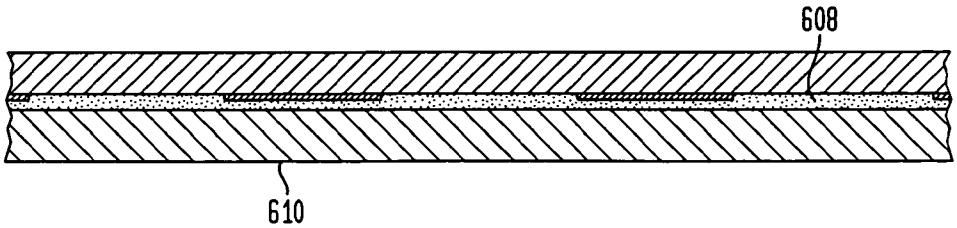


FIG. 6E

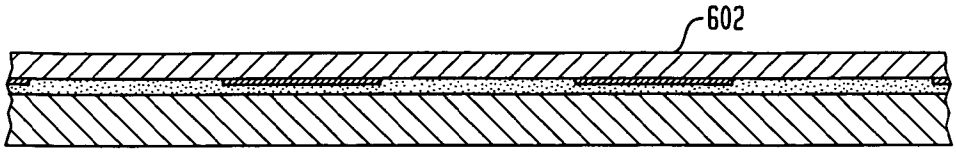


FIG. 6F

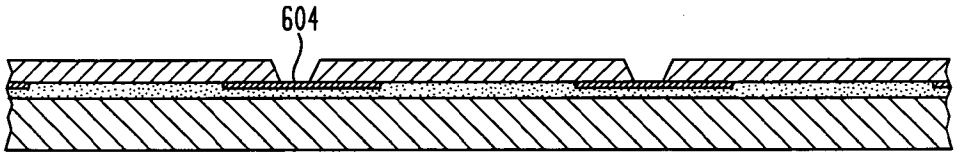


FIG. 6G

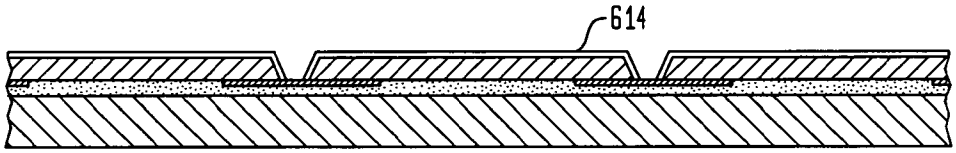


FIG. 6H

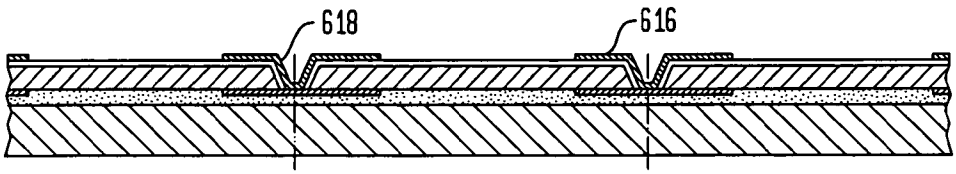


FIG. 6I

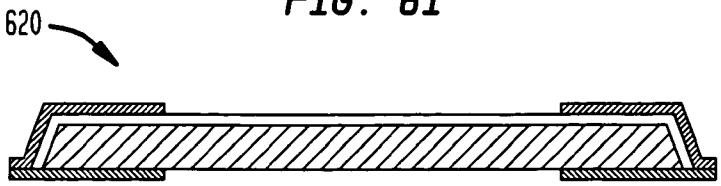


FIG. 7

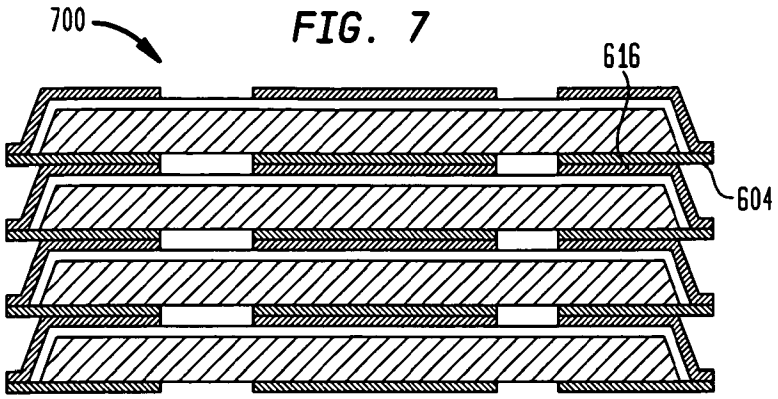


FIG. 8A

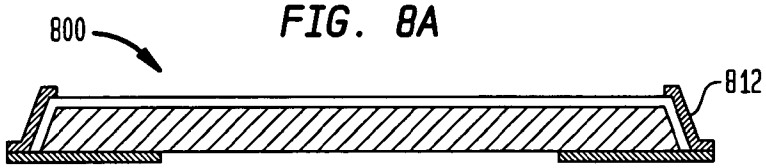


FIG. 8B

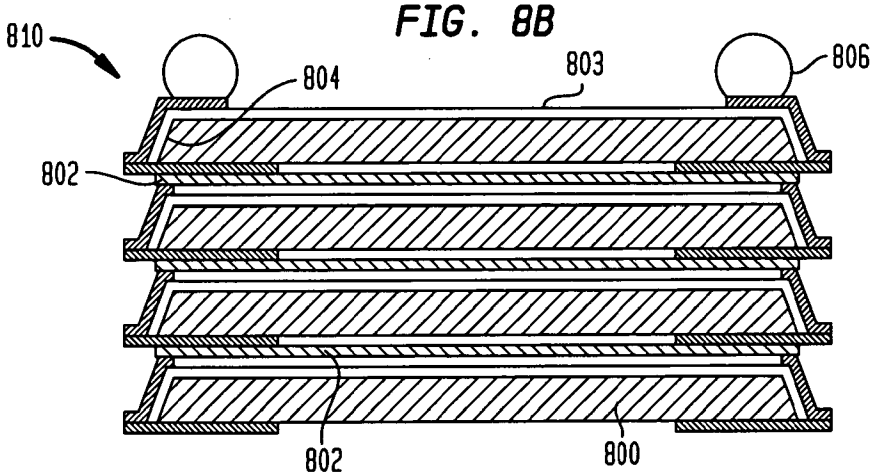


FIG. 8C

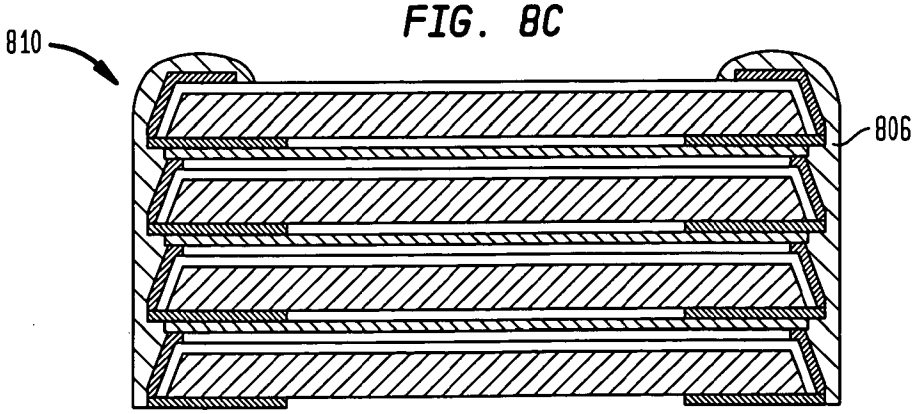


FIG. 9

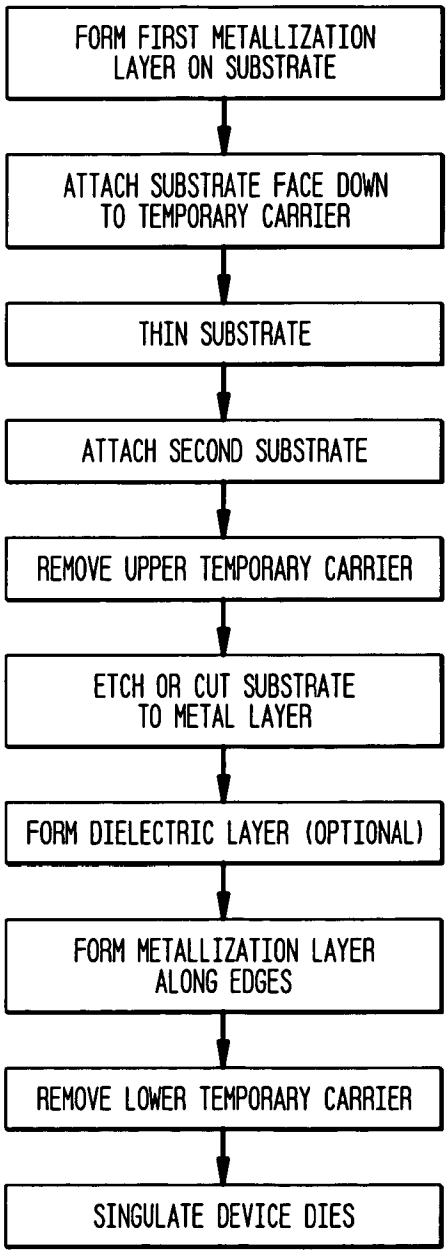

FORM FIRST METALLIZATION LAYER ON SUBSTRATE
ATTACH SUBSTRATE FACE DOWN TO TEMPORARY CARRIER
THIN SUBSTRATE
ATTACH SECOND SUBSTRATE
REMOVE UPPER TEMPORARY CARRIER
ETCH OR CUT SUBSTRATE TO METAL LAYER
FORM DIELECTRIC LAYER (OPTIONAL)
FORM METALLIZATION LAYER ALONG EDGES
REMOVE LOWER TEMPORARY CARRIER
SINGULATE DEVICE DIES

FIG. 10A

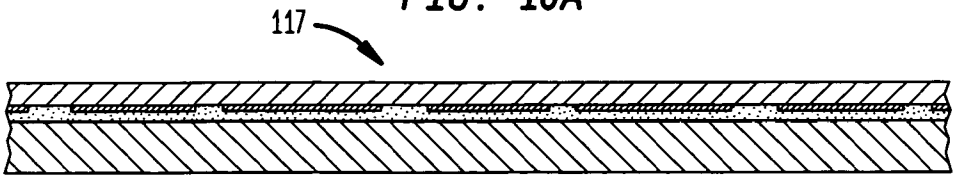


FIG. 10B

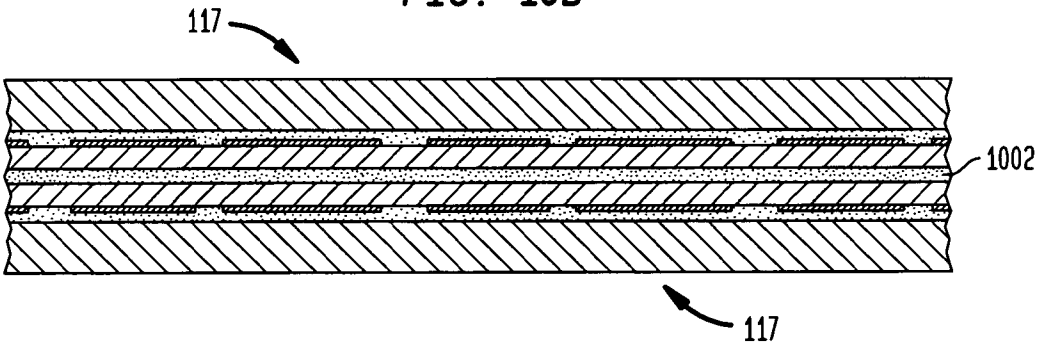


FIG. 10C

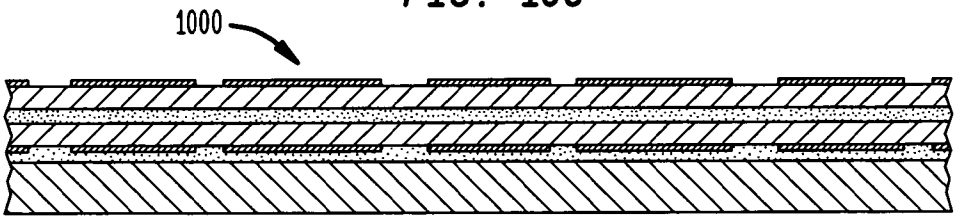


FIG. 10D

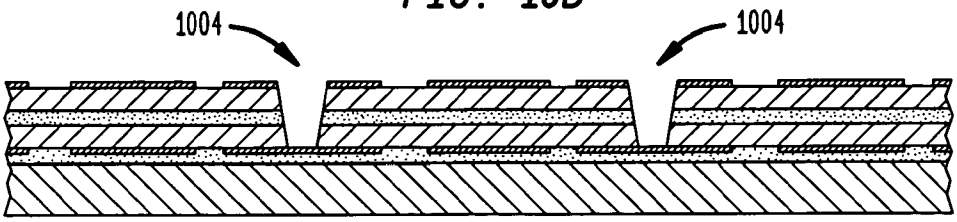


FIG. 10E

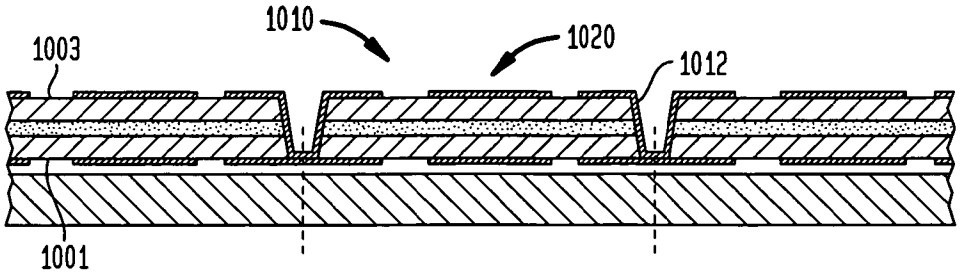


FIG. 10F

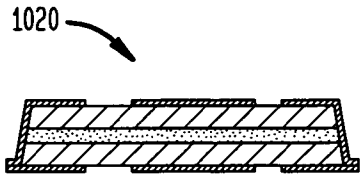


FIG. 10G

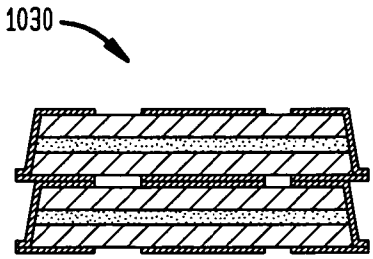


FIG. 10H

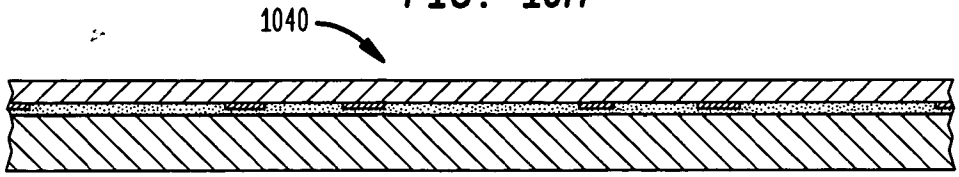


FIG. 11A

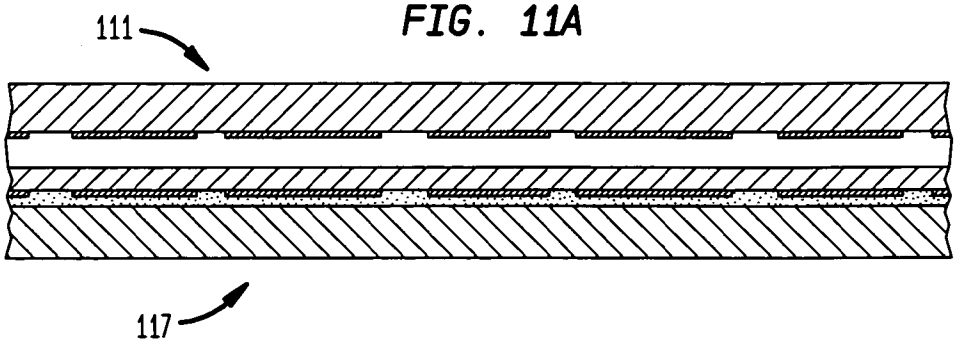


FIG. 11B

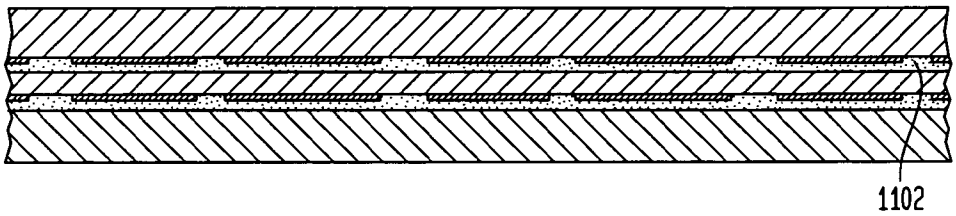


FIG. 11C

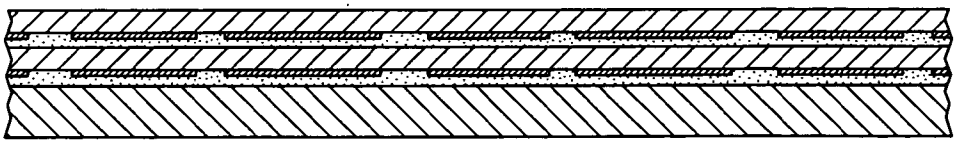


FIG. 11D

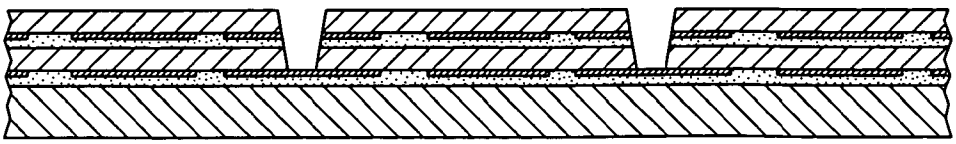


FIG. 11E

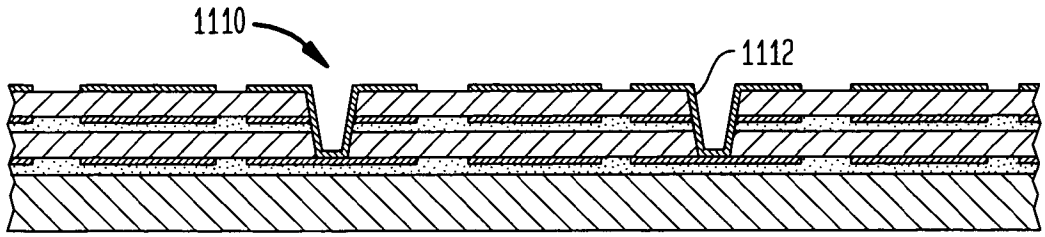


FIG. 11F

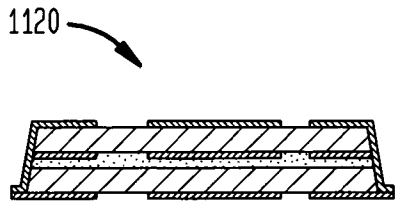
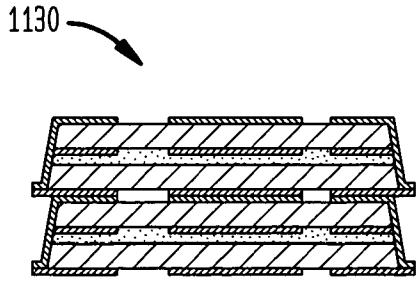


FIG. 11G



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/003643

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/10 H01L23/31
ADD. H01L21/98 H01L25/065

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2005/067680 A1 (BOON SUAN JEUNG [SG] ET AL) 31 March 2005 (2005-03-31) paragraphs [0041] - [0065], [0105], [0109]; figures 1-14,41	18,23 1-17
X Y	US 2006/094165 A1 (HEDLER HARRY [DE] ET AL) 4 May 2006 (2006-05-04) paragraphs [0027] - [0030], [0032], [0033]; figures 1-10,13 paragraph [0032]	18-21,24 1-8,10, 11,15
Y	US 2003/209772 A1 (PRABHU ASHOK [US]) 13 November 2003 (2003-11-13) paragraphs [0033], [0034]; figure 2 paragraphs [0037] - [0053]; figures 5A-5I	3,4

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2009	04/09/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Gallo, Thomas

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/003643

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	paragraph [0180]; figure 19	16,17
A	paragraphs [0113] - [0145]; figures 1-11	1-15
X	US 2007/158807 A1 (LU DAOQIANG [US] ET AL) 12 July 2007 (2007-07-12) paragraphs [0024] - [0027]; figures 12-16	18,23
Y	paragraph [0028]; figure 17	16,17
A	paragraphs [0017] - [0024]; figures 2-11	1-15
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Y	paragraphs [0036] - [0077]; figures 1-8	9
Y	US 2008/083977 A1 (HABA BELGACEM [US] ET AL) 10 April 2008 (2008-04-10) paragraphs [0115], [0116]; figure 20A	12-14
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P,X	US 2008/315407 A1 (ANDREWS JR LAWRENCE DOUGLAS [US] ET AL) 25 December 2008 (2008-12-25) paragraphs [0053], [0054]; figures 11-13	1,18,23, 24

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