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(54) **Integrated circuit projection system**

(57) A temperature control system for adjusting the temperature of a projection mask 23 to cause it to align or register optically with a wafer 24 on which a circuit pattern carried by the mask is to be printed includes a heater 14 within a chamber 13. Air is introduced to the chamber 13 by way of a pipe 15 passing through a cooler 16 and a filter 17, and the heated air passes along tubes 21 and 22 to fan out on either side of the mask 23. The operator views the alignment of the mask 23 and wafer 24 through a viewer 26 connected to projection optics 25 and adjusts the heater 14 by a control unit 30 until the correct temperature difference is achieved between the mask and wafer to bring them into optical alignment.

Fig. 1.

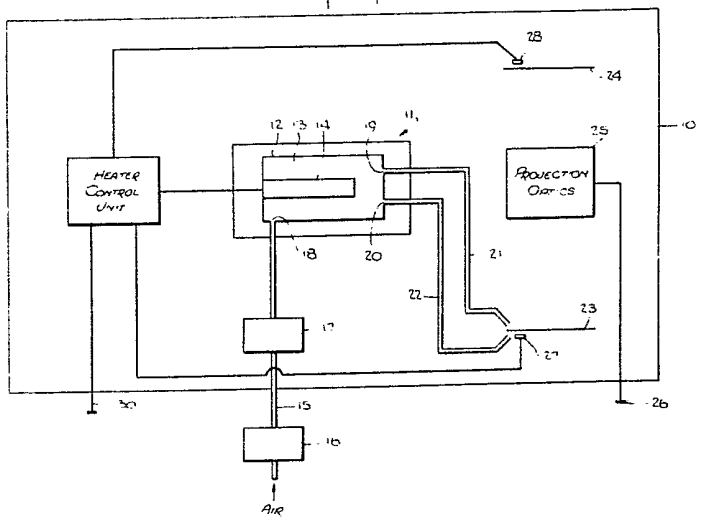

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Fig. 1.

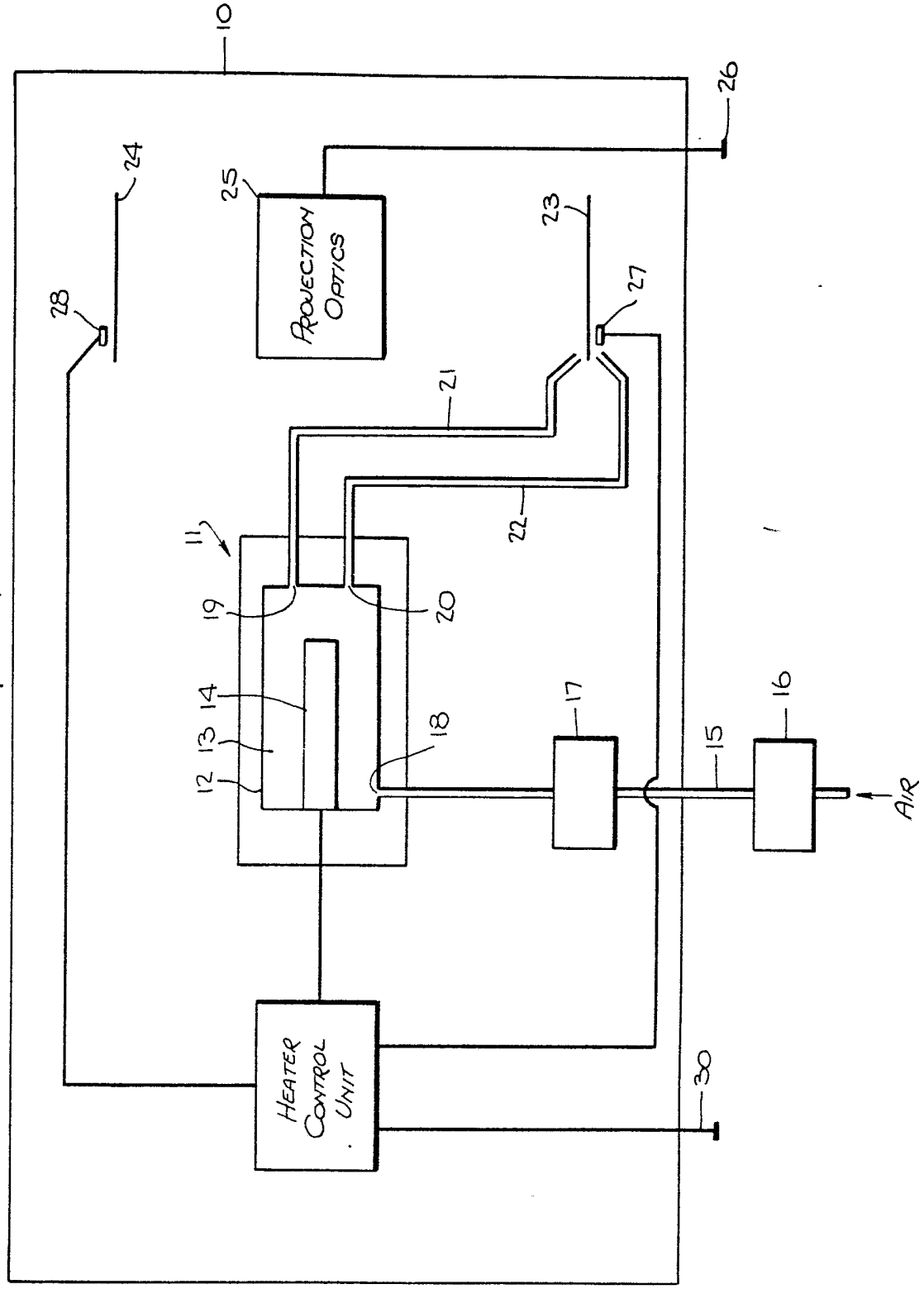

10
26
24
25
PROJECTION OPTICS
23
28
27
21
22
11
19
20
14
13
12
18
17
16
15
AIR
HEATER CONTROL UNIT
30

Fig. 2.

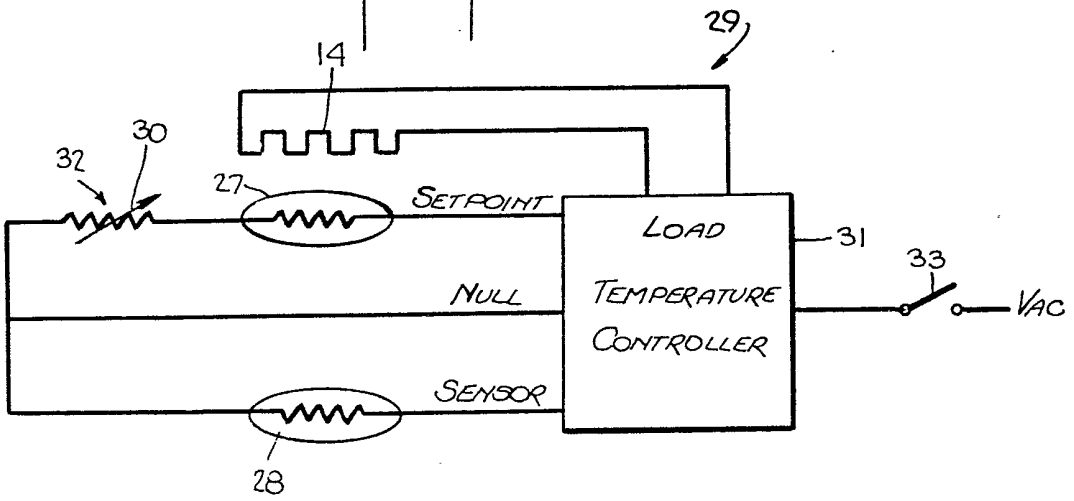
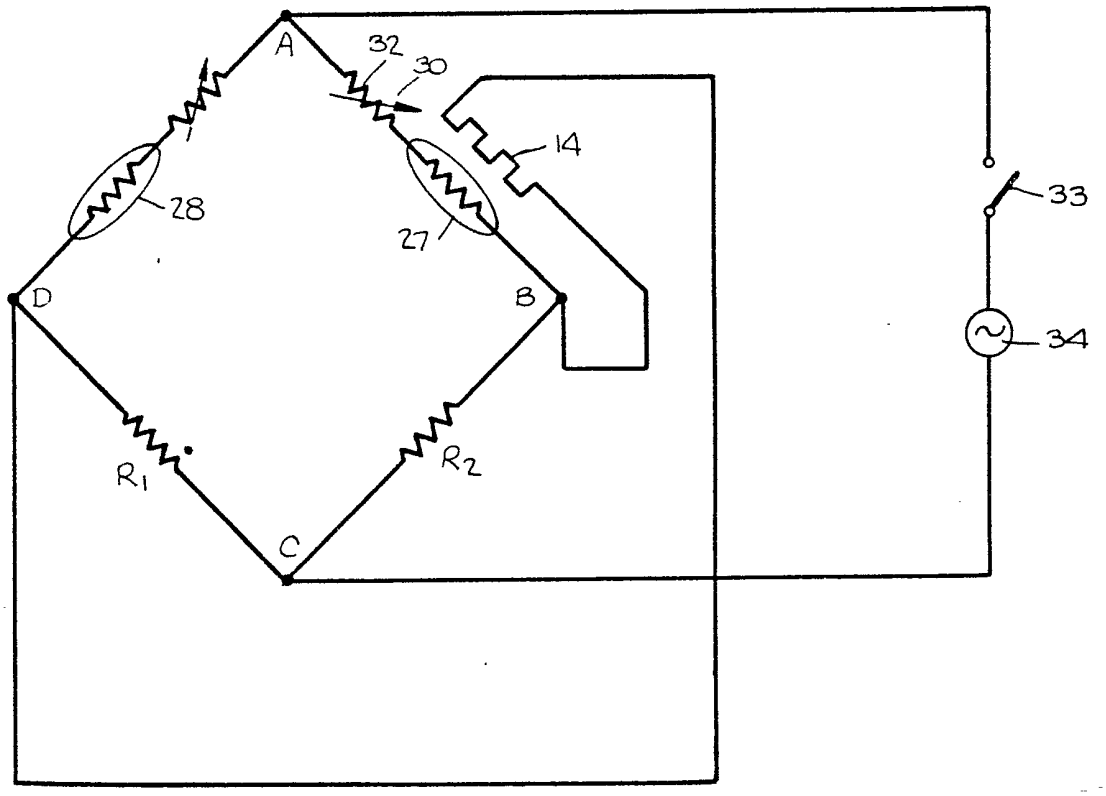

29
14
30
32
27
SETPOINT
LOAD
TEMPERATURE
CONTROLLER
31
33
NULL
VAC
SENSOR
28

Fig. 3.


A
32
30
14
33
28
27
D
B
34
R1
R2
C

SPECIFICATION

Integrated circuit projection system

The maufacture of integrated circuits involves the printing of circuit patterns on a wafer of silicon. One method of achieving this involves coating the wafer with a photo-resist material. When exposed to light the photo-resist material polymerizes into a hard tenacious coating, whereas the unexposed portions of the layer are easily removed, e.g. by means of a solvent or developer. A glass or quartz disc forming a mask which is opaque except for transparent areas comprising the circuit pattern is disposed in an optical arrangement for projecting the circuit pattern on to the wafer. In practice the circuit pattern is repeated on the mask in rows and columns such that each wafer contains a plurality of identical circuit patterns. Also circuit patterns on each wafer are built up layer by layer using a different mask for each layer until a complete circuit is formed. The wafer which contains a plurality of identical circuits is then cut along rows and columns producing a plurality of separate circuits or chips.

One system for projecting circuit patterns of a mask on to a wafer is disclosed in U S patent no: 4,011,011 which discloses the optical projection and alignment arrangement necessary to such a system.

In such a projection system alignment of the mask and wafer, that is to say registration of the image of the mask with the wafer, is critical. This is particularly true where layers of circuits are formed sequentially on a wafer. Errors of just a few microns may result in unaligned elements of a circuit pattern. The system disclosed in the above U.S. patent overcomes to a large extent the problems of alignment. However, it has been found that a mask cannot be perfectly aligned for projection on to a wafer without taking into account the change in size due to thermal expansion or contraction of the glass mask in the transverse direction. On the other hand changes of dimension in the axial or thickness direction do not affect alignment.

The present invention is concerned with a system for compensating for changes in the transverse dimensions of the mask due to temperature.

According to the present invention a projection system for exposing a silicon wafer to circuit patterns on a mask by optically projecting the circuit patterns on to the wafer includes apparatus for correcting mis-alignment between the mask and wafer due to changes in the transverse dimension of the mask or wafer due to temperature comprising means for viewing the projection of the mask on the wafer and means for adjusting the temperature of the mask or wafer until the viewed mask and wafer are aligned according to a predetermined standard.

The adjusting means may include heating means for bathing each side of the mask or wafer with temperature-controlled air, the heating means preferably comprising a housing enclosing a chamber and a heater within the chamber, the housing having an inlet for introducing air and and outlet for emitting air to each side of the mask or wafer. Preferably also the system includes heater control means connected to the heater for varying the temperature of the heater to change the temperature of the air bathing the mask or wafer from the outlet.

The invention will now be described by way of example in conjunction with the accompanying drawings, in which:-

Figure 1 illustrates a system according to the present invention:

Figure 2 is a detailed representation of the circuit of a heater control unit shown in Figure 1; and

Figure 3 is a representation of an alternative circuit for the heater control unit of Figure 1.

The temperature control system shown in Figure 1 along with other portions (not shown) of the mask projection system as described in U.S. patent no: 4,011,011 previously referred to, are disposed in a housing 10. Housing 10 is relatively airtight and provides through filtering and air conditioning a clear air temperature controlled environment for the mask projection system. The means for filtering and conditioning the air in housing 10 forms no part of the present invention and is, therefore, not shown. It should be noted, however, that the air in housing 10 is maintained relatively dust free to prevent particles from depositing on the wafer and particularly on the mask so that, on projection of the mask onto the wafer, the circuit patterns are not distorted or incorrect due to the dust particles being projected as part of the circuit pattern. In addition, the air in the housing is maintained at a constant temperature of e.g. 70°F.

Disposed in housing 10 is a temperature control unit 11 which comprises a housing 12 which may be formed of any heat resistant material e.g. PTFE. The housing 12 encloses a cylindrical space or chamber 13 which contains a heater element 14 fixed to one end of a wall of the chamber 13.

Air is introduced into chamber 13 via tube 15. Prior to entry into chamber 13, the air is passed through an air conditioner 16 so that the air introduced into the chamber 13 is at a temperature less than the ambient temperature of the housing 10. This is necessary inasmuch as the heater unit 14 can only heat the air and not cool it. The air is also filtered in filter 17 to remove dust particles therefrom prior to entry into chamber 13. The other end of the chamber 13 has ports 19 and 20 connected to tubes 21 and 22, having their ends disposed on opposite sides of a mask 23.

The mask 23 is inserted and held within the housing 10 in a manner similar to that described in U.S. patent 4,011,011. As disclosed in that patent the mask 23 is disposed for projection of the circuit pattern thereon on to a silicon wafer via the projection optics. In the present application, a wafer 24 is shown with the projection optics 25 positioned between it and the mask 23.

Reference numeral 26 indicates a viewer disposed outside of housing 10 and connected to the projection optics 25 by which an operator may view the alignment of the mask 23 and the wafer 24 in a manner similar to that disclosed in U.S. patent no: 4,011,011.

A temperature indicator such as, for example, a thermistor 27 is disposed adjacent the mask 23 for

sensing the temperature thereof. A second thermistor 28 is disposed adjacent the wafer 24 for sensing the temperature thereof. The thermistors 27 and 28 are electrically connected to heater control unit 29. A control 30 located outside the vicinity of the heater is also connected to heater control unit 29.

Air entering the chamber 13 via port 18 spirals around the heater 14 and passes through the ports 19 and 20. The air passes through the tubes 21 and 22, the ends of which may be fanned to heat sides of the mask 23 evenly. It should be noted that even though filtered, this air may contain some dust particles which often contain a charge and are therefore, prone to stick to the mask. Thus, it may be desirable to place a de-ionizing element in the vicinity of the emitted air to neutralise the particles and prevent their sticking to the mask. The particles are then blown away from the mask 23 by the emitted air.

The mask 23 is made of conventional mask material such as glass and changes dimension with temperature according to its co-efficient of thermal expansion. Thus, even after the mask 23 has been inserted and positioned with respect to the wafer 24, the size of the mask may be such as to prevent precise alignment and projection of the circuit pattern. Therefore, by use of temperature regulated air bathing each side of the mask 23, the size of the mask can be expanded until precise alignment with the wafer 24 is obtained. Once alignment is obtained, the temperature differential of the air bathing the mask 23 and the temperature of the wafer 24 or more particularly the air ambient to the wafer 24 can be adjusted and hence maintained constant.

In operation, initial sizing of the mask to cause it to expand and increase its radial dimensions to align precisely with the wafer is accomplished by an operator viewing the projection of the mask pattern on wafer through eye piece 26. While so viewing control 30 is turned to vary e.g. increase power to the heater 14 to heat air entering chamber 13 and change the temperature of the air bathing the mask 23 via tubes 21 and 22. At some point the alignment is precise as may be determined by the alignment of targets on the mask 23 with corresponding targets on the wafer 24. At this time, the heater control unit functions to maintain the temperature differential between the wafer 24 and mask 23.

Figure 2 illustrates heater control unit 29 in schematic form. A temperature controller 31 is connected to a source of AC voltage via switch 33. The thermistor 28, which is associated with the wafer 24, has one end connected as a sensor input to the controller 31 and its other end connected to a null input to the controller 31.

The thermistor 27, which is associated with the mask 23 has one end connected as a set point input to the controller 31 and its other end connected to one side of a potentiometer 32. The other side of the potentiometer is connected to the null input to the controller 31. The heater 14 which is the load is also connected to the controller 31.

The resistance varying portion 30 of the potentiometer 32 is the same as control 30 in Figure 1 and is initially in the zero resistance position. When switch 33 is closed, heater 14 is turned on until the resistance of the potentiometer 32 plus the resistance of thermistor 27 equals the resistance of the thermistor 28, i.e. the resistance between set point and null equals the resistance between the sensor and null. When the resistances are equal the heater 14 turns off. When this occurs the resistance of the thermistor 27 increases creating an unbalance. The heater 14 again turns on to lower the resistance of the thermistor 27. As a result, the heater 14 is constantly turned on and off to maintain the null. The temperature of the air around the wafer 24 is followed by the temperature of the air around the mask 23 keeping the temperatures of the mask 23 and wafer 24 equal.

Once this stabilisation is achieved, an operator views the alignment of the wafer 24 and mask 23 to see if mask temperature must be increased to obtain alignment. If so, he turns control 30 to increase the resistance in the set point of the circuit. The heater 14 is turned on until the resistance of the thermistor 27 decreases until the balance point is reached. Since the operator will have increased the resistance of the potentiometer 32 until the mask 23 has changed in size to correctly align with the wafer 24, the resistances will balance at a null point that maintains a temperature difference between the mask 23 and the wafer 24. As before, the heater 14 will turn off at the null point and on again when the resistance of the thermistor 27 has increased to an unbalanced state. The heater 14 will turn on and off as necessary to maintain the balance point and the temperature differential to keep mask temperature at the set point.

If in order to align the mask and wafer, it is necessary to decrease the mask temperature from the initial balance point, i.e. after initally balancing the circuit of Figure 2, the potentiometer 32 would have to be switched into the sensor side of the circuit or, alternatively, have a potentiometer built into that side and controlled by separate control similar to control 30.

The temperature controller 31 is a conventional item such as the temperature controller Model 72A manufactured by RFL Industries Inc., of Boonton, New Jersey, United States of America.

Figure 3 illustrates another arrangement for adjusting the temperature of the mask 23 and then maintaining the temperature difference between the mask 23 and the wafer 24, with like reference numerals indicating like elements. The circuit is a Wheatstone bridge with thermistor 28 and the thermistor 27 along with potentiometer 32 forming the two balancing legs of the bridge. The other legs contain equal resistance R_1 and R_2.

Power is supplied via AC source 34 connected as shown to points A and C. Heater 14 is connected between points B and D.

With potentiometer 32 set at zero resistance, the resistances of thermistors 27 and 28 will equalise when switch 33 is closed, since any voltage difference between points B and D will cause heater 14 to change the resistance of thermistor 27 appropriately.

To obtain alignment of the mask 23 and wafer 24

control 30 is moved until alignment is achieved, i.e. by unbalancing the bridge, voltage is applied to heater 14 which changes the temperature and, therefore, the size of mask 23 until alignment takes place. At this time, control 30 is stopped and the bridge automatically re-balances by changing the resistance of the thermistor 27 such that its resistance plus the resistance of the potentiometer 32 now in the circuit equals the resistance of the thermistor 28. When this occurs, the temperature difference between the mask 23 and wafer 24 is automatically maintained constant by the action of the bridge. Thus, any change in temperature of the mask 23 or wafer 24 is sensed by the resistance change of the respective thermistors 27 and 28 with the bridge automatically changing the resistance of the thermistor 27 by the heater 14 to maintain the balanced condition and, therefore, the temperature differential necessary to maintain alignment.

It should be noted that alignment could also be achieved by heat controlling the size of the wafer 24 instead of mask 23. In this case the wafer 23 would be bathed in temperature controlled air from tubes 21 and 22 with thermistors 27 and 28 physically changing places in the system of Figure 1 and electrically in the circuits of Figures 2 and 3.

CLAIMS

1. A projection system for exposing a silicon wafer to circuit patterns on a mask by optically projecting the circuit patterns on to the wafer including apparatus for correcting mis-alignment between the mask and wafer due to changes in the transverse dimension of the mask or wafer due to temperature comprising means for viewing the projection of the mask on the wafer and means for adjusting the temperature of the mask or wafer until the viewed mask and wafer are aligned according to a predetermined standard.

2. A system according to claim 1 wherein the viewing means comprises projection optics including means for viewing the alignment of the mask with the wafer.

3. A system according to claim 1 or claim 2 wherein the adjusting means includes a heating means for bathing each side of the mask or wafer with temperature controlled air.

4. A system according to claim 3 wherein the heating means comprises a housing enclosing a chamber and a heater within the chamber, the housing having an inlet for introducing air and an outlet for emitting air to each side of the mask or wafer.

5. A system according to claim 4 wherein the inlet includes a filter for removing solid impurities from the air and air conditioning means for cooling the air to a predetermined temperature level.

6. A system according to claim 4 or claim 5 wherein the outlet comprises two tubes for directing air on each side of the mask or wafer.

7. A system according to any one of claims 4 to 6 and also including heater control means connected to the heater, for varying the temperature of the heater to charge the temperature of the air bathing the mask or wafer from the outlet.

8. A system according to claim 7 wherein the heater control means further comprises temperature sensing means associated with the mask and the wafer and connected to the temperature means so as to maintain the temperature difference between mask and wafer constant after alignment has been achieved.

9. A system according to claim 8 wherein said temperature sensing means includes first and second thermistors disposed respectively adjacent the wafer and the mask.

10. A system according to claim 9 wherein the heater control mean comprises a source of electrical power, a variable resistance having one end connected to one side of the second thermistor and its other end connected to a balance point, to which the first thermistor has one side connected, balancing means connected to the source, to the balance point, to the other side of each of the first and second thermistors and to the heater for continuously causing the resistance of the second thermistor plus the resistance of the variable resistance to be equal to the resistance of the first thermistor.

11. A system according to claim 10 further including means for varying the variable resistance until the mask and wafer are in alignment.

12. A system according to any one of claims 3 to 11 wherein the adjusting means includes means for maintaining the temperature difference between the mask and wafer constant after the mask and wafer are aligned.

13. A system according to claim 9 wherein the heater control means comprises a Wheatstone bridge, having one arm constituted by a variable resistance and the second thermistor, the second arm constituted by the first thermistor and the third and fourth arms constituted by equal resistances, and a source of electrical power connected between the junction of the first and second arms and the junction of the third and fourth arms, the heater being connected between the junction of the second and fourth arms and the junction of the first and third arms of the bridge.

14. A system according to claim 14 wherein the second arm contains a variable resistor.

15. A projection system for exposing a silicon wafer to circuit patterns on a mask by optically projecting the circuit patterns on to the wafer substantially as described and as illustrated with reference to Figures 1 and 2 or Figures 1 and 3 of the accompanying drawings.

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