US 20100240283A1

(19) **United States**

(12) **Patent Application Publication**

Nemoto et al.

(10) **Pub. No.: US 2010/0240283 A1**

(43) **Pub. Date: Sep. 23, 2010**

(54) **METHOD OF CHEMICAL MECHANICAL POLISHING**

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(21) Appl. No.: **12/567,092**

(22) Filed: **Sep. 25, 2009**

(30) **Foreign Application Priority Data**

Mar. 18, 2009 (JP) 2009-066145

Publication Classification

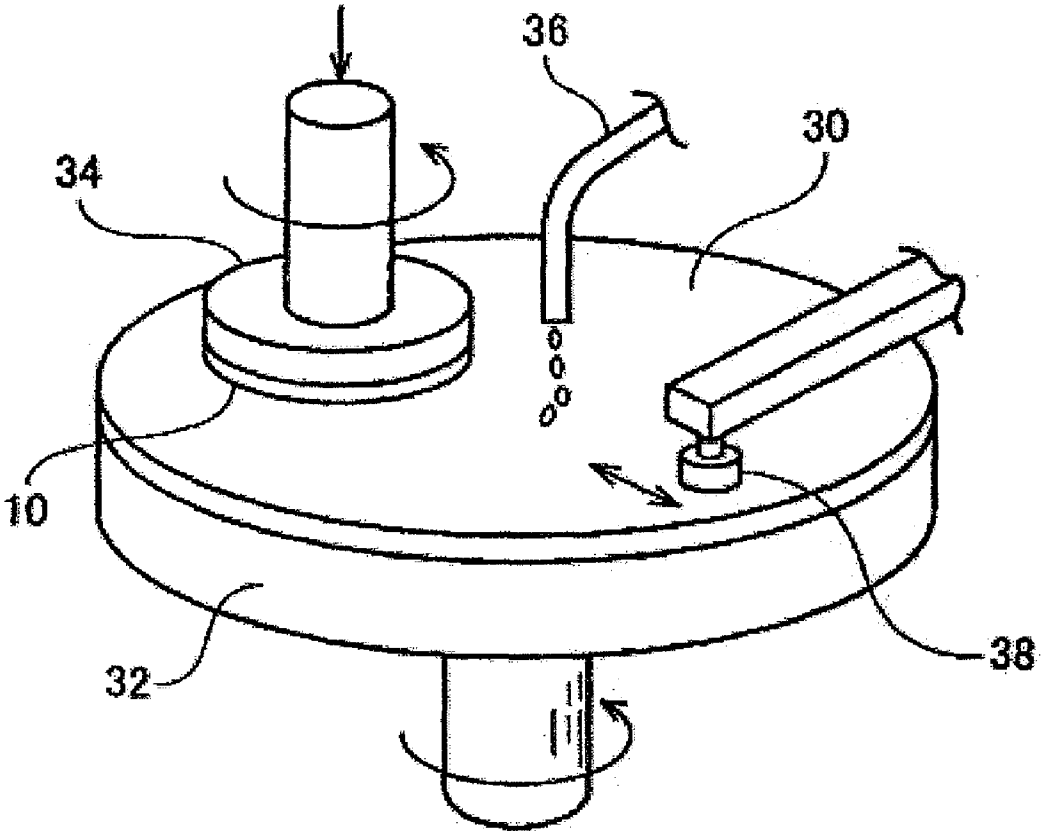
(51) **Int. Cl.**
B24B 1/04 (2006.01)

(52) **U.S. Cl.** **451/36**

(57) **ABSTRACT**

[Problem] To improve polishing efficiency while lowering shear force added to semiconductor wafers while increasing polishing speed, without damaging the wafer's processing surface or the membrane under it.

[Solution Method] Pressing the revolving head or carrier **34** that holds fixed the semiconductor wafer **10** to the polishing pad or polishing cloth **30** attached to rotating polishing table **32** in this CMP device and while rotating carrier **34** and polishing table **32** respectively, and supplying liquid slurry to polishing pad **30** from nozzle **36**, planarization by chemical processes and mechanical processes is carried out by removing membranes of the lower face of semiconductor wafer **10** (the processing surface). The chemical mechanical polishing process of the present invention in regard to the size of the relationship between the rotation rate of semiconductor wafer **10** f_W and the number of rotations of polishing pad **30** f_P has $3\ f_p<f_W$ as its lower limit and $4\ f_p<f_W<8\ f_p$ is ideal conditions.



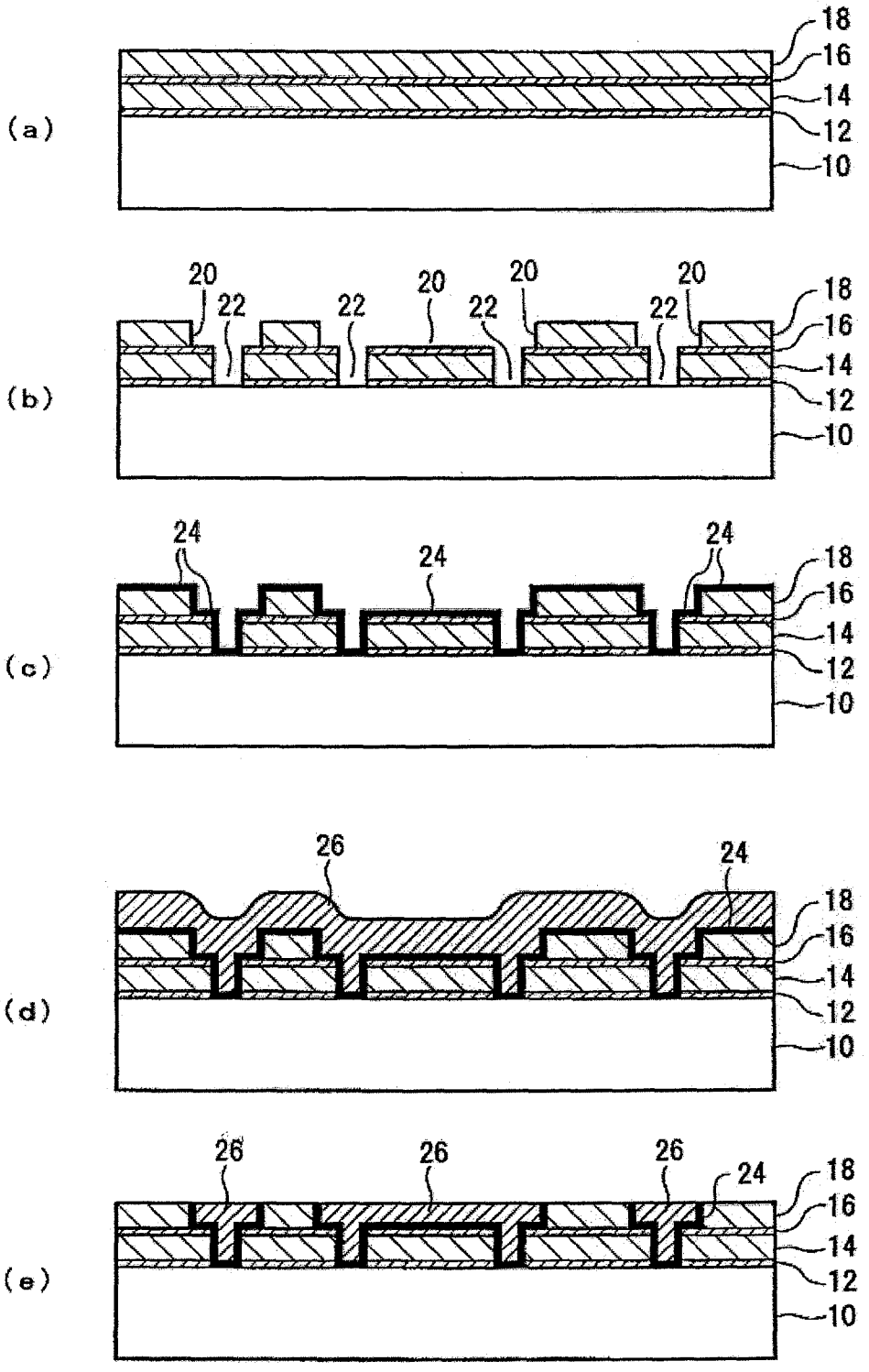

(a)
18
16
14
12
10
(b)
20
22
20
22
20
22
20
18
16
14
12
10
(c)
24
24
24
18
16
14
12
10
(d)
26
24
18
16
14
12
10
(e)
26
26
26
24
18
16
14
12
10

Figure 1.

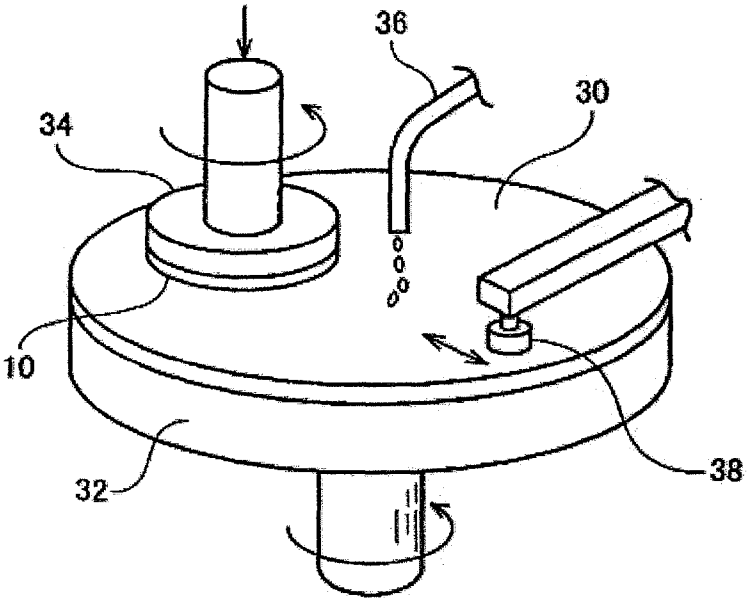


Figure 2

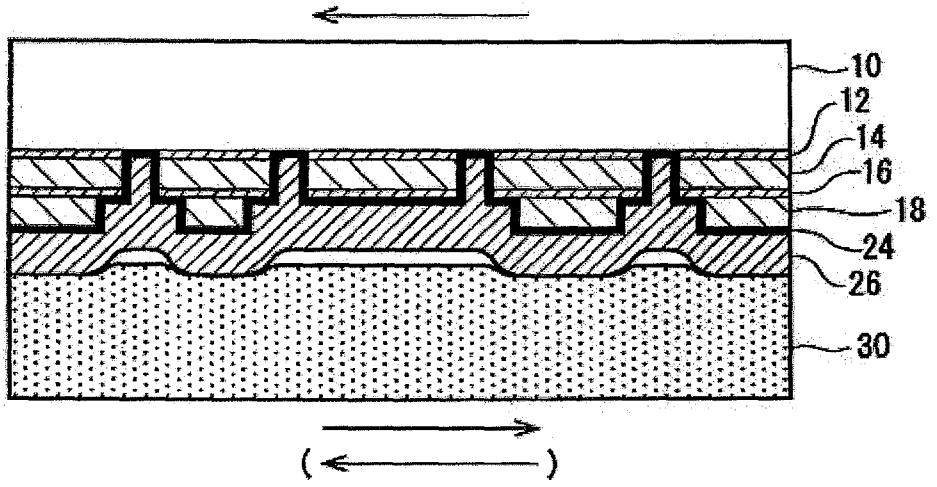


Figure 3

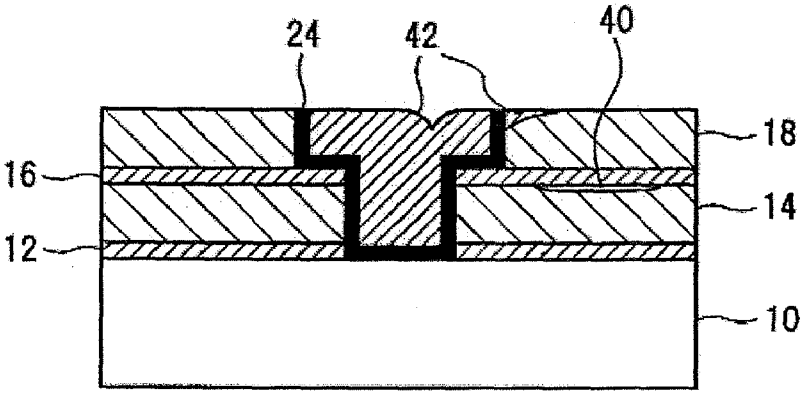


Figure 4A.

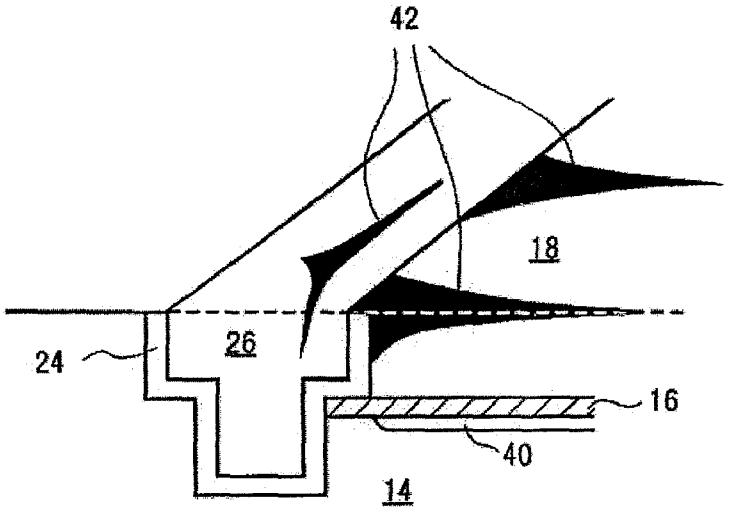


Figure 4b

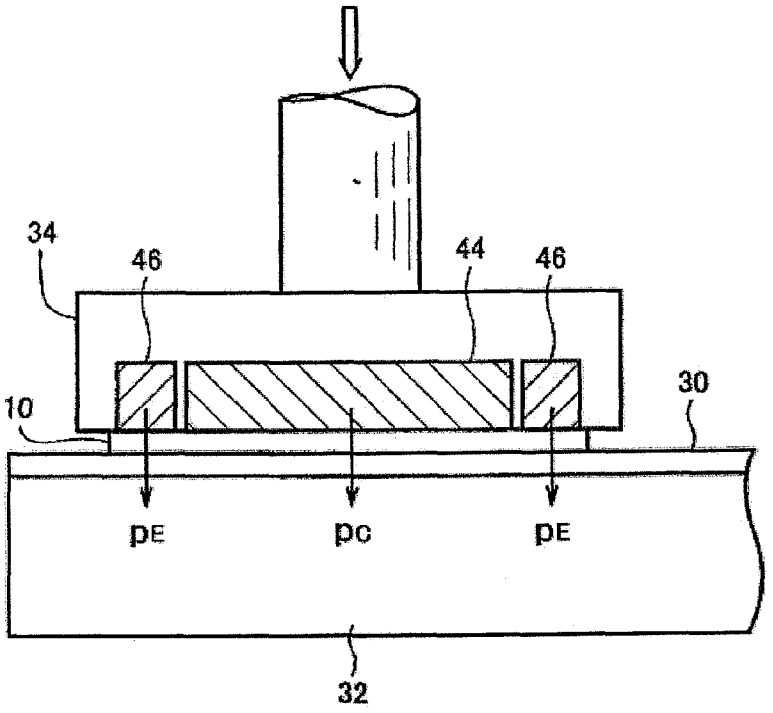


Figure 5.

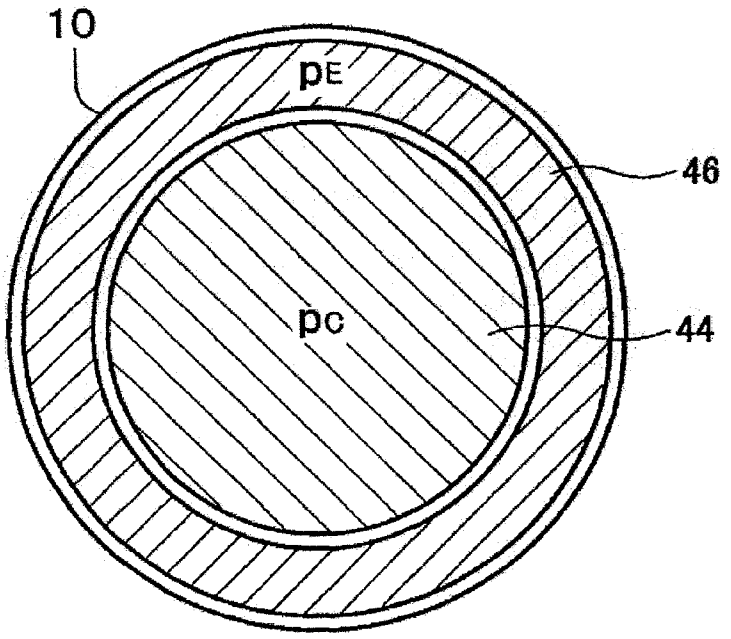


Figure 6.

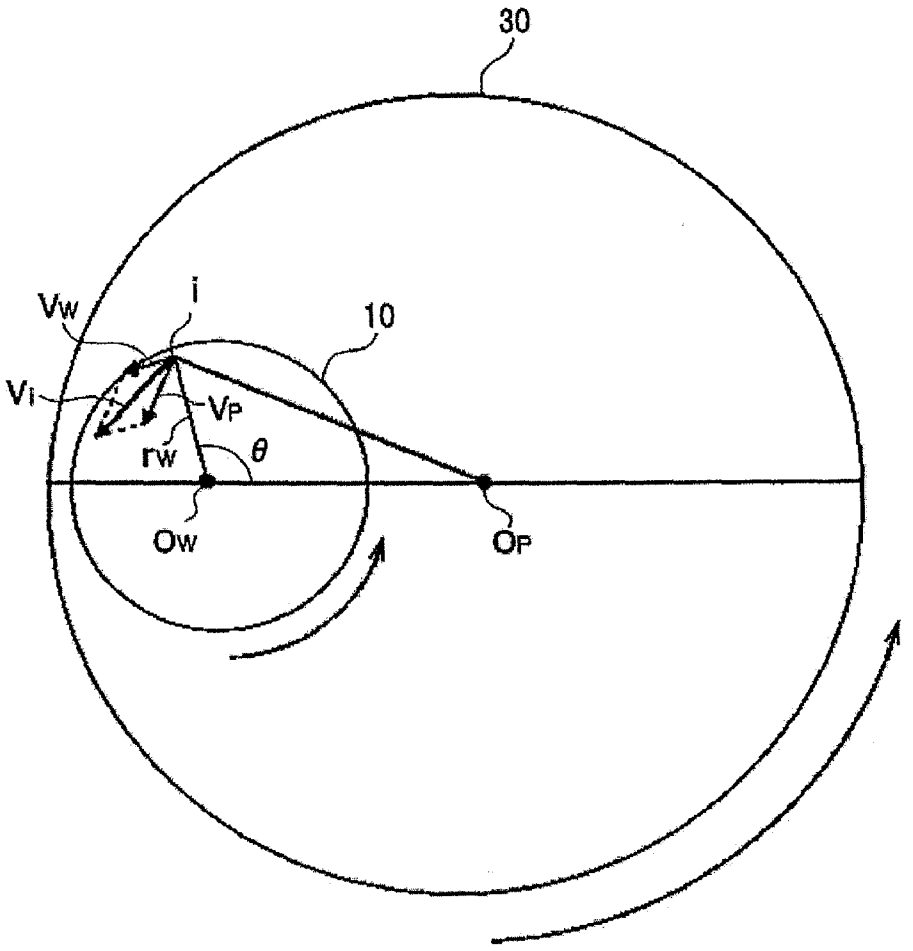


Figure 7.

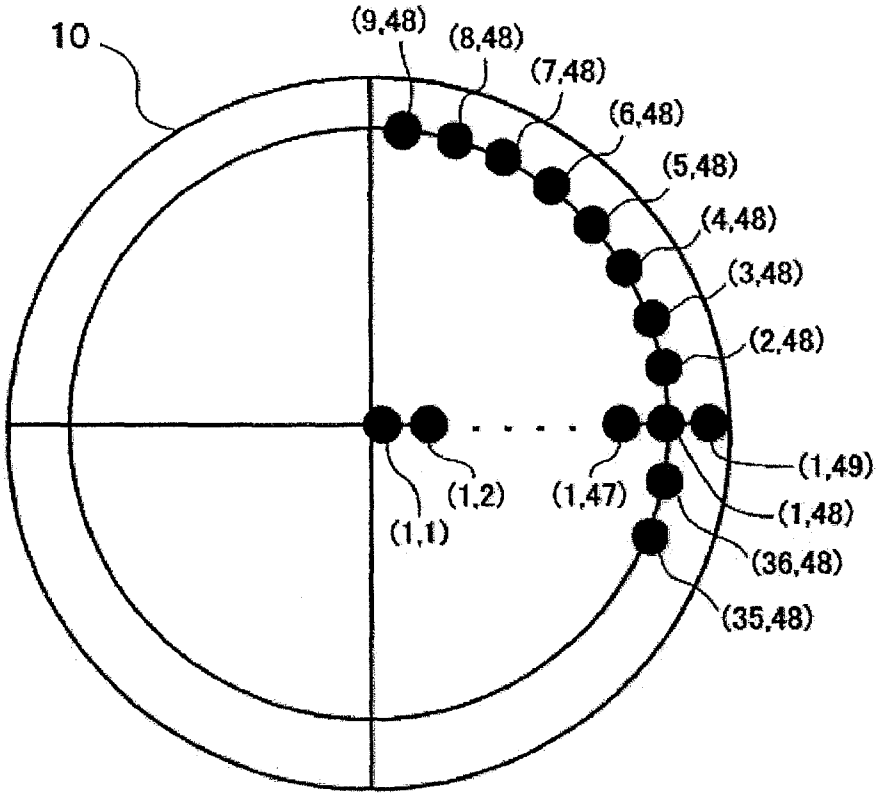


Figure 8.

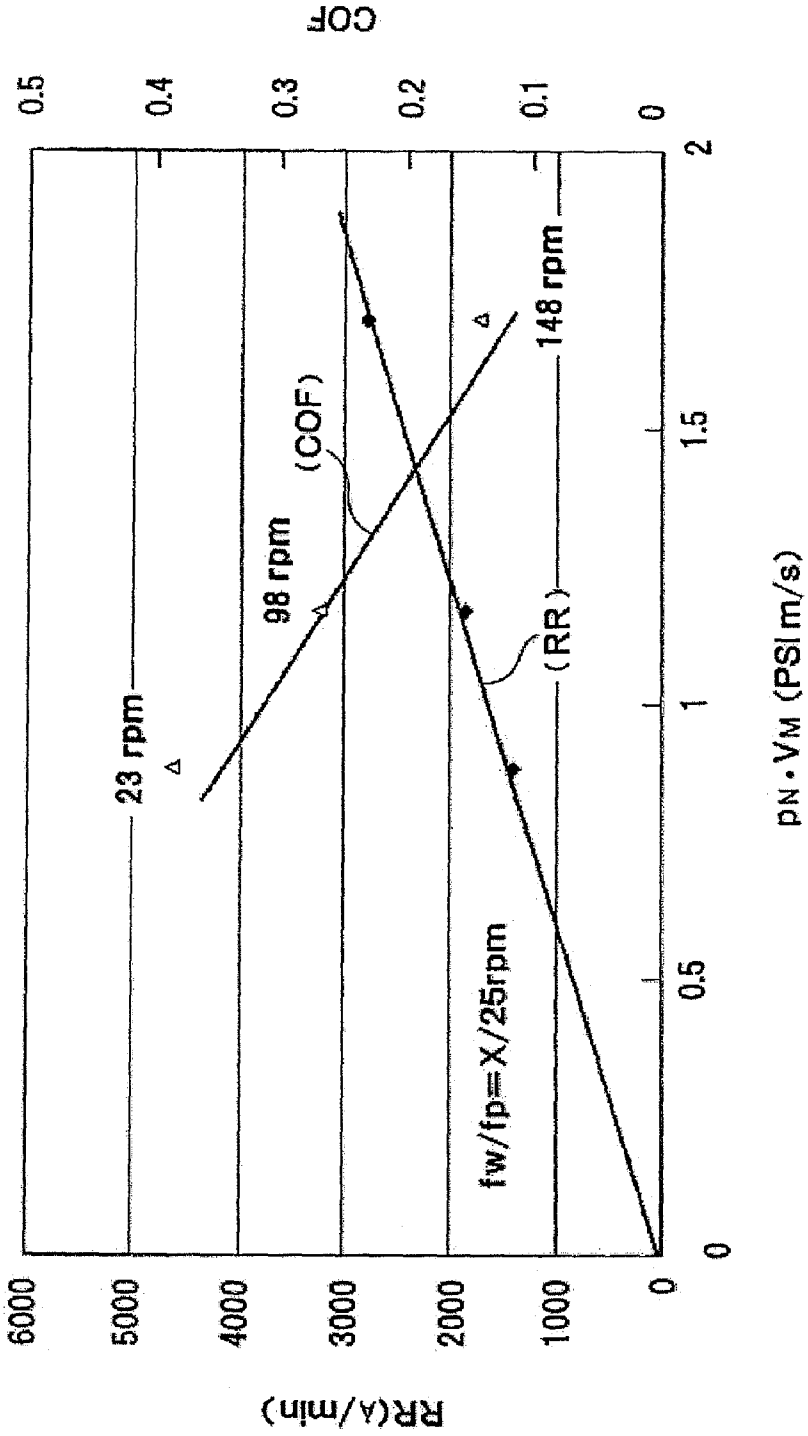

COF
0.5
0.4
0.3
0.2
0.1
0
2
1.5
1
0.5
0
$P_N \cdot V_M$ (PSI m/s)
RR(Å/min)
6000
5000
4000
3000
2000
1000
0
23 rpm
98 rpm
148 rpm
(COF)
(RR)
fw/fp=X/25rpm

Figure 9

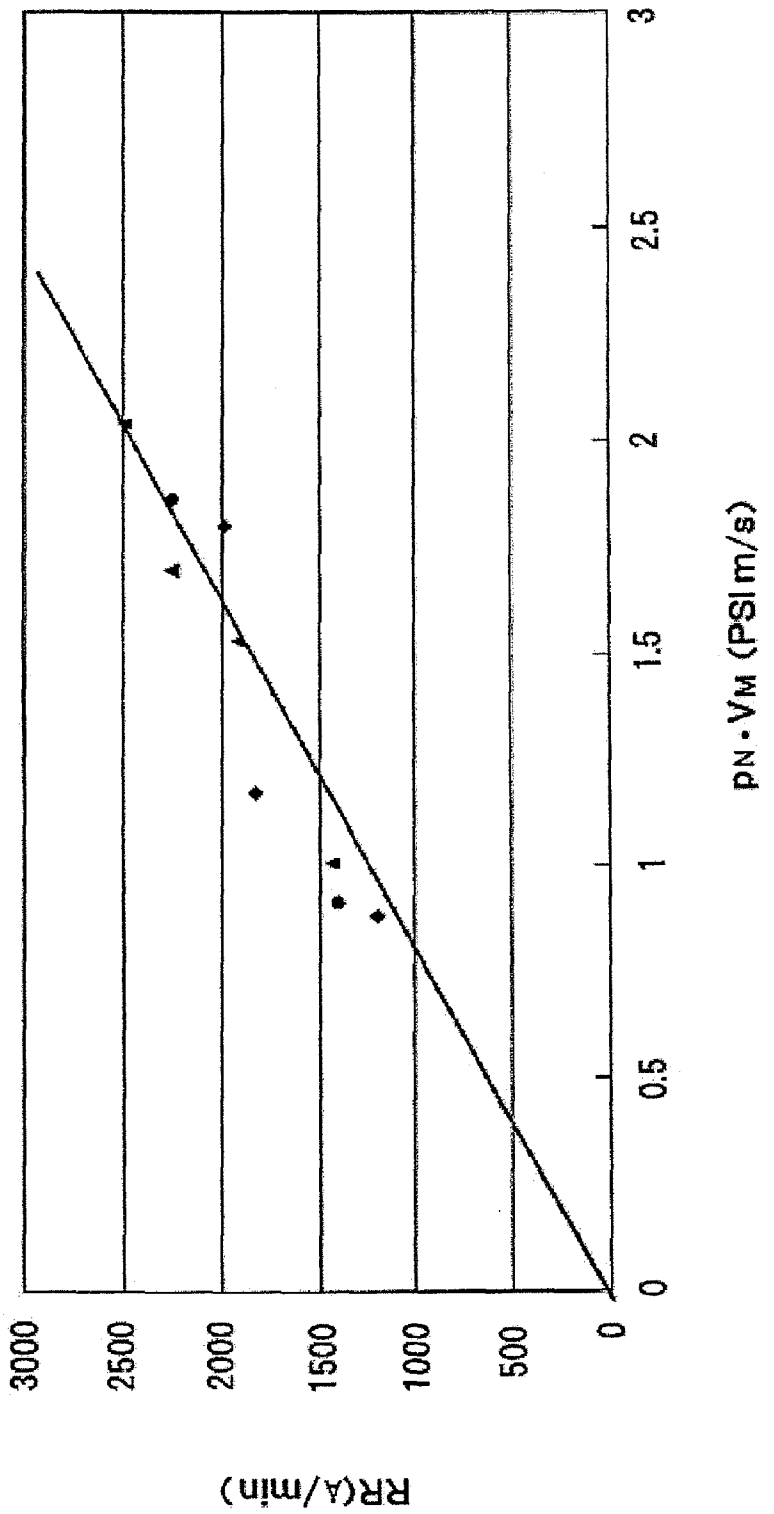


Figure 10

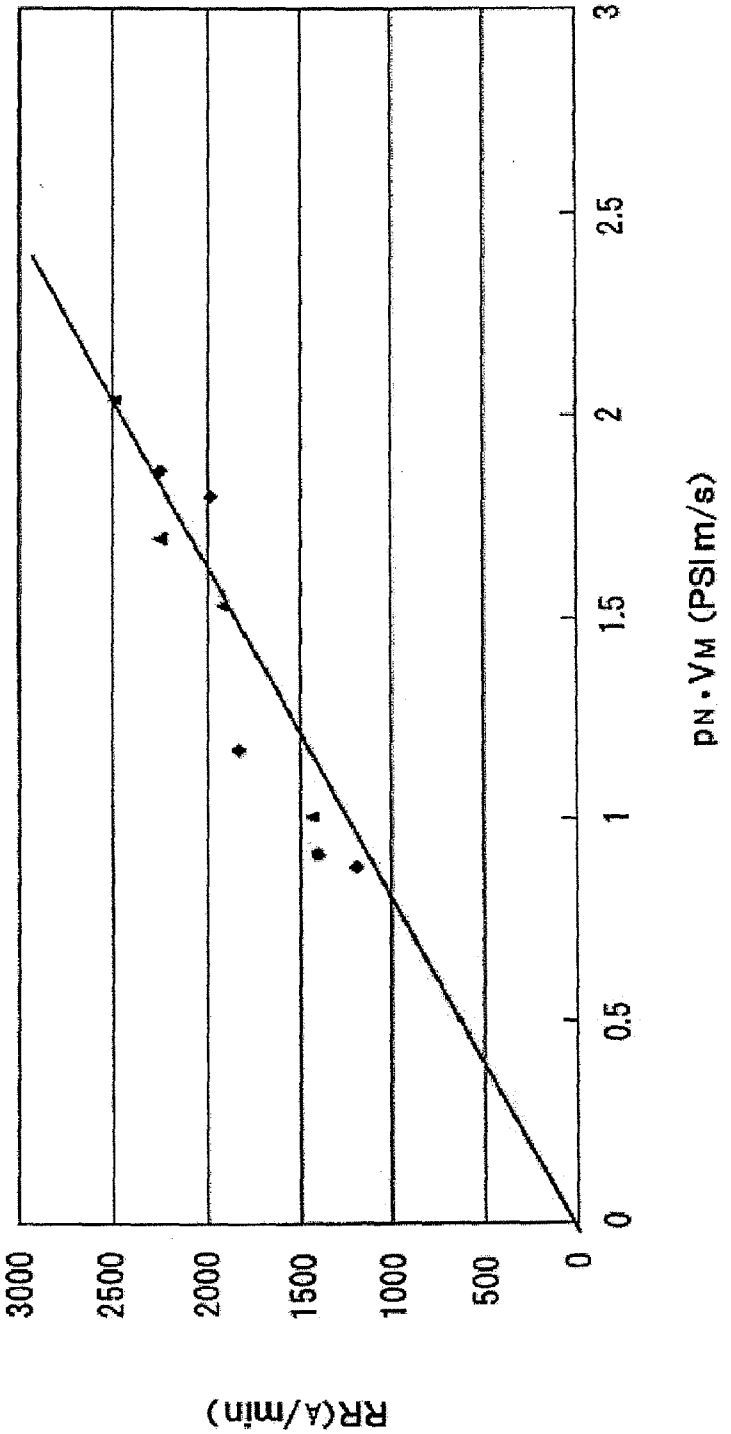


Figure 11

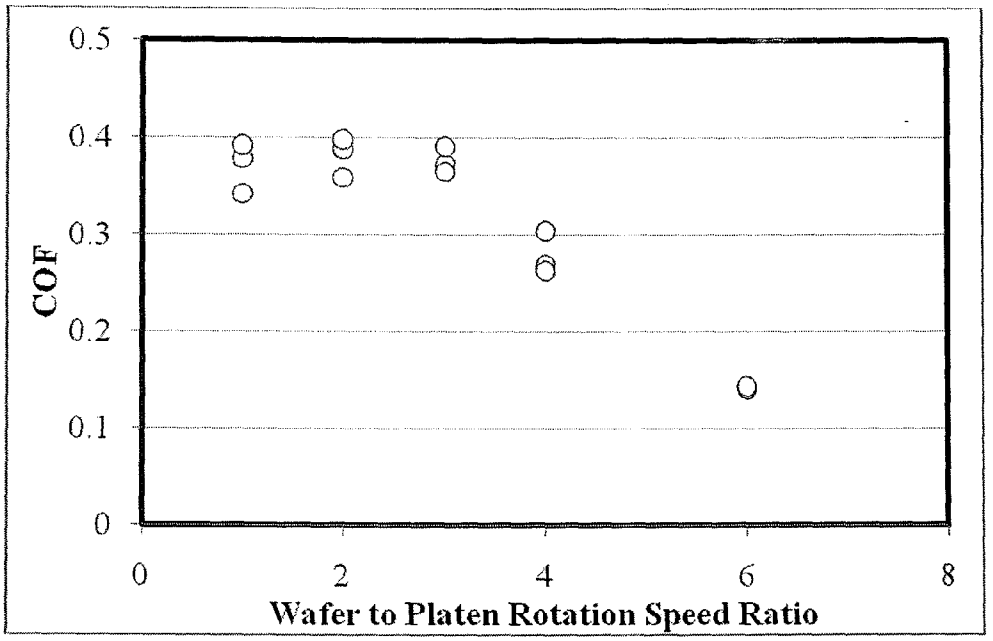
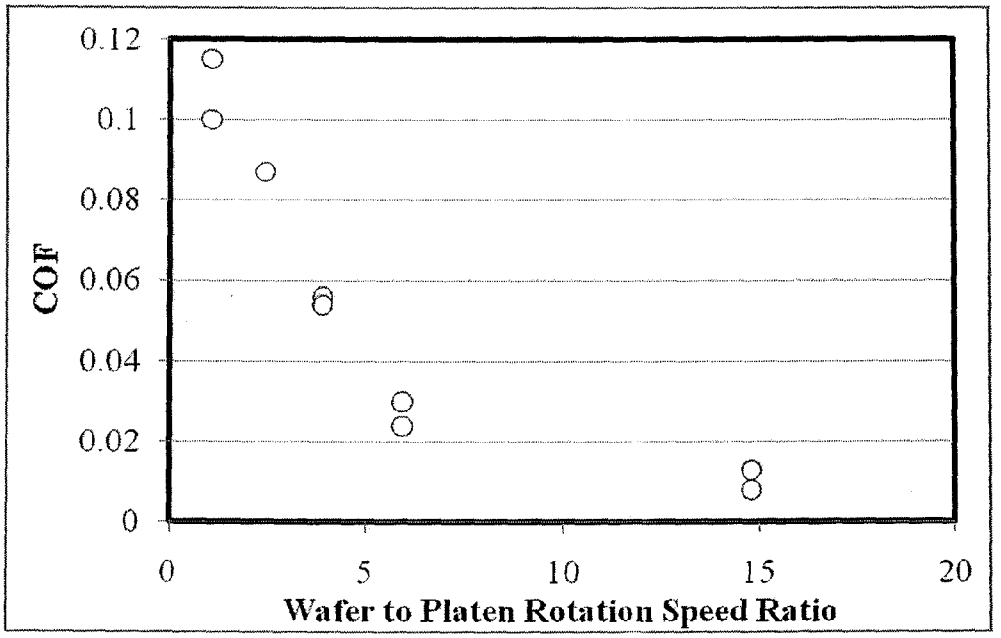


Figure 12



Figures 13

METHOD OF CHEMICAL MECHANICAL POLISHING

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a method of polishing the processed surface of a semiconductor wafer by mechanical polishing using the mutually rotary motion of the semiconductor wafer and the polishing pad and a chemical reaction. The present invention particularly relates to a superior method of chemical mechanical polishing (CMP) using a damascene process to shape the copper wiring embedded in an interlayer dielectric comprising a low-k organic membrane.

FIELD OF THE INVENTION

[0002] Today's integrated circuits, particularly large scale integrated circuits (LSI), possess multilayer wiring structures comprising multiple stacked circuit layers to increase the degree of miniaturization and integration. The process of forming the wiring of the prior art in multilayer wiring structures is that of forming a metal wire pattern by lithography or dry etching of aluminum and the like accumulated on the dielectric membrane. However, the fact that the electromigration resistance of the aluminum wiring is low or the electrical resistance is relatively high causes delay and the like present problems. Recently, based on this, copper wire Damascene processes are used in processes for fabrication of multilayer wiring.

[0003] To increase the computation power of LSI and to lower their electrical power consumption, it is necessary to minimize the capacitance between multilayer wires. This can be achieved by requiring the incorporation of a low dielectric (low-k) membrane as the layer insulating membrane. Low-k membranes of SiOF and the like that are made of inorganic materials have been studied for LSI. However, organic materials like fluorine resin membranes or amorphous fluorocarbons and the like that obtain relative dielectric ratios of 2.5 or less are thought to be desirable.

[0004] A damascene process for copper wires using an organic low-k membrane as the layer insulation membrane is explained in FIG. **1**.

[0005] First, on top of semiconductor wafer **10** formed to the lower level wiring (not shown in the diagram) as is shown in FIG. **1** (*a*), **12**, an etch-stop membrane **16** composed of, for example, SiCN, and organic low-k membrane **14** made from, for example, amorphous fluorocarbon **18** are laminated by chemical vapour deposition methods, or CVD, in the order of from the bottom, **12**→**14**→**16**→**18**.

[0006] Next, lithography processes and etching processes are carried out alternatively in repetition and as is shown in FIG. **1***b*, on?in? the top layer low-k organic membrane **18** a wire structure **20** is formed and on the bottom layer, a low-k organic membrane **12** is formed via through holes **22***s*. Here, pronounced areas and declivities are formed corresponding wiring structure **20** on the surface of semiconductor wafer **10** and through holes **22**.

[0007] Next as is shown in FIG. **1**(*c*) a membrane formation by CVD creates barrier metal **24** composed of, for example, TaN on the surface of semiconductor wafer **10** containing the center of through holes **22** and wiring structure **20**. Additionally, a copper sheet layer is formed by sputter method (not shown in the Figure) on top of barrier metal **24**.

[0008] Next, as shown in FIG. **1**(*d*) copper **26** is accumulated by electroplating on the top of semiconductor wafer **10** so that the center of through holes **22** and wiring structure **20** are filled. After copper electroplating, the wafer surface topography corresponding to wiring structure **20** and through holes **22** are reflected on the surface of copper **26**.

[0009] Copper **26** on the top of semiconductor wafer **10** is planarized by CMP. As shown in FIG. **1**(*e*), copper **26** remained only in the center of through holes **22** and wire structure **20**. An embedded copper wiring system is thus formed.

[0010] The Damascene process as stated above is a dual damascene method where copper wires and copper plugs are formed at once (i.e. copper **26** embedded at through holes **22** and wiring structure **20** at the same time). In comparison, a single damascene method forms copper wires and copper plugs in two separate processes. In those two separate processes, similar CMP process as are used in the dual damascene process are employed to remove overburden copper layer other than in the holes and structures.

[0011] FIG. **2** shows a schematic of a CMP. This CMP equipment presses the rotating head or carrier (upper fixed plate) **32** solidly holding the semiconductor wafer **10** against the rotating table (lower fixed plate) **34** to which is attached the polishing cloth or polishing pad **30**, so that while carrier **34** and rotary table **32** are each independently rotated, liquid slurry (polishing agent) is applied to polishing pad **30** from nozzle **36**, so that by chemical processes and mechanical polishing the lower face of semiconductor wafer **10** (processed surface) membrane is removed and the wafer surface is planarized (FIG. **3**). In the examples in the Figures, so as to polish the semiconductor wafer **10** by the polishing pad **30** which normally needs to maintain a rough surface condition during polishing, a diamond pad (conditioner) **38** is pressed against the polishing pad **30** at a position separated from semiconductor wafer **10** and this, while scanning in a radial direction, removes the surface of polishing pad **30** and roughens it.

[0012] The polishing rate of CMP like that above is reported by the Preston Equation for the proportion between the velocity generated by the polishing pad **30** rotation rate and the load pressing semiconductor wafer **10** on the polishing pad **30** with the semiconductor wafer fabrication rate. Up until now, from the standpoint of good uniformity of the polishing speed on semiconductor wafer **10**, together with holding the application of pressure at a constant rate, to make the aforementioned wafer fabrication rate uniform, the rotation rate of each of semiconductor wafer **10** and polishing pad **30** are made roughly the same.

SUMMARY OF THE INVENTION

The Problem to be Solved by the Present Invention

[0013] When polishing copper using the CMP equipment aforementioned (FIG. **2**) according to the methods of the prior art like those described above for the damascene process for copper wiring using organic low-k membranes in the interlayer insulation membranes (methods where rotation rates of wafer and polishing pad are similar), for example as shown in FIGS. **4**A and **4**B, peeling occurs at the boundary surfaces of fluorocarbon membranes (organic low-k membrane) **14** and **18** and etch-stop membranes **12** and **16** producing gap **40**, and as a result of CMP the scratches **42** on surface of copper **26** or fluorocarbon membrane **18** are easily produced which is a

problem. If this kind of membrane peeling or scratch occurs on a damascene interlayer insulation membrane and or embedded wires, the transmission characteristics of high frequency electrical current that flows along the surface of the wires (signal) or wire electrical properties are very greatly influenced and in some cases the LSI in question becomes defective.

[0014] In damascene processing, given that the polishing material copper is a relatively soft metal, and because the Young ratio of fluorocarbon membranes (organic low-k membranes) forming the interlayer insulation membrane is low, addition of a large shear stress due to the friction between the semiconductor wafer surface **10** and the polishing pad **30**, will more easily result in damage such as the aforementioned peeling of the fluorocarbon insulation membrane or scratches to the copper and the like.

[0015] The present invention solves the aforementioned problems of the prior art and possesses the objective of providing a chemical mechanical polishing method that increases polishing performance without damaging the material of the wafer being polished or the lower membranes by lowering the shear stress added to the semiconductor while increasing the polishing speed.

[0016] To achieve the aforementioned objective, a chemical mechanical polishing method from the standpoint **1** of the present invention, is a chemical mechanical polishing method that, while rotating the semiconductor wafer and the polishing pad respectively and pressing the said semiconductor wafer against said polishing pad, supplies slurry to the contact boundary between the said wafer and the said pad, and chemically and mechanically polishes the processed face of the semiconductor wafer, characterized by a ratio of rotation rate of the aforesaid semiconductor wafer to the aforesaid polishing pad of greater than 2:1.

[0017] Moreover, the chemical mechanical polishing method from standpoint **2** of the present invention is a chemical mechanical polishing method for the overburden copper layer on the aforementioned semiconductor wafer in a damascene process for making copper wiring using an organic membrane with a low dielectric in the interlayer insulation membrane of the said semiconductor wafer, and is characterized by making the ratio of rotation rate of the aforesaid semiconductor wafer to the aforesaid polishing pad greater than 2:1, while rotating the semiconductor pad and while rotating the said semiconductor wafer and the said polishing pad thusly presses the said semiconductor wafer to the said polishing pad and supplies slurry to the contact surface between the said wafer and the said pad and thus chemically and mechanically polishing the processed surface of the said semiconductor wafer.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0018] The inventor(s) of the present invention in order to solve the problem of scratches, peeling and other deformation formed on lower layers of semiconductor wafers by shear stress during CMP have with considerable effort and investigation developed the method of the present invention.

[0019] More particularly, they have devised a chemical mechanical polishing method in which, while a semiconductor wafer is pressed on a polishing pad and each are rotated, slurry is provided to their contact surface and the processed surface of the said semiconductor wafer is chemically and mechanically polished, a method for chemical mechanical polishing wherein the ratio of the rotation rate of said semiconductor wafer and the rotation rate of the said polishing pad are 2:1 or more.

[0020] The method of the present invention has been developed in response to the present state of the art, and, in particular, in response to the problems and needs in the art that have not yet been fully solved by currently available CMP methods for reducing the level of scratching, peeling and other damage to lower layers and membranes within the semiconductor wafer caused by shear stress induced by the rotation of the semiconductor wafer surface and the polishing pad against each other. Thus it is an overall objective of the present invention to provide a method for CMP that achieves significant reduction in the scratch, peeling and other damage to lower layers in the semiconductor wafer during the CMP process.

[0021] The purpose of the method is to allow the consistent production of a significantly higher quality of LSI and other polishing products without significantly increasing the expense or difficulty of operation of the CMP process.

[0022] Through application of the method of the present invention, the consistent production of a significantly higher quality of LSI and other polishing products without significantly increasing the expense or difficulty of operation of the CMP process has been achieved.

[0023] All dimensions in the present invention are based on a pad size of about 20" to 30" in diameter and a wafer size of between [8"] and [12"] in diameter and may be altered as needed in proportion to changes in the size of the polishing pad and wafer used. The specific dimensions given herein are in no way limiting but are by way of example to demonstrate an effective embodiment of the invention. For the avoidance of doubt, dimensions include, without limitation, dimensions of parts, flow rates, measurement of damage, rates of rotation and velocities.

[0024] In the CMP polishing equipment used by the chemical mechanical polishing method of the present invention, when the rotation rate of the semiconductor wafer, fw, and/or the rotation rate of the polishing pad, fp, are increased, the composite velocity (the average over the wafer), Vm, of the speed, Vp, generated by the rotation of the polishing pad and the speed, Vw, generated by the rotation of the semiconductor wafer increases and RR, the polishing speed (average value over the wafer) increase in rough linear proportion to $Pn \cdot Vm$. Here Pn is the load pressure pressing the semiconductor wafer onto the polishing pad. (normally this is a constant value).

[0025] On the one hand, the coefficient of friction, COF (average value over the semiconductor wafer), to the extent that the ratio of the rotation rate of the semiconductor pad to the rotation rate of the polishing pad is within the scope of being smaller than 2:1 will not change greatly even if $pn \cdot Vm$ increases, and continues to take values in excess of a constant value. However, if the ratio of semiconductor rotation rate, fw, and polishing pad rotation rate, fp, is larger than 2:1, the coefficient of friction (COF) decreases to the degree that the ratio increases and it decreases strikingly when the said ratio is larger than 4:1.

[0026] According to the present invention, under the conditions of $2\ fp<fw$, or more preferably $4\ fp<fw$, by the increase in $pn \cdot Vm$ the wafer's polished material or the underlying membranes (particularly organic membranes like the fluorocarbon membrane) are not damaged and then it is possible to increase polishing efficiency.

[0027] Additionally, under conditions of fw>2 fp, if the difference between fw and fp becomes too large, because the polishing speed RR variation becomes excessively large, from this standpoint, a range of 2 fp<fw<15 fp is preferred, and from the standpoint of achieving surely a broad decrease in COF, a range of 3 fp<fw<8 fp is preferred and 4 fp<fw<8 fp is more preferred.

[0028] If the rotation rate of the polishing pad, fp, is too high, it becomes too easy to scatter the slurry (outside the area of its useful application) and the efficiency of usage of slurry declines. Because, if the pad rotation rate declines too greatly, the polishing speed RR declines, and rates between 20 rpm and 70 rpm are preferred.

[0029] Moreover, it is preferred that the rotation direction with respect to the rotation axis of the semiconductor wafer and the polishing pad respectively be the same. For example, when the polishing pad is rotating counter-clockwise, it is preferred that the direction of rotation of the semiconductor wafer selected be counter-clockwise as well. Additionally, it is possible to reverse the rotation directions of both the semiconductor wafer and the polishing pad

[0030] Moreover, in a manner suitable to the present invention, the entirety of the polished surface of the semiconductor wafer may be pressed to the polishing pad in an area offset to the outside in terms of radial direction from the center of rotation of the polishing pad.

[0031] Moreover, in a manner suitable to the present invention, the pressure pressing the semiconductor wafer to the polishing pad is relatively higher at the central portion of the wafer than at the periphery of the wafer. That is to say, in the semiconductor wafer, the pressure on the semiconductor may be modified by multiple wafer pressure control. For example, though the pressure on the wafer surface need not be varied, the pressure applied to the central portion of the wafer is in comparison with the pressure received by the wafer periphery may also be set or regulated at a ratio of between 1.1 and 3 times or more preferably between 1.3 and 2.5 times.

[0032] Moreover, the slurry flow rate of the present invention is not particularly limited and any slurry flow rate suitable for CMP polishing may be used, however, from the standpoint of efficiency of slurry use, a slurry flow rate of 300 m/min in a manner suitable to the present invention or less is preferred".

[0033] The chemical mechanical polishing method of the present invention, in a preferred embodiment, is applicable to damascene process for forming embedded copper wiring, and, without limitation, can be applied, for example, in a damascene process as in FIG. **1**, to a CMP process for planar polishing (FIG. **1** (*d*)→**3**(*e*)) of accumulated copper **26** on an amorphous fluorocarbon membrane (low-k organic membrane) **18** in semiconductor **10**. It may also be applied to SiOF or SiO_2 surfaces. In this case, it is possible to use, ideally, the CMP device in FIG. **2**

[0034] This CMP equipment fixes semiconductor wafer **10** facedown to rotate in same fashion/direction as carrier **34**, and also attaches polishing pad **30** to revolving table **32** (diameter) whose diameter (diameter) is several times larger than that of semiconductor wafer **10**. A holding means to fix semiconductor itself to carrier **34** so that it remains freely removable, for example a backing film (now shown in the Figure) is supplied.

[0035] Additionally, carrier **34** may possesses or carry a function or mechanism that maintains the desired distance between the central and peripheral parts of the wafer of load applied where the semiconductor wafer **10** presses on polishing pad **30** on rotating table **32**. For example, as shown schematically in FIG. **5** and FIG. **6**, pressure addition parts **44** and **46** to add distinct pressures Pc and Pe to the center of the disc and the periphery of the disc respectively of semiconductor wafer **10** are supplied to the interior of carrier **34**. In this embodiment, setting or regulation is carried out so that the pressure Pc applied to the center of the wafer is larger than the pressure Pe applied to the outer part of the wafer, at least 1.1 times, and preferably 1.3 times or more and more preferably 2 times or more.

[0036] The CMP process presses the entire polished surface of semiconductor wafer **10** on the area offset to the outer radial direction from the center of revolution of polishing pad **30**, and revolves polishing pad **30** and semiconductor wafer **10** respectively. Normally, the direction of revolution of both are selected so that they rotate in the same direction around their respective axes. For example, looking from above, when polishing pad **30** is rotated in a counter-clockwise direction, the direction of rotation of semiconductor wafer **10** is also selected to be counter clockwise.

[0037] As shown in FIG. **7**, in the mutual rotary movement by Polishing Pad **30** and semiconductor wafer **10**, when you focus on a certain point, composite speed Vi of polishing pad **30** and semiconductor wafer **10** at one point i on the wafer, is determined primarily from the respective rotation rates fw and fp and the position (coordinates) of that point. Accordingly, the average composite speed Vm on the surface of the wafer can be provided theoretically by the following formula (1)

Formula (1)

$$V_M = \frac{\int_0^{2\pi}\int_0^{Rw} Vi\, dr_w\, d\theta}{\pi Rw^2} \tag{1}$$

However, Rw is the radius of semiconductor wafer **10**.

[0038] The operation of the above formula (1) is very complicated and intricate. So it is also possible, as is shown in FIG. **8**, to select a suitable number of representative points on the wafer discretely over an even density, and to use the average value of composite speed Vi in these representative points as the average composite speed Vm on the surface of the wafer. The average determination method of FIG. **8** selects 49 points on the wafer surface at a constant separation interval (for a 200 mm diameter wafer the separation is 2 mm) and selects 36 representative points on the wafer azimuthal directions with a fixed angular separation (10 degrees separation).

[0039] As stated below, to the extent that the average composite speed Vm on the surface of the wafer **10** is raised, the polishing removal rate (RR) becomes higher with regard to it. In the prior art, under the condition that as the fw (the wafer rotation rate) is approximately the same as fp (the pad rotation rate) the average composite speed Vm is increased and the RR increased accordingly. However, when, as stated above, a large stress was added to the polished surface of the wafer surface **10**, by this, there is the danger of the fluorocarbon membrane (low-k organic membrane) or other membrane or layer **12** and distortion or scratches and the like in copper **26** or fluorocarbon or other membrane or layer **18**.

[0040] In regard to this, the present invention, in relation to the ratio of the rotation rate, fp, of the polishing pad **30** as compared with that of the rotation rate, fw, of the semiconductor wafer **10**, has a lower limit of 2 fp<fw and a most appropriate condition of 4 fp<fw<8 fp.

[0041] Below, in connection with FIGS. **9-11**, are shown the characteristics of the polishing speed RR (the value for the

surface of the wafer) or the coefficient of friction (COF) (the value on the surface of the wafer) in these embodiments when the average composite speed Vm being changed by selecting as parameters the rotation rate, fw, of the semiconductor wafer **10** and/or the rotation rate, fp, of polishing pad **30**. Additionally, between the coefficient of friction, COF, and the shear force, Fs, if the vertical load is made pN, the there esists relationship described by the following the formula (2)

$$COF=Fs/pN \quad (2)$$

[0042] [FIG. **1**.] A Figure showing the damascene process for copper wiring using organic low-k dielectric membranes in the interlayer insulation membrane. FIGS. **1** *a, b, c, d*, and *e* represent from the same viewpoint different stages in the wafer manufacture and CMP process.

[0043] [FIG. **2**.] A diagonal view Figure showing a the structure of a representative CMP device (tool)

[0044] [FIG. **3**.] A cross sectional Figure showing the contact between the semiconductor wafer and the polishing pad during CMP polishing.

[0045] [FIG. **4**A] A simplified cross sectional drawing showing an example of a defect produced by CMP of a damascene process using a chemical mechanical polishing method of the prior art.

[0046] [FIG. **4***b*] A diagonal drawing showing an example of the above defect.

[0047] [FIG. **5**] A simplified cross sectional drawing showing schematically the structure of the pressure application mechanism of the carrier in the CMP device using a chemical mechanical polishing method embodiment.

[0048] [FIG. **6**] A simplified horizontal drawing showing how the form of the pressure added differed (pressure distribution) between the center and the periphery of the wafer according to the pressure addition method of FIG. **5**.

[0049] [FIG. **7**] A Figure showing the composite speed at one point of the wafer and the situation of mutual revolutions of the polishing pad and the semiconductor wafer in the embodiment.

[0050] [FIG. **8**] A Figure showing a method requiring simply the average composite speed on the wafer in the embodiment.

[0051] [FIG. **9**] A Figure showing the rotation speed RR and the coefficient of friction COF characteristics in the embodiment.

[0052] [FIG. **10**] A Figure showing the rotation speed RR characteristics in the embodiment.

[0053] [FIG. **11**] A Figure showing the COF characteristics in Example 1.

[0054] [FIG. **12**] A Figure showing the COF versus wafer to platen speed ratio characteristics in Example 1

[0055] [FIG. **13**] A A Figure showing the COF versus wafer to platen speed ratio characteristics in Example 2

Example 1

[0056] Below, a preferred embodiment of the invention will be explained referring to the drawings.

[0057] The main conditions of this CMP process are as follows.

[0058] (i) semiconductor wafer **10**—diameter 200 mm blanket copper membrane attached.

[0059] (ii) polishing pad Rohm and Haas IC1000® with K-groove design, with diameter of 800 mm. The polishing pad was installed on top of Suba IV® sub-pad.

[0060] (iii) Polishing agent Hitachi Kasei Kogyo Corp. HS-H-635-12®. Mixing ratio is Polishing agent:H_2O:H_2O_2=7:7:6. Slurry flow rate of 300 ml/min.

[0061] (iv) Loading—vertical force p_N=1.5 PSI Wafer central pressure p_C=1.8 PSI, wafer peripheral pressure p_E=1.3 PSI

[0062] FIG. **9** shows the characteristics of RR and COF obtained by carrying out CMP processes fixing the rotation rate of the pad, f_p, under the aforementioned process conditions as 25 rpm, and selecting the rotation rate of the wafer, f_w, at the three values of 23 rpm (f_w: f_p=apprx 1:1), 98 rpm (f_w:f_p=apprx 4:1), and 148 rpm (f_w:f_p=apprx 6:1). Moreover, the horizontal axis, of $p_N \cdot V_M$ shows P_N (vertical force)×V_M (average composite speed). In each CMP process, the rate of rotation of the pad, f_p, and the rate of rotation of the wafer, f_w, from the beginning of the process to the end are each held constant.

[0063] As in the Figures, with the pad rotation rate, fp,=25 (constant), and raising the rotation rate, fw, of the wafer from 25 rpm→98 rpm→148 rpm, (A) $p_N \cdot V_M$ rises from about 0.89 PSI·m/s→1.18 PSI·m/s→1.70 PSI·m/s, (B) Polishing Speed RR rises from 1400 Angstrom/min→1800 Angstron/min→2750 Angstrom/min and (C) COF declines from about 0.38→about 0.22→about 0.17.

[0064] Here, the phenomena (A), (B) although these are experimental results, are within the scope of prediction, and the aforementioned (C) COF was outside the scope of prediction. That is to say, the COF values of FIG. **9** are indices of the motive friction or the friction of the respective rates of rotation of the semiconductor **10** and the polishing pad **30**. Generally, the frictional force between two bodies moving mutually is the COF, X the vertical force, and the COF is not thought to be very related to the rate of the movement. Accordingly, even if $p_N \cdot V_M$ increases, it is common sense to assume that COF will not change greatly. In fact as shown in FIG. **11** and FIG. **12**, COF determination versus wafer platen speed ratio, as explained later, under the conditions of fw<2 fp, even if $p_N \cdot V_M$ increases, results obtained for COF do not change much. However, if, under conditions of fw>2 fp, surprisingly, the aforementioned (C) phenomenon is observed.

[0065] So under the condition of COF descending below 0.3, it is possible to confirm strikingly the disappearance of peeling of fluorocarbon membranes **14**, and **18** (low-k organics) on the surface of the semiconductor wafer **10** and/or scratching of the copper **26** and/or fluorocarbon membrane **18**. Accordingly, the aforementioned phenomenon (C) is thought to generate material semiconductor wafer CMP process technical problems.

[0066] In this connection, when much of the experimental data obtained under conditions where there are anomalies in the rotation rate of the wafer, f_w, and/or the rotational numbers of polishing pads and/or number of rotations of the pad, f_p, is plotted, it may be observed that there is a basic linear relationship for both/

[0067] Moreover, when the plot of much COF data (measured index) obtained where the wafer rotation rate, fw, and/or the pad rotation rate, fp, changed within the scope of (f_w:f_p)=approximately (1:1) to (6:1), as shown in FIG. **11**, a strikingly vast distance is observed in COF characteristics between the region fw<2 fp and the region fw>2 fp. That is to say, in the region of fw<2 fp, even if the ratio of fw and fp (fw/fp) increases or $p_N \cdot V_M$ increases COF remains all but

unchanged. However, on the other hand, in the region of fw>2 fp to the extent the ratio of fw and fp (fw/fp) increases, COF decreases.

[0068] Thus, even in the region of fw>2 fp, if the difference between the wafer rotation rate, fw, and the pad rotation rate, fp, becomes too large, because of the scattering of the polishing removal rate on the wafer' surface, from this standpoint, 2 fp<fw<8 fp is preferred and 3 fp<fw<8 fp is more preferred. From the standpoint of obtaining COF of less than 0.3, 4 p<fw<8 fp is yet more preferred.

[0069] In addition, the slurry volume, although it is acceptable to select them optimally in conjunction with values other than $p_N \cdot V_M$, and they are not particularly limited from the standpoint of economy, 300 ml/min is preferred.

[0070] Moreover, although any load ratio between different regions on the wafer applicable to CMP may be used in the present invention, and there is no limitation, the ratio of the load on the center of the wafer pC and the load on the periphery of the wafer pE (pC/pE) is preferred within the range of 1 to 3 and more preferably within the range of between 1.3 and 2.5. In this embodiment, as written above, because the wafer center and the wafer periphery experience the application of different pressures, the independent pressure additions **44** and **46** are equipped on carrier **34**. However, it is also possible to use a carrier formed to have a constant ratio (for example, pC/pE=1.3) of the pressure applied to the center of the wafer and the pressure applied to the periphery of the wafer surface using one common pressure application part

[0071] If the rotation rate of polishing pad **30** is too high, the slurry utilization efficiency decreases. If it becomes too low, because the polishing removal rate is also low, the range of 20 to 70 rpm is preferred.

[0072] The Chemical Mechanical Polishing Method of the present invention, possesses the significant benefits, particularly for the copper damascene CMP process discussed above. However, it is possible to use it ideally even other CMP processes of semiconductor wafers having a processed surface and underlying organic membranes such as fluorocarbon membranes, and furthermore, it is possible to apply to any CMP processes on the semiconductor wafer.

Example 2

[0073] A trial was conducted according to the same conditions as Example 1 except that the polishing pad Rohm and Haas IC1000® possessed floral groove.

[0074] The results of COF determination versus wafer platen speed ratio are displayed in FIG. **13**. In this case the results show marked decline in COF starting from a ration of Wafer to Platen rotation speed of 2 ad it was possible to maintain this until the said ratio was at least 15. The precise parameters determining the ideal rations vary somewhat depending upon the condition and type of materials used and the cut-off should be determined based on the particular materials, apparatus and conditions being used.

EFFECTS OF THE INVENTION

[0075] According to the chemical mechanical polishing method of the present invention, by the above configurations and action, the shear stress acting on the semiconductor wafer decreases as the rate of the wafer rotation to the rate of pad rotation increases and the polishing efficiency is increased without damaging the wafer polished materials or the membranes beneath them.

SIMPLE EXPLANATION OF THE DRAWINGS

[0076] **10** semiconductor wafer
[0077] **14**, **18** amorphous fluorocarbon membrane
[0078] **26** copper
[0079] **30** Polishing pad
[0080] **32** rotary table
[0081] **34** carrier (rotary head)
[0082] **36** nozzle
[0083] **38** Diamond head (Conditioner)
[0084] **44**, **46** Pressure application part

What we claim is:

1. In a chemical mechanical polishing method for reducing damage to the wafer surface in which while a semiconductor wafer is pressed on a polishing pad and each are rotated, slurry is provided to their contact surface and the processed surface of the said semiconductor wafer is chemically and mechanically polished, a method for chemical mechanical polishing wherein the ratio of the rotation rate of said semiconductor wafer and the rotation rate of the said polishing pad are 2:1 or more.

2. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the processed surface layer of the said semiconductor wafer includes organic membranes under that layer.

3. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the processed surface layer of the said semiconductor wafer includes inorganic membranes under that layer.

4. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the processed surface layer of the said semiconductor wafer includes layers of SiO_2 and SiOF under that layer.

5. In a method for chemical mechanical polishing to remove in a planar fashion copper that has been accumulated on an organic membrane in a damascene process for copper wiring using an organic membrane with a low dielectric in the insulating interlayer membrane in the semiconductor wafer, a chemical mechanical polishing process that reduces damage to the wafer surface wherein the ratio of the rotation rate of said semiconductor wafer and the rotation rate of the said polishing pad is 2:1 or more and the said semiconductor wafer is pressed on the said polishing pad and each are rotated, slurry is provided to their contact surface and the processed surface of the said semiconductor wafer is chemically and mechanically polished.

6. The chemical mechanical polishing method of claim **2** or claim **5** wherein the said organic membrane is a fluorocarbon membrane.

7. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the ratio of the rotation rate of said semiconductor wafer and the rotation rate of the said polishing pad is 3:1 or more.

8. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the ratio of the rotation rate of said semiconductor wafer and the rotation rate of the said polishing pad is 4:1 or more.

9. The chemical mechanical polishing method of claim **5** wherein the ratio of the rotation rate of said semiconductor

wafer and the rotation rate of the said polishing pad is 8:1 or more

10. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the said pad rotation rate is from 20 rpm to 70 rpm.

11. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the said semiconductor wafer and the said polishing pad rotate in the same direction with respect to their respective rotation axes.

12. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the entire processed surface of the semiconductor wafer is pressed against the said polishing pad in an area offset in the outer radial direction from the center of the said polishing pad.

13. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **12** wherein the pressure by which the said semiconductor wafer is pressed to the polishing pad is relatively greater in the central part of the wafer than at the periphery of the wafer

14. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **12** wherein the pressure received in the central part of the said semiconductor wafer is 1.1 to 3 times the pressure received at the periphery of the wafer.

15. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **12** wherein the pressure received in the central part of the said semiconductor wafer is 1.3 to 2.5 times the pressure received at the periphery of the wafer.

16. The chemical mechanical polishing method for reducing damage to the wafer surface of claim **1** wherein the said slurry supply flow rate is 300 ml/min or less.

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