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(54) Title: SYSTEM AND METHOD OF USING A COMPLIANT LEAD INTERPOSER

(57) Abstract: The present invention relates to a compliant leaded interposer for resiliently attaching and electrically connecting a ball grid array package to a circuit board. The interposer may include a substrate, a plurality of pads, and a plurality of pins. The plurality of pads may be positioned substantially on the top surface of the substrate and arranged in a predetermined pattern substantially corresponding to the solder ball pattern on the ball grid array package. The plurality of pins may be positioned substantially perpendicular to the substrate and may extend through the substrate and the plurality of pads. The interposer may be configured to attach the ball grid array package to the circuit board such that each of the solder balls on the ball grid array package contacts at least a portion the plurality of pins and at least a portion of the plurality of pads and such that the each of the plurality of pins also connects to a contact on the circuit board.

SYSTEM AND METHOD OF USING A COMPLIANT LEAD INTERPOSER

FIELD OF THE INVENTION

[0001] The present invention is related to electromechanical leads connecting integrated circuit packages to printed wire boards, and more particularly to a method of attaching a compliant leaded interposer to a plastic ball grid array in order to compensate for non-coplanarity or warpage.

BACKGROUND OF THE INVENTION

[0002] Early attempts at mounting and connecting integrated circuits and semiconductor chips to printed wiring boards (PWBs) frequently resulted in unreliable connections. More particularly, attempts at connecting commercial-off-the-shelf ("COTS") large-size, high-pin-count ("HPC") plastic ball grid arrays (PBGAs) to PWBs included additional difficulties during attachment and use due certain characteristics to the PBGAs. Some of the COTS PBGAs display warpage and non-coplanarity, which may cause shorting and/or structural weaknesses after soldering. These difficulties may be enhanced or exaggerated when the PWBs are exposed to harsh environments, such as environments having thermal cycling and mechanical vibrations.

[0003] Non-coplanarity in a PBGA is measured by the largest distance between a given ball and a theoratical plane formed by three highest balls. Non-coplanarity may be observed by placing a PBGA on a flat plate or surface where only three balls make contact with the flat plate. The non-coplanarity prevents other balls from contacting the surface, leaving a gap. Non-coplanarity may, however, change during thermal cycling, depending in some cases on the thermal coefficient of expansion mismatch of the materials used in the PBGA, such as silicon, substrate, encapsulant, and die adhesive and structural inconsistencies.

[0004] In some cases, the COTS PBGAs, "as received" from the manufacturer, include non-coplanarity characteristics even at room temperature. COTS components, despite following commercial standards, may display deviations of 0.004 inch for a small-size COTS PBGA, which for 0.020 inch diameter solder balls indicates a 0.004/0.020 deviation or 20% non-coplanarity. For small-size COTS PBGA, this deviation, equaling approximately 1/5th of the height of the joint, results in a weak joint between corresponding contacts on the PBGA

and the PWB. For large-size COTS PBGA, the problem may be exaggerated with the deviation from coplanarity exceeding 0.006 in some cases. The PGBAs may experience additional warpage during soldering when localized temperatures may increase dramatically. For example, the soldering temperature may range from about 215°C to about 220°C for Tin63%:Lead37% solder and about 245°C to about 250 °C for lead-free Tin:Silver:Copper (SAC) alloy. At these soldering temperatures, previously planar PBGAs may experience new warpage and originally warped PBGAs may further deform, exacerbating the issue.

[0005] Figure 1A shows an example of a PBGA prior to soldering to a PWB. As shown in Figure 1, a PBGA 10 may include an encapsulant 11, a substrate 12 and solder balls 13. Although the PBGA 10 may be coplanar at room temperature when received from the manufacturer, the PBGA may warp during soldering when localized temperatures increase. As shown in Figure 1A, for most COTS PBGA the encapsulant 11 does not extend across the entire upper surface of the substrate 12. As such, the substrate 12 has been shown to experience localized warpage of the outer portions of the substrate 12 without the encapsulant 11 during soldering of the solder balls 13.

[0006] Figure 1B shows the effects of warpage on the quality of the solder joints. As shown, the PBGA 10 may warp during or after soldering, especially at the edges of the PBGA 10, with the substrate 12 departing from coplanarity. For example in Figure 1B, at the edges of the PBGA 10, a distinctive downward curve is shown. This downward warpage may cause shorts in the electrical circuits if the solder balls 13 flatten and touch one another as shown in Figure 1 when the PBGA is soldered to the PWB 30. Alternatively, if the PBGA is warped with an upward curve (not shown in the figures), the solder ball may fail to make contact with the PWB, resulting in a gap or open circuit.

[0007] If a warped or non-coplanar PBGA is received from the manufacturer and soldered to a PWB in the normal process, the warpage may be exaggerated during the soldering process and compound the problem. In COTS HPC PBGA, the warpage due to the soldering process may be difficult to predict due to several variables associated with the materials and processes. For example, the PBGA typically warps at the usual 215°C to 220°C soldering temperature. However, even when cooling from about 183°C, the temperature at which typical solder solidifies, to room temperature, the PBGA may continue to warp, inducing stress into the solder joints. Further, repeated thermal cycling, such as for example from -40°C to + 100°C, during actual use may induce additional warping in the PBGA and result in stressed solder joints due to repeated warping and unwarping actions.

[0008] Even if the induced warpage or non-coplanarity is not sufficient to cause a short or gap, a non-coplanar PBGA may induce greater stress and strain on the solder joints used to attach the PBGAs to the PWBs. Typically, PBGAs and PWBs have different thermal coefficients of expansion (TCE), resulting in problems when exposed to harsh thermally cyclic environments and vibration. When warped or non-coplanar PBGAs experience thermal expansion and contraction, the individual solder joints the PBGA to the PWB often experience different amounts of stress and strain. Stresses induced by thermal cycling, vibration and shock during use limit the life of the solder joint and the reliability of the system. Highly stressed, weak solder joints inherently include a lower life expectancy. Over time, degradation and cracking results at the solder joints from temperature cycling, especially where localized warping of the PBGA has already induced stress on the solder joints. As a result, the thermal expansion and contraction experienced by the solder joints increases with the amount of warpage of the PBGA, resulting in possible mechanical and electrical failure over time.

[0009] Previous attempts to connect certain components to PWBs have included the use of compliant leaded interposers. Such compliant leaded interposers have included etched leads, formed from thin copper leaf, which directly connect the electrical contacts on lightweight components, such as chip scale packages, to the electrical contacts on the PWB. An example of such a compliant leaded interposer is taught in US Patent No. 6,830,177. However, the thin etched leads of previously taught interposers are incapable of supporting larger components, such are large area grid array components. More particularly, the previously taught interposers fail to provide sufficient mechanical support and robustness for heavy PBGA components used in may advance electronic packages.

[0010] Therefore, it would be desirable to compensate for warpage or non-coplanarity in PBGA and to provide a robust mechanical and electrical connection between the PBGA and the PWB after soldering.

SUMMARY OF THE INVENTION

[0011] The present invention is related to a compliant leaded interposer for resiliently attaching and electrically connecting a ball grid array package to a circuit board where the ball grid array package includes solder balls arranged in a solder ball pattern. The compliant leaded interposer may include a substrate having a top surface and a bottom surface and a plurality of pads positioned substantially on the top surface of the substrate and arranged in a

predetermined pattern substantially corresponding to the solder ball pattern with each of the plurality of pads being associated with one of the solder balls. The interposer may also include a plurality of pins positioned substantially perpendicular to the top surface of the substrate and extending through the substrate and the plurality of pads. The plurality of pins may be arranged in the predetermined pattern with each of the plurality of pins being associated with one of the solder balls and each of the plurality of pins may include a first end configured to extend a first distance beyond the top surface of the substrate and a second end configured to extend a second distance beyond the bottom surface of the substrate. The interposer may be configured to attach the ball grid array package to the circuit board such that each of the solder balls contacts at least a portion the first end of one of the plurality of pins and at least a portion of one of the plurality of pads and such that the second end of each of the plurality of pins attaches to an associated contact on the circuit board.

[0012] In another embodiment of the present invention, a method of connecting a grid array package to a printed wiring board (PWB) includes the steps of aligning a compliant leaded interposer in an assembly tool. The interposer may include a plurality of pins positioned substantially perpendicular to a substrate and extending through the substrate. Each of the plurality of pins may include a first end configured to extend a first distance beyond a top surface of the substrate and a second end configured to extend a second distance beyond a bottom surface of the substrate. Further, each of the plurality of pins may include a pad aligned with the pin and positioned substantially on the top surface of the substrate. The assembly tool may include a plurality of holes in a plate member configured to receive the second end of the plurality of pins in a predetermined pattern. The method may also include the steps of orienting a plurality of solder balls on the grid array package with the first end of the plurality of pins using tooling pins mounted on the plate member of the assembly tool and electrically connecting each of the plurality of solder balls to the first end of one of the plurality of pins and to at least a portion of one of the plurality of pads. The method may then include removing the interposer and the ball grid array package from the assembly tool and orienting the second end of each of the plurality of pins with at least one conductive contact on the PWB. Finally, the method may include electrically connecting the second end of each of the plurality of pins to at least one conductive contact of the PWB thereby establishing an electrical connection between the ball grid array package and the PWB. The plurality of pins may define a space between the PWB and the bottom surface of the substrate of the interposer.

[0013] These and other objects and advantages of the invention will be apparent from the following description, the accompanying drawings and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] While the specification concludes with claims particularly pointing out and distinctly claiming the present invention, it is believed the same will be better understood from the following description taken in conjunction with the accompanying drawings, which illustrate, in a non-limiting fashion, the best mode presently contemplated for carrying out the present invention, and in which like reference numerals designate like parts throughout the Figures, wherein:

[0015] FIG. 1A shows a side view of a plastic ball grid array prior to soldering on a printed wiring board;

[0016] FIG. 1B shows a side view of a plastic ball grid array soldered on a printed wiring board;

[0017] FIG. 2 shows a top view of the compliant leaded interposer in accordance with one embodiment of the present invention;

[0018] FIGs. 3A shows a side view of the compliant leaded interposer shown in FIG. 2

[0019] FIG. 3B shows an enlarged side view of the a portion of the compliant leaded interposer shown in FIG. 3A;

[0020] FIG. 4A shows a top view of an assembly tool in accordance with another embodiment of the present invention;

[0021] FIG. 4B shows a side view of the assembly tool shown in FIG. 4A;

[0022] FIG. 5 shows the compliant leaded interposer of FIG. 2 positioned in the assembly tool of FIG. 4 with a ball grid array package positioned prior to soldering in accordance with one embodiment the present invention;

[0023] FIG. 6 shows the assembled compliant leaded interposer and the ball grid array in accordance with the present invention; and

[0024] FIG. 7 shows the assembled compliant leaded interposer and the ball grid array soldered to the printed wiring board in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0025] The present disclosure will now be described more fully with reference to the Figures in which various embodiments of the present invention are shown. The subject

matter of this disclosure may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein.

[0026] The present invention relates to a method and system for mounting plastic ball grid arrays ("PBGA") to circuit boards or printed wiring boards and more particularly to using a compliant leaded interposer for compensating for non-coplanarity or warpage of a PBGA.

[0027] Figure 2 shows an interposer 100 in accordance with one embodiment of the present invention. As shown, the interposer 100 includes an interposer substrate 110, copper pads 120, and compliant pins 130 (shown in Figure 3A). In accordance with the present invention, the substrate may be formed from a laminate material with or without fiber-glass reinforcement, which may be commercially obtained to match as closely as possible the TCE of the PBGA and/or ceramic ball grid array (CBGA). The substrate may also be formed from high temperature FR4 such as Nelco 4000-13. Other material known to those of skill in the art may be used including, but no limited to, Bismatemide Triazine (BT), Polyamide and Cyanate Ester. The copper pads 120 and the compliant pins 130 may be arranged in the pattern shown in Figure 2. As would be obvious to one of skill in the art, the arrangement of the pads 120 and pins 130 may be configured to match that of the PBGA and the PWB.

[0028] Referring to Figure 3A, a side view of the interposer 100 from Figure 2 is shown. The compliant pins 130 are configured to extend through the substrate 110 and the pads 120, extending a predetermined amount above the surface of the substrate 110. In accordance with one embodiment of the present invention, the compliant pins 130 may be 0.012 inches in diameter and 0.088 inches in length. The pins 130 may be formed from electrically conductive materials known to those of skill in the art such as Be:Cu alloy, pure copper, phosphorus bronze, and Cu:Be alloys. The pins may also be surface finished with materials known to those of skill in the art such as Ni:Au, Ni:Pd:Au, Sn:Pb, Ag and Sn, depending on the application. Further, the pins may include a less than 20 microinch gold finish.

[0029] As shown in Figures 3A and 3B, the pads 120 are positioned on only one side of the substrate 110. The copper pads may be formed from copper with a liquid solder mask or other suitable materials known to those of skill in the art. Further, in one embodiment, the pads 120 are configured at about a 0.025 inch diameter for each pad 120 if a pitch of 0.050 inch is used for spacing on the PBGA. If a 0.040 inch pitch is used, a diameter of about 0.020 inch may be used for the diameter of the pads 120. It should be understood that alternative pitches and pad sizes may be used without deviating from the scope and spirit of the present invention.

[0030] Figure 3B shows a blown up view of a portion of the interposer 100. A single compliant pin 130 is shown extending a distance B above the upper surface of the substrate 110, which includes a thickness A. The length C of the pin defines the total height of the interposer 100. The distance B may vary depending on the pitch used. For example, the distance B may be about 0.010 inch for a pitch of 0.050 inch and about 0.008 inch for a pitch of 0.040 inch. In accordance with one embodiment of the present invention, the thickness A of the substrate 110 may be about 0.010 inch and the length C of the pin may be about 0.070 inch to about 0.100 inch. It should be understood that other dimensions for the interposer may be used without deviating from the scope and spirit of the present invention.

[0031] Referring to Figure 4A, top view of a soldering tool 400 is shown. The soldering tool 400 includes four tooling pins 410 mounted on an alignment plate 420. In accordance with one embodiment of the present invention, the tooling pins 410 may be about 0.030 inch diameter. Further, the alignment plate 420 may include about 0.015 inch diameter holes 430, which are configured to match the pin pattern of the interposer footprint. The alignment plate 420 may be formed from about 0.060 inch aluminum plate or other suitable material known to one of skill in the art. As shown in Figure 4A, which shows a side view of the assembly tool, the tooling pins 410 may be configured to extend above the surface of the alignment plate 420.

[0032] Figure 5 shows a cross-section view of the PBGA 200, the interposer 100, and the soldering tool 400 with the PBGA 200 being aligned on the interposer 100 using the soldering tool 400. The PBGA 200 is shown positioned between the tooling pins 410, allowing the PBGA 200 to be properly aligned over the interposer such that the soldering balls 230 are aligned with the compliant pins 130 of the interposer 100. The pins 130 of the interposer 100 are shown aligned and inserted into the holes 430 of the alignment plate 420 of the soldering tool 400. Once aligned and positioned as shown in Figure 5, the soldering balls 230 of the PBGA 200 may be soldered to the interposer 100 using soldering processes and techniques known to those of skill in the art.

[0033] Although not visible in Figure 5, it should be understood that the copper pads 120 of the interposer 100 are positioned on the top surface of the interposer 100 and are intended to make contact with the soldering balls 230 once soldering is complete. The solder balls 230 of the PBGA 200 may be formed from Tin 63%:Lead 37% with a soldering temperature of 215°C to 220°C or lead-free Tin:Silver:Copper (SAC) alloy solder with a soldering

temperature of 245°C to 250 °C. Alternatively, other solders may be used without deviating from the scope and spirit of the present invention.

[0034] The soldered assembly of the PBGA 200 and the interposer 100 is shown in Figure 6 according to one embodiment of the present invention. It should be understood that the portion of the compliant pin 130 extending above the surface of the substrate 110 the distance B extends into the solder joint or solder ball 230, securely making a mechanical connection and an electrical connection. This distance B serves to accommodate warping in the PBGA and help form a joint between the interposer solder pad 120 and the PBGA pad/contact. The distance B also serves to reinforcement of the conductive pin and the solder joint between the interposer and the PBGA. The distance B helps reduce the possibility of a gap or open circuit forming in the event the PBGA 200 warps upward away from the interposer 100. By extending beyond the top surface of the substrate 110 of the interposer 100, the compliant pin 130 increases the likelihood of contact with the solder ball 230 without reducing the distance between the substrate 220 and the substrate 110. As shown in Figure 6, the assembly is ready to be soldered to the PWB. The distance of the pin below the substrate (C-(A+-B)) may be intentionally kept long for compliancy of the pin and to accommodate thermal cycling and TCE mismatch.

[0035] Referring to Figure 7, the assembly of the PBGA 200 and the interposer 100 is shown in a side view soldered to the PWB 300. The solder 310 mechanically and electrically connects the pins 130 of the interposer 100 to contacts on the PWB 300. The soldering of the interposer 100 to the PWB 300 may be performed according to the typical soldering process known to those of skill in the art. As would be apparent to one of ordinary skill in the art, the present invention may be configured to be used with various ball arrangements including full grid ball arrangements, perimeter ball arrangements, or other ball arrangements.

[0036] It should be understood that the compliant pins 130 are configured to provide sufficient compliance between the PBGA 200 and the PWB 300 during thermal cycling. The stresses and strains caused by the different thermal expansions and contractions of the PBGA 200 and the PWB 300, due to different TCEs, may be absorbed by the pins 130 of the interposer 100 rather than the solder joints 230 and 310. As such, the compliant interface between the PBGA 200 and the PWB 300 provides a robust and efficient mechanical and electrical connection that resists damage due to thermal cycling and compensates for variations in the coplanarity of the PBGA.

[0037] It should be understood that the compliant interposer in accordance with the present invention may be used with other grid ball array components without deviating from the scope and spirit of the present invention. For example, the interposer 100 may be used with a CBGA using lead-free solder balls such as tin:silver:copper (SAC). Since the ball grid array (BGA) are soldered twice, a step soldering process known to those of skill in the art may use two different alloys of two different melting temperatures to effectively solder the BGA

[0038] The foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations are possible in view of the above teachings. While the embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, thereby enabling others skilled in the art to best utilize the invention, various embodiments with various modifications as are suited to the particular use are also possible. The scope of the invention is to be defined only by the claims appended hereto, and by their equivalents.

CLAIMS

What is claimed is:

1. A compliant leaded interposer for resiliently attaching and electrically connecting a ball grid array package to a circuit board, the ball grid array package having solder balls arranged in a solder ball pattern, the compliant leaded interposer comprising:

a substrate having a top surface and a bottom surface;

a plurality of pads positioned substantially on the top surface of the substrate and arranged in a predetermined pattern substantially corresponding to the solder ball pattern, each of the plurality of pads being associated with one of the solder balls; and

a plurality of pins positioned substantially perpendicular to the top surface of the substrate and extending through the substrate and the plurality of pads, the plurality of pins being arranged in the predetermined pattern with each of the plurality of pins being associated with one of the solder balls, each of the plurality of pins having a first end configured to extend a first distance beyond the top surface of the substrate and a second end configured to extend a second distance beyond the bottom surface of the substrate;

wherein the interposer is configured to attach the ball grid array package to the circuit board such that each of the solder balls contacts at least a portion the first end of one of the plurality of pins and at least a portion of one of the plurality of pads and such that the second end of each of the plurality of pins attaches to an associated contact on the circuit board.

2. The compliant leaded interposer according to claim 1, wherein the ball grid array package is a plastic ball grid array package.

3. The compliant leaded interposer according to claim 1, wherein the ball grid array package is a ceramic ball grid array package.

4. The compliant leaded interposer according to claim 1, wherein each of the plurality of pins is substantially aligned with a centerline of at least one of the plurality of pads.

5. The compliant leaded interposer according to claim 1, wherein the substrate is formed from a laminate material.

6. The compliant leaded interposer according to claim 1, wherein each of the plurality of pins includes a diameter of approximately 0.012 inch and a length of approximately 0.088 inch.

7. The compliant leaded interposer according to claim 4, wherein the plurality of pins are formed from at least one of pure copper, berillium:copper alloy, and phosphorus bronze alloy.

8. The comliant leaded interposer according to claim 7, wherein the plurality of pins are surface finished with at least one of pure tin, silver, nickel:palledium:gold, nickel:gold, and gold.

9. The compliant leaded interposer according to claim 1, wherein each of the plurality of pads includes a diameter of approximately 0.025 inch when a pitch of approximately 0.050 inch is used for the solder balls.

10. The compliant leaded interposer according to claim 1, wherein each of the plurality of pads includes a diameter of approximately 0.020 inch when a pitch of approximately 0.040 inch is used for the solder balls.

11. The compliant leaded interposer according to claim 1, wherein the plurality of pads include copper and are surface finished with at least one of pure tin, immersion silver, tin:lead, nickel;palladium:gold, and nickel:gold.

12. The compliant leaded interposer according to claim 1, wherein the first distance is approximately 0.010 when a pitch of approximately 0.050 inch is used for the solder balls.

13. The compliant leaded interposer according to claim 1, wherein the first distance is approximately 0.008 when a pitch of approximately 0.040 inch is used for the solder balls.

14. A method of connecting a grid array package to a printed wiring board (PWB), comprising the steps of:

aligning a compliant leaded interposer in an assembly tool, the interposer including a plurality of pins positioned substantially perpendicular to a substrate and extending through

the substrate, each of the plurality of pins having a first end configured to extend a first distance beyond a top surface of the substrate and a second end configured to extend a second distance beyond a bottom surface of the substrate, each of the plurality of pins further including a pad aligned with the pin and positioned substantially on the top surface of the substrate; the assembly tool including a plurality of holes in a plate member configured to receive the second end of the plurality of pins in a predetermined pattern;

orienting a plurality of solder balls on the grid array package with the first end of the plurality of pins using tooling pins mounted on the plate member of the assembly tool;

electrically connecting each of the plurality of solder balls to the first end of one of the plurality of pins and to at least a portion of one of the plurality of pads;

removing the interposer and the ball grid array package from the assembly tool;

orienting the second end of each of the plurality of pins with at least one conductive contact on the PWB; and

electrically connecting the second end of each of the plurality of pins to at least one conductive contact of the PWB thereby establishing an electrical connection between the ball grid array package and the PWB, the plurality of pins defining a space between the PWB and the bottom surface of the substrate of the interposer.

15. The method according to claim 16, wherein the ball grid array package is a plastic ball grid array package.

16. The method according to claim 16, wherein the ball grid array package is a ceramic ball grid array package.

17. The method according to claim 16, wherein each of the plurality of pins of the interposer includes a diameter of approximately 0.012 inch and a length of approximately 0.088 inch.

18. The method according to claim 16, wherein the pad includes a diameter of approximately 0.025 inch when a pitch of approximately 0.050 inch is used for the solder balls.

19. The method according to claim 16, wherein the pad includes a diameter of approximately 0.020 inch when a pitch of approximately 0.040 inch is used for the solder balls.

20. The method according to claim 16, wherein the first distance is approximately 0.010 when a pitch of approximately 0.050 inch is used for the solder balls.

21. The method according to claim 16, wherein the first distance is approximately 0.008 when a pitch of approximately 0.040 inch is used for the solder balls.

22. A method of connecting a ball grid array package to a printed wiring board (PWB), comprising the steps of:

forming a compliant leaded interposer having conductive leads, each of the leads having a body and a first end and a second end, the leads extending through a substrate and a set of conductive pads positioned substantially on a top surface of the substrate;

providing an assembly tool having a plate member, a set of tooling pins mounted on the plate member, and a set of holes formed in a plate member;

mounting the interposer in the assembly tool such the leads are received in the set of holes;

aligning the ball grid array package on the interposer using tooling pins such that a set of solder balls on the ball grid array package is substantially aligned with the first ends of the leads;

electrically connecting the ball grid array package and the leads of the interposer such that each of the set of solder balls contacts at least a portion of the first end of one of the leads and at least a portion of one of the set of pads;

removing the ball grid array package and the interposer from the assembly tool;

orienting the second end of the leads to align with contacts on the PWB; and

electrically connecting the second end of the leads to the contacts on the PWB thereby establishing an electrical connection between the ball grid array package and the PWB, the leads defining a space between the PWB and the substrate of the interposer.

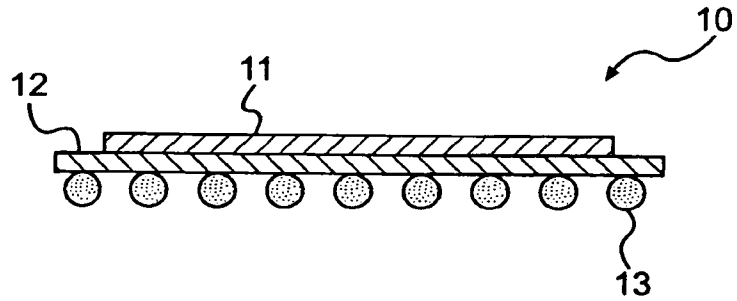


FIG. 1A

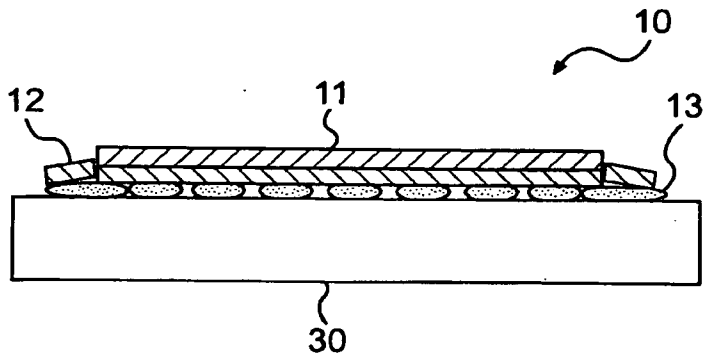


FIG. 1B

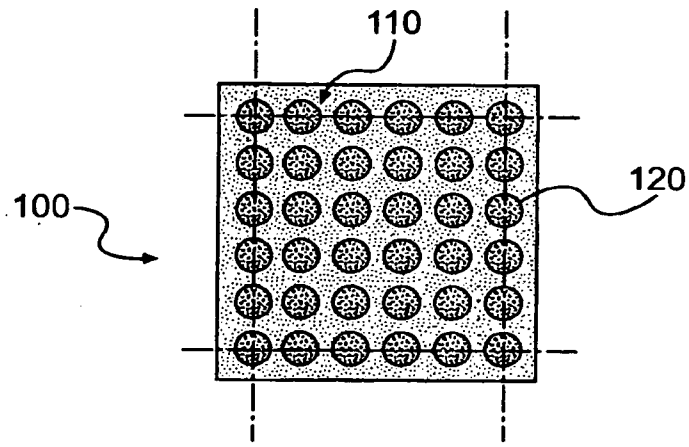


FIG. 2

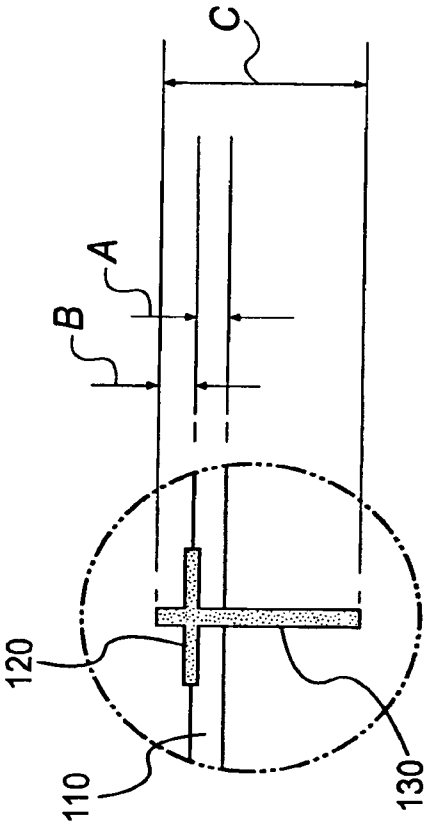


FIG. 3B

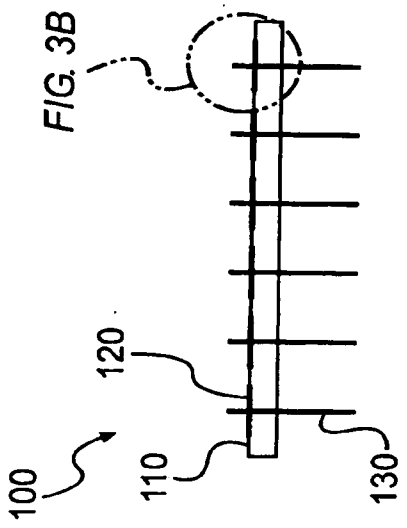


FIG. 3A

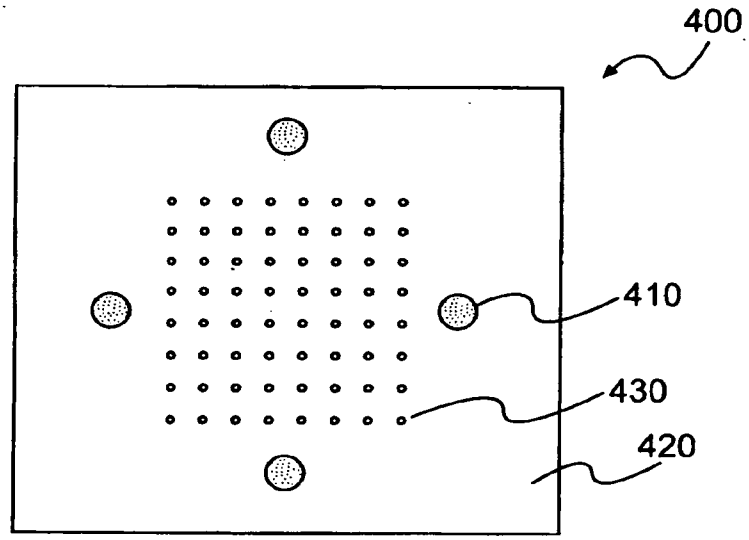


FIG. 4A

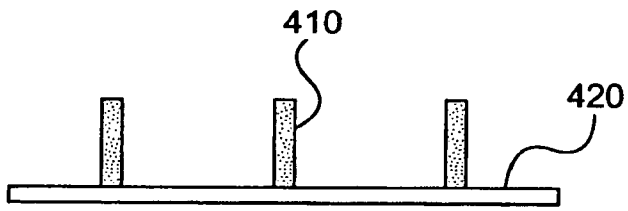


FIG. 4B

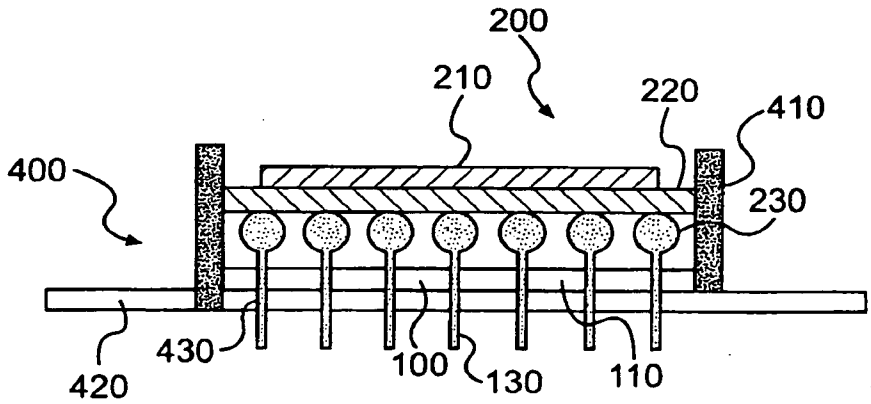


FIG. 5

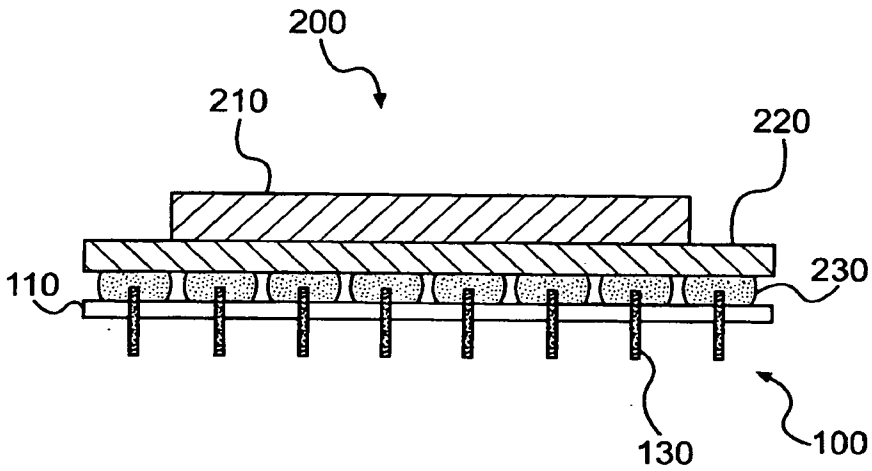


FIG. 6

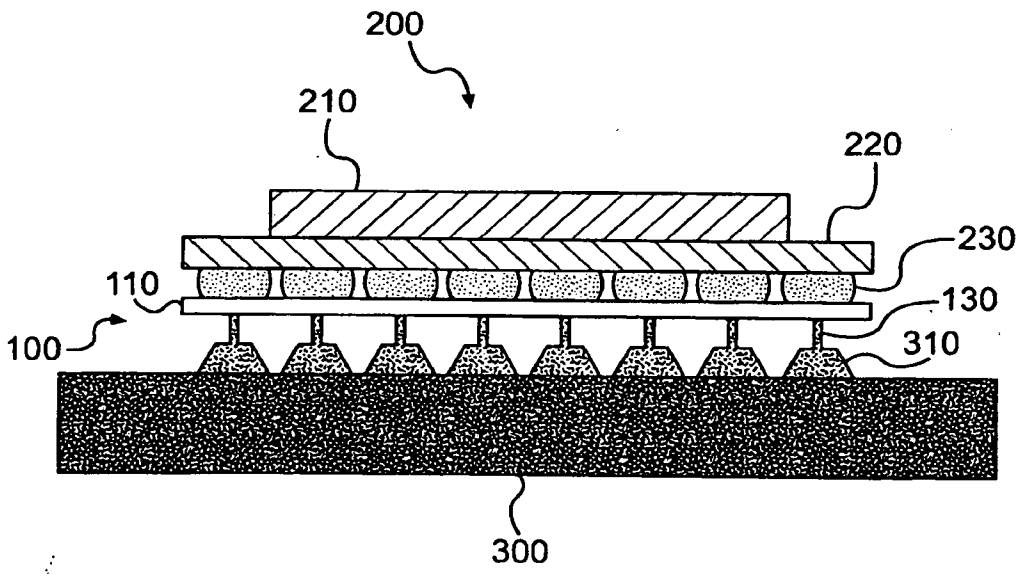


FIG. 7