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(54) Title: PARTIAL BLOCK ERASE ARCHITECTURE FOR FLASH MEMORY

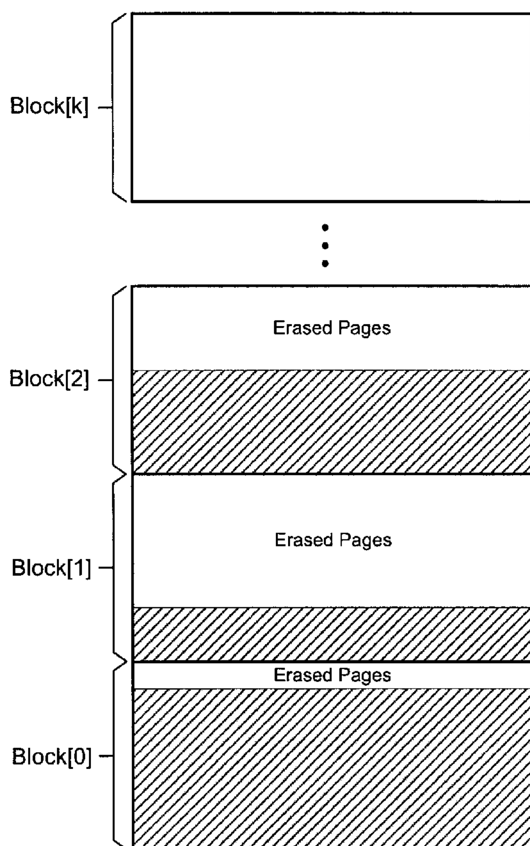

Figure 3

(57) Abstract: A method and system for increasing the lifespan of a flash memory device by selectively erasing sub-blocks of a memory block. Each physical memory block of the flash memory device is dividable into at least two logical sub-blocks, where each of the at least two logical sub-blocks is erasable. Therefore, only the data of the logical sub-block is erased and reprogrammed while unmodified data in the other logical sub-block avoids unnecessary program/erase cycles. The logical sub-blocks to be erased are dynamically configurable in size and location within the block. A wear leveling algorithm is used for distributing data throughout the physical and logical sub-blocks of the memory array to maximize the lifespan of the physical blocks during programming and data modification operations.

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

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— *with amended claims and statement*

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6 November 2008

AMENDED CLAIMS
received by the International Bureau on 22 September 2008

CLAIMS: **(22.09.2008)**

1. A flash memory device comprising:

a memory array having at least one block of NAND flash memory cell strings arranged in columns, the at least one block having pages programmable in a predetermined direction from a first wordline to a last wordline, and a dynamically selectable number of flash memory cells being erasable; and,

row circuitry for driving first wordlines corresponding to the preset number of flash memory cells to a first voltage when the substrate is biased to an erase voltage for erasing the dynamically selectable number of flash memory cells, the row decoders driving second wordlines to a second voltage for inhibiting erasure of the flash memory cells coupled to the second wordlines, the second wordlines including the first wordline up to a last unselected wordline and the first wordlines including a first selected wordline adjacent to the last unselected wordline, up to a last selected wordline.

2. The flash memory device of claim 1, wherein the last selected wordline includes the last wordline.

3. The flash memory device of claim 1, wherein the dynamically selectable number of flash memory cells are multi-bit-cells (MBC).

4. The flash memory device of claim 1, wherein the dynamically selectable number of flash memory cells correspond to one sequential set of flash memory cells.

5. The flash memory device of claim 1, wherein the dynamically selectable number of flash memory cells correspond to two sequential sets of flash memory cells, the two sequential sets of flash memory cells being non-adjacent to each other.

6. The flash memory device of claim 1, wherein the NAND flash memory cell strings of the at least one block are coupled to a common source line, and the flash memory device further includes a source line voltage control circuit for setting a voltage of the common source line between a third voltage and a fourth voltage during an erase verify operation.

7. The flash memory device of claim 6, wherein the fourth voltage is less than the third voltage, and the voltage of the common source line decreases as a number of first wordlines

increases.

8. A method for erasing a sub-block of a memory block, the memory block having a NAND memory cell string coupled to a first wordline, a last wordline, and intermediate wordlines between the first wordline and the last wordline, comprising

issuing a first input address command with a first address;

issuing a second input address command with a second address;

issuing a partial erase command; and,

erasing the sub-block having a set of wordlines bound by wordlines corresponding to the first address and the second address.

9. The method of claim 8, wherein the first address includes a null address.

10. The method of claim 9, wherein the sub-block includes the set of wordlines bound by one wordline corresponding to the second address and the first wordline.

11. The method of claim 8, wherein the second address includes a null address.

12. The method of claim 11, wherein the sub-block includes the set of wordlines bound by one wordline corresponding to the first address and the last wordline.

13. The method of claim 8, further including erase verifying the erased sub-block.

14. The method of claim 13, wherein erase verifying includes

precharging a bitline coupled to the NAND memory cell string to a precharge voltage level,

biasing the set of wordlines to a first voltage for turning on erased memory cells coupled to the set of wordlines,

biasing unselected wordlines to a second voltage for turning on memory cells coupled to the unselected wordlines, and

sensing a change in the precharge voltage level.

15. The method of claim 14, wherein the first voltage is a negative voltage and the second voltage is a read voltage used during a read operation.

16. The method of claim 14, wherein the first voltage is 0V and the second voltage is a read voltage used during a read operation.

17. The method of claim 16, wherein a common source line coupled to the NAND memory cell string is biased to a variable source bias voltage.

18. The method of claim 17, wherein the variable source bias voltage increases from 0V to a maximum voltage as a number of the set of wordlines decreases.

19. A method for wear leveling control when modifying data in a sub-block of a memory block, comprising:

programming modified data to an empty sub-block of a new memory block;

erasing the sub-block of the memory block.

20. The method of claim 19, further including programming new data to a lowest ranking available sub-block, where each memory block includes at least two sub-blocks and the lowest ranking available sub-block includes a set of wordlines most proximate to a first wordline to be programmed in a sequential programming scheme.

21. The method of claim 19, further including updating an address mapping table to map a logical address of the modified data to a physical address corresponding to the empty sub-block of the new memory block.

22. The method of claim 19, wherein the empty sub-block is a lowest ranking available sub-block.

23. The method of claim 19, wherein the empty sub-block has a ranking equal to the sub-block.

24. The method of claim 23, wherein the new memory block is empty.

25. The method of claim 23, wherein the new memory block includes other data stored in another sub-block having a lower ranking than the empty sub-block.

26. The method of claim 19, wherein the empty sub-block has a ranking higher than the sub-block.

27. The method of claim 19, further including swapping data in the sub-block with other data in one other sub-block of the memory block when a difference between program/erase cycles of the sub-block and the one other sub-block reaches a predetermined value.

STATEMENT UNDER ARTICLE 19 (1)

The claims have been amended to recite features described in the specification, and no new subject matter is being claimed.