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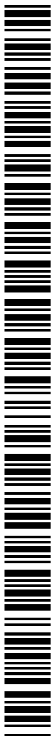


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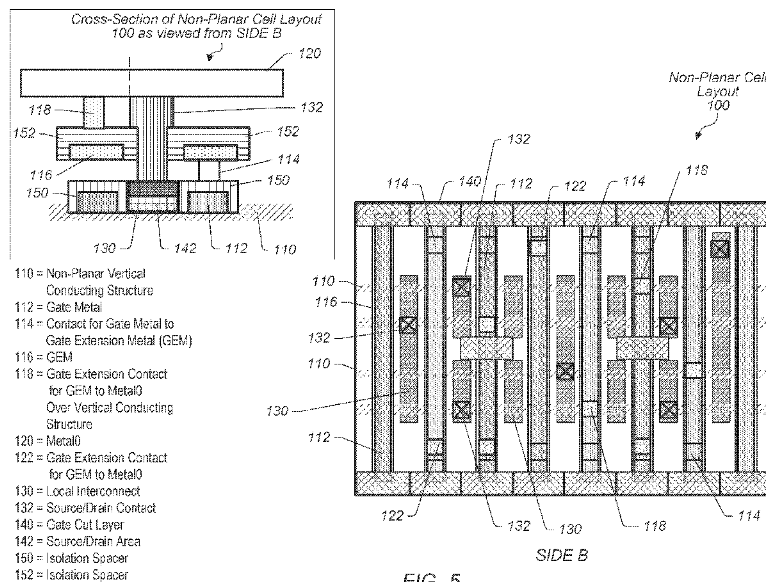


FIG. 5

(57) **Abstract:** A system and method for laying out power grid connections for standard cells are described. In various implementations, gate metal is placed over non-planar vertical conducting structures, which are used to form non-planar devices (transistors). Gate contacts connect gate metal to gate extension metal (GEM) above the gate metal. GEM is placed above the gate metal and makes a connection with gate metal through the one or more gate contacts. Gate extension contacts are formed on the GEM above the active regions. Similar to gate contacts, gate extension contacts are formed with a less complex fabrication process than using a self-aligned contacts process. Gate extension contacts connect GEM to an interconnect layer such as a metal zero layer. Gate extension contacts are aligned vertically with one of the non-planar vertical conducting structures. Therefore, in an implementation, one or more gate extension contacts are located above the active region.

*[Continued on next page]*

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# GATE CONTACT OVER ACTIVE REGION IN CELL

## BACKGROUND

5 **Description of the Relevant Art**

**[0001]** As both semiconductor manufacturing processes advance and on-die geometric dimensions reduce, semiconductor chips provide more functionality and performance while consuming less space. While many advances have been made, design issues still arise with
10 modern techniques in processing and integrated circuit design that limit potential benefits. For example, capacitive coupling, electro migration, leakage currents and processing yield are some issues which affect the placement of devices and the routing of signals across an entire die of a semiconductor chip. Additionally, as the transistor dimensions decrease, the short channel effects increase. Other examples of short channel effects other than leakage current are latch-up
15 effects, drain-induced barrier lowering (DIBL), punch-through, performance dependency on temperature, impact ionization, and parasitic capacitance to the silicon substrate and to the wells used for the source and drain regions. Thus, these issues have the potential to delay completion of the design and affect the time to market.

**[0002]** Non-planar transistors are a recent development in semiconductor processing for reducing
20 short channel effects. Tri-gate transistors, Fin field effect transistors (FETs) and gate all around (GAA) transistors are examples of non-planar transistors. The processing steps for non-planar devices (transistors) are more complex than the processing steps for planar devices (transistors). In order to improve each of scaling and metal routing for standard cell layouts with non-planar devices, changes to the processing steps are made when these changes provide sufficient yield
25 and do not increase the manufacturing costs above a limit. When these changes are made in the layout, the place-and-route (PNR) layout tools and rules setup for non-planar devices also change.

**[0003]** When the placement of contacts is flexible within a standard cell layout, each of the scaling and metal routing improves for the entire standard cell library. However, the flexibility
30 reduces when short circuits occur, which reduce yield, and the processing steps become appreciably complex. When the flexibility of the contact placement reduces, the standard cells increase in size and the amount of available metal tracks for routing decreases.

**[0004]** In view of the above, efficient methods and systems for creating layout for non-planar cells are desired.

35

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0005]** The advantages of the methods and mechanisms described herein may be better
5 understood by referring to the following description in conjunction with the accompanying drawings, in which:

**[0006]** FIG. 1 is a generalized diagram of top and cross-sectional views of a cell layout with non-planar devices.

**[0007]** FIG. 2 is a generalized diagram of top and cross-sectional views of a cell layout.

10 **[0008]** FIG. 3 is a generalized diagram of a method for creating cell layout with contacts over gates in an active region of a non-planar device.

**[0009]** FIG. 4 is a generalized diagram of a method for creating cell layout with contacts over gates in an active region of a non-planar device.

**[0010]** FIG. 5 is a generalized diagram of top and cross-sectional views of a cell layout with
15 non-planar devices.

**[0011]** FIG. 6 is a generalized diagram of top and cross-sectional views of a cell layout with non-planar devices.

**[0012]** FIG. 7 is a generalized diagram of a method for creating cell layout with contacts over gates in an active region of a non-planar device.

20 **[0013]** While the invention is susceptible to various modifications and alternative forms, specific implementations are shown by way of example in the drawings and are herein described in detail. It should be understood, however, that drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the scope of the present
25 invention as defined by the appended claims.

## DETAILED DESCRIPTION

**[0014]** In the following description, numerous specific details are set forth to provide a thorough
30 understanding of the methods and mechanisms presented herein. However, one having ordinary skill in the art should recognize that the various implementations may be practiced without these specific details. In some instances, well-known structures, components, signals, computer program instructions, and techniques have not been shown in detail to avoid obscuring the approaches described herein. It will be appreciated that for simplicity and clarity of illustration,

elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements.

**[0015]** Systems and methods for creating layout for non-planar cells are contemplated. In some implementations, the cell layout is a standard cell in a cell layout library. In other implementations, the cell layout is a custom designed cell, which is separate from the standard cell layout library. In various implementations, gate metal is placed over non-planar vertical conducting structures. The non-planar vertical conducting structures are used to form non-planar devices (transistors). Examples of non-planar devices are tri-gate transistors, fin field effect transistors (FETs) and gate all around (GAA) transistors. In some implementations, gate contacts connect gate metal to gate extension metal (GEM) above the gate metal. In an implementation, GEM is only used above the gate metal.

**[0016]** In an implementation, a single gate contact per column of gate metal is included in cell layout to connect gate metal to GEM. In other implementations, two or more gate contacts are used to connect gate metal to GEM, which increases yield. In some implementations, the separate two or more gate contacts are placed at the top and bottom of cell layout for several columns.

**[0017]** Typically, a gate contact or gate via is not located directly over the active region such as over one of the non-planar vertical conducting structures. To do so typically includes a complex semiconductor fabrication process, which includes using a self-aligned contacts process for the diffusion contact and gate contact. By placing gate contacts outside the active regions, and thus, placed separate from the non-planar vertical conducting structures, a complex semiconductor fabrication process, which includes using a self-aligned contacts process for gate contacts, is not used. Rather, a less complex fabrication process is used instead to place gate contacts. Following, GEM is placed above the gate metal and makes a connection with gate metal through the one or more gate contacts.

**[0018]** In various implementations, gate extension contacts are formed above the active regions on the GEM. Similar to gate contacts between the gate metal and the GEM, in various implementations, gate extension contacts are formed with a less complex fabrication process than using a self-aligned contacts process. Gate extension contacts connect GEM to an interconnect layer such as a metal zero layer. Gate extension contacts do not connect to the gate contacts or the gate metal. In some implementations, gate extension contacts are aligned vertically with one of the non-planar vertical conducting structures. Therefore, in an implementation, one or more gate extension contacts are located above the active region. Accordingly, in an implementation, the height of cell layout is reduced, which improves scalability and metal track routing.

**[0019]** Referring to FIG. 1, a generalized block diagram of non-planar cell layout 100, which is a top view of cell layout, is shown. Additionally, a generalized block diagram of a cross-section view of the same cell layout from Side A, is shown. As shown, Side A is to the left of non-planar cell layout 100. In the illustrated implementation, the p-type metal oxide semiconductor (pmos) field effect transistors (fets) are at the top of cell layout 100. The n-type metal oxide semiconductor (nmos) field effect transistors (fets) are at the bottom of cell layout 100. Here, the active regions are not shown in the cell layout 100 for ease of illustration. In some implementations, cell layout 100 is part of a standard cell layout library. In other implementations, cell layout 100 is custom layout cells for particular areas of a chip design.

**[0020]** In various implementations, the layout techniques shown in figures 1-2 and 5-7 are used for a variety of other standard cells and custom cells used for a variety of complex gates and functional units. In various implementations, the devices (transistors) in the cell layout 100 are non-planar devices (transistors). Non-planar devices are a recent development in semiconductor processing for reducing short channel effects. Tri-gate transistors, Fin field effect transistors (FETs) and gate all around (GAA) transistors are examples of non-planar devices.

**[0021]** The non-planar vertical conducting structures 110 come up out of the page in a three-dimensional manner. As used herein, the non-planar vertical conducting structures 110 are also referred to as "vertical structures 110." It is noted that the vertical structures 110 are considered vertical due to coming out of the page in a three-dimensional manner although the vertical structures 110 are routed in a horizontal direction. In various implementations, the vertical structures 110 are included in one of the above types of non-planar devices such as tri-gate transistors, fin field effect transistors (FETs) and gate all around (GAA) transistors.

**[0022]** In some implementations, the non-planar devices in cell layout 100 are fabricated by one of the immersion lithography techniques, the double patterning technique, the extreme ultraviolet lithography (EUV) technique, and the directed self-assembly (DSA) lithography technique. In some implementations, the EUV technique provides more flexibility relative to via and contact modules relative to other techniques. As shown, cell layout 100 uses gate metal 112 in a vertical direction. In some implementations, titanium nitride (TiN) is used for the gate metal 112. The boundaries of the active regions are not shown for ease of illustration, but the rectangular boundaries of active regions are within a relatively close proximity of the vertical structures 110 and gate metal 112. The layer 140 is used to cut the gate layer and shows where the gate metal 112 start and stop. As shown, each of the third and sixth columns have separate gates for the top and bottom of the columns due to layer 140 placed in the middle of cell layout 100.

**[0023]** The local interconnect 130 is routed in a vertical direction similar to the gate metal 112. In some implementations, local interconnect 130 is copper, tungsten or cobalt and the material used is based on the design tradeoff between resistance and process dependability. In an implementation, copper, tungsten or cobalt contacts 132 are used for the source and drain regions. Metal 0 (M0 or Metal0) 120 is used for local interconnections in the horizontal direction. For ease of illustration, Metal0 120 is not shown in cell layout 100, but rather only in the cross-section view.

**[0024]** The gate contact 114 connects gate metal 112 to gate extension metal (GEM) 116. In the illustrated implementation, GEM 116 is only used above the gate metal 112. The separate gate contacts 114 are seen at the top of cell layout 100 and the bottom of cell layout 100 for several columns. In some implementations, a single gate contact 114 per column is included in cell layout 100 to connect gate metal 112 to GEM 116. In other implementations, two or more gate contacts 114 are used to connect gate metal 112 to GEM 116, which increases yield.

**[0025]** Typically, a gate contact or gate via is not located directly over the active region such as over one of the vertical structures 110. To do so typically includes a complex semiconductor fabrication process, which includes using a self-aligned contacts process for the diffusion contact and gate contact. Here, as shown in each of cell layout 100 and the cross-section view, gate contacts 114 are placed outside the active regions, and thus, placed separate from the vertical structures 110. Therefore, a complex semiconductor fabrication process, which includes using a self-aligned contacts process for gate contacts 114, is not used. Rather, a less complex fabrication process is used instead to place gate contacts 114 outside the active regions. Following, GEM 116 is placed above the gate metal 112 and makes a connection with gate metal 112 through the gate contacts 114. Now, in various implementations, gate contacts 118 are formed above the active regions. Similar to gate contacts 114, in various implementations, gate extension contacts 118 are formed with a less complex fabrication process than using a self-aligned contacts process.

**[0026]** Gate extension contacts 118 connect GEM 116 to the horizontal Metal0 120. Gate extension contacts 118 do not connect to the gate contacts 114 or the gate metal 112. It is noted that one or more of the gate extension contacts 118 are aligned vertically with one of the vertical structures 110. Therefore, in an implementation, one or more gate extension contacts 118 are located above the active region. Accordingly, in an implementation, the height of cell layout 100 is reduced, which improves scalability and metal track routing.

**[0027]** Turning now to FIG. 2, a generalized block diagram of non-planar cell layout 100, which is a top view of cell layout, is shown. Additionally, a generalized block diagram of a cross-

section view of the same cell layout from Side B, is shown. As shown, Side B is at the bottom of non-planar cell layout 100. Layout elements described earlier are numbered identically. Although each of cell layout 100 is shown as a two-dimensional diagram, there are three-dimensional elements depicted in the diagrams. As described earlier, each of the vertical 5 structures 110 is considered vertical due to coming out of the page in a three-dimensional manner although the vertical structures 110 are routed in a horizontal direction.

**[0028]** In an implementation, in the cross-section view, source/drain contact 132 is further out of the page in a three-dimensional manner than gate extension contact 118. Next, gate extension contact 118 is further out of the page than each of gate contacts 114. Metal0 120 making contact 10 with source/drain contact 132 is further out of the page than metal0 120 making contact with gate extension contact 118. Therefore, a dashed line in the cross-section view is used to separate the two separate horizontal routes of metal0 120. The metal0 120 on the right of the dashed line is further out of the page than the metal0 120 on the left of the dashed line. In an implementation, in the cross-section view, each of gate extension contact 118 and vertical structure 110 is no 15 further out of the page than the other. Accordingly, gate extension contact 118 is aligned vertically with vertical structures 110 in the cross-section view, and gate extension contact 118 is located above the active region.

**[0029]** Referring now to FIG. 3, a generalized block diagram of a method 300 for creating cell layout with contacts over gates in an active region of a non-planar device is shown. For purposes 20 of discussion, the steps in this implementation (as well as in Figures 4 and 8) are shown in sequential order. However, in other implementations some steps occur in a different order than shown, some steps are performed concurrently, some steps are combined with other steps, and some steps are absent.

**[0030]** One or more non-planar vertical conducting structures are formed on a silicon substrate 25 (block 302). In various implementations, the non-planar vertical conducting structures are used to fabricate one of a variety of non-planar devices such as tri-gate transistors, fin field effect transistors (FETs) and gate all around (GAA) transistors. Gate metal is placed on a portion of the one or more non-planar vertical conducting structures (block 304). A gate contact is formed on one or more of the ends the metal gate (block 306). In various implementations, the gate contacts 30 are not formed over one of the non-planar vertical conducting structures.

**[0031]** Gate extension metal (GEM) is placed above the metal gate on the one or more gate contacts (block 308). In an implementation, the length of the GEM is the same or greater than the length of the gate metal. In another implementation, the length of the GEM is less than the length of the gate metal. A gate extension contact is formed at a location on the GEM both

above and aligned with one of the non-planar vertical conducting structures (block 310). Therefore, in various implementations, the gate extension contact is formed above the active region. Local metal layers are placed for connecting local routes and power connections (block 312). For example, a metal zero layer is placed to make contact with the gate extension contact and route a signal to other vias. In some implementations, the cell layout is a standard cell in a cell layout library. In other implementations, the cell layout is a custom designed cell, which is separate from the standard cell layout library.

**[0032]** Referring now to FIG. 4, a generalized block diagram of a method 400 for creating cell layout with contacts over gates in an active region of a non-planar device is shown. A region is selected with an existing gate extension contact on gate extension metal (GEM) over a non-planar vertical conducting structure formed on a silicon substrate (block 402). In one example, referring briefly again to cell layout 100 of FIG. 2, the region including the gate extension contact 118 at the top of the sixth column from the left is selected. A local interconnect layer is placed running parallel with a portion of a metal gate below the GEM between the selected region and a source/drain region that does not include a gate extension contact (block 404).

**[0033]** A source/drain contact is formed at a location on the local interconnect layer in the source/drain region (block 406). Referring briefly again to cell layout 100 of FIG. 2, source/drain contact 132 is placed to the right and below gate extension contact 118 at the top of the sixth column from the left. As shown in the cross-section view of FIG. 2, each of the local interconnect layer 130 and the source/drain contact 132 are placed between each of two gate metals and two gate extension metals (GEMs). Local metal layers for connecting local routes and power connections are placed (block 408). In some implementations, the cell layout is a standard cell in a cell layout library. In other implementations, the cell layout is a custom designed cell, which is separate from the standard cell layout library.

**[0034]** Turning now to FIG. 5, a generalized block diagram of non-planar cell layout 100, which is a top view of cell layout, is shown. Additionally, a generalized block diagram of a cross-section view of the same cell layout from Side B, is shown. As shown, Side B is at the bottom of non-planar cell layout 100. Layout elements described earlier are numbered identically. Although each of cell layouts 100 and 500 is shown as a two-dimensional diagram, there are three-dimensional elements depicted in the diagrams. As described earlier, each of the vertical structures 110 is considered vertical due to coming out of the page in a three-dimensional manner although the vertical structures 110 are routed in a horizontal direction. Additionally, in an implementation, in the cross-section view, source/drain contact 132 is further out of the page in a

three-dimensional manner than gate extension contact 118. Next, gate extension contact 118 is further out of the page than each of gate contacts 114.

**[0035]** As described earlier, metal0 120 making contact with source/drain contact 132 is further out of the page than metal0 120 making contact with gate extension contact 118. Therefore, a dashed line in the cross-section view is used to separate the two separate horizontal routes of metal0 120. The metal0 120 on the right of the dashed line is further out of the page than the metal0 120 on the left of the dashed line. In an implementation, in the cross-section view, each of gate extension contact 118 and vertical structure 110 is no further out of the page than the other. Accordingly, gate extension contact 118 is aligned vertically with vertical structures 110 in the cross-section view, and gate extension contact 118 is located above the active region.

**[0036]** As shown, local interconnect layer 130 is formed over source/drain region (area) 142. In various implementations, source/drain area 142 is formed by an implantation process. In the illustrated implementation, each of the gate metals 112 in the cross-section view is surrounded by isolated spacers 150. Similarly, each of the GEMs 116 is surrounded by isolated spacers 152. In some implementations, each of the isolated spacers 150 and 152 includes a same material. In other implementations, each of the isolated spacers 150 and 152 includes a different material. In an implementation, the material used for one or more of isolated spacers 150 and 152 is silicon nitride.

**[0037]** In an implementation, the gate metal 112 is placed with a height reaching the top of the isolated spacers 150. The isolated spacers are formed over the gate metal 112 and the two materials are etched to near the final height of the gate metal 112. More isolated spacer 150 is placed on top of the gate metal 112 followed by etching and polishing. For example, SiN deposition and chemical mechanical planarization (CMP) steps are used. An area is etched into the isolated spacer 150 for the gate contact 114, so that the gate contact 114 makes a physical connection with GEM 116 and gate 112. Next, tetraethyl orthosilicate (TEOS) or other oxide deposition occurs followed by a trench is formed for GEM 116. In another implementation, the isolated spacer 150 is patterned and etched after it is deposited on the gate metal 112 followed by an oxide deposition, such as a TEOS deposition. Afterward, the trench for the GEM 116 is formed and then the final via etch.

**[0038]** Cell layout 500 shows the source/drain contact 132 is dual self-aligned by the GEM 116 and Metal0 layer 120. The Metal0 layer 120 self-aligns the source/drain contact 132 into and out of the page. The isolated spacer 152 on the GEM 116 self-aligns the source/drain contact 132. If the GEM 116 is misaligned, then the isolated spacer 150 on the gate meal 112 self-aligns the source/drain contact 132 to the local interconnect layer 130.

**[0039]** Turning now to FIG. 6, a generalized block diagram of non-planar cell layout 100, which is a top view of cell layout, is shown. Additionally, a generalized block diagram of a cross-section view of the same cell layout from Side B, is shown. As shown, Side B is at the bottom of non-planar cell layout 100. Layout elements described earlier are numbered identically. In the illustrated implementation, the isolated spacer 154 reaches down to the gate metal 112 as shown in the cross-section view. Isolated spacer 154 provides further alignment and further isolation. In some implementations, each of the isolated spacers 150 and 154 includes a same material. In other implementations, each of the isolated spacers 150 and 154 includes a different material.

**[0040]** Referring now to FIG. 7, a generalized block diagram of a method 700 for creating cell layout with contacts over gates in an active region of a non-planar device is shown. Gate metal is placed on a portion of one or more non-planar vertical conducting structures (block 702). Isolating spacers are placed on either side of the gate metal (block 704). Isolating spacers are placed on top of the gate metal (block 706). A local interconnect layer is placed running parallel with a portion of a metal gate between the side spacers of the gate metals (block 708).

**[0041]** Gate extension metal (GEM) is placed above the metal gate on the one or more gate contacts (block 710). Isolating spacers are placed on either side of the GEM (block 712). Isolating spacer is placed on top of the GEM (block 714). A source/drain contact is formed at a location on the local interconnect layer in the source/drain region (block 716). Local metal layers are placed for connecting local routes and power connections (block 718). In some implementations, the cell layout is a standard cell in a cell layout library. In other implementations, the cell layout is a custom designed cell, which is separate from the standard cell layout library.

**[0042]** It is noted that one or more of the above-described implementations include software. In such implementations, the program instructions that implement the methods and/or mechanisms are conveyed or stored on a computer readable medium. Numerous types of media which are configured to store program instructions are available and include hard disks, floppy disks, CD-ROM, DVD, flash memory, Programmable ROMs (PROM), random access memory (RAM), and various other forms of volatile or non-volatile storage. Generally speaking, a computer accessible storage medium includes any storage media accessible by a computer during use to provide instructions and/or data to the computer. For example, a computer accessible storage medium includes storage media such as magnetic or optical media, e.g., disk (fixed or removable), tape, CD-ROM, or DVD-ROM, CD-R, CD-RW, DVD-R, DVD-RW, or Blu-Ray. Storage media further includes volatile or non-volatile memory media such as RAM (e.g. synchronous dynamic RAM (SDRAM), double data rate (DDR, DDR2, DDR3, etc.) SDRAM, low-power DDR

(LPDDR2, etc.) SDRAM, Rambus DRAM (RDRAM), static RAM (SRAM), etc.), ROM, Flash memory, non-volatile memory (e.g. Flash memory) accessible via a peripheral interface such as the Universal Serial Bus (USB) interface, etc. Storage media includes microelectromechanical systems (MEMS), as well as storage media accessible via a communication medium such as a network and/or a wireless link.

**[0043]** Additionally, in various implementations, program instructions include behavioral-level descriptions or register-transfer level (RTL) descriptions of the hardware functionality in a high level programming language such as C, or a design language (HDL) such as Verilog, VHDL, or database format such as GDS II stream format (GDSII). In some cases the description is read by a synthesis tool, which synthesizes the description to produce a netlist including a list of gates from a synthesis library. The netlist includes a set of gates, which also represent the functionality of the hardware including the system. The netlist is then placed and routed to produce a data set describing geometric shapes to be applied to masks. The masks are then used in various semiconductor fabrication steps to produce a semiconductor circuit or circuits corresponding to the system. Alternatively, the instructions on the computer accessible storage medium are the netlist (with or without the synthesis library) or the data set, as desired. Additionally, the instructions are utilized for purposes of emulation by a hardware based type emulator from such vendors as Cadence®, EVE®, and Mentor Graphics®.

**[0044]** Although the implementations above have been described in considerable detail, numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

**WHAT IS CLAIMED IS**

1. A semiconductor device fabrication process for creating a standard cell layout comprising:
   forming one or more non-planar vertical conducting structures on a silicon substrate;
5  placing gate metal on a portion of the one or more non-planar vertical conducting structures;
   forming one or more gate contacts on one or more ends of the metal gate;
   placing gate extension metal (GEM) above the gate metal on the one or more gate contacts; and
10 forming a gate extension contact at a location on the GEM above and aligned with one of the one or more non-planar vertical conducting structures where a local metal zero layer is available to be used for routing a gate connection.

2. The semiconductor device fabrication process as recited in claim 1, further comprising:
15 selecting a region with a gate extension contact on gate extension metal (GEM) over a non-planar vertical conducting structure formed on a silicon substrate; and
   placing a local interconnect layer running parallel with a portion of a gate metal below the GEM between the selected region and a source/drain region that does not include a gate extension contact.

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3. The semiconductor device fabrication process as recited in claim 2, further comprising forming a source/drain contact at a location on the local interconnect layer in the source/drain region that does not include a gate extension contact.

25 4. The semiconductor device fabrication process as recited in claim 1, further comprising:
   placing isolating spacers on either side of the gate metal and on top of the gate metal; and
   placing a local interconnect layer running parallel with a portion of the gate metal along a spacer on the side of the gate metal.

30 5. The semiconductor device fabrication process as recited in claim 1, further comprising:
   placing isolating spacers on either side of the GEM and on top of the GEM; and
   forming a source/drain contact along a spacer on the side of the GEM.

6. The semiconductor device fabrication process as recited in claim 1, wherein a length of the
35 GEM is greater than or equal to a length of gate metal below the GEM.

7. The semiconductor device fabrication process as recited in claim 1, wherein each of the one or more non-planar vertical conducting structures comprises a semiconductor Fin.

8. The semiconductor device fabrication process as recited in claim 1, wherein each of the one or more non-planar vertical conducting structures comprises a semiconductor nanowire.

9. A semiconductor structure comprising:
one or more non-planar vertical conducting structures on a silicon substrate;
gate metal on a portion of the one or more non-planar vertical conducting structures;
one or more gate contacts on one or more ends of the metal gate;
gate extension metal (GEM) above the gate metal on the one or more gate contacts; and
a gate extension contact at a location on the GEM above and aligned with one of the one or more non-planar vertical conducting structures where a local metal zero layer is available to be used for routing a gate connection.

10. The semiconductor structure as recited in claim 9, further comprising:
a region with a gate extension contact on gate extension metal (GEM) over a non-planar vertical conducting structure formed on a silicon substrate; and
a local interconnect layer running parallel with a portion of a gate metal below the GEM between the selected region and a source/drain region that does not include a gate extension contact.

11. The semiconductor structure as recited in claim 10, further comprising a source/drain contact at a location on the local interconnect layer in the source/drain region that does not include a gate extension contact.

12. The semiconductor structure as recited in claim 9, further comprising:
isolated spacers on either side of the gate metal and on top of the gate metal; and
a local interconnect layer running parallel with a portion of the gate metal along a spacer on the side of the gate metal.

13. The semiconductor structure as recited in claim 9, further comprising:
isolated spacers on either side of the GEM and on top of the GEM; and
a source/drain contact along a spacer on the side of the GEM.

14. The semiconductor structure as recited in claim 9, wherein a length of the GEM is greater than or equal to a length of gate metal below the GEM.

15. The semiconductor structure as recited in claim 9, wherein each of the one or more non-planar vertical conducting structures comprises a semiconductor Fin.

16. The semiconductor structure as recited in claim 9, wherein each of the one or more non-planar vertical conducting structures comprises a semiconductor nanowire.

17. A non-transitory computer readable storage medium storing program instructions, wherein the program instructions for performing a semiconductor fabrication process are executable by a processor to:

form one or more non-planar vertical conducting structures on a silicon substrate;

place gate metal on a portion of the one or more non-planar vertical conducting structures;

form one or more gate contacts on one or more ends of the metal gate;

place gate extension metal (GEM) above the gate metal on the one or more gate contacts; and

form a gate extension contact at a location on the GEM above and aligned with one of the one or more non-planar vertical conducting structures where a local metal zero layer is available to be used for routing a gate connection.

18. The non-transitory computer readable storage medium as recited in claim 17, wherein the program instructions are further executable by a processor to:

select a region with a gate extension contact on gate extension metal (GEM) over a non-planar vertical conducting structure formed on a silicon substrate; and

place a local interconnect layer running parallel with a portion of a gate metal below the GEM between the selected region and a source/drain region that does not include a gate extension contact.

19. The non-transitory computer readable storage medium as recited in claim 18, wherein the program instructions are further executable by a processor to form a source/drain contact at a location on the local interconnect layer in the source/drain region that does not include a gate extension contact.

20. The non-transitory computer readable storage medium as recited in claim 17, wherein the program instructions are further executable by a processor to:

place isolating spacers on either side of the gate metal and on top of the gate metal; and

place a local interconnect layer running parallel with a portion of the gate metal along a
5 spacer on the side of the gate metal.

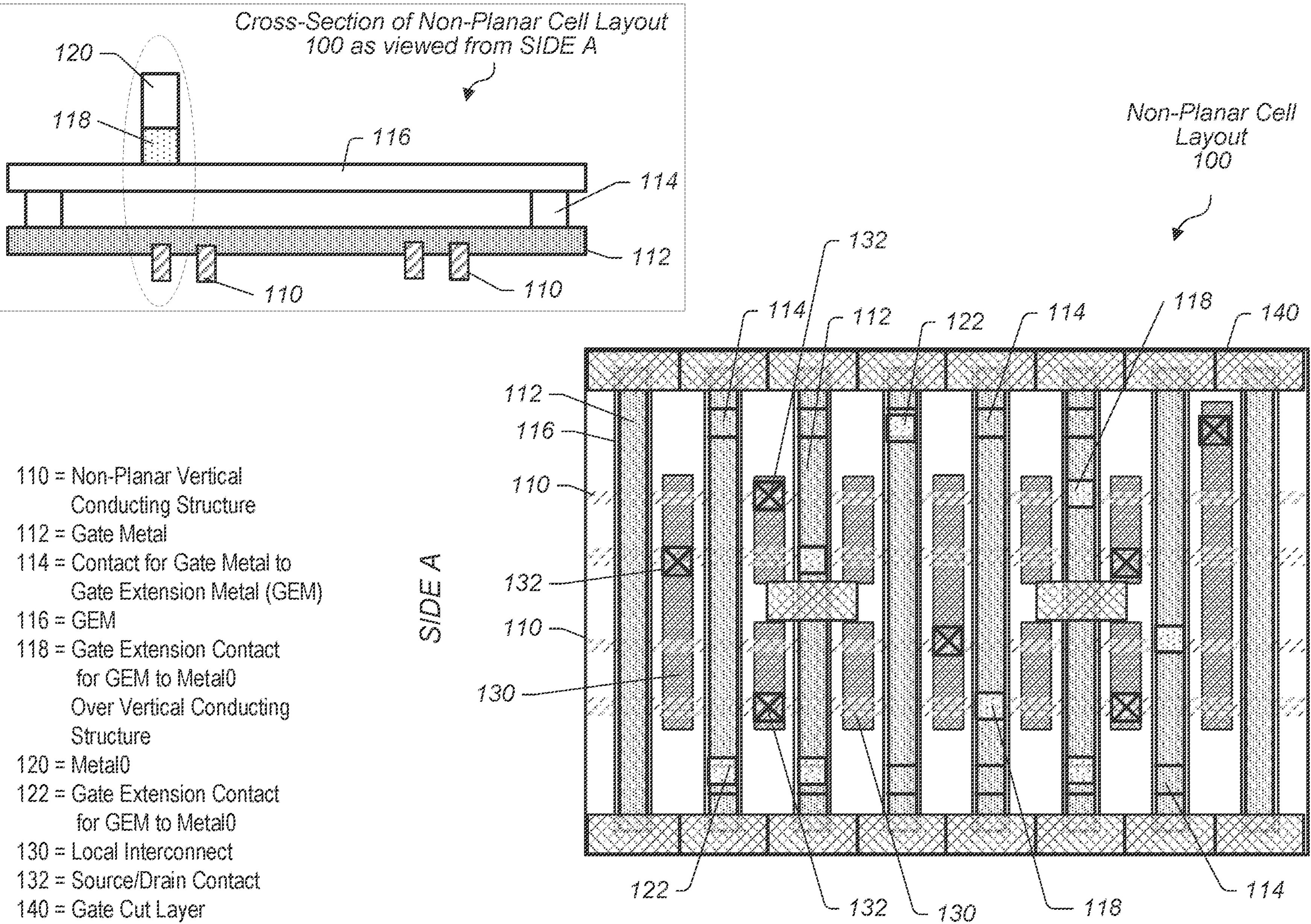
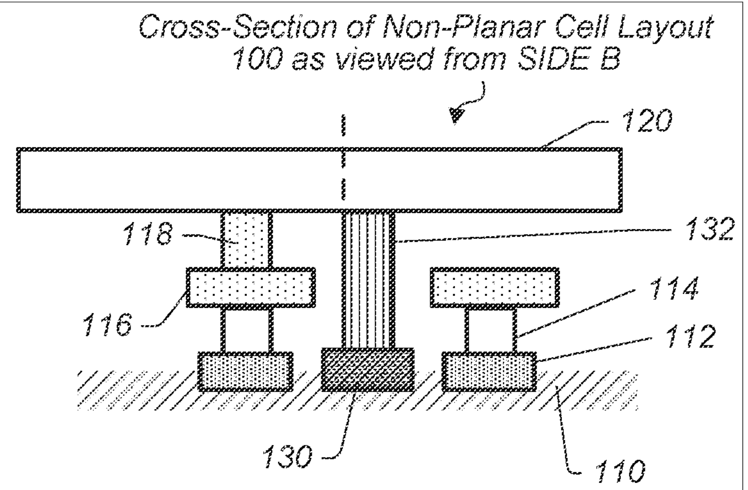
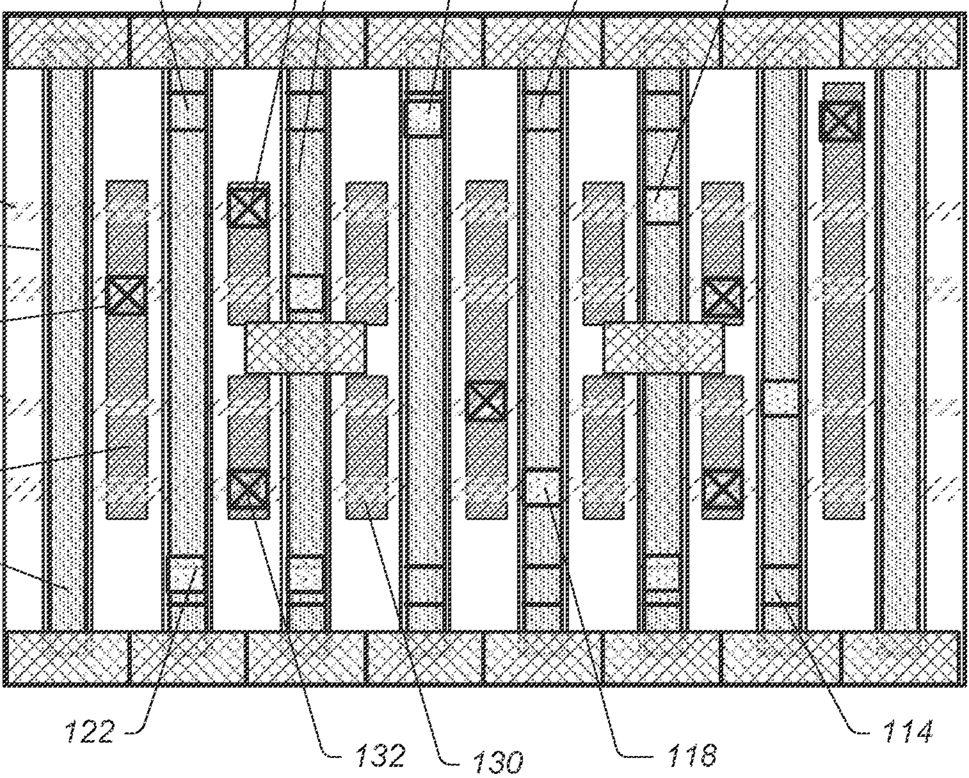



FIG. 1




110 = Non-Planar Vertical Conducting Structure
112 = Gate Metal
114 = Contact for Gate Metal to Gate Extension Metal (GEM)
116 = GEM
118 = Gate Extension Contact for GEM to Metal0 Over Vertical Conducting Structure
120 = Metal0
122 = Gate Extension Contact for GEM to Metal0
130 = Local Interconnect
132 = Source/Drain Contact
140 = Gate Cut Layer

FIG. 2

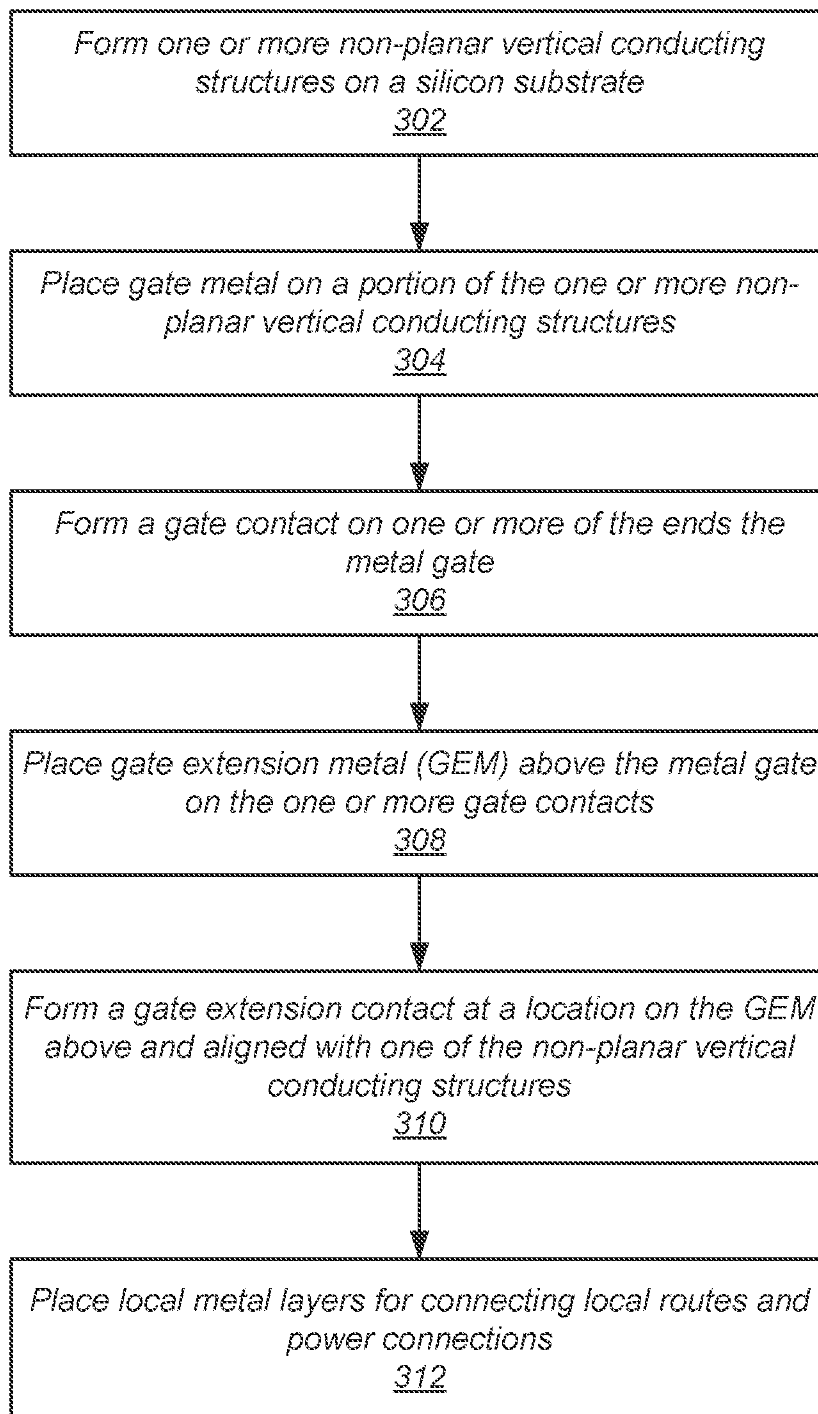



FIG. 3

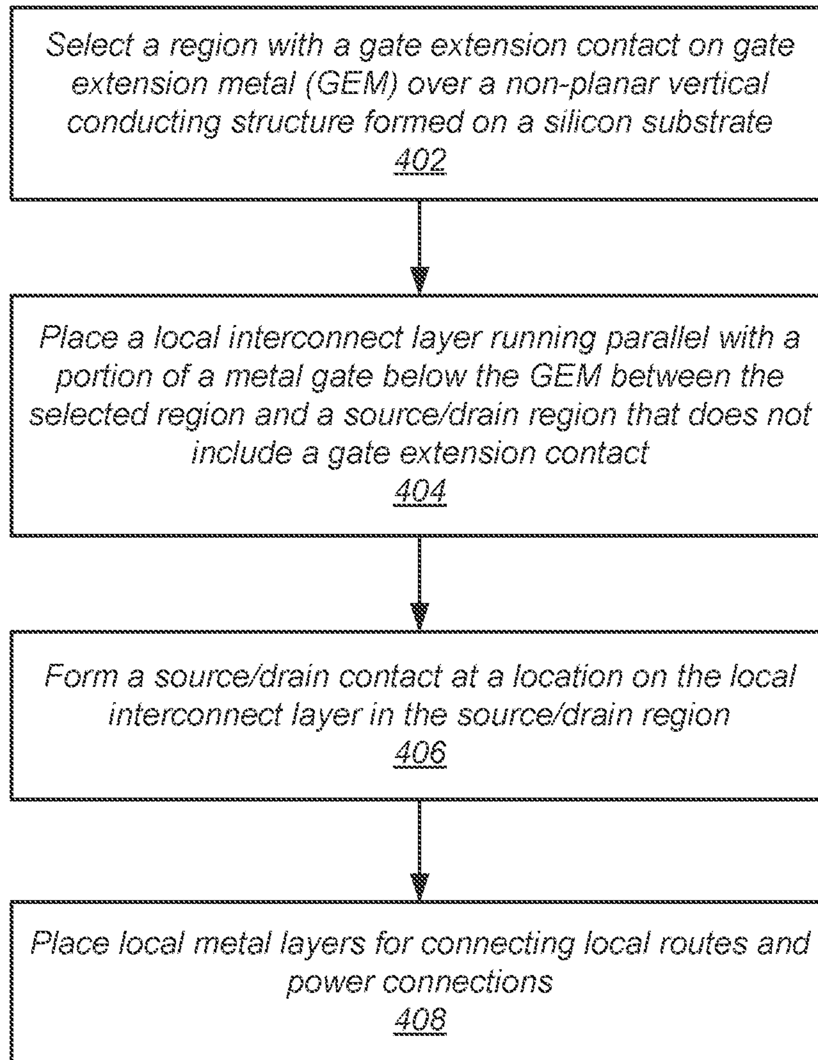



FIG. 4

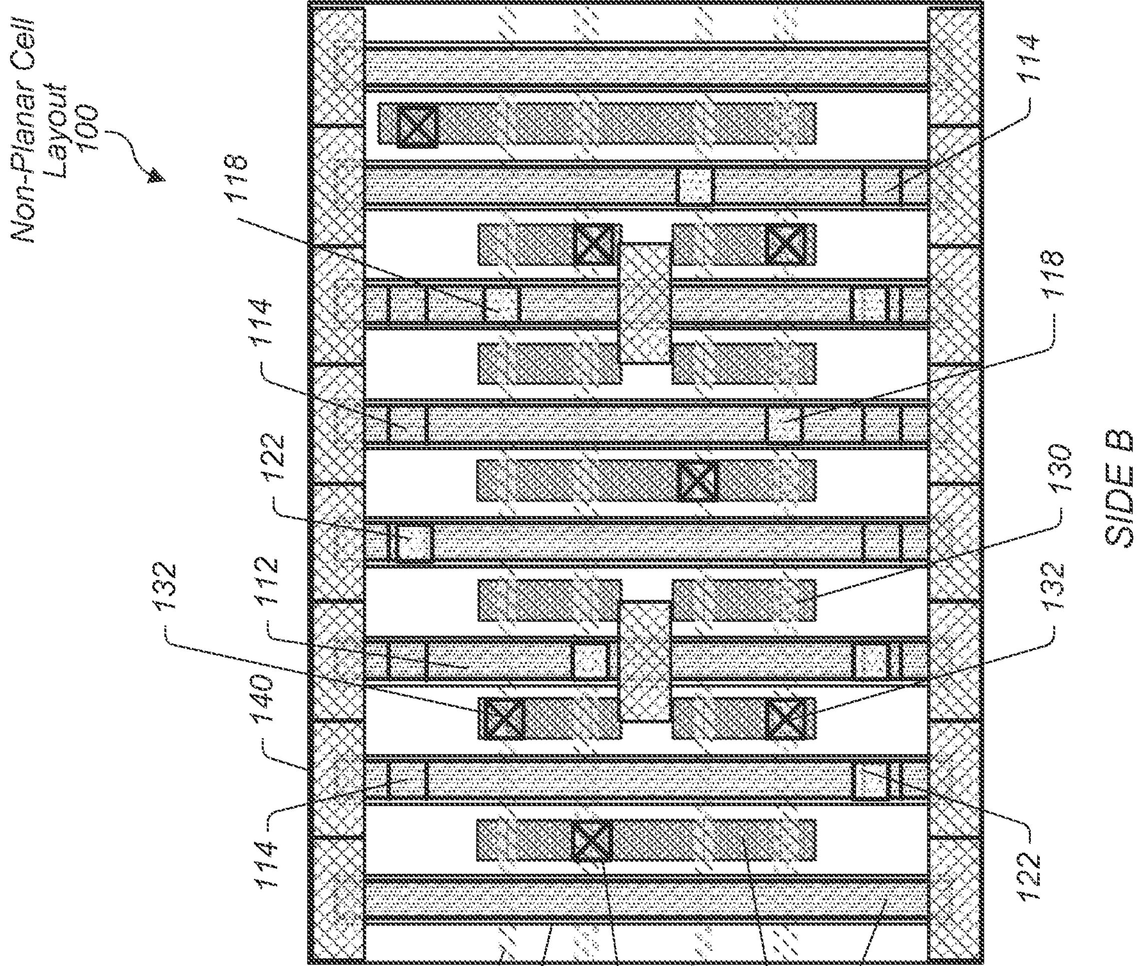
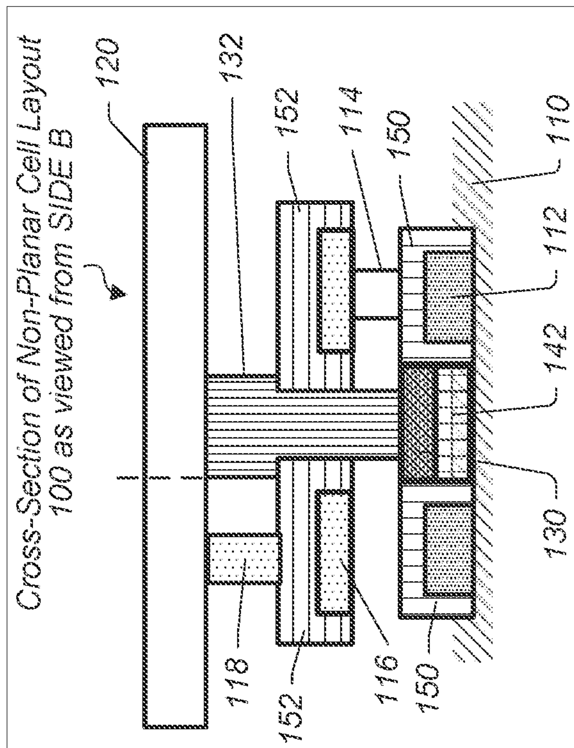
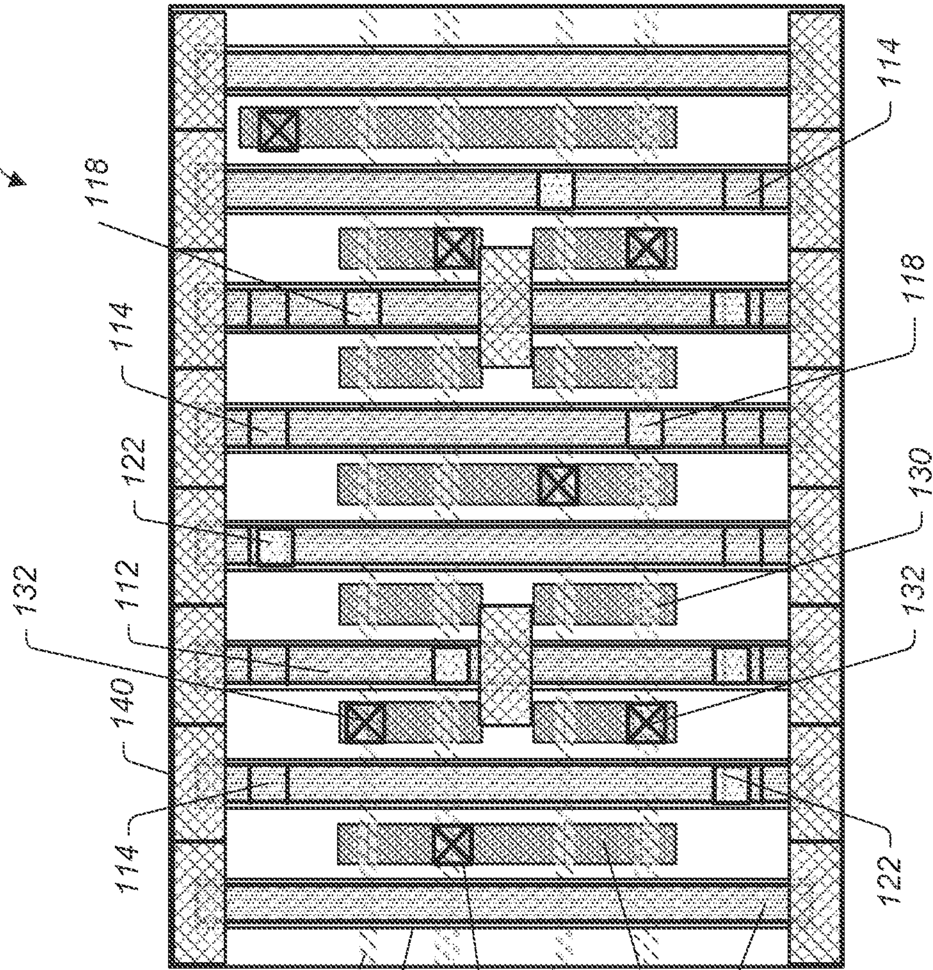


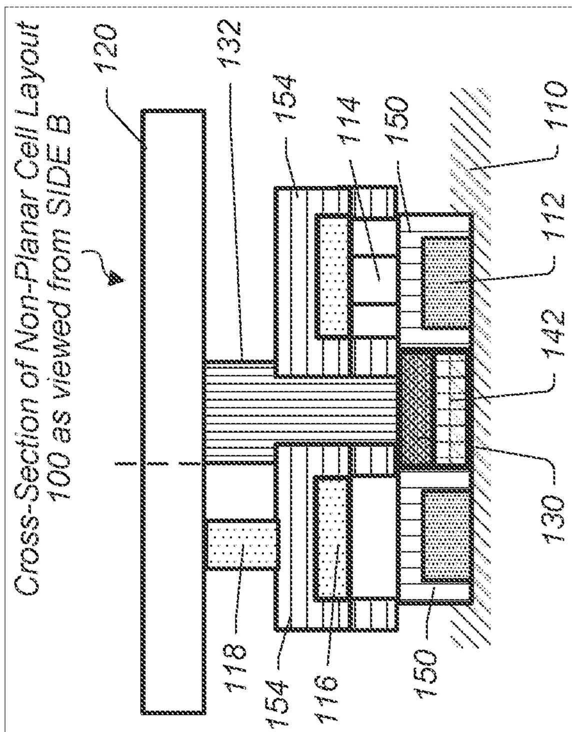

FIG. 5




110 = Non-Planar Vertical Conducting Structure
112 = Gate Metal
114 = Contact for Gate Metal to Gate Extension Metal (GEM)
116 = GEM
118 = Gate Extension Contact for GEM to Metal0 Over Vertical Conducting Structure
120 = Metal0
122 = Gate Extension Contact for GEM to Metal0
130 = Local Interconnect
132 = Source/Drain Contact
140 = Gate Cut Layer
142 = Source/Drain Area
150 = Isolation Spacer
152 = Isolation Spacer

Non-Planar Cell Layout 100




110 = Non-Planar Vertical Conducting Structure
112 = Gate Metal
114 = Contact for Gate Metal to Gate Extension Metal (GEM)
116 = GEM
118 = Gate Extension Contact for GEM to Metal0 Over Vertical Conducting Structure
120 = Metal0
122 = Gate Extension Contact for GEM to Metal0
130 = Local Interconnect
132 = Source/Drain Contact
140 = Gate Cut Layer
142 = Source/Drain Area
150 = Isolation Spacer
154 = Isolation Spacer

SIDE B

FIG. 6

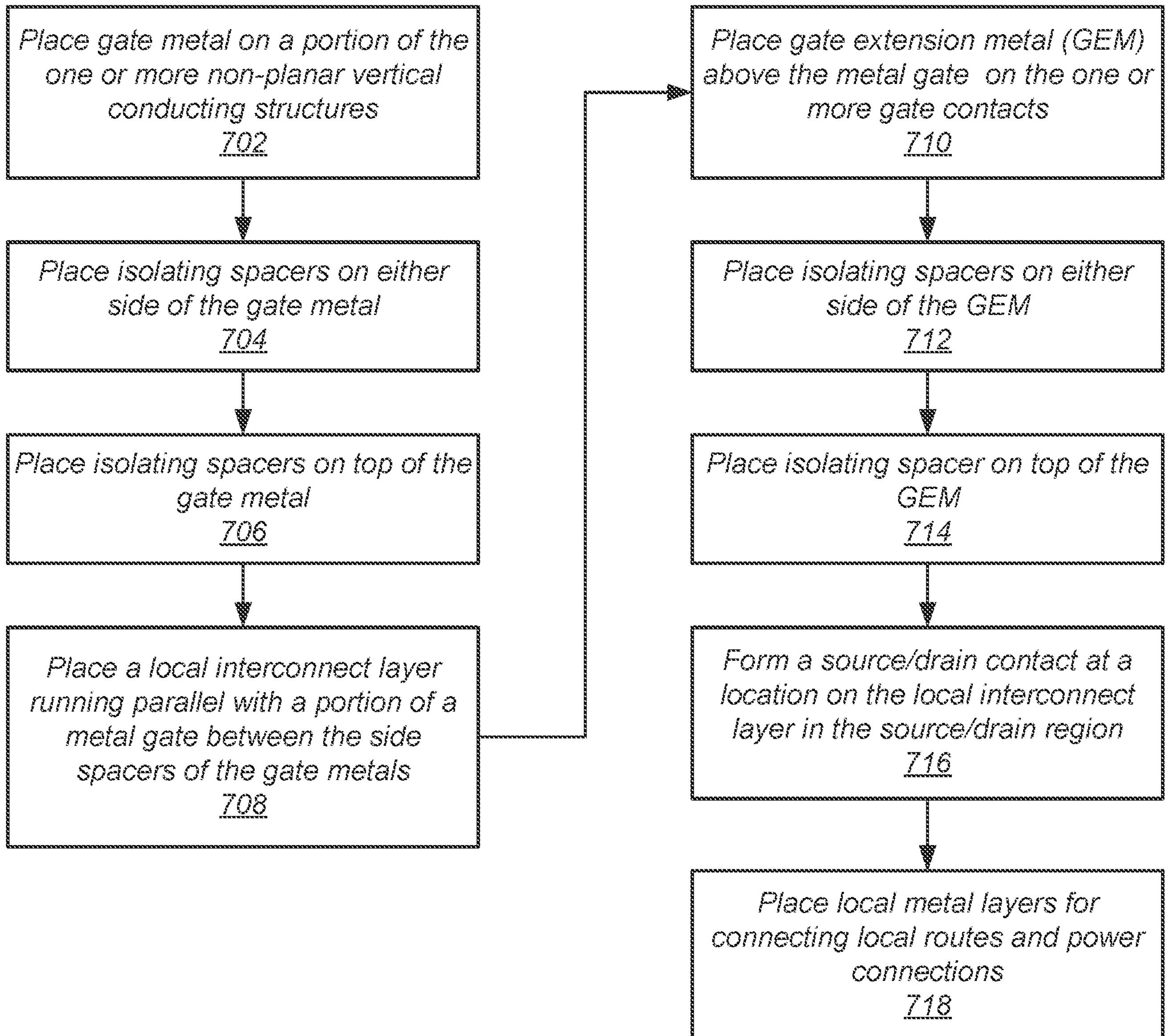



FIG. 7

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/024364

**A. CLASSIFICATION OF SUBJECT MATTER**
INV. H01L21/768 H01L21/8234 H01L21/8238
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | EP 3 174 105 A1 (INTEL CORP [US]) 31 May 2017 (2017-05-31) paragraph [0009] - paragraph [0056]; figures 1-6 | 1-20 |
| A | US 2017/207166 A1 (LAI JUI-YAO [TW] ET AL) 20 July 2017 (2017-07-20) figures 11A-D, 12 | 1-20 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 3 July 2019 | 15/07/2019 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Norga, Gerd |

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International application No
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