(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 October 2017 (05.10.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/166284 A1

(51) International Patent Classification:
H01L 23/552 (2006.01) *H01L 23/28* (2006.01)

(21) International Application Number:
PCT/CN2016/078304

(22) International Filing Date:
1 April 2016 (01.04.2016)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).

(72) Inventor; and
(71) Applicant *(for BZ only)*: **GUO, Mao** [CN/CN]; Room 602, Buliding 151, Nong 155 Liming Road, Minhang, Shanghai 201199 (CN).

(74) Agent: **NTD PATENT AND TRADEMARK AGENCY LIMITED**; 10th Floor, Block A, Investment Plaza, 27 Jinrongdajie, Xicheng District, Beijing 100033 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) **Title**: MOLD COMPOUND WITH COATED BEADS

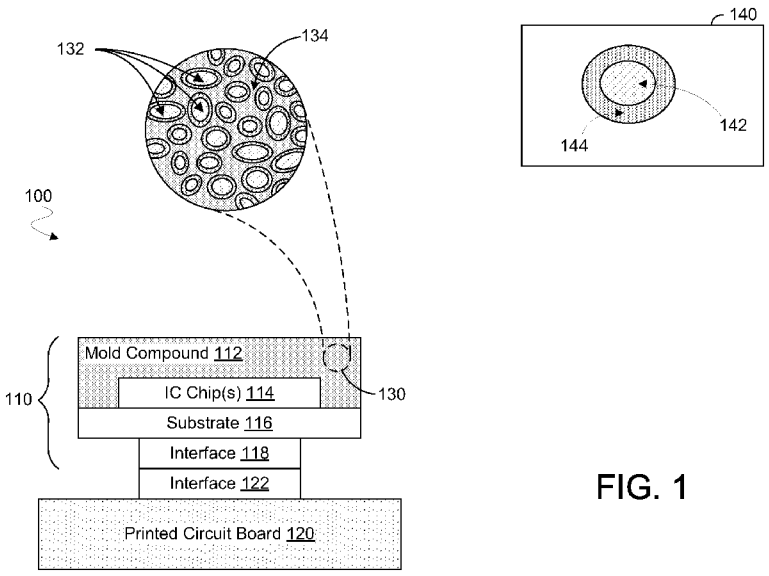


FIG. 1

(57) **Abstract**: Techniques and mechanisms for providing a packaged integrated circuit (IC) device. In an embodiment, a packaged IC device includes a mold compound disposed at least partially around an IC chip. The mold compound comprises coated beads suspended in a media that is to aid in mechanical reinforcement of such coated beads. Some or all such beadseach include a conductive core and an insulative coating surrounding the core. The cores contribute to an electrical shielding property of the mold compound as a whole. The coatings prevent the conductive cores from shorting circuitry of the packaged IC device. In another embodiment, a softness of the coatings mitigates damage to integrated circuitry during processing which forms and hardens the mold compound on an IC chip.

WO 2017/166284 A1

MOLD COMPOUND WITH COATED BEADS

BACKGROUND

1. Technical Field

Embodiments of the invention relate generally to a packaged integrated circuit devicesuch as a system-in-package and more particularly, but not exclusively, to a mold compound that protects integrated circuit structures.

2. Background Art

Solid State Drives (SSDs) based on NAND flash memory are just one type of integrated circuit (IC) technology that has proliferated in recent years, both in high performance enterprise storage applications and in consumer devices. To satisfy customer demand, much effort has been taken to decrease the form factor of IC devices while maintaining or improving their capabilities.

BRIEF DESCRIPTION OF THE DRAWINGS

The various embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which:

FIG. 1 is a cross-sectional diagram illustrating elements of a system including a packaged integrated circuit device according to an embodiment.

FIG. 2 is a flow diagram illustrating elements of a method of manufacturing a packaged device according to an embodiment.

FIG. 3 shows cross-sectional views of processing to manufacture a packaged integrated circuit device according to an embodiment.

FIGs. 4A, 4B show cross-sectional views of respective packaged integrated devices each according to a corresponding embodiment.

FIG.5 is a high-level functional block diagram illustrating features of a computing device in accordance with one embodiment.

FIG. 6 is an interposer implementing one or more embodiments.

FIG. 7 is a high-level functional block diagram illustrating features of a computing device built in accordance with an embodiment.

DETAILED DESCRIPTION

Embodiments discussed herein variously include techniques or mechanisms to protect integrated circuitry that is disposed in a mold compound (MC) of a packaged device. A MC according to one embodiment includes coated beads that mitigate exposure of an IC chip to electromagnetic radiation. Alternatively or in addition, such beads may mitigate exposure of such integrated circuitry to mechanical damage during mold processing. For example, a coating

of the beads may help avoid scratching of passivation (and/or other) structures that might otherwise be caused by conventional mold compound materials.

As used herein, "packaged IC device" refers to any of a variety of devices that comprise integrated circuitry that has been packaged. A packaged IC device may include mold compound, one or more IC chips and, in some embodiments, a substrate to couple the one or more IC chips to each other and/or to a hardware interface. Such a substrate – e.g., comprising any of a variety of thin core or coreless structures – may include one or more layers of an insulator material and interconnect structures disposed therein. The interconnect structures may provide for coupling of the IC chip to conductive contacts (such as pads, bumps or other such structures) that are disposed on an opposite side of the substrate. Coated beads of an MC may serve as a substitute, at least in part, for any of a variety of one or more conventional shielding structures.

One technique for attaining smaller form factor devices is to package integrated circuitry in a relatively thin (lower z-height) amount of a mold compound. However, thinner packaging tends to result in one or more IC dies of a packaged IC device being exposed to higher levels of electromagnetic radiation from a surrounding environment. One source of such radiation is lasers that are typically used during production to mark an external surface of the packaged IC device. Another source is X-rays and other highly energized radiation used in manufacturing processes to inspect circuit connectivity. This increased radiation exposure is more likely to damage, or otherwise affect the operation of, flash memory transistors and/or other active circuit elements of an IC die.

Moreover, conventional package processing typically includes applying very high pressures while a mold compound is disposed around one or more IC chips. Mold compounds will often include a silica material that, when under such pressure, tends to scratch or otherwise damage relatively soft passivation regions disposed on or around integrated circuitry. As the demand for small form factor IC devices continues to grow, there is expected to be an increasing premium placed on incremental improvements to the reliability of packaged IC devices.

An MC according to an embodiment may include one or more other materials in which coated beads of the MC are suspended. For brevity, such one or more other materials are referred to herein as a "suspension media." In one illustrative embodiment, a suspension media includes an epoxy resin. A suspension media may have fluid characteristics during a molding process. Subsequently (e.g., after a curing of the MC), such a suspension media may form a solid with coated beads of the MC. A suspension material may function as a binder to mechanically and/or chemically aid the coated beads in the formation of support structures within a package mold. For example, a suspension material may reinforce an arrangement of coated beads in the MC which aid in electromagnetic shielding of an IC chip.

The technologies described herein may be implemented in one or more electronic devices. Non-limiting examples of electronic devices that may utilize the technologies described herein include any kind of mobile device and/or stationary device, such as cameras, cell phones, computer terminals, desktop computers, electronic readers, facsimile machines, kiosks, netbook computers, notebook computers, internet devices, payment terminals, personal digital assistants, media players and/or recorders, servers (e.g., blade server, rack mount server, combinations thereof, etc.), set-top boxes, smart phones, tablet personal computers, ultra-mobile personal computers, wired telephones, combinations thereof, and the like. Such devices may be portable or stationary. In some embodiments the technologies described herein may be employed in a desktop computer, laptop computer, smart phone, tablet computer, netbook computer, notebook computer, personal digital assistant, server, combinations thereof, and the like. More generally, the technologies described herein may be employed in any of a variety of electronic devices including a package comprising amold compound including coated beads.

FIG. 1 shows features of a system 100 including a package material according to an embodiment. System 100 may include, or function as a component of, a computer (e.g., a server, desktop computer, laptop computer, tablet or the like), smart phone or any of a variety of other hardware platforms including a packaged IC device.

In the illustrative embodiment shown, system 100 includes a packaged device 110 comprising one or more IC chips (as represented by the illustrative IC chip 114), an interface 118 and a substrate 116 coupling the one or more IC chips to interface 118. IC chip 114 may include a system-on-chip (SoC) or any of various other circuitry comprising processor logic, memory logic, controller logic and/or the like. In some embodiments, packaged device 110 comprises one or more additional and/or different IC chips.

IC chip 114 and interface 118 may be variously coupled, directly or indirectly, on opposite sides of substrate 116. Interface 118 may include input/output (I/O) contacts (e.g., including conductive pads, bumps, pins and/or other such structures) to enable access to IC chip 114 via substrate 116. Substrate 116 may include one or more layers of an insulator material and interconnect structures – e.g., including conductive vias, traces and/or the like – disposed therein. Such interconnect structures may aid in providing access to IC chip 114 via interface 118. By way of illustration and not limitation, substrate 116 may include a laminate core or, alternatively, a monolithic core – e.g., where substrate 116 includes a thin core. Although some embodiments are not limited in this regard, substrate 116 includes structures adapted from any of various conventional coreless substrate designs.

In an embodiment, a package material of device 110 includes a mold compound (MC) 112 disposed on – e.g., around – one or both of IC chip 114 and substrate 116. MC 112 may include

coated beads that, during and/or after manufacture of packaged device 110, aid in mitigating damage to IC chip 114. For example, MC 112 may include a media 134 and beads 132 suspended therein (as illustrated in the detail view of a region 130).

As used herein with reference to a mold compound, "beads" (or "coated beads") refers to spheroid – e.g., ellipsoid – structures that each comprise a core and a coating disposed around the core. Such beads may vary from one another with respect to size, shape and/or materials. A core of a bead may include a conductor (e.g., comprising one or more metals) and the coating may comprise a different material that, as compared to the conductor, is more electrically insulating and/or softer. By way of illustration and not limitation, the bead shown in inset 140 includes a core 142 and a coating 144 disposed around core 142.

The conductive cores of beads 132 may contribute to an overall electrical shielding characteristic of MC 112. Such shielding may mitigate exposure of IC chip 114 to electromagnetic radiation that might enter MC 112 from an environment near system 100. Moreover, the coatings of beads 132 may, due to their relative softness, mitigate damage to IC chip 114 that might otherwise be caused by the cores during packaging that compresses and/or otherwise disposes MC 112 on and around IC chip 114. Alternatively or in addition, the coatings of MC 112 may prevent conductive cores of beads 132 from shorting out integrated circuitry of IC chip 114.

For example, core 142, and/or other cores of beads 132, may include iron, copper, zinc, aluminum and/or any of various other suitable metals. Bead coating 144, and/or other coatings of beads 132, may include any of a variety of materials that are insulative and/or soft – e.g., as compared to the beads' cores. By way of illustration and not limitation, a coating material may comprise any of various polymers including, but not limited to, polyimide, polyethylene terephthalate (PET) and/or the like. In one embodiment, a coating material has a dielectric constant that is equal to or more than 3.0 – e.g., wherein the dielectric constant that is equal to or more than 3.2 and, in some embodiments, equal to or more than 3.4. Such a coating material may be deformable (soft) to mitigate damage that might otherwise result from the MC being disposed on and/or pressured against integrated circuitry. By way of illustration and not limitation, PET has a Rockwell hardness of M94-101 and polyimide has a Rockwell hardness of E52-99. However, other insulative coating materials may be softer or harder, in various embodiments, provided any such coating material is softer than the conductive core it surrounds.

Formation of beads 132 (and/or other such coated beads) may include operations adapted, for example, from processing used in the pharmaceutical industry – e.g., where such processing is to coat particles of a fine powder with a sprayed insulator material that is dispensed in a rotating chamber. The particular techniques for coating such particles are not detailed herein to

avoid obscuring certain features of some embodiments.

Although some embodiments are not limited in this regard, system 100 may further include, or couple to, a support structure for packaged device 110, such as the illustrative printed circuit board 120. Printed circuit board 120 may aid in coupling of packaged device 110 – e.g., via I/O contacts of an interface 122 – to hardware, software, a user interface and/or any of various other such mechanisms (not shown) that are included in, or are to couple to, system 100.

FIG. 2 shows features of a method 200 for producing a packaged circuit device according to an embodiment. Method 200 may produce a device having some or all of the features of packaged device 110, for example. In an embodiment, method 200 includes, at 210, forming contacts on a first side of a substrate such as substrate 116. For example, interface 118 may include some or all of the contacts formed at 210. In one embodiment, the forming at 210 includes semiconductor processing (such as one or more mask, photolithography, etch, metal deposition and/or other fabrication operations) adapted from conventional techniques for building respective conductive contacts on a substrate and on one or more IC chips. Some embodiments are not limited with respect to such techniques, which are not detailed herein to avoid obscuring certain features of various embodiments.

Method 200 may further comprise, at 220, coupling an integrated circuit (IC) chip to the contacts via a second side of the substrate – e.g., where the second side is opposite the first side. The coupling at 220 may include, for example, wire bonding the IC chip to the substrate in addition to adhering or otherwise mechanically attaching the IC chip to the substrate. In some embodiments, one or more additional IC chips may be variously coupled directly or indirectly to the substrate – e.g., where multiple IC chips are arranged in a side-by-side configuration or a stacked configuration. The one or more additional IC chips may each be mechanically attached, directly of via another IC chip, to the substrate – e.g., in addition to being wire bonded to the substrate and/or another IC chip. In some embodiments, the coupling at 220 includes only indirectly coupling the IC chip to the substrate. For example, the IC chip may itself be part of a first package device prior to the coupling at 220 – e.g., wherein method 200 is to fabricate a package-in-package IC device which includes the first packaged device. In an illustrative embodiment, the coupling at 220 may be part of operations that variously surface mount (for example) a packaged NAND memory, a controller and one or more passive circuit components onto the substrate. Any of a variety of conventional chip stacking, wire bonding, surface mounting and/or other techniques may be adapted to perform the coupling at 220.

Method 200 may further comprise, at 230, packaging the IC chip with a mold compound which includes a suspension media and coated beads disposed therein. The packaging at 230 may be performed after the coupling at 220, for example. In an embodiment, the packaging at

230 includes disposing the mold compound at least partially around the IC chip – e.g., using operations adapted from any of a wide range of conventional encapsulation techniques such as resin transfer molding, sheet molding and/or the like.

Some or all of the suspension media may be adapted from any of a wide range of conventional package materials. Examples of such materials include, but are not limited to, an epoxy resin, such as biphenyl or modified biphenyl, and/or any of various filler materials such as a silica, thermally conductive aluminum nitride (AlN) and boron nitride (BN) and/or other additives such as mold release agents, surfactants, etc. Some or all coated beads of the mold compound may mitigate damage to integrated circuitry during or after the packaging at 230. For example, coated beads of the mold compound may each include a conductive core and a coating including an insulation material.Beads of the mold compound may have an average cross-sectional width (e.g., a diameter) in a range from 10 micrometers (μm) to 100μm – e.g., wherein an average volume of beads is within a range from 400 μm^3 to 2000000 μm^3. Alternatively or in addition, such beads may have an eccentricity of 0.9 or less. In some embodiments, the average thickness of a layer of coating material on the beads is in a range from 2 μm^3 to 5 μm^3. However, these parameters of coated beads are merely illustrative, and may vary significantly in different embodiments, according to implementation-specific details.

In some embodiments, a fractional proportion of coated beads in the mold compound may contribute to electrical shielding and/or other mechanical properties that provide for improved protection of integrated circuitry. By way of illustration and not a limitation, beads may comprise 35% or more of a mold compound by volume. Such beads may comprise, for example, between 50% and 80% of the mold compound by volume. In some embodiments, a mold compound comprises between 60% and 75% beads by unit volume. However, the fractional proportional of coated beads in a mold compound may vary significantly in various embodiments.

Although some embodiments are not limited in this regard, method 200 may include one or more additional operations (not) shown to provide a packaged device and/or connectivity thereof. Such additional operations may include, for example, metallization processes to form a ball grid array or other conductive contacts of a hardware interface. Additionally, method 200 may further include singulation operations to separate two or more packaged devices from one another. In some embodiments, method 200 couple the packaged IC device to a printed circuit board or other external structure.

FIG. 3 shows cross-sectional views illustrating respective stages 300, 302 of processing to fabricate a packaged integrated circuit device according to one embodiment. The processing represented in FIG. 3 may include operations of method 200 – e.g., where such processing is to

fabricate packaged device 100 at least in part.

At stage 300, an IC chip 320 may be bonded to an upper surface of a substrate 310 – e.g., by a flip chip process. In an embodiment, substrate 310 includes a thin core or a coreless substrate, comprising layers of interconnections and vias, with one surface having conductive bumps or other contacts for electrical connection to corresponding contacts of IC chip 320. The lower surface of the substrate 310 may comprise or have disposed thereon an array 340 of electrical connects, such as solder balls, serving as input/output electrical connections for the package. While various embodiments are described herein as variously including a thin core or coreless substrate, other embodiments are not limited to such context, i.e., practice of other embodiments may have uses with various types of chips, substrates and/or mounting technologies, e.g., such as a flip chip pin grid array. Although some embodiments are not limited in this regard, an underfill material 330 may dispensed – e.g., at the edges of IC die 320 – and allowed to seep to a space between the IC die 320 and substrate 310 by a capillary action.

At stage 302, a mold compound 350 may be disposed at least partially (e.g., in at least two dimensions) around IC chip 320 and/or substrate 310. Deposition of mold compound 350 may include operations adapted from any of various conventional molding techniques such as injection molding, resin transfer molding, sheet molding and/or the like. In an embodiment, mold compound 350 includes coated beads that mitigate damage to structures such as those of IC chip 320 and/or substrate 310. For example, such coated beads may be suspended in a media of mold compound 350 that, when cured, reinforces such beads. The beads may contribute to electrical shielding of mold compound 350, while at the same time mitigating scratching and/or electrical shorting at IC chip 320 and/or at substrate 310.

The number, arrangement and type of IC chips and/or other components packaged in mold compound 350 is merely illustrative, and may vary in different embodiments according to implementation-specific details. In one embodiment, IC chip 320 is one of multiple IC chips that, for example, are arranged to form an IC stack configuration and/or a side-by-side IC chip configuration. Such IC chips may be variously wire bonded to each other and/or to substrate 310. The arrangement of such IC chips may be adapted, for example, from conventional chip stacking and wire bonding techniques.

In some embodiments, IC chip 320 is surrounded by mold compound 350, but is not directly in contact with mold compound 350. For example, processing such as that illustrated by stages 300, 302 may manufacture a package-in-package device wherein a first packaged device – e.g., a packaged NAND memory device – is surface mounted or otherwise coupled, directly or indirectly, to substrate 310. In such an embodiment, one or more other components – e.g., another packaged device, any of various passive circuit elements, an application specific IC

(ASIC) and/or the like – may be similarly coupled to such substrate. Mold compound 350 may be subsequently disposed around the first packaged device and the one or more other components to form a package-in-package integrated circuit device.

FIGs. 4A, 4B show in cross-sectional view respective packaged IC devices 400, 450 each according to a corresponding embodiment. One or both of packaged IC devices 400, 450 may include features of packaged device 110, for example. In an embodiment, performance of method 200 results in packaged IC device 400 and/or packaged IC device 450.

In the embodiment illustrated by FIG. 4A, packaged device 400 includes a mold compound 430 and a stack 420 of IC dies disposed within mold compound 430. A substrate 410 of packaged device 400 may facilitate coupling of stack 420 to other circuitry that is included in, or is to couple to, packaged device 400. For example, stack 420 may be adhered, or otherwise mechanically coupled, to a side 412 of substrate 410 – e.g., wherein conductive contacts 416 of a hardware interface are disposed on an opposite side 414 of substrate 410. Individual IC dies of stack 420 may be variously wire bonded or otherwise coupled directly or indirectly to one another. Alternatively or in addition, such IC dies may be coupled to contacts 416 via substrate 410. To protect damage to integrated circuitry of stack 420 – and in some embodiments, to further prevent an electrical short at such integrated circuitry – mold compound 430 may include coated beads having features variously described herein.

Packaged IC device 450 is one example of an embodiment including a package-in-package device which comprises a mold compound including coated beads. For example, a mold compound 480 of packaged IC device 450 may include coated beads to facilitate electrical shielding and/or other protection of integrated circuitry. Mold compound 480 may be disposed on a substrate 460 and further disposed around components that are variously coupled, directly or indirectly, to a side 462 of substrate 460. In the illustrative embodiment shown, such components include a packaged device 470 and various other components 468 such as one or more passive circuit components, IC chips and/or the like. However, the particular type, arrangement and number of component coupled at side 462 may vary, in different embodiments, according to implementation specific details.

A hardware interface 472 – e.g., including surface mount contacts – may provide for coupling of packaged device 470 to side 462. Conductive contacts 466 of another hardware interface may be disposed on a side 464 of substrate 410 which is opposite side 462. Substrate 460 may variously provide for interconnection between packaged device 470, components 468 and contacts 466 may be variously coupled each other via interconnect structures (not shown) disposed in substrate 460.

FIG.5 illustrates a computing device500in accordance with one embodiment. The

computing device500 houses a board502. The board502 may include a number of components, including but not limited to a processor504 and at least one communication chip506. The processor504 is physically and electrically coupled to the board502. In some implementations the at least one communication chip506 is also physically and electrically coupled to the board502. In further implementations, the communication chip506 is part of the processor504.

Depending on its applications, computing device500 may include other components that may or may not be physically and electrically coupled to the board502. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip506 enables wireless communications for the transfer of data to and from the computing device500. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip506 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device500 may include a plurality of communication chips506. For instance, a first communication chip506 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip506 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor504 of the computing device500 includes an integrated circuit die packaged within the processor504. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The communication chip506 also includes an integrated circuit die packaged within the communication chip506.

In various implementations, the computing device500 may be a laptop, a netbook, a

notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device500 may be any other electronic device that processes data.

Some embodiments may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to an embodiment. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

FIG. 6 illustrates an interposer 600 that includes one or more embodiments. The interposer 600 is an intervening substrate used to bridge a first substrate 602 to a second substrate 604. The first substrate 602 may be, for instance, an integrated circuit die. The second substrate 604 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 600 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 600 may couple an integrated circuit die to a ball grid array (BGA) 606 that can subsequently be coupled to the second substrate 604. In some embodiments, the first and second substrates 602, 604 are attached to opposing sides of the interposer 600. In other embodiments, the first and second substrates 602, 604 are attached to the same side of the interposer 600. And in further embodiments, three or more substrates are interconnected by way of the interposer 600.

The interposer 600 may be formed of an epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 608 and vias 610, including but not limited to through-silicon vias (TSVs) 612. The interposer 600 may further include embedded devices 614, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and

electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 600. In accordance with some embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 600.

FIG. 7 illustrates a computing device 700 in accordance with one embodiment. The computing device 700 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 700 include, but are not limited to, an integrated circuit die 702 and at least one communication chip 708. In some implementations the communication chip 708 is fabricated as part of the integrated circuit die 702. The integrated circuit die 702 may include a CPU 704 as well as on-die memory 706, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 700 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within anSoC die. These other components include, but are not limited to, volatile memory 710 (e.g., DRAM), non-volatile memory 712 (e.g., ROM or flash memory), a graphics processing unit 714 (GPU), a digital signal processor 716, a crypto processor 742 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 720, an antenna 722, a display or a touchscreen display 724, a touchscreen controller 726, a battery 729 or other power source, a power amplifier (not shown), a global positioning system (GPS) device 728, a compass 730, a motion coprocessor or sensors 732 (that may include an accelerometer, a gyroscope, and a compass), a speaker 734, a camera 736, user input devices 738 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 740 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communications chip 708 enables wireless communications for the transfer of data to and from the computing device 700. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 708 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth,

derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 700 may include a plurality of communication chips 708. For instance, a first communication chip 708 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 708 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. In various embodiments, the computing device 700 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 700 may be any other electronic device that processes data.

In one implementation, a packaged device comprises a substrate including a first side and a second side opposite the first side, wherein contacts are disposed on the first side, an integrated circuit (IC) chip disposed on the second side, the IC chip coupled to the contacts via the substrate, and a mold compound disposed at least partially around the IC chip, the mold compound comprising a suspension media and coated beads disposed in the suspension media, wherein the coated beads each include a conductive core and layer of an insulator material disposed around the conductive core.

In an embodiment, the conductive cores of the coated beads includes a metal, and wherein the insulator material is softer than the metal. In another embodiment, a dielectric constant of the insulator material is equal to or more than 3.0. In another embodiment, the dielectric constant is equal to or more than 3.2. In another embodiment, the dielectric constant is equal to or more than 3.4. In another embodiment, the coated beads are 35% or more of the mold compound by volume. In another embodiment, the coated beads are between 50% and 80% of the mold compound by volume. In another embodiment, the coated beads are between 60% and 75% of the mold compound by volume. In another embodiment, the conductive cores of the coated beads include iron, copper, zinc or aluminum. In another embodiment, the insulator material includes a polymer.

In another implementation, a method comprises forming contacts on a first side of a substrate, coupling an integrated circuit (IC) chip to the contacts via a second side of the substrate, the second side opposite to the first side, and while the IC chip is coupled to the

contacts, packaging the IC chip, including disposing mold compound at least partially around the IC chip, the mold compound including a suspension media and coated beads disposed in the suspension media, wherein the coated beads each include a conductive core and layer of an insulator material disposed around the conductive core.

In another embodiment, the conductive cores of the coated beads includes a metal, and wherein the insulator material is softer than the metal. In another embodiment, a dielectric constant of the insulator material is equal to or more than 3.0. In another embodiment, the dielectric constant is equal to or more than 3.2. In another embodiment, the dielectric constant is equal to or more than 3.4. In another embodiment, the coated beads are 35% or more of the mold compound by volume. In another embodiment, the coated beads are between 50% and 80% of the mold compound by volume. In another embodiment, the coated beads are between 60% and 75% of the mold compound by volume. In another embodiment, the conductive cores of the coated beads include iron, copper, zinc or aluminum. In another embodiment, the insulator material includes a polymer.

In another implementation, a system comprises a packaged device including a substrate including a first side and a second side opposite the first side, wherein contacts are disposed on the first side, an integrated circuit (IC) chip disposed on the second side, the IC chip coupled to the contacts via the substrate, and a mold compound disposed at least partially around the IC chip, the mold compound comprising a suspension media and coated beads disposed in the suspension media, wherein the coated beads each include a conductive core and layer of an insulator material disposed around the conductive core. The system further comprises a display device coupled to the packaged device, the display device to display an image based on signals exchanged with the IC chip.

In another embodiment, the conductive cores of the coated beads includes a metal, and wherein the insulator material is softer than the metal. In another embodiment, a dielectric constant of the insulator material is equal to or more than 3.0. In another embodiment, the dielectric constant is equal to or more than 3.2. In another embodiment, the dielectric constant is equal to or more than 3.4. In another embodiment, the coated beads are 35% or more of the mold compound by volume. In another embodiment, the coated beads are between 50% and 80% of the mold compound by volume. In another embodiment, the coated beads are between 60% and 75% of the mold compound by volume. In another embodiment, the conductive cores of the coated beads include iron, copper, zinc or aluminum. In another embodiment, the insulator material includes a polymer.

Techniques and architectures for packaging integrated circuitry are described herein. In the above description, for purposes of explanation, numerous specific details are set forth in

order to provide a thorough understanding of certain embodiments. It will be apparent, however, to one skilled in the art that certain embodiments can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the description.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

Some portions of the detailed description herein are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the computing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally, conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the discussion herein, it is appreciated that throughout the description, discussions utilizing terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Certain embodiments also relate to apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs)

such as dynamic RAM (DRAM), EPROMs, EEPROMs, magnetic or optical cards, or any type of media suitable for storing electronic instructions, and coupled to a computer system bus.

The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear from the description herein. In addition, certain embodiments are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of such embodiments as described herein.

Besides what is described herein, various modifications may be made to the disclosed embodiments and implementations thereof without departing from their scope. Therefore, the illustrations and examples herein should be construed in an illustrative, and not a restrictive sense. The scope of the invention should be measured solely by reference to the claims that follow.

CLAIMS

What is claimed is:

1. A packaged device comprising:

a substrate including a first side and a second side opposite the first side, wherein contacts are disposed on the first side;

an integrated circuit (IC) chip disposed on the second side, the IC chip coupled to the contacts via the substrate; and

a mold compound disposed at least partially around the IC chip, the mold compound comprising a suspension media and coated beads disposed in the suspension media, wherein the coated beads each include a conductive core and layer of an insulator material disposed around the conductive core.

2. The packaged device of claim 1, wherein the conductive cores of the coated beads includes a metal, and wherein the insulator material is softer than the metal.

3. The packaged device of any of claims 1 and 2, wherein a dielectric constant of the insulator material is equal to or more than 3.0.

4. The packaged device of claim 3, wherein the dielectric constant is equal to or more than 3.2.

5. The packaged device of claim 4, wherein the dielectric constant is equal to or more than 3.4.

6. The packaged device of any of claims 1-3, wherein the coated beads are 35% or more of the mold compound by volume.

7. The packaged device of claim 6, wherein the coated beads are between 50% and 80% of the mold compound by volume.

8. The packaged device of claim 7, wherein the coated beads are between 60% and 75% of the mold compound by volume.

9. The packaged device of any of claims 1-3 and 6, wherein the conductive cores of the coated beads include iron, copper, zinc or aluminum.

10. The packaged device of any of claims 1-3, 6 and 9, wherein the insulator material includes a polymer.

11. A method comprising:

forming contacts on a first side of a substrate;

coupling an integrated circuit (IC) chip to the contacts via a second side of the substrate, the second side opposite to the first side; and

while the IC chip is coupled to the contacts, packaging the IC chip, including disposing mold compound at least partially around the IC chip, the mold compound including a suspension media and coated beads disposed in the suspension media, wherein the coated beads each include a conductive core and layer of an insulator material disposed around the conductive core.

12. The method of claim 11, wherein the conductive cores of the coated beads includes a metal, and wherein the insulator material is softer than the metal.

13. The method of any of claims 11 and 12, wherein a dielectric constant of the insulator material is equal to or more than 3.0.

14. The method of claim 13, wherein the dielectric constant is equal to or more than 3.2.

15. The method of claim 14, wherein the dielectric constant is equal to or more than 3.4.

16. The method of any of claims 11-13, wherein the coated beads are 35% or more of the mold compound by volume.

17. The method of claim 16, wherein the coated beads are between 50% and 80% of the mold compound by volume.

18. The method of claim 17, wherein the coated beads are between 60% and 75% of the mold compound by volume.

19. The method of any of claims 11-13 and 16, wherein the conductive cores of the coated beads include iron, copper, zinc or aluminum.

20. The method of any of claims 11-13, 16 and 19, wherein the insulator material includes a polymer.

21. A system comprising:

a packaged device including:

a substrate including a first side and a second side opposite the first side, wherein contacts are disposed on the first side;

an integrated circuit (IC) chip disposed on the second side, the IC chip coupled to the contacts via the substrate; and

a mold compound disposed at least partially around the IC chip, the mold compound comprising a suspension media and coated beads disposed in the suspension media, wherein the coated beads each include a conductive core and layer of an insulator material disposed around the conductive core; and

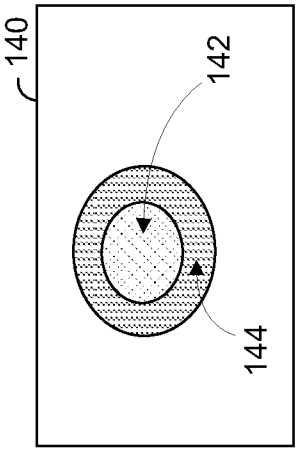
a display device coupled to the packaged device, the display device to display an image based on signals exchanged with the IC chip.

22. The system of claim 21, wherein the conductive cores of the coated beads includes a metal, and wherein the insulator material is softer than the metal.

23. The system of any of claims 21 and 22, wherein a dielectric constant of the insulator material is equal to or more than 3.0.

24. The system of any of claims 21-23, wherein the coated beads are 35% or more of the mold compound by volume.

25. The system of any of claims 21-24, wherein the insulator material includes a polymer.


140
142
144

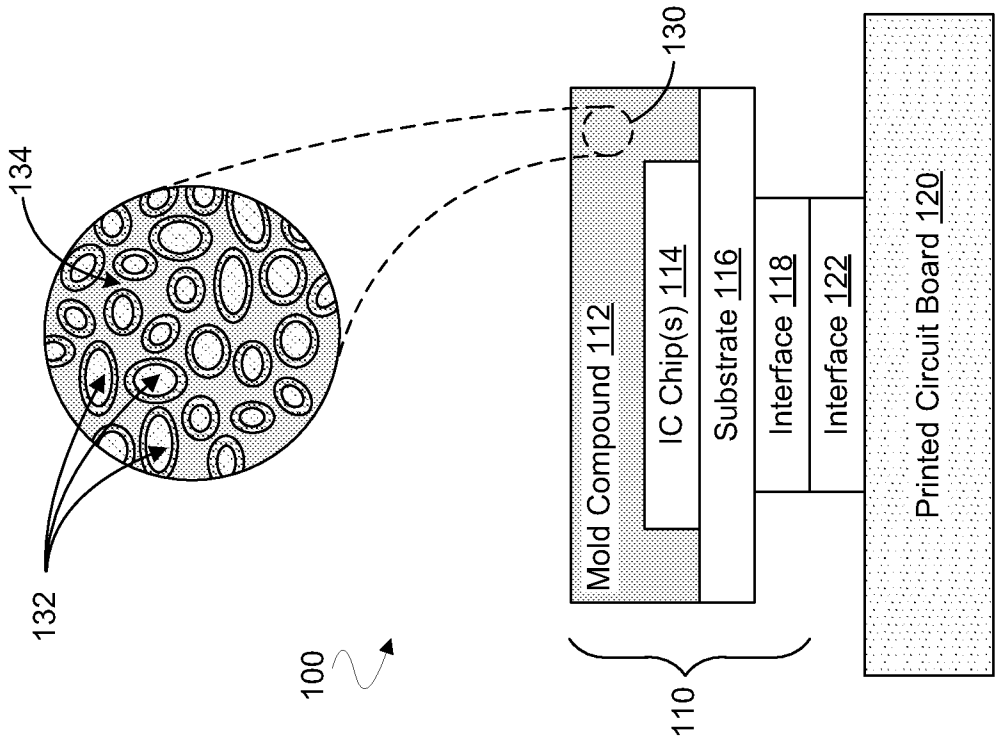

134
132
100
130
Mold Compound 112
IC Chip(s) 114
Substrate 116
Interface 118
Interface 122
Printed Circuit Board 120
110

FIG. 1

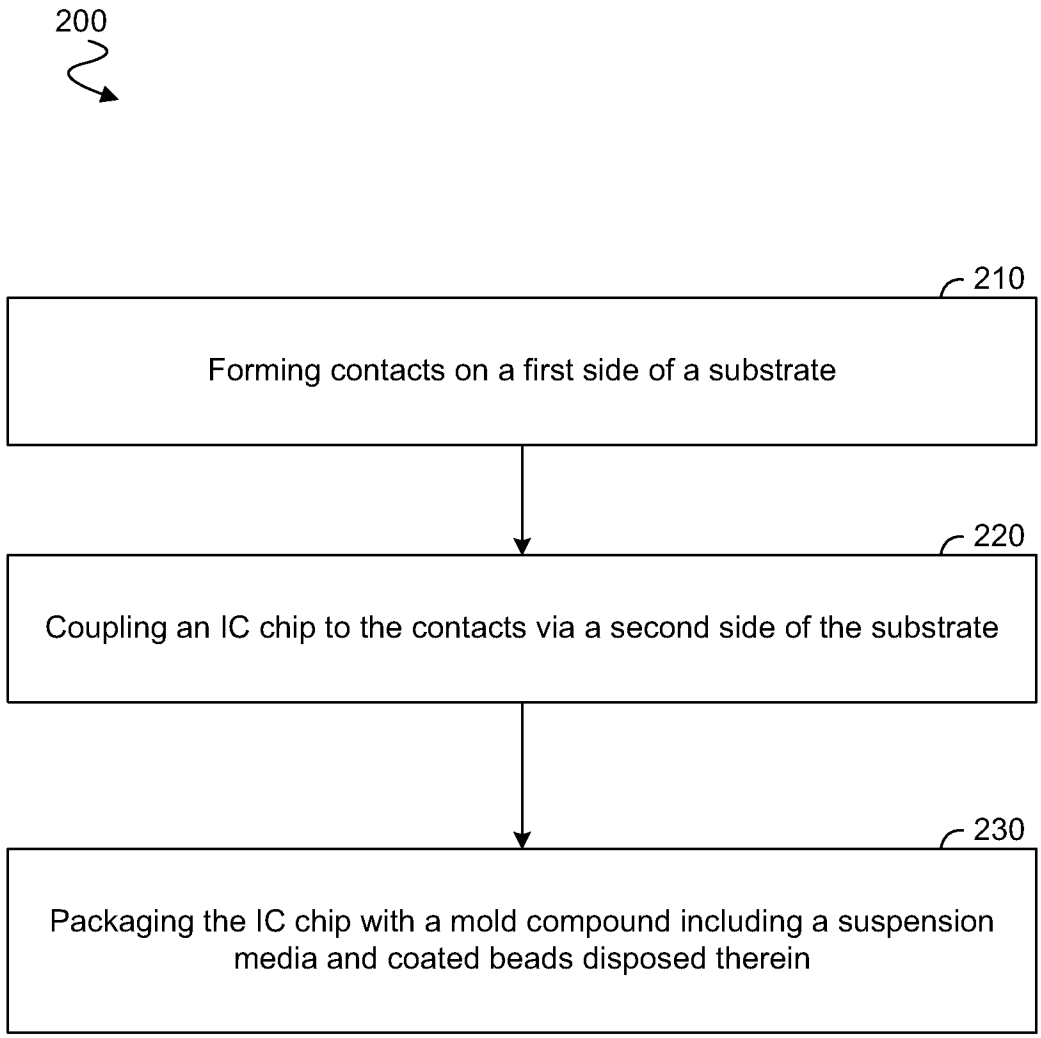

200
210
Forming contacts on a first side of a substrate
220
Coupling an IC chip to the contacts via a second side of the substrate
230
Packaging the IC chip with a mold compound including a suspension media and coated beads disposed therein

FIG. 2

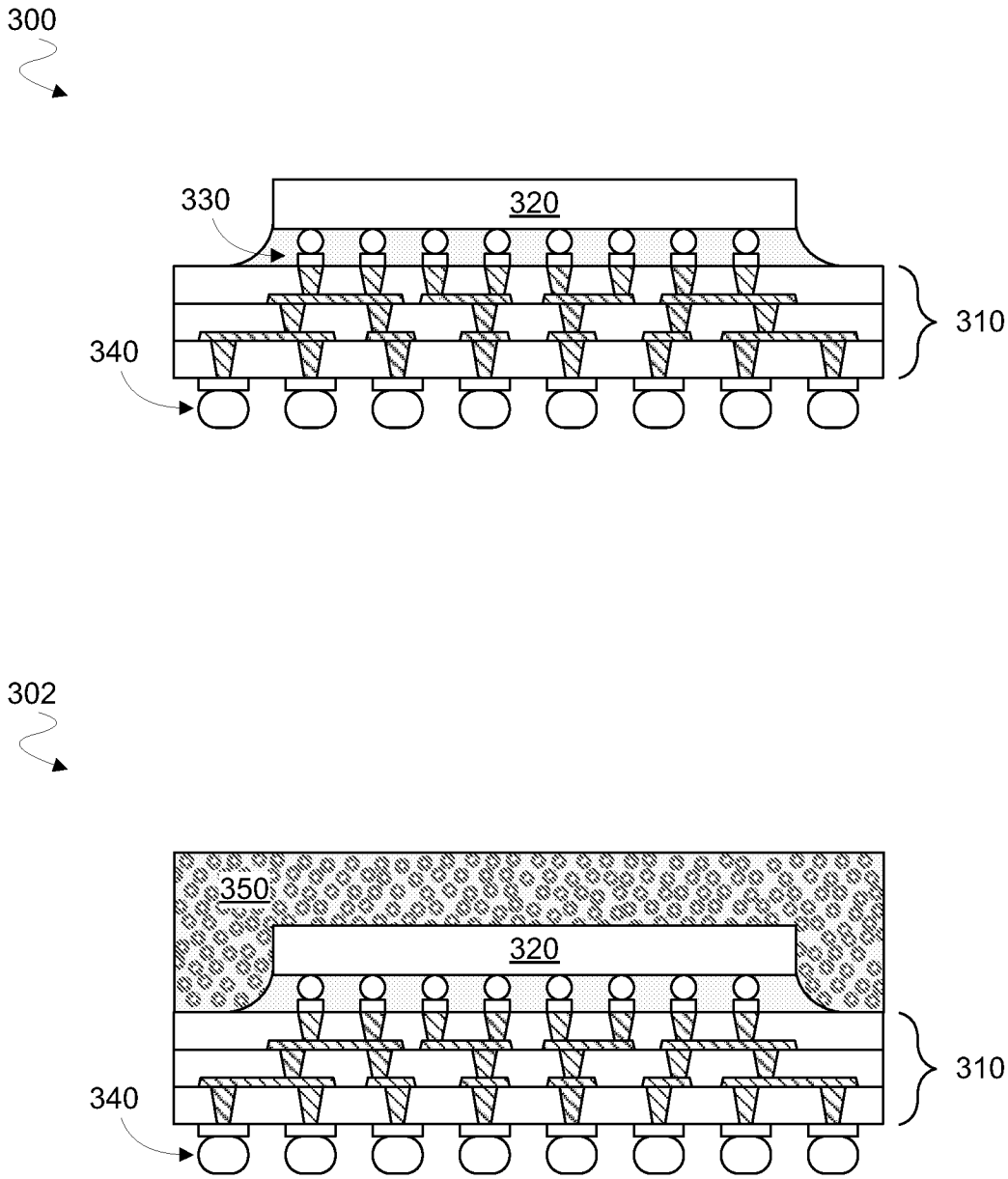


FIG. 3

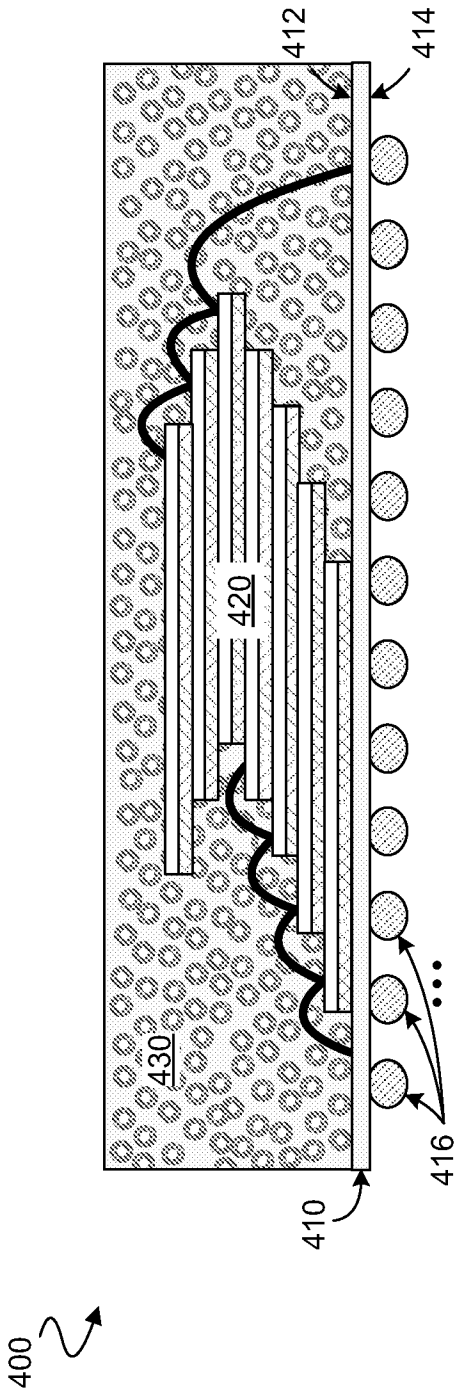

400
410
412
414
416
420
430

FIG. 4A

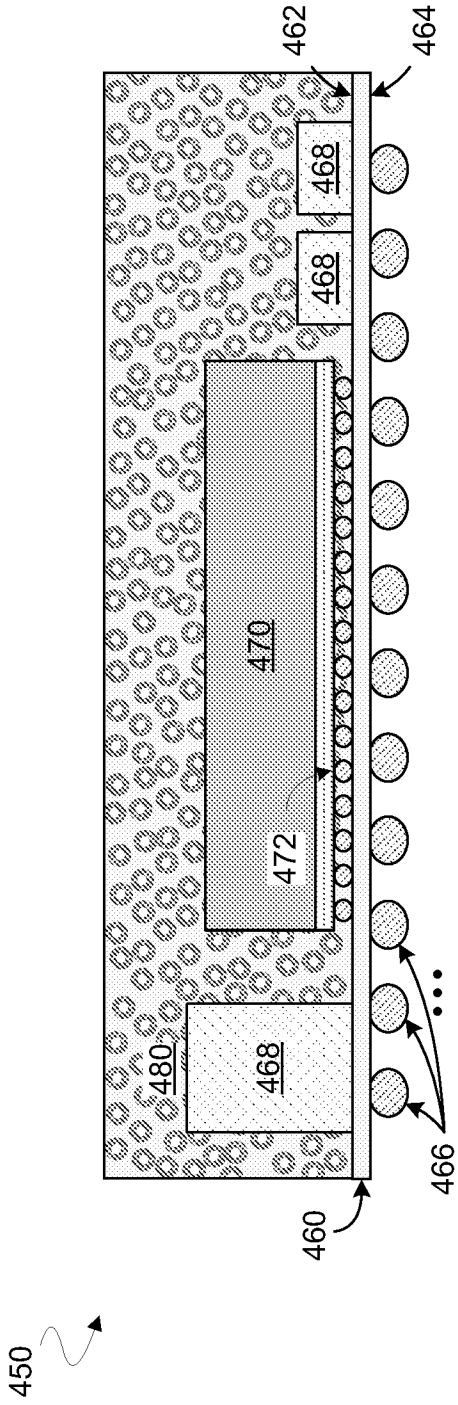

450
460
462
464
466
468
468
468
470
472
480

FIG. 4B

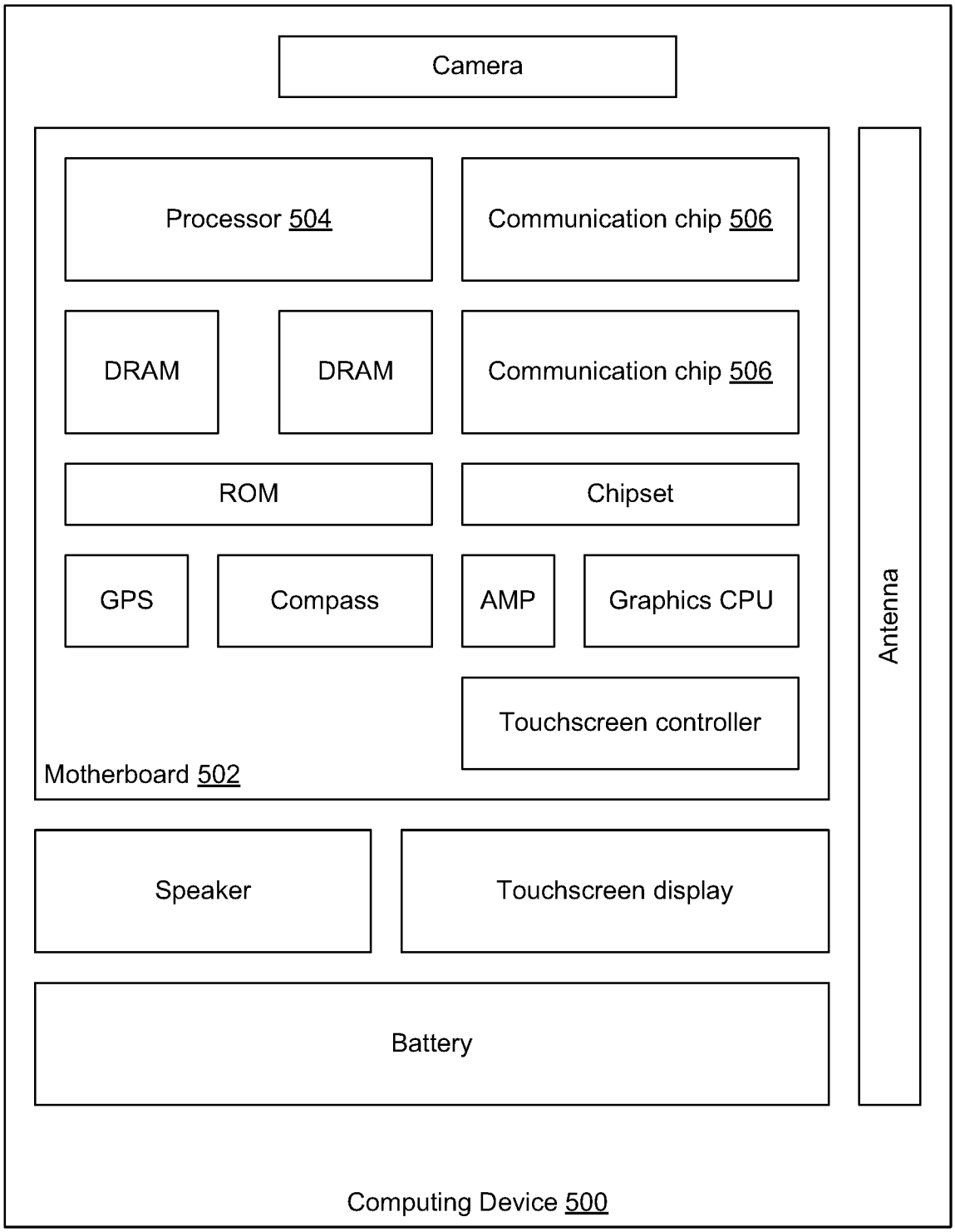

Camera
Processor 504
Communication chip 506
DRAM
DRAM
Communication chip 506
ROM
Chipset
GPS
Compass
AMP
Graphics CPU
Touchscreen controller
Motherboard 502
Antenna
Speaker
Touchscreen display
Battery
Computing Device 500

FIG. 5

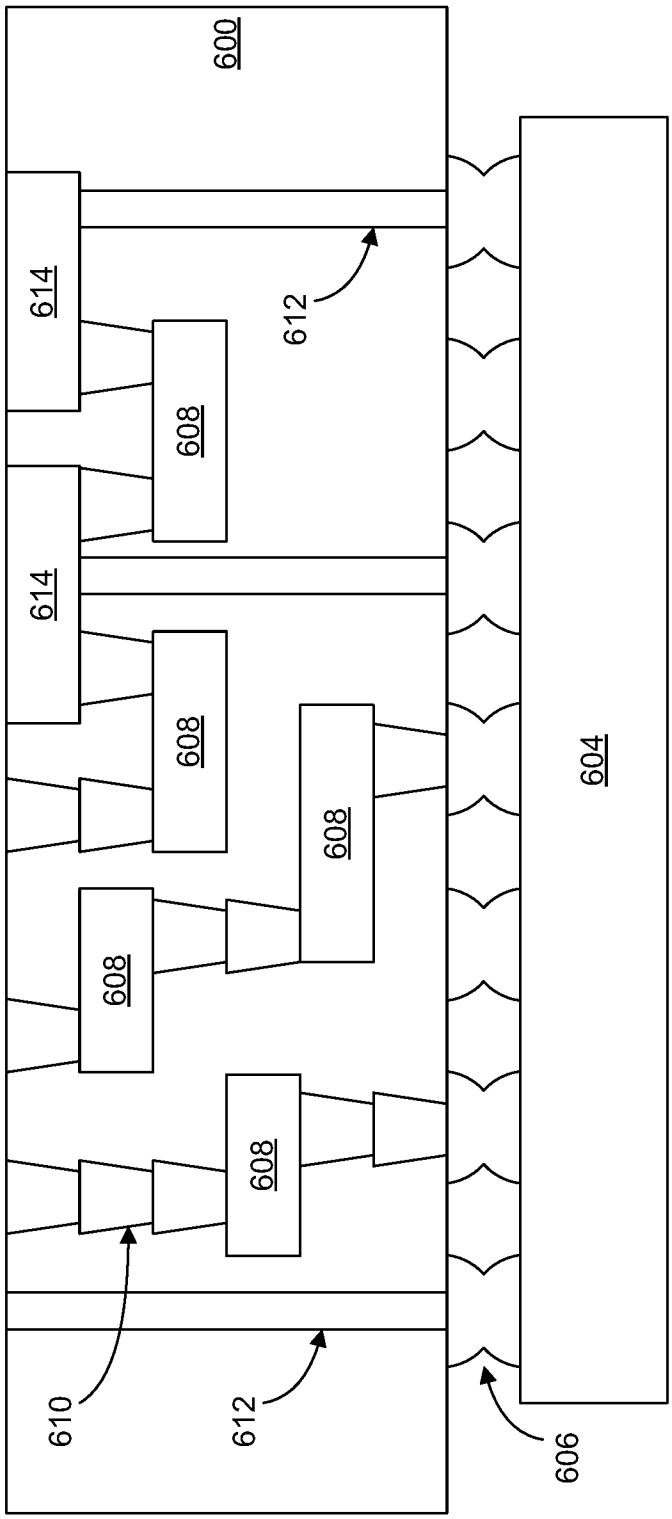


FIG. 6

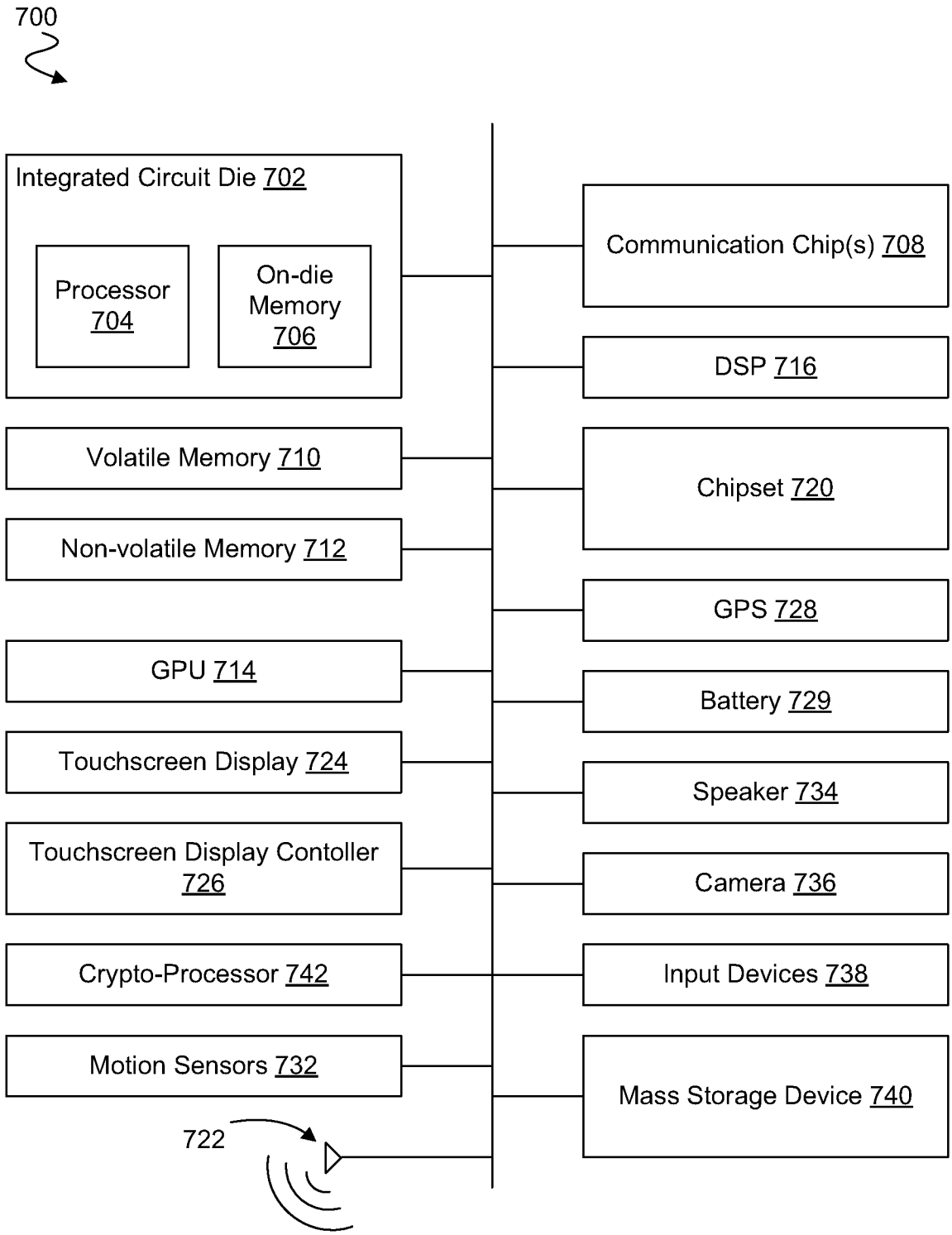

700
Integrated Circuit Die 702
Processor 704
On-die Memory 706
Volatile Memory 710
Non-volatile Memory 712
GPU 714
Touchscreen Display 724
Touchscreen Display Contoller 726
Crypto-Processor 742
Motion Sensors 732
722
Communication Chip(s) 708
DSP 716
Chipset 720
GPS 728
Battery 729
Speaker 734
Camera 736
Input Devices 738
Mass Storage Device 740

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/078304

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/552(2006.01)i; H01L 23/28(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, CNPAT, WPI, EPODOC: substrate?, chip?, die?, package+, seal+, +capsulat+, mold+, compound, composite, suspen+, dispers+, matrix, media, coat+, bead?, particle?, powder?, core?, shell?, insulator, polymer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2015243881 A1 (SANKMAN, R. ET AL.) 27 August 2015 (2015-08-27) description, paragraphs 21-24,43-47,49,54 and figures 1,10	1-25
Y	US 2002039667 A1 (TDK CORP.) 04 April 2002 (2002-04-04) description, paragraphs 191-203 and figures 1A-1C	1-25
Y	US 2013082368 A1 (SAMSUNG ELECTRONICS CO., LTD.) 04 April 2013 (2013-04-04) description, paragraphs 30-43 and figure 1	2-10, 12-20, 22-25
A	CN 1665025 A (STACK DEVICES CORP.) 07 September 2005 (2005-09-07) the whole document	1-25
A	CN 102623482 A (FREESCALE SEMICONDUCTOR INC.) 01 August 2012 (2012-08-01) the whole document	1-25

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 December 2016	**29 December 2016**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**LAI,Fengping**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)82246717**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/078304

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2015243881	A1	27 August 2015	JP	2016532309	A	13 October 2016
				CN	105556659	A	04 May 2016
				WO	2015057209	A1	23 April 2015
				KR	20160044514	A	25 April 2016
				EP	3058588	A1	24 August 2016
US	2002039667	A1	04 April 2002	US	7060350	B2	13 June 2006
				EP	1150311	A2	31 October 2001
				JP	2001303102	A	31 October 2001
				JP	2001313208	A	09 November 2001
				JP	2001338813	A	07 December 2001
				KR	20010104611	A	26 November 2001
				KR	100533097	B	02 December 2005
				JP	2003297634	A	17 October 2003
				JP	2004006909	A	08 January 2004
US	2013082368	A1	04 April 2013	KR	20130035620	A	09 April 2013
				CN	103035620	A	10 April 2013
				JP	2013080926	A	02 May 2013
CN	1665025	A	07 September 2005	None			
CN	102623482	A	01 August 2012	US	2012193737	A1	02 August 2012