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GB 2579007 B

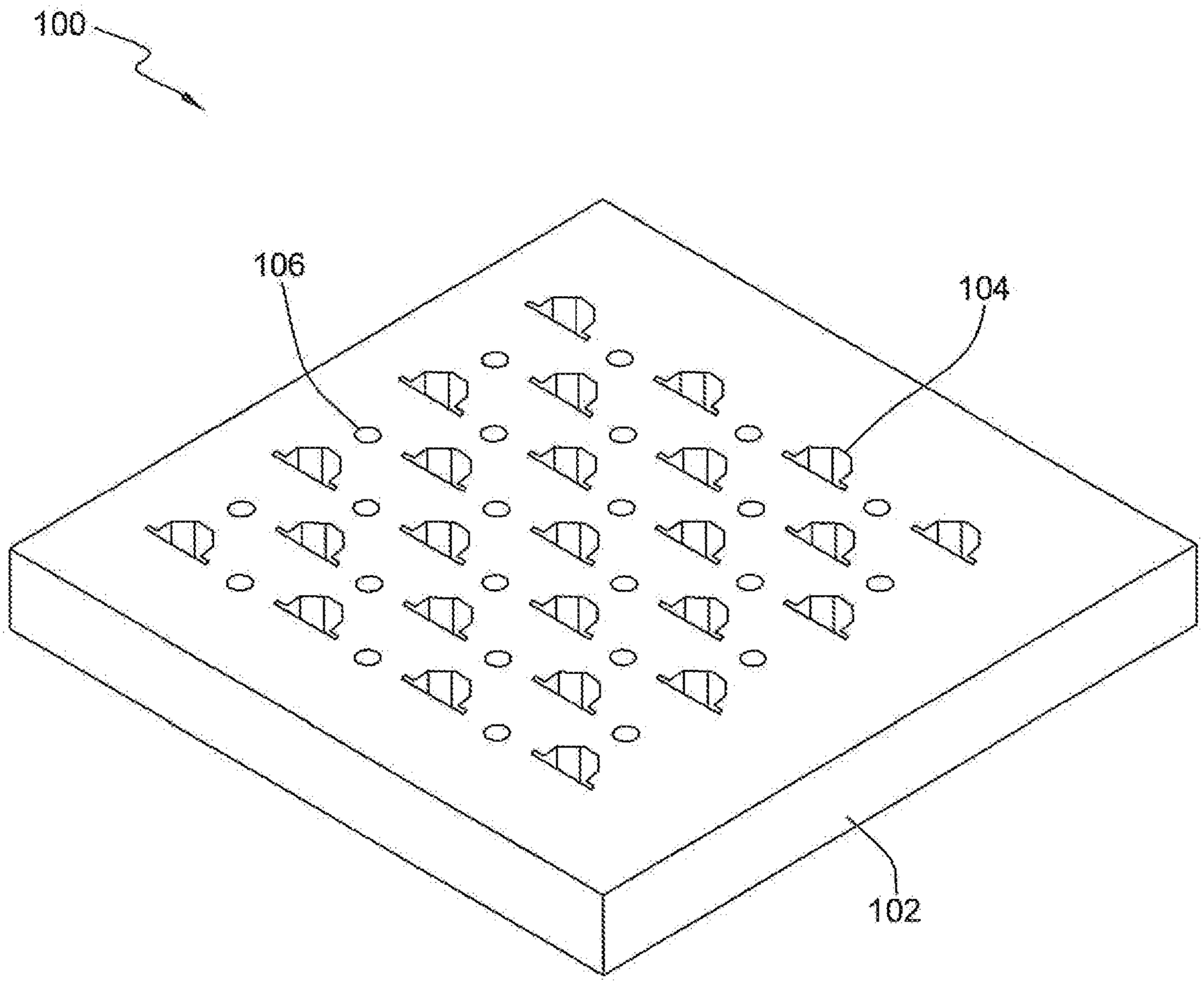


FIG. 1

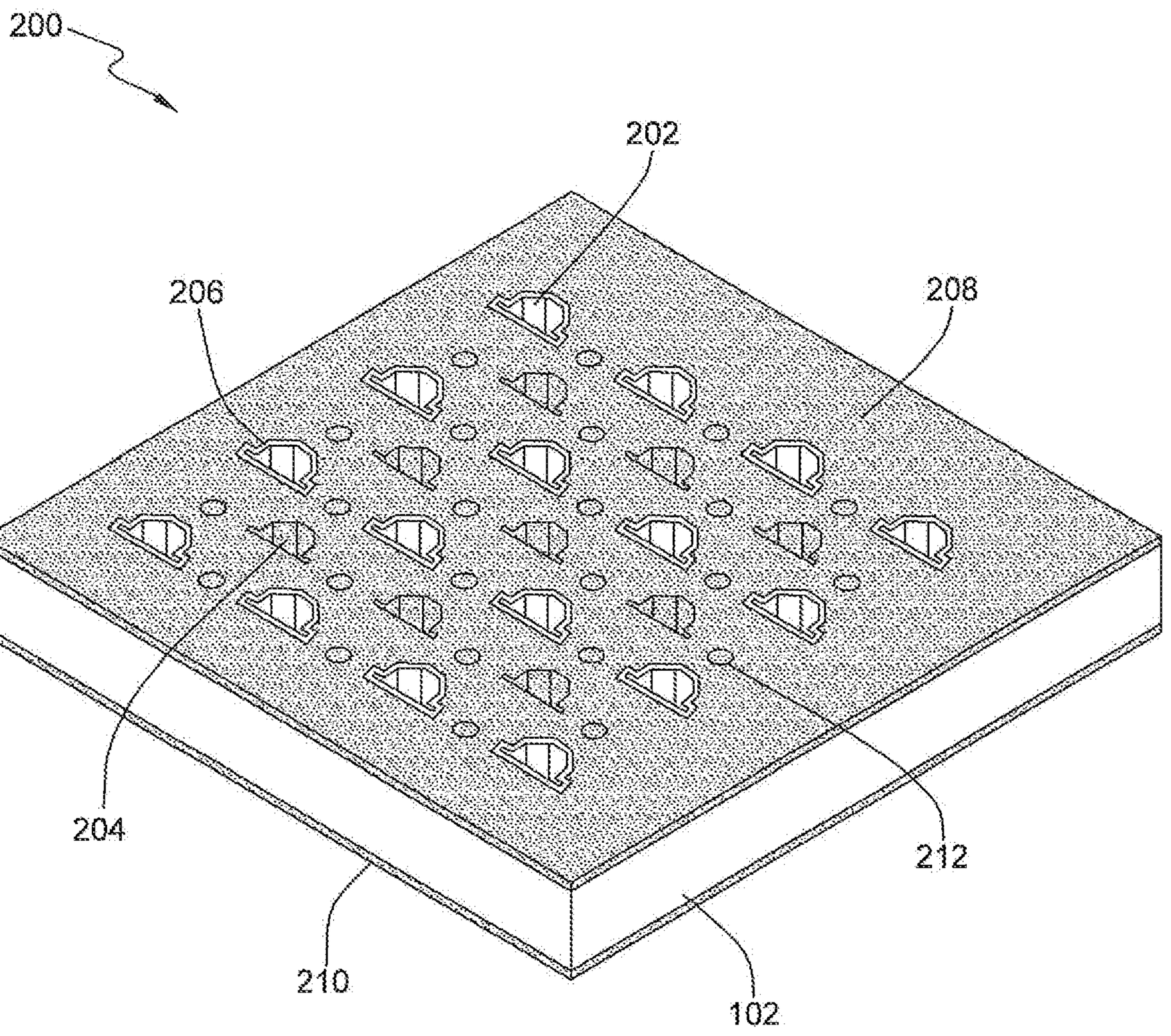


FIG. 2

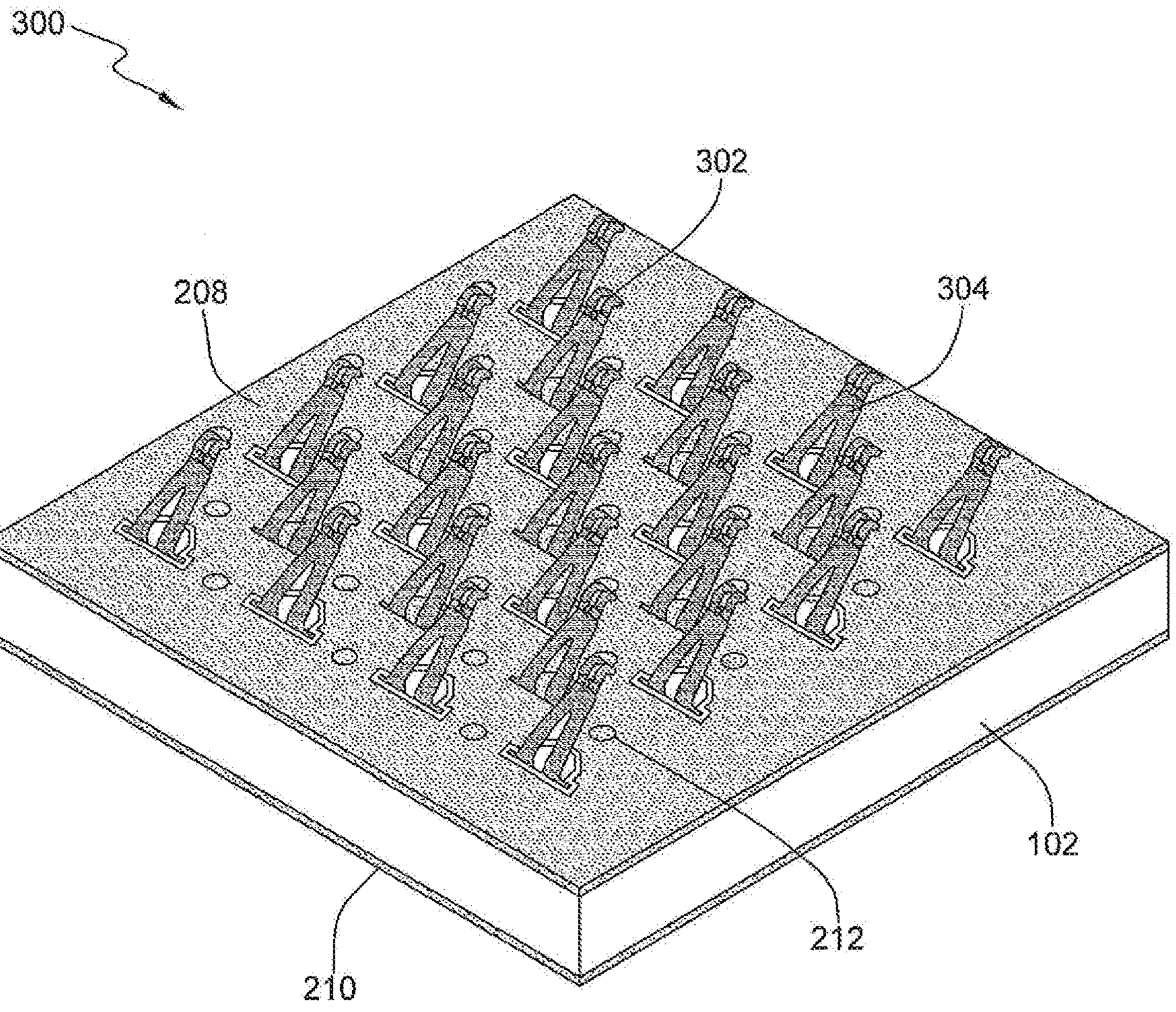


FIG. 3

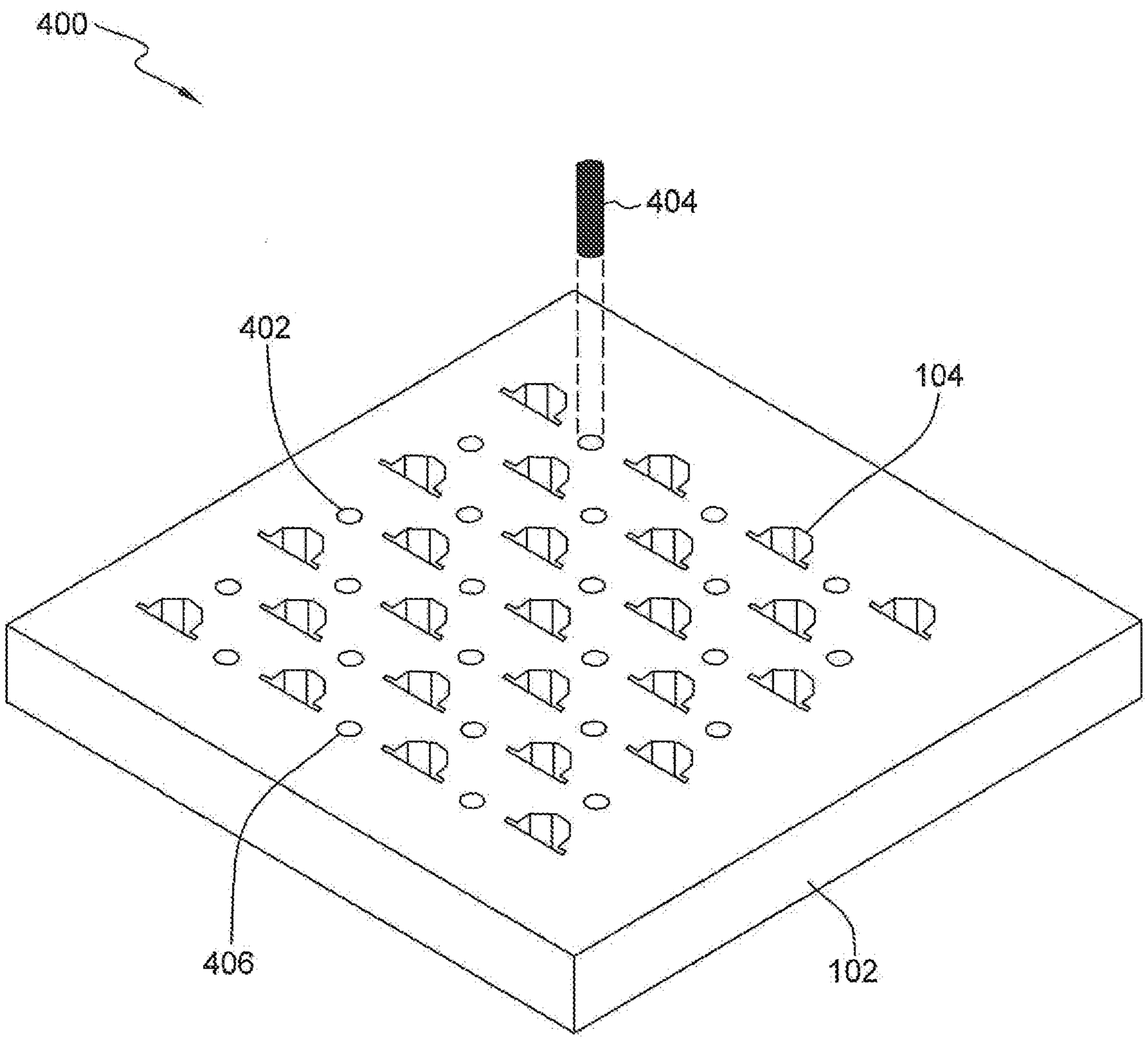


FIG. 4

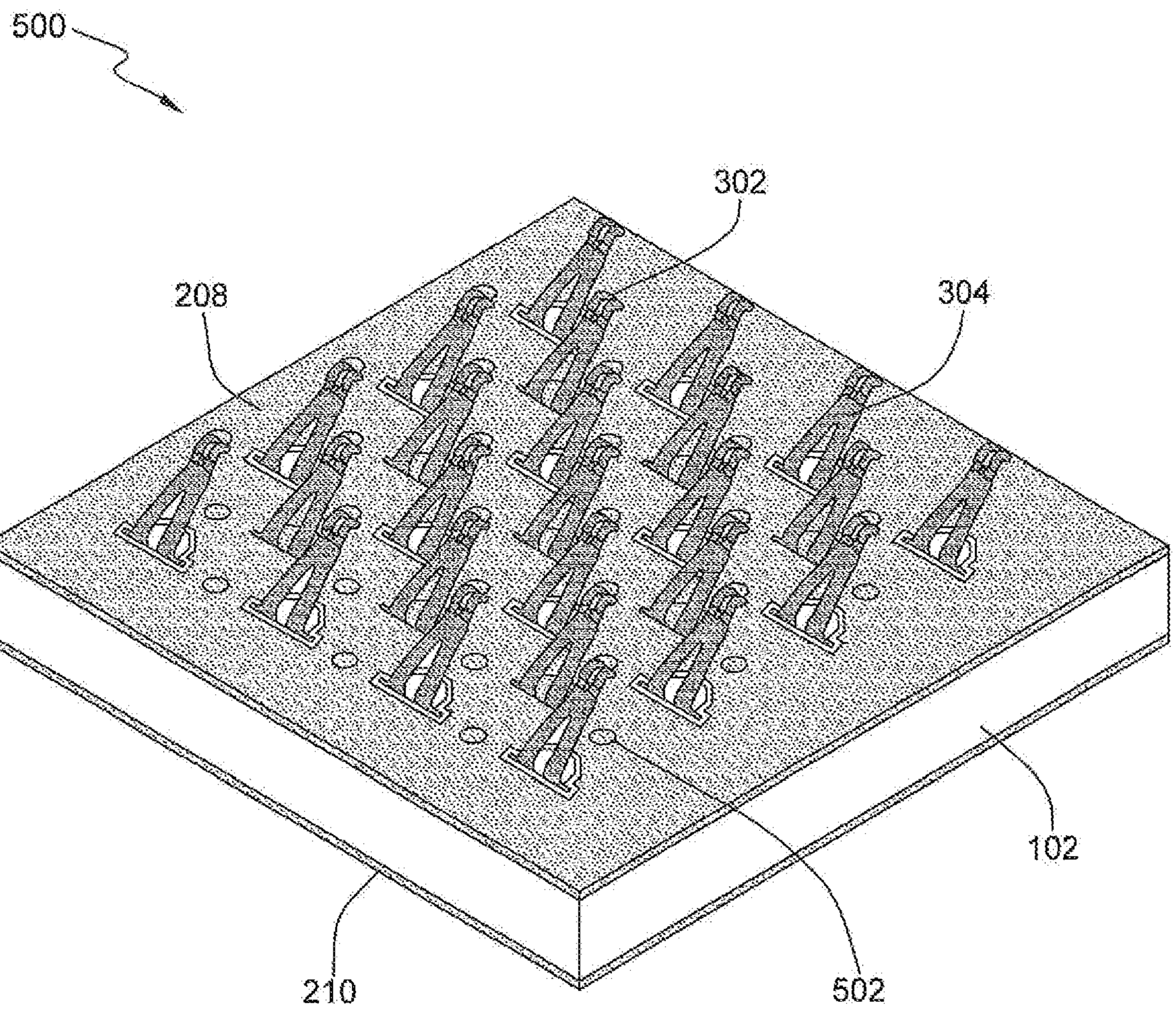


FIG. 5

# HYBRID LAND GRID ARRAY CONNECTOR FOR IMPROVED SIGNAL INTEGRITY

## BACKGROUND

**[0001]** The present invention relates generally to the field of connectors, and more particularly to hybrid land grid array connectors for improved signal integrity properties.

**[0002]** A hybrid land grid array (HLGA) connector provides an interconnect between a chip carrier package (e.g., a central processing unit or CPU package) and a printed circuit board (PCB). The HLGA, which is soldered to the PCB by way of ball grid array (BGA) balls, includes spring contacts that mate to the chip carrier pads, which are plated with nickel and gold, and which provide an electrical connection between the chip carrier package and the PCB. The chip carrier package is placed into the HLGA and is held in place by a spring-loaded mechanism. Should the chip carrier package fail to function properly, the HLGA allows for a simple field replacement of the non-functioning chip carrier package without needing to replace the entire PCB.

## SUMMARY OF THE INVENTION

**[0003]** The invention provides a method for fabricating a hybrid land grid array connector, as claimed in claim 1.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** Figure 1 depicts an example hybrid land grid array (HLGA) connector body populated with holes for plated vias and holes for spring contacts, in accordance with an embodiment of the present invention;

**[0005]** Figure 2 depicts the HLGA connector body of Figure 1 after plating and etching fabrication steps, in accordance with an embodiment of the present invention;

**[0006]** Figure 3 depicts the HLGA connector body of Figure 2 after the installation of the signal spring contacts and ground spring contacts, in accordance with an embodiment of the present invention;

**[0007]** Figure 4 depicts an example HLGA connector body populated with holes for conductive posts and holes for spring contacts, in accordance with an embodiment of the present invention; and Figure 5 depicts the HLGA connector body of Figure 4 after the installation of the plating, conductive posts, the signal spring contacts, and the ground spring contacts, in accordance with an embodiment of the present invention.

## DETAILED DESCRIPTION

**[0008]** The present invention provides for a hybrid land grid array (HLGA) connector for improved signal integrity. In use, an HLGA connector is soldered to pads on a printed circuit board (PCB). The connection is made

between ball grid array (BGA) balls on the HLGA and copper pads on the PCB. A chip carrier package (e.g., a central processing unit or CPU) is seated into the HLGA, firmly held in place by a spring-loaded clamping assembly. The HLGA connector includes metal spring contacts, mounted in a plastic body, which provide an electrical connection between the CPU and the PCB. For example, electrical signals travel from a first CPU, through a first HLGA, into the PCB, through a second HLGA, and to a second CPU. The electrical signals can get attenuated, gather noise and crosstalk, and encounter impedance mismatches. Current HLGA connectors can have data transfer rates of up to 25 Gbps (gigabits/second). Achieving higher data rates with existing HLGA connectors is challenging due to high impedance mismatch and crosstalk concerns.

**[0009]** The present invention recognizes that there is an approach for designing an HLGA for better signaling integrity capable of achieving data transfer rates in excess of 25 Gbps. Plated vias or conductive posts are placed at half-pitch (interstitially) between the holes in the body of the plastic (i.e., dielectric material) connector body that accept the spring contacts. The plated vias/conductive posts are electrically connected to the ground contact springs. The network of grounded plated vias/conductive posts create capacitance in the HLGA connector which decreases the overall inductive mismatch in the connector. Additionally, a shorter and denser return path creates the correct environment to decrease electrical crosstalk noise and push any connector crosstalk resonances higher in frequency.



**[0010]** For purposes of the description hereinafter, the terms “upper”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom”, and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing Figures. The terms “overlaying”, “atop”, “positioned on”, or “positioned atop” mean that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements, such as an interface structure may be present between the first element and the second element. The term “direct contact” means that a first element, such as a first structure, and a second element, such as a second structure, are connected without any intermediary conducting, insulating or semiconductor layers at the interface of the two elements.

**[0011]** As referred to herein, certain elements referred to as singular can also be considered to be plural. In the following examples, the term “X” refers to both a single “X” and two or more of “X”: “hole”, “signal contact clearance area”, “plated conductive via”, “ground spring contact”, signal spring contact”, “conductive post”, “inserted conductive post”, and “plated conductive post”.

**[0012]** The present invention will now be described in detail with reference to the Figures.

**[0013]** Figure 1 is an example HLGA connector body, generally designated 100.

**[0014]** HLGA connector 100 includes connector body 102, holes for spring contacts 104, and holes for plated vias 106. In example embodiments, HLGA connector 100 may include other attributes (not shown in Figure 1) such

as identification markings, electrical circuitry, electrical components, etc. In an embodiment, HLGA connector 100 can be four-sided (e.g., a square or a rectangle) but is not limited to a particular shape and is only constrained from a shape and size perspective by the CPU/PCB combination.

**[0015]** Connector body 102 is preferably composed of a solid dielectric material. Example dielectric materials include, but are not limited to, plastic, ceramic, glass, mica, and various metal oxides. Dielectric materials are electrically insulating, and therefore, poor conductors of electrical current. Dielectric materials also efficiently support electrostatic fields. In an embodiment, a dielectric material is used for connector body 102 so that good signal integrity is maintained for electrical signals guided by electrical contacts, such as metal spring contacts (e.g., see Figure 3, ground spring contact 302 and signal spring contact 304), included in connector body 102.

**[0016]** Holes for spring contacts 104 are holes in connector body 102 which begin at the top surface of connector body 102 and end at the bottom surface of connector body 102 going completely through connector body 102. The bottom surface of connector body 102 is opposite the top surface of connector body 102. Holes for spring contacts 104 can be used to allow placement of metal spring contacts into connector body 102. In an embodiment, holes for spring contacts 104 are positioned in a repetitive grid pattern within connector body 102. Holes for spring contacts 104 are shaped in a manner which securely holds the spring contacts in connector body 102 so that the spring contacts do not become loose as HLGA connector 100 is used. Holes for spring contacts 104 remain empty after the placement of the metal spring contacts. Alternatively, holes for spring contacts 104 used for ground spring contact 302 are filled with a dielectric material, prior to any plating of a conductive material (discussed below), after the placement of all of the ground spring contacts 302. The additional dielectric material in the holes for spring contacts 104 provides for improved electrical performance of the HLGA connector.



**[0017]** Holes for plated vias 106 are holes in connector body 102 which begin at the top surface of connector body 102 and end at the bottom surface of connector body 102 going completely through connector body 102. Holes for plated vias 106 can be plated with a conductive material providing an electrical connection between a conductive plating on the top surface of connector body 102 and a conductive plating on the bottom surface of connector body 102. Holes for plated vias 106 are positioned at the mid-points (i.e., at half-pitch) between the holes for spring contacts 104 in connector body 102. Holes for plated vias 106 are substantially smaller in size relative to holes for spring contacts 104.

**[0018]** Figure 2 depicts the HLGA connector of Figure 1 after plating and etching fabrication steps, and is generally designated 200.

**[0019]** HLGA connector 200 includes the previously discussed feature connector body 102, and new features holes for signal contacts 202, holes for ground contacts 204, signal contact clearance area 206, top conductive layer 208, bottom conductive layer 210, and plated conductive via 212.

**[0020]** Holes for signal contacts 202 and holes for ground contacts 204 are holes for spring contacts 104 which have been identified as either a signal connection or a ground connection between the chip carrier package (e.g., central processing unit or CPU) and the printed circuit board (PCB). The other features of holes for spring contacts 104 that have been previously discussed apply to holes for signal contacts 202 and holes for ground contacts 204. Hole for ground contact 204 is ultimately plated with a conductive metal such as copper and when the spring contact is placed into hole for ground contact 204, electrical contact between the spring contact and the surface plated metal is required. Hole for ground contact 204 is not filled with any other material other than air. With a dielectric material filling hole for ground contact 204 after placement of the spring contacts, a surface plating over the dielectric material in hole for ground contact 204 (e.g., plating with a conductive metal such as copper) provides an electrical connection between the ground spring contacts (such as ground spring contact 302 in Figure 3), top conductive layer 208 (discussed below), and bottom conductive later 210 (discussed below) by virtue of being in physical contact with the ground spring contacts, top conductive layer 208, and bottom conductive later 210.

**[0021]** Top conductive layer 208 and bottom conductive layer 210 are the top surface and bottom surface, respectively, of connector body 102 following application of a conductive layer. The conductive layer applied to top conductive layer 208 and to bottom conductive layer 210 is copper applied with a plating process. The applied conductive layer applied to the top surface of connector body 102 is in direct contact with the top surface of connector body 102. The applied conductive layer applied to the bottom surface of connector body 102 is in direct contact with the bottom surface of connector body 102. Alternatively, the conductive layer applied to top conductive layer 208 and to bottom conductive layer 210 is any sufficiently conductive material known in the art applied by any process known in the art. Following the application of the conductive layer, top conductive layer 208 is completely covered with the conductive material and is electrically common. Also, following the application of the conductive layer, bottom conductive layer 210 is also completely covered with the conductive material and is also electrically common. The wall surfaces for hole for signal contact 202, the wall surfaces for hole for ground contact 204, and the wall surfaces for plated conductive via 212 are plated and electrically common with top conductive layer 208 and bottom conductive layer 210, until signal contact clearance area 206 (discussed below) is created.

**[0022]** Signal contact clearance area 206 is an area around holes for signal contact 202 that has the conductive layer removed. A portion of top conductive layer 208 is removed from the top surface of connector body 102 around each of the holes for signal contacts 202. A portion of bottom layer 210 is also removed from the bottom surface of connector body 102 around each of the holes for signal contacts 202. Also, the plating on the wall surfaces of hole for signal contact 202 is removed. A subtractive photolithography process is used to remove the portion of top conductive layer 208 and the portion of bottom conductive layer 210. For example, with respect to top conductive layer 208, a photoresist is applied over top conductive layer 208. An expose pattern is developed in the photoresist defining each signal contact clearance area 206. Connector body 102 is baked to stabilize the remaining photoresist. An etch process is then used to remove the portion of top conductive layer 208 around each of the holes for signal contact 202 resulting in the formation of the signal contact clearance area 206. A photoresist

strip process removes the balance of the photoresist from top conductive layer 208. Connector body 102 is then processed through a cleaning process to remove any residual process materials. The same process is used to define each of the signal contact clearance area 206 in bottom conductive layer 210. The results of the above photolithography processes are removing the plating from the wall surfaces of hole for signal contact 202, the creation of signal contact clearance area 206 (for electrically isolating signal spring contact 304 in Figure 3), and leaving the plating on the wall surfaces of hole for ground contact 204 intact. Any process known in the art can be used to define each of the signal contact clearance area 206 in both the top conductive layer 208 and the bottom conductive layer 210.

**[0023]** Plated conductive via 212 is a hole for a plated via 106 that has been plated with a conductive material. The conductive material applied to plated conductive via 212 is copper applied using an electrolytic plating process. Alternatively, the conductive material applied to plated conductive via 212 is any sufficiently conductive material known in the art applied by any process known in the art. In an embodiment, following the application of the conductive material to holes for plated vias 106, plated conductive via 212 is electrically connected to both top conductive layer 208 and bottom conductive layer 210.

**[0024]** Figure 3 depicts the HLGA connector of Figure 2 after the installation of metal spring contacts, and is generally designated 300.

**[0025]** HLGA connector 300 includes the previously discussed features connector body 102, top conductive layer 208, bottom conductive layer 210, and plated conductive via 212, and new features ground spring contact 302 and signal spring contact 304.

**[0026]** Ground spring contact 302 is a pre-formed, metal spring contact that is inserted (i.e., stitched) into holes for ground contacts 204 in connector body 102. Ground spring contact 302 will contact both the ground land grid array (LGA) pads on the CPU and solder to the ground pads on the PCB providing an interconnection between the CPU and the PCB. Ground spring contact 302 is pre-formed from copper. Alternatively, ground spring contact 302 is pre-formed from any other sufficiently conductive metal known in the art. Ground spring contact 302 is stitched into holes for spring contacts 204 and is mechanically held in place. Ground spring contact 302 has an electrical connection to top conductive layer 208, bottom conductive layer 210, and plated conductive via 212 due to ground spring contact 302 physically in contact with top conductive layer 208, bottom conductive layer 210, and the conductive plating inside hole for ground contact 204.

**[0027]** Signal spring contact 304 is a pre-formed, metal spring contact that is inserted (i.e., stitched) into holes for signal contacts 202 in connector body 102. Signal spring contact 304 will contact both signal land grid array (LGA) pads on the CPU and solder to the signal pads on the PCB providing an interconnection between the CPU and the PCB. Signal spring contact 304 is pre-formed from copper. Alternatively, signal spring contact 304 is pre-formed from any other conductive metal known in the art. In an embodiment, signal spring contact 304 is stitched

into holes for signal contacts 202 and is mechanically held in place. Signal spring contact 304 is not electrically connected any of top conductive layer 208, bottom conductive layer 210, and plated conductive via 212.

**[0028]** Figure 4 is an example HLGA connector body, generally designated 400.

**[0029]** HLGA connector 400 includes the previously discussed features connector body 102 and holes for spring contacts 104, and new features holes for conductive posts 402 and conductive post 404.

**[0030]** Holes for conductive posts 402 are substantially similar to holes for plated vias 106. Holes for conductive posts 402 are holes in connector body 102 which begin at the top surface of connector body 102 and end at the bottom surface of connector body 102 going completely through connector body 102. Holes for conductive posts 402 are positioned at the mid-points between the holes for spring contacts 104 in connector body 102. Holes for conductive posts 402 are substantially smaller in size than holes for spring contacts 104.

**[0031]** Conductive post 404 is a solid post (e.g., a pin) that is stitched into holes for conductive posts 402 and is mechanically held in place. According to an embodiment, conductive post 404 is made from copper. Alternatively, conductive post 404 is made from any conductive metal known in the art.

**[0032]** Inserted conductive post 406 is conductive post 404 inserted into connector body 102. The top and bottom of inserted conductive post 406 are on the same plane as the top surface and bottom surface of connector body 102, respectively. Alternatively, the top and bottom of inserted conductive post 406 extend beyond the plane of the top surface and the plane of the bottom surface of connector body 102, respectively, to a maximum height above each plane.

**[0033]** Figure 5 is the HLGA connector of Figure 4 after plating and etching fabrication steps, and is generally designated 500.

**[0034]** HLGA connector 500 includes the previously discussed features connector body 102, top conductive layer 208, bottom conductive layer 210, ground spring contact 302, and signal spring contact 304, and new feature plated conductive post 502.

**[0035]** Plated conductive post 502 is inserted conductive post 406 that has been through the previously described photolithography process resulting in top conductive layer 208, bottom conductive layer 210, signal contact clearance area 206 (not shown in Figure 5), plating on the top of inserted conductive post 406, plating on the bottom of inserted conductive post 406, and an electrical connection of the plating to ground spring contact 302. The plating on the top and the bottom of plated conductive post 502 is copper plating. The plating on the top and the bottom of plated conductive post 502 is any conductive plating known in the art.

## CLAIMS

1. A method, the method comprising:

providing a body for a hybrid land grid array connector, wherein the body includes a first plurality of holes and a second plurality of holes;

depositing a conductive layer on a top surface of the body, a bottom surface of the body, and wall surfaces of the first plurality of holes, wherein the top surface of the body is electrically common with the bottom surface of the body;

removing the conductive layer from wall surfaces of a first subset of the first plurality of holes; and

removing a portion of the conductive layer on the top surface of the body and the bottom surface of the body from an area surrounding the first subset of the first plurality of holes.

2. The method of claim 1, further comprising:

inserting a plurality of spring contacts into the first plurality of holes, wherein:

the plurality of spring contacts inserted into the first subset of the first plurality of holes are electrically isolated from one another; and

the plurality of spring contacts inserted into a second subset of the first plurality of holes are electrically common with, at least, one another, the conductive layer on the top surface of the body, and the conductive layer on the bottom surface of the body.

3. The method of claim 1, wherein a subtractive photolithography process is used to remove the conductive layer from the wall surfaces of the first subset of the first plurality of holes and the area surrounding the first subset of the first plurality of holes.

4. The method of claim 1, further comprising:

depositing a material into a second subset of the first plurality of holes.

5. The method of claim 4, wherein the material is a dielectric material.

6. The method of claim 1, wherein the step of depositing a conductive layer on a top surface of the body, a bottom surface of the body, and wall surfaces of the first plurality of holes further comprises:

depositing the conductive layer on wall surfaces of the second plurality of holes.

7. The method of claim 1, further comprising:

inserting a conductive post into each of the second plurality of holes, wherein the conductive post provides an electrical connection between the conductive layer on the top surface of the body and the conductive layer on the bottom surface of the body.