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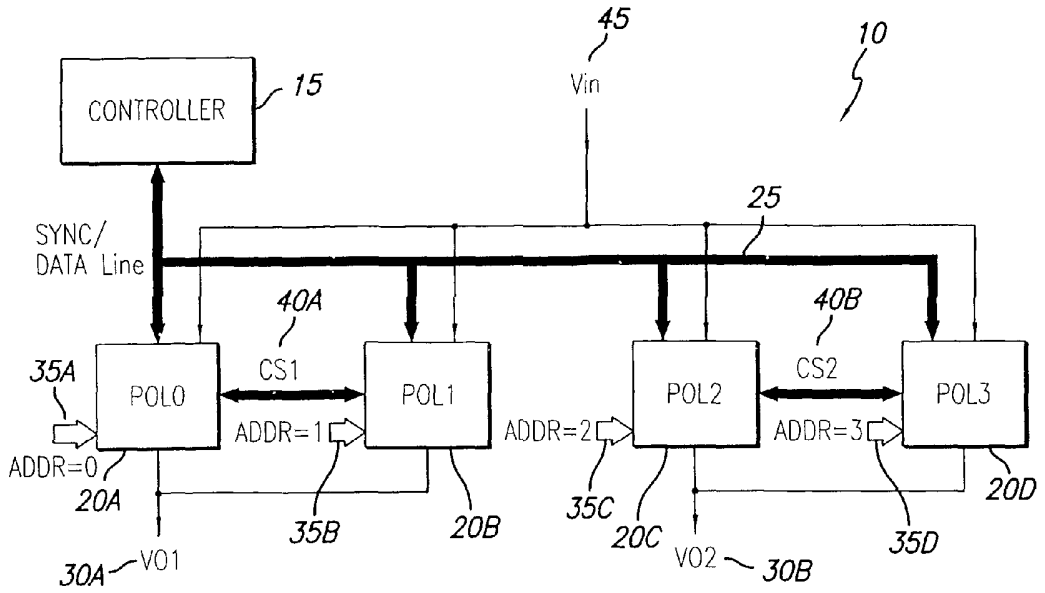
(54) **Title:** SYSTEM AND METHOD FOR INTERLEAVING POINT-OF-LOAD REGULATORS



(57) **Abstract:** A system and method for providing interleaving point-of-load (POL) regulators (20A-20D) such that each regulator's switching cycle is phase displaced with respect to those of other POL regulators in the array is disclosed. As a result, the aggregate input and/or output reflected ripple and noise of the input, output, or both is reduced. Each regulator in the array is associated with an unique address (ADDR). A serial data-line (25) writes the phase spacing programmed to each addressable POL regulator in the array. The present invention permits phase displacement of POL regulators without limitation to the input and output voltages of each of the regulators in the array. The array of POL regulators may also operate in a phase displaced mode with only a single control line. The need for separate controllers and multiple control lines is thereby eliminated.

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SYSTEM AND METHOD FOR INTERLEAVING POINT-OF-LOAD REGULATORS

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to power supply circuits and more particularly, to voltage regulator systems for use in power supply systems.

2. Background Of The Invention

Multi-phase regulators are commonly used in generating a single output voltage. For conventional multi-phase systems, a common control circuit drives several out-phased power circuits. The power stages typically consist of several chokes connected to a single section of output capacitors. The benefits of the conventional multi-phase design is the reduction of both input reflected ripple currents and output ripple current in the output capacitor resulting from the displaced phasing of the choke currents. In this type of arrangement, the output voltage is normally fed back into the master pulse width modulation (PWM) controller. In turn, the PWM controller compensates the loop and distributes a pulse width modulated signal out-phased to each of the several output power stages over multiple lines.

As discussed above, in comparison to single-phase systems, multi-phase regulators have a low output capacitor ripple and low input reflected ripple current. Unfortunately, conventional multi-phase regulators also have a number of disadvantages. Conventional multi-phase systems are limited to a single common input voltage and a single common output voltage. Because conventional multi-phase systems include a multi-phase PWM controller that controls multiple slave power stages, these systems also require multiple control lines running from the controller to the slave power stages. Moreover, the phase location is fixed and is not adjustable from the master controller.

In view of the foregoing, it is believed that a need exists for an improved multi-phase regulator system that overcomes the aforementioned obstacles and deficiencies of currently-available multi-phase regulator systems. More particularly, a need exists for a flexible multi-phase regulator system for use in power supply circuits.

SUMMARY OF THE INVENTION

The present invention is directed toward a multi-phase regulator system that is configured to provide multiple independent output voltages or currents and programmable phase offsets via a single control line.

The present system and method provides an array of point-of-load (POL) regulators in which the switching cycle of each regulator is displaced with respect to those of other regulators in the array to reduce the aggregate reflected ripple and noise of the input, output, or both. Each regulator in the array is provided with an address. A serial data-line may write the phase spacing to each addressable POL in the array. In an alternative exemplary embodiment, the phase spacing is determined based on the address. Accordingly, the system and method of the present invention provides phase displacement of the regulators without being limited by the input and output voltages of each of the regulators in the array. Moreover, the array may operate in a phase displaced mode with only a single control line and without the need for separate controllers or multiple control lines.

The present system and method further provides for the control of independent single phase regulators. Therefore, because the phase displacement is independent of the input voltage, the system and method may provide multiple independent input voltages within the array. In an alternative exemplary embodiment, the array is capable of being configured as a single output multi-phase system. The array does not require a master controller because the control system is distributed in all regulators. Thus, the above functionality is independent of the regulator topology. Moreover, the array may utilize a single control line, instead of multiple control lines.

The present invention removes the restriction of a common output voltage. In addition, the common input voltage does not restrict the operation of the array. The phasing determination is either made at a system controller or at each of the power stages. Furthermore, the control loops are closed locally at each power stage, rather than centrally. The present invention reduces the system noise generated by the array of POL regulators and thereby reduces the filter requirements to manage such noise by out-phasing the switching of the regulators. A further advantage is that the phase location of the start of each POL switching cycle is programmable and thereby provides flexibility and adjustability. For example, this flexibility in phase location of each regulator can be used to optimize the noise performance of the array. The addressable nature of the regulators provides an additional degree of flexibility for the array.

Other aspects and features of the present invention will become apparent from consideration of the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an exemplary block diagram of one embodiment of an array of point-of-load (POL) regulators in accordance with the present invention.

Figure 2 illustrates another exemplary embodiment of the POL regulator array.

Figure 3 is an exemplary embodiment of communication over a single-wire bus.

Figure 4 illustrates an exemplary embodiment of a data transmission scheme utilized by the POL regulators and controller.

Figure 5 illustrates an exemplary embodiment of a voltage regulator.

Figure 6 illustrates an exemplary embodiment of a clock recovery circuit.

Figure 7 illustrates an exemplary embodiment of a delay bus.

Figure 8 illustrates an exemplary embodiment of the timing diagram of the clock recovery circuit of Figure 6.

Figures 9-11 illustrate exemplary embodiments of the timing diagrams and input ripple of the POL regulator array.

It should be noted that the figures are not drawn to scale and that elements of similar structures or functions are generally represented by like reference numerals for illustrative purposes throughout the figures. It also should be noted that the figures are only intended to facilitate the description of the preferred embodiments of the present invention. The figures do not describe every aspect of the present invention and do not limit the scope of the invention.

DETAILED DESCRIPTION

The present invention is directed to a system and method for providing interleaving point-of-load (POL) regulators such that each regulator's switching cycle is phase displaced with respect to those of other regulators in the array. As a result, the aggregate reflected ripple and noise of the input, output or both is reduced. Each regulator in the array is associated with an address. A serial data-line may write the phase spacing programmed to each addressable POL regulator in the array. Alternatively, the phase spacing data may be provided from memory. Accordingly, the present invention permits phase displacement of the regulators without limiting the input and output voltages of each of the regulators in the array. The array of regulators may also operate in a phase displaced mode with only a single control line. The need for separate controllers and multiple control lines is thereby eliminated.

Figure 1 shows an exemplary embodiment of a point-of load (POL) regulator array system of the present invention, shown generally at 10. The system 10 includes an array of POL regulators or converters 20 and a controller 15. POL regulators 20 and controller 15 may be configured to form a board level distributed power architecture, for example. Although the exemplary embodiment depicted in Figure 1 shows a controller 15, the present invention does not require controller 15, as will be shown and described below with reference to Figure 2. Controller 15 and POL regulators 20 communicate via interface 25. Interface 25, shown as SYNC/DATA line 25, may be a one line, bi-directional interface.

Each POL regulator 20 is associated with a selected address. The address configuration for each POL regulator 20 specifies an ID for that POL regulator 20. A

selected POL regulator 20, shown as POL regulator 20A, may be designated as the Master POL regulator 20. This designation may be based on a selected address, e.g., the least significant address or Address 0. The Master POL regulator 20A generates the SYNC portion of the SYNC/DATA line signal 25. Controller 15 and all other POL regulators 20 synchronize to this SYNC signal. Any other device connected to the SYNC/DATA line 25 may provide the clock, e.g., POL regulator 20, controller 15 or an additional external clock generator (not shown).

The power conversion switching frequency of each POL regulator 20 is synchronized to a (integer or fractional) multiple of the SYNC/DATA line frequency. Therefore, the POL regulators 20 do not have to operate at the same frequency. As a result, this provides greater system flexibility and optimized efficiency because each POL regulator 20 may operate at its optimal frequency depending on its input voltage and output voltage setting instead of operating at the same frequency as every other POL regulator in the system.

Each POL regulator 20 may receive input voltage Vin 45. The output voltage Vo of each POL regulator 20 may be provided to devices connected to system 10 in any suitable manner. In the exemplary embodiment shown in Figure 1, for example, the output of two or more POL regulators 20 may be connected in parallel. In this embodiment, an additional current share line 40 may be used to ensure an equal load share between the POL regulators 20.

As discussed above, controller 15 and POL regulators 20 communicate via interface 25, e.g., a one line, bi-directional SYNC/DATA line. Controller 15 may transmit data through SYNC/DATA line 25 to each of the POL regulators 25. Controller 15 may set the specific phase displacement for each of the POL regulators 25 through this interface. Controller 15 may set the phase displacements for each POL regulator 25 to minimize the switching noise on the intermediate bus voltage. Alternatively or additionally, controller 15 may set the phase displacements to minimize the noise on the output of the POL regulators 25 connected in parallel. Controller 15 may set the phase displacement statically, e.g., the phase displacement is programmed or set in a

permanent or semi-permanent manner. Alternatively, controller 15 may adapt the phase displacement dynamically to minimize the noise in the system when specific system parameters change. These system parameters may include, for example, load currents, output or input voltages or the number of POL regulators (e.g., the phase displacement may be dynamically adapted when POL regulators are added or removed physically or enabled or disabled electrically).

Because of the flexible nature of the present invention, system 10 may be configured in a variety of modes. For example, in one exemplary embodiment, system 10 may include a common input bus with several voltage outputs. In another exemplary embodiment, system 10 may include several input buses and several voltage outputs. In another exemplary embodiment, system 10 may include a common input bus and a single voltage output. In this particular embodiment, the single voltage output may be a multi-phase voltage output.

Figure 2 illustrates another exemplary embodiment of the present invention. The POL regulator array, indicated generally at 200, includes POL regulators 220 and SYNC line 225. The outputs of POL regulators 235A and 235B are connected in parallel to provide output voltage 230 (Vo1). Similarly, the outputs of POL regulators 235C and 235D provide output voltage 230B (Vo2). Current share lines 240A and 240B are provided for these two pairs, respectively, to provide an equal load share. The input voltage 245 (Vin) is provided to each POL regulator 220. In this particular exemplary embodiment, system 200 does not include a controller. A selected POL regulator 235A, e.g., the POL regulator with Address=0, acts as the Master POL regulator and generates the SYNC portion of the SYNC line signal. All other POL regulators 220 synchronize to this signal. Any internal or external device connected to SYNC line 225 may provide the clock.

Data transmission over SYNC line 225 is not necessary to set the phase displacement of POL regulators 235. In this exemplary embodiment, the address of each POL regulator 235 may be used to determine the phase displacement of the POL regulator 235. For example, as discussed below in reference to Figure 5, the address

of the POL regulators 235 may be used to determine the phase displacement of the pulse width modulated (PWM) signals of each POL regulator 235 as compared to the SYNC line 225. For instance, the address of each POL regulator 20 may set the initial phase displacement and this phase displacement can be overwritten or changed by the controller 15. The addresses for the POL regulators 235 do not need to be unique. For instance, POL regulators 235 with the same address will be phase synchronized. Thus, the optimal phase position of each POL regulator 235 may be chosen to minimize a specific design parameter by wiring or programming the address via input 235 accordingly. For example, POL regulator 220A ("POL 0") may have a phase displacement of 0°, POL regulator 220B ("POL 1") may have a phase displacement of 180°, POL regulator 220C ("POL 2") may have a phase displacement of 90° and POL regulator 220D ("POL 3") may have a phase displacement of 270°. In this particular example, the POL regulators connected in parallel, as shown in Figure 2, will have a 180° phase shift, which is optimal for the outputs of system 200. Similarly, the pairs are 90° phase shifted with respect to each other, which therefore provides an optimal current distribution for the input of system 200.

Figure 3 illustrates one exemplary method of communicating over a single-wire serial bus, e.g., the SYNC/DATA line. Specifically, a transmission line 340 is created by propagating a clock signal 300 over the serial bus. The clock signal 300 can be generated by the controller, a particular POL regulator (e.g., the POL regulator with the least significant address or Address=0), or an external device. The clock signal 300 synchronizes the various communicating devices (e.g., the POL regulators and the controller) and creates a series of clock cycles 310, each one including a data bit 320. This data bit 320 allows the various communicating devices to transmit a single bit of data for every clock cycle 310. Accordingly, each communicating device transmits data by leaving/pulling the data bit 320 high or low (i.e., binary one or zero). It should be appreciated that Figure 3, as discussed herein, is not intended to limit the present invention, but to provide an example as to how communication can occur over a single-wire serial bus.

Figure 4 illustrates one exemplary method of transmitting information between the controller and at least one POL regulator. In this particular example, a forty-two bit communication cycle 450 can be used to transmit initial-configuration data, fault-monitoring data, unique ID data or any combination thereof. As shown in Figure 4, the forty-two bit transmission cycle 450 includes a four bit start sequence 410, a sixteen bit (with parity) address set 420, an eight bit (with parity) command set 430, a first acknowledgement bit 440, an eight bit (with parity) data set 460, and a second acknowledge bit 470. An additional bit 450 has been added to ensure that the command set 430 is executed before the data set 460 is provided. It should be appreciated that the communication cycle 450 depicted in Figure 4 is not intended to limit the present invention, but to illustrate how information can be transmitted over a serial bus. Therefore, communication cycles containing more or less information or bits are within the spirit and scope of the present invention.

The first and second acknowledgement bits 440 and 470, respectively, are used to acknowledge the reception of the command set 430 and the data set 460, respectively. It should be appreciated that the device responsible for the providing the first and second acknowledgement bits 440 and 470 varies depending upon whether the information is being sent to or from the POL regulator (e.g., whether the information is being written, read, or provided).

The command set 430, data set 460 and address set 420 enable the controller and the POL regulators to write, read and provide data. For example, the command set 430 is used to identify whether and what the controller is writing (e.g., writing to the status register), the controller is reading (e.g., reading the status register), or the POL regulator is providing (e.g., providing status register information). The address set 420 is used to identify the POL regulator(s) that is being written to or read or the POL regulator that is providing information. The data set 460 is used to identify the actual data that is being written, read, or provided.

The start sequence 410 and address set 420 are used, in part, to identify the sender of the information. For example, the controller uses a different start sequence

410 than the POL regulators. Thus, the controller can determine, by reading the start sequence 410 of the communication cycle 450 being transmitted, whether a POL regulator is also attempting to send a communication cycle 450 at the same time. Similarly, each POL regulator has a different address set 420. Thus, a POL regulator can determine, by reading the start sequence 410 and address set 420 of the communication cycle 450 being transmitted, whether another POL regulator or the controller is also attempting to send a communication cycle 450 at the same time. If multiple devices are attempting to send a communication cycle 450, sequencing data is used to allocate or arbitrate bus use. It should be appreciated that the sequence data can either be stored (or hard wired) as a default value or provided as initial-configuration data and stored in the storage device (e.g., a sequencing configuration register).

Figure 5 shows an exemplary embodiment of a voltage regulation module, indicated generally at 500, according to the present invention. The voltage regulation module 500 has an input stage and an output stage accessible via an input terminal 510 and an output terminal 520 with a return terminal 530. Generally, voltage regulation module 500 is designed to convert the input voltage Vin between the terminals 510 and 530 into an output voltage Vo between the terminals 520 and 530. The voltage regulation module 500 includes a L/C low pass filter, indicated generally at 560, driven by switching elements Q1 and Q2. A non-inverting driver 540 and an inverting driver 545 are provided for power switches Q1 and Q2, respectively, and these drivers are both controlled or activated by a pulse width modulated control signal generated by the PWM signal generator or pulse width modulator 570, discussed below.

The voltage regulation module also includes an output voltage or power train controller 550. The output voltage controller 550 includes a feedback controller 565 and pulse width modulator 570 that is synchronized to the TRIGGER signal 575. The module 500 further includes a clock recovery circuit 580, a serial interface handler 585 and a memory block 590. The clock recovery circuit 580 generates the phase shifted, synchronized TRIGGER signal 575. The serial interface handler 585 decodes any messages that are sent over the SYNC/DATA line 595 and stores the data in the

memory block 590, e.g. the required phase displacement. The clock recovery circuit 580 and serial interface handler 585 receive address data via input 555. If there is no communication over the SYNC/DATA line 595, for instance, in the case of the exemplary embodiment of the POL regulator array shown in Figure 2 or before any communication over the SYNC/DATA line 595 has taken place, in the case of the exemplary embodiment shown in Figure 1, the memory 590 may be initialized with pre-defined data. This data can either be hardwired or programmed by an OTP (one time programmable) method or any other method. As discussed above, the TRIGGER signal 575 is sent to the voltage regulator's pulse width modulator 570 to start a new PWM control signal used to control the drivers 540 and 545 associated with the power switches Q1 and Q2.

Figure 6 shows an exemplary embodiment of the clock recovery circuit, indicated generally at 600, of the present invention. Generally, clock recovery circuit 600 receives a SYNC/DATA signal 605 and generates a phase-shifted synchronized TRIGGER signal 630. Clock recovery circuit 600 includes an inverter 610, a phase detector (PD) 615, a filter 620, a ring oscillator 625, a delay bus 635, a multiplexer 640 and a frequency divider 680. Clock recovery circuit 600 may access a memory location 645. For example, this memory location may be a memory location in the voltage regulator (e.g., memory 590 as shown in Figure 5).

Inverter 610 inverts SYNC/DATA line signal 605. Phase detector 615 generates a signal which is proportional to the frequency and phase difference of the positive slopes of signals S1 (generated by the inverter 610) and S2 (generated by the frequency divider 680). Filter 620 filters the phase difference and controls the ring-oscillator frequency and phase. Ring oscillator 625 is an oscillator that may generate a delay bus 635. The signals of delay bus 635 are equally spaced to each other (see Figure 7, described below). As discussed above, the D0 signal is used as the TRIGGER signal 630 to synchronize the PWM generator of the power train feedback loop (see, for example, Figure 5). Multiplexer 640 selects, based on the settings in memory block 645, at least one output of delay bus 635. Frequency divider 680 divides

the frequency of the output of multiplexer 640 according the settings in memory block 645 and feeds the signal (shown in Figure 6 as S2) back to phase detector 615.

Generally, the components of clock recovery circuit 600 form a phase locked loop. The phases of the signals S1 and S2 are aligned in steady state. Depending on which signal is chosen by multiplexer 640 from delay bus 635, the D0 positive transition can be shifted relative to the negative transition of the SYNC/DATA line 605. The D0 positive transition defines the starting point of the PWM signal in the power train, e.g., power train 550 shown in Figure 5. In another exemplary embodiment, a selected voltage regulator 500 may serve as the master voltage regulator. The master voltage regulator includes the master clock generator to generate the synchronization signal, as discussed above. In this case, the clock recovery circuit 600 of the master voltage regulator may be configured to act as the master clock generator. For example, this clock recovery circuit 600 may be configured to serve as the master clock generator by opening the phase locked loop of the clock recovery circuit and using the ring oscillator 625 as a free-running oscillator.

Figure 7 shows an exemplary embodiment of the signals generated by the delay bus 635 as shown in Figure 6. In the exemplary embodiment of Figure 7, the ring oscillator 625 generates a delay bus consisting of 2^m signals, wherein each signal is equally delayed by t_d. Note that the delay bus need not generate 2^x number of signals. In a system without a controller (e.g., as depicted in the exemplary embodiment of Figure 2), the phase lead or phase displacement may accordingly be expressed as:

Phi = {[value (address)]/(maximum number of POL regulators)} x 360°

The value (address) corresponds to the address of the selected POL regulator or delay bus signal. The denominator corresponds to the maximum number of POL regulators in the system that may be addressed, e.g., 32.

Figure 8 shows an exemplary embodiment of the various timing signals of the voltage regulation module and clock recovery circuit of the present invention. In this example, m=4. The multiplexer 640 (shown in figure 6) selects signal D3 from delay bus 635. The frequency divider 680 is set to K=1. Accordingly, the clock recovery

circuit 600 aligns the selected delay bus signal D3 to the SYNC/DATA line. As a result, using the formula discussed above, the delay bus signal D0 (e.g., the SYNC signal) has a predictable phase lead of Phi= $3/2^m$ x 360° = 67.5° compared to the SYNC/DATA line. The positive slope of the D0 signal (e.g., the TRIGGER signal) triggers the starting of the PWM signal. Therefore, the PWM signal has the same phase lead as the D0 signal. By changing the multiplexer selection, the phase lead of the PWM signal is therefore selectable by the value stored in memory.

Figures 9-11 illustrate exemplary embodiments of timing diagrams and simplified input ripple waveforms. Figure 9 shows an in-phase set of waveforms. In this exemplary embodiment, four downstream buck converter signals i(i1), i(i2), i(i3) and i(i4), which correspond to the input current of regulators with 3.3 V at 20 A, 2.5 V at 30 A, 1.8 V at 20 A and 1.2 V at 20 A, respectively, are shown. Signal i(co) is the ripple current in an input capacitor. As shown in Figure 9, the resulting capacitor ripple voltage is 1.198 V. Figure 10 illustrates the effects of out-phasing. In this case, the regulators are equally out-phased. It may be noted that the first two waveforms overlap. The resulting capacitor ripple voltage in this case is 406 mV. Figure 11 shows an even more advantageous phasing distribution that results from choosing voltage and current dependant phase displacements. Accordingly, the capacitor ripple voltage is lower. In this case, the capacitor ripple is 263 mV. This shows clearly the advantage of being able to choose the phase displacement according the operating point of the system to reduce system noise. It may be understood that further optimization is possible. Thus, phase displacing these pulses may result in lowered capacitor ripple or, alternatively, lower amounts of bus capacitance may be required to support a given ripple voltage.

The invention is susceptible to various modifications and alternative forms, and specific examples thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the invention is not to be limited to the particular forms or methods disclosed, but to the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the claims.

CLAIMS

What is claimed is:

1. A power supply system comprising:

a plurality of voltage regulators, wherein each voltage regulator is operable to provide a voltage output and is associated with an address;

a master clock generator operable to generate a synchronization signal;

an interface line operable to communicatively couple the voltage regulators and carry the synchronization signal to allow the voltage regulators to receive the synchronization signal; and

a plurality of clock recovery circuits, wherein each clock recovery circuit is associated with a voltage regulator and wherein each clock recovery circuit is operable to generate a phase shifted trigger signal, wherein the phase shifted trigger signal is phase shifted with respect to the synchronization signal by a selected phase difference and synchronized to a selected frequency multiple of the synchronization signal based on the address of the associated voltage regulator such that a first switching cycle associated with a first voltage regulator may be phase displaced with respect to a second switching cycle associated with a second voltage regulator and a different frequency from the second switching cycle.

2. The supply system of Claim 1, wherein a selected one of the plurality of voltage regulators further comprises the master clock generator.

3. The supply system of Claim 1, wherein a selected one of the plurality of clock recovery circuits further comprises the master clock generator.

4. The power supply system of Claim 1, further comprising a controller communicatively coupled to the interface line and operable to transmit data to the voltage regulators and set the selected phase difference for each voltage regulator via the interface line.

5. The power supply system of Claim 4 wherein the controller is operable to set the selected phase difference to minimize system noise.

6. The power supply system of Claim 5, wherein the controller is operable to dynamically set the selected phase difference to minimize system noise in response to a change in a selected system parameter.

7. The power supply system of Claim 6, wherein the selected system parameter is the number of enabled voltage regulators.

8. The power supply system of Claim 1, wherein the phase displacement and selected frequency multiple of each voltage regulator is selected based on the input voltage of the respective voltage regulator.

9. The power supply system of Claim 1, wherein the phase displacement and selected frequency multiple of each voltage regulator is selected based on the output voltage of the respective voltage regulator.

10. The power supply system of Claim 1, wherein each voltage regulator further comprises:

an input terminal, an output terminal and a return terminal, wherein the voltage regulator is operable to convert an input voltage between the input terminal and the return terminal into an output voltage between the return terminal and the output terminal;

a power device;

a memory operable to store the selected phase displacement; and

an output voltage controller operable to receive the phase shifted trigger signal and transmit a pulse width modulated signal based on the phase shifted trigger signal to control the operation of the power device, wherein an associated one of the plurality of clock recovery circuits is operable to access the memory, receive the synchronization signal and transmit the phase shifted trigger signal to the pulse width modulator based on the selected phase displacement.

11. The power supply system of Claim 10, wherein the voltage regulator further comprises a serial interface handler operable to decode data transmitted via the interface line and store the selected phase displacement in the memory.

12. The power supply system of Claim 10, wherein the output voltage controller further comprises a pulse width modulator operable to generate the pulse width modulated signal.

13. The power supply system of Claim 10, wherein the clock recovery circuit comprises a ring oscillator operable to generate a delay bus associated with a plurality of delay bus signals, wherein the phase shifted trigger signal is based on the selected delay bus signal.

14. The power supply system of Claim 13, wherein the clock recovery circuit further comprises a multiplexer operable to select the delay bus signal based on the selected phase displacement stored in the memory.

15. The power supply system of Claim 14, wherein the memory is initialized with the address of the voltage regulator.

16. The power supply system of Claim 1, wherein the voltage regulator is a point-of-load (POL) regulator.

17. The power supply system of Claim 1, wherein the power supply system is operable to receive multiple independent voltage inputs.

18. The power supply system of Claim 1, wherein the power supply system further comprises a single multiple-phase voltage output.

19. The power supply system of Claim 1, wherein the voltage outputs of at least two voltage regulators are connected in parallel.

20. The power supply system of Claim 19, wherein the power supply system further comprises a current share line communicatively coupled between at least two voltage regulators that are connected in parallel to thereby provide an equal load share between the voltage regulators that are connected in parallel.

21. A method for providing the interleaving of a plurality of voltage regulators, comprising the steps of:

selecting a phase displacement for each voltage regulator;

assigning an address for each voltage regulator;

generating a synchronization signal;

generating a trigger signal that is phase displaced from the synchronization signal by the selected phase displacement and synchronized to a selected frequency multiple of the synchronization signal; and

providing a phase displaced switching frequency based on the trigger signal.

22. The method of Claim 21, wherein the phase displacement for a selected voltage regulator is based on the address of the selected voltage regulator.

23. The method of Claim 22, further comprising the step of transmitting the phase displacement for the selected voltage regulator to the selected voltage regulator.

24. The method of Claim 21, further comprising the steps of:

receiving an input voltage via a common input bus; and

providing a single multi-phase voltage output.

25. The method of Claim 21, further comprising the steps of:

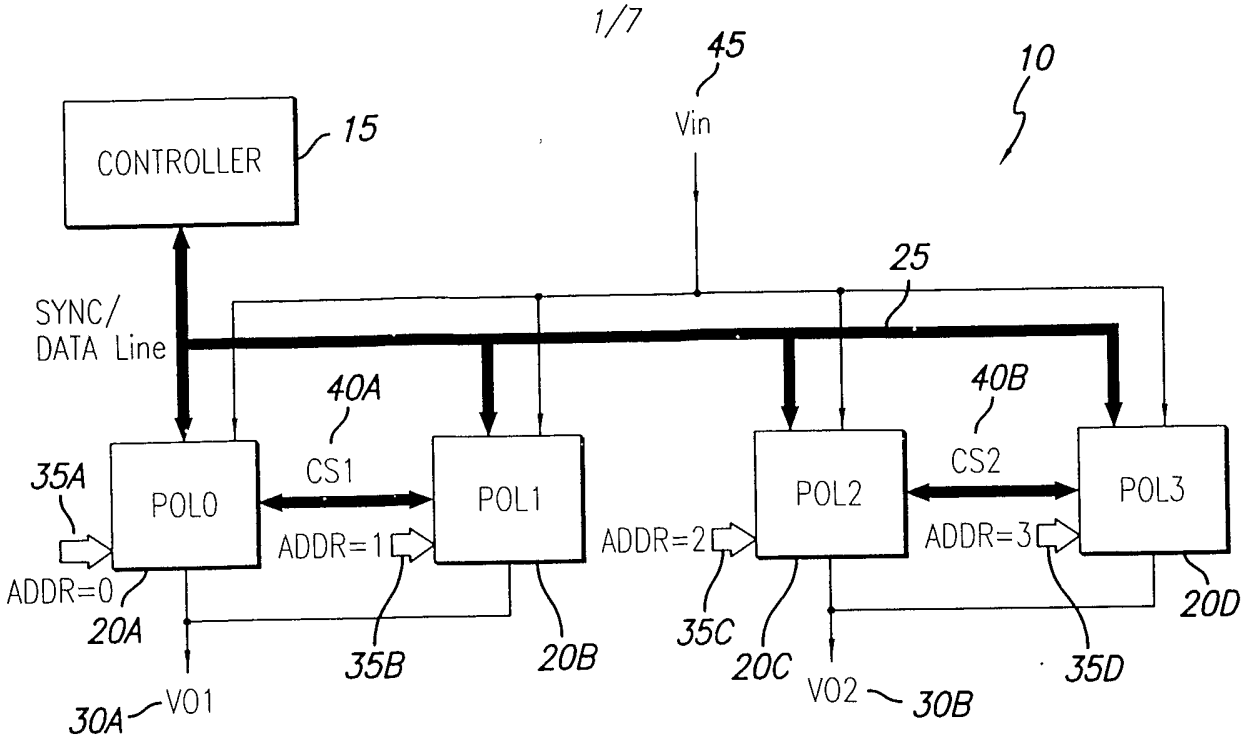
receiving a plurality of input voltages; and

providing a plurality of output voltages, wherein each output voltage is phase displaced with respect to each other.

26. The method of Claim 21, further comprising the steps of

receiving a plurality of input voltages; and

providing a single multi-phase voltage output.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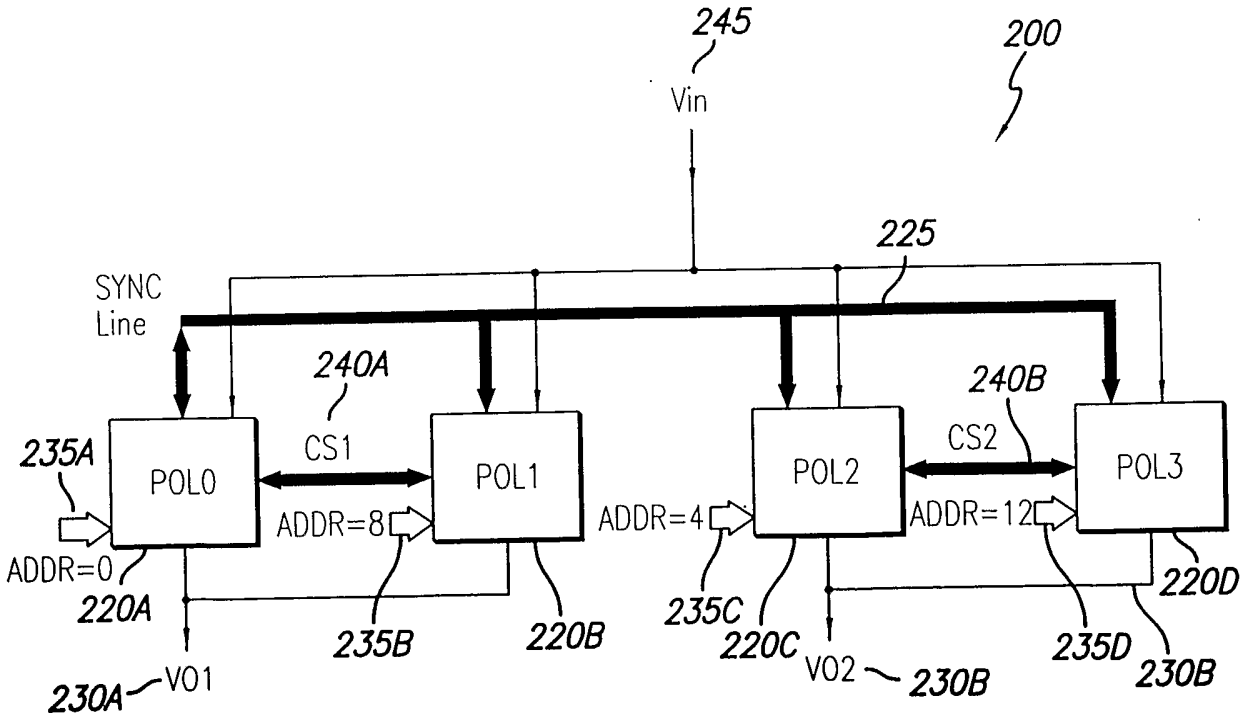
VO1

FIG. 1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Vin
200
225
SYNC
Line
240A
240B
235A
POL0
CS1
POL1
POL2
CS2
POL3
ADDR=8
ADDR=4
ADDR=12
ADDR=0
220A
235B
220B
235C
220C
220D
235D
VO2
230B
230A
VO1

FIG. 2

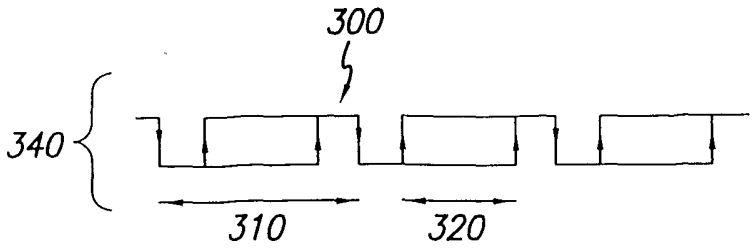

FIG. 3

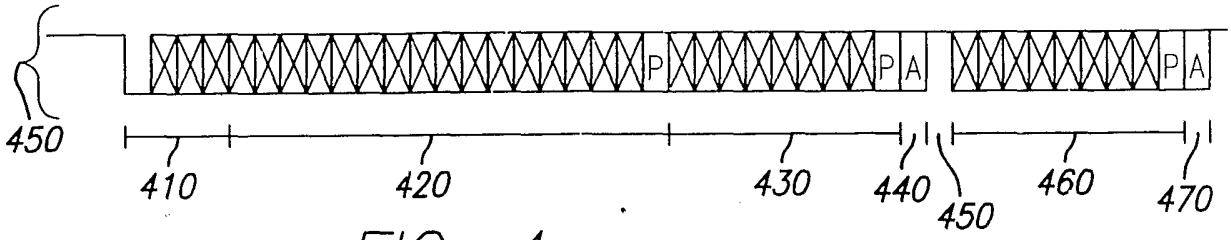

FIG. 4

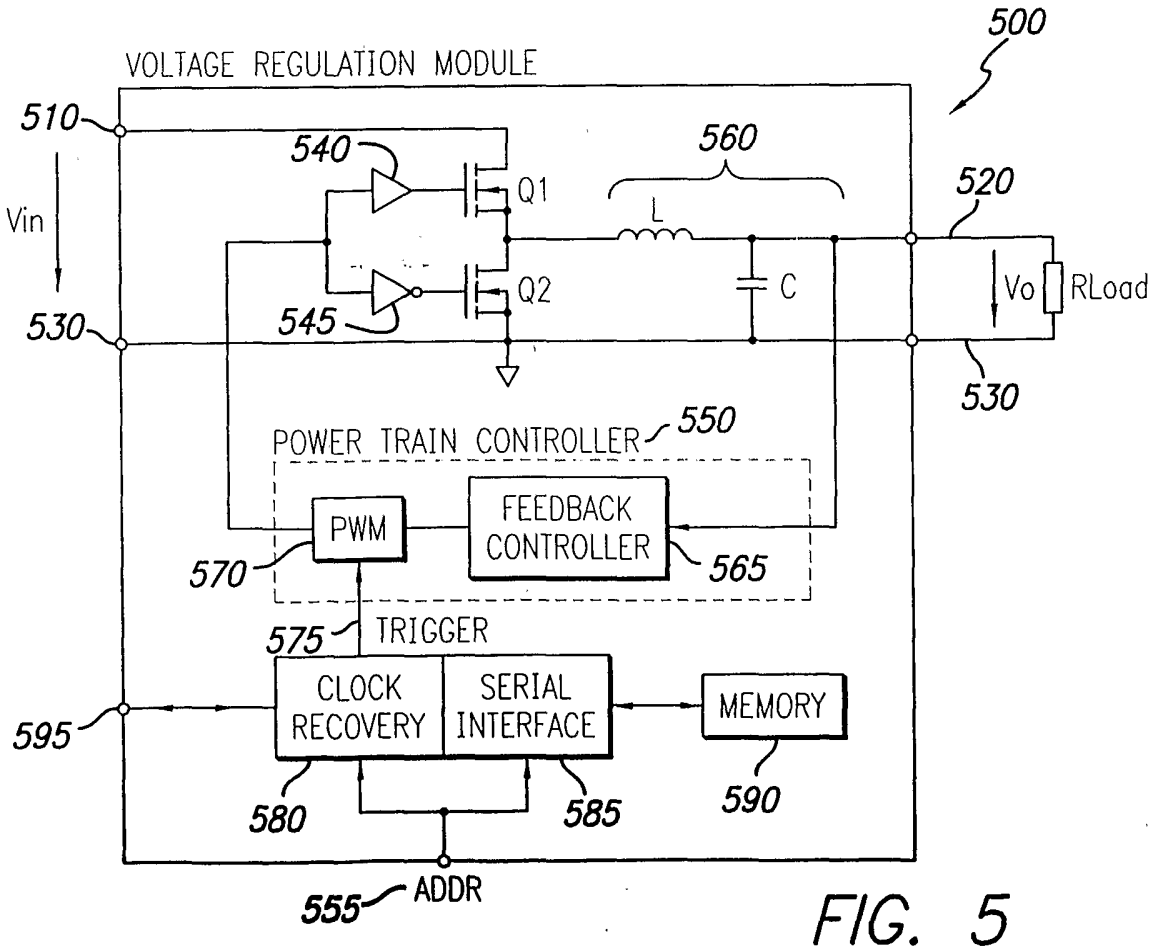

FIG. 5

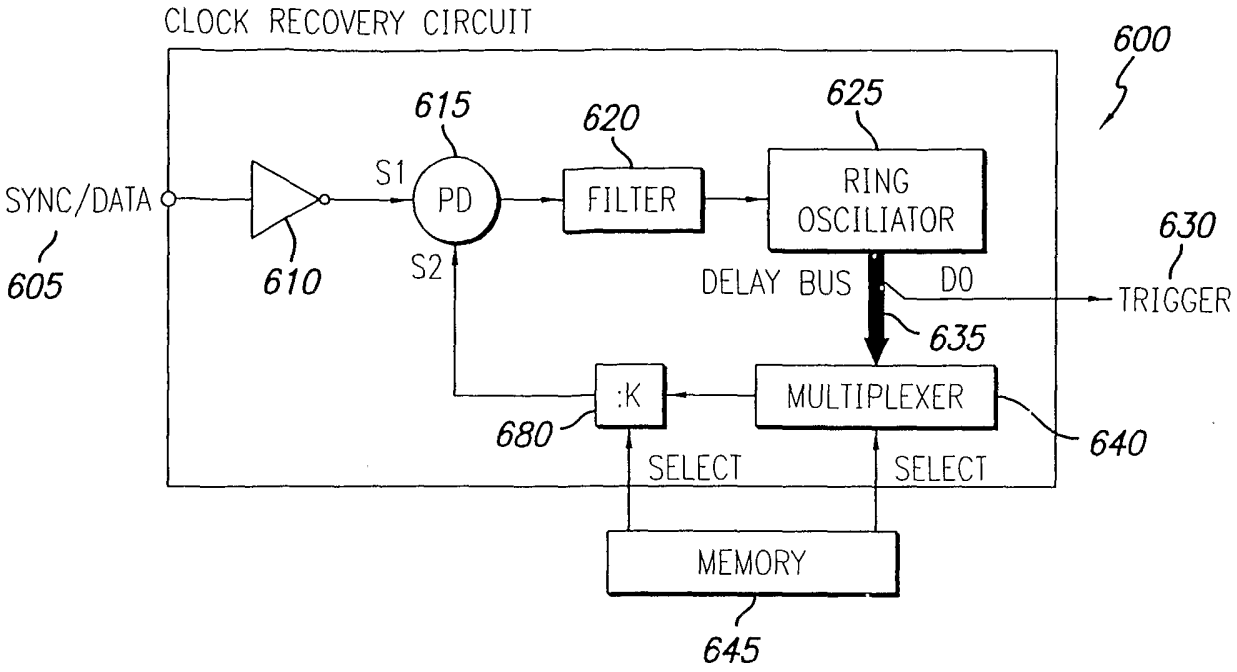
CLOCK RECOVERY CIRCUIT
600
615
620
625
SYNC/DATA
605
610
S1
PD
S2
FILTER
RING
OSCILIATOR
630
DELAY BUS
D0
TRIGGER
635
:K
MULTIPLEXER
680
640
SELECT
SELECT
MEMORY
645

FIG. 6

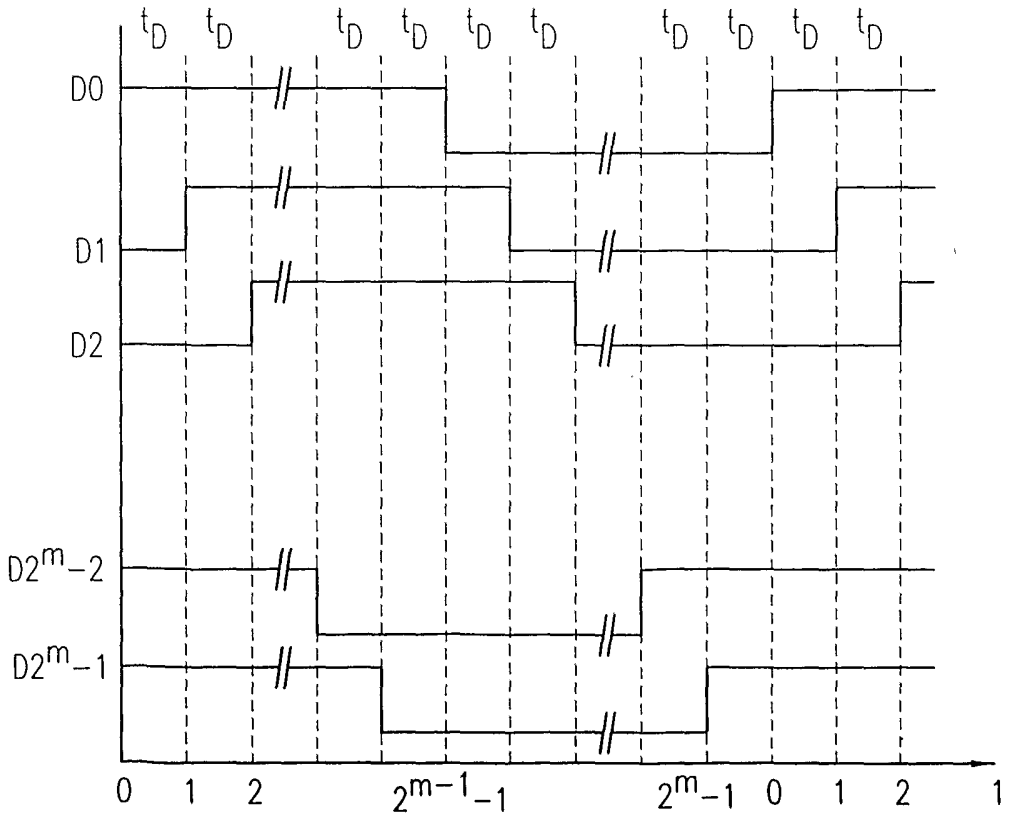
t_D t_D t_D t_D t_D t_D t_D t_D t_D t_D
D0
D1
D2
$D2^m-2$
$D2^m-1$
0 1 2 $2^{m-1}-1$ 2^{m-1} 0 1 2 1

FIG. 7

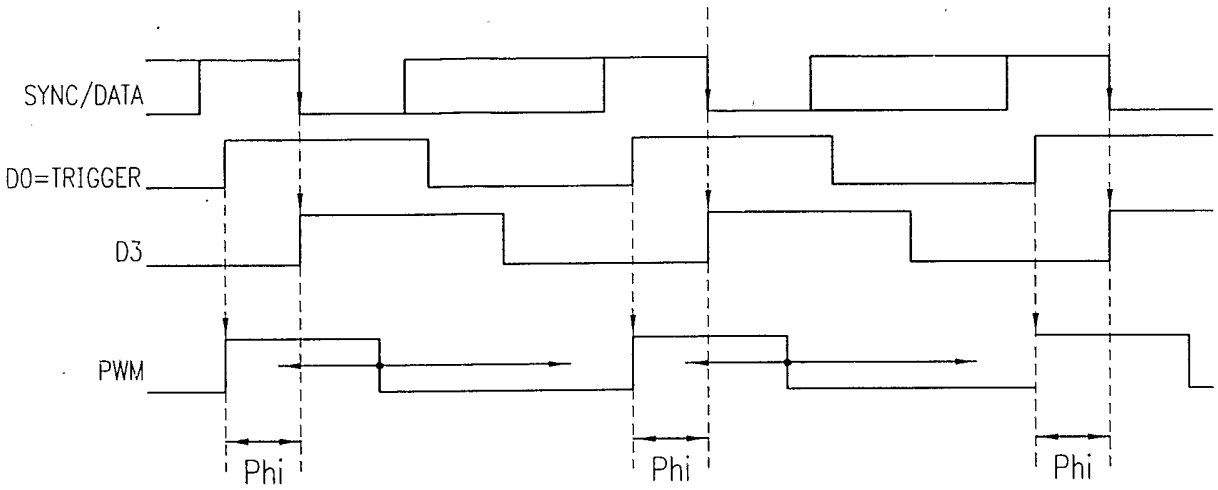

FIG. 8

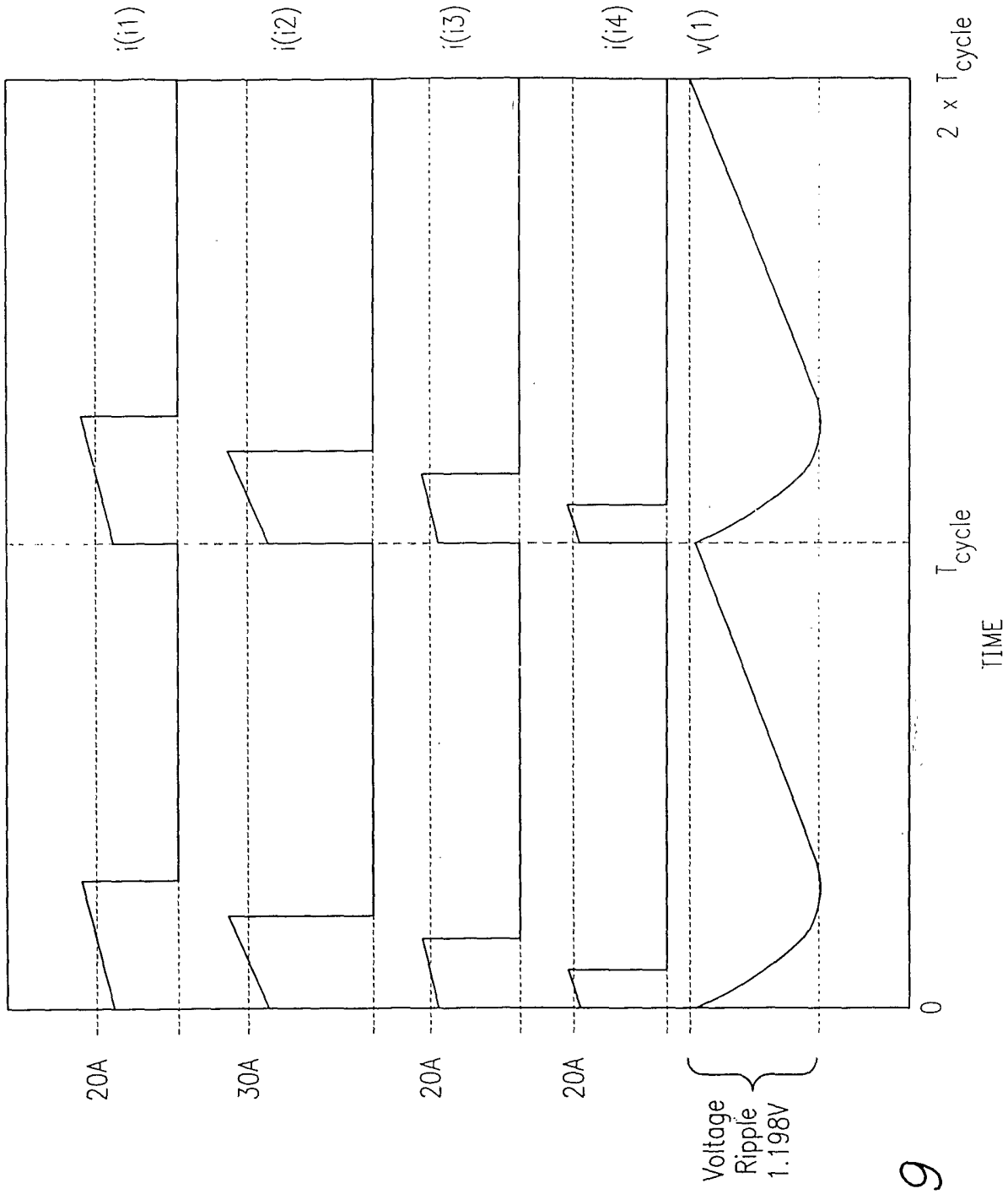
i(i1)
i(i2)
i(i3)
i(i4)
v(1)
2 x Tcycle
Tcycle
0
TIME
20A
30A
20A
20A
Voltage Ripple 1.198V

FIG. 9

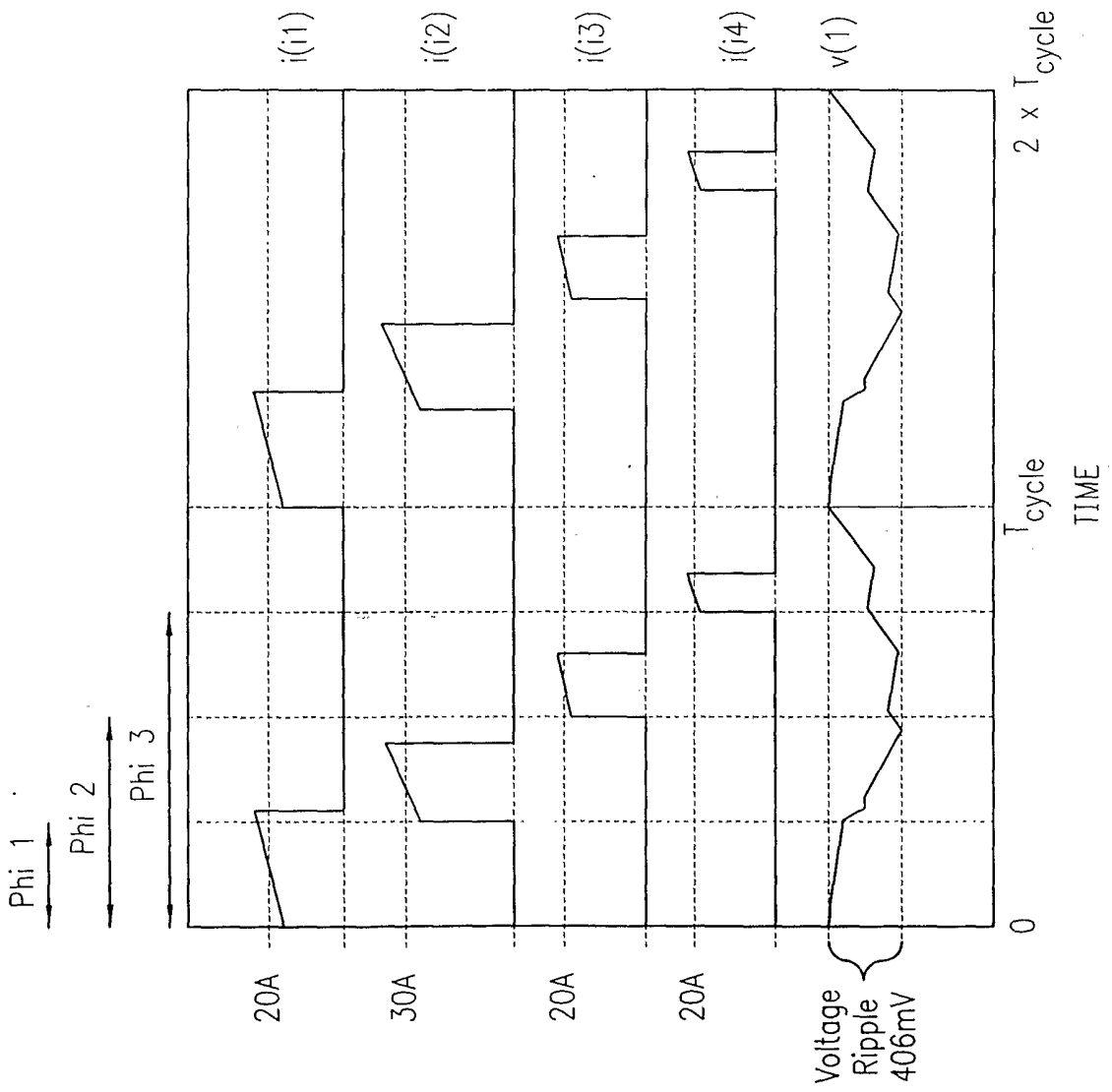
Phi 1
Phi 2
Phi 3
i(i1)
i(i2)
i(i3)
i(i4)
v(1)
20A
30A
20A
20A
Voltage Ripple 406mV
0
T_{cycle}
2 x T_{cycle}
TIME

FIG. 10

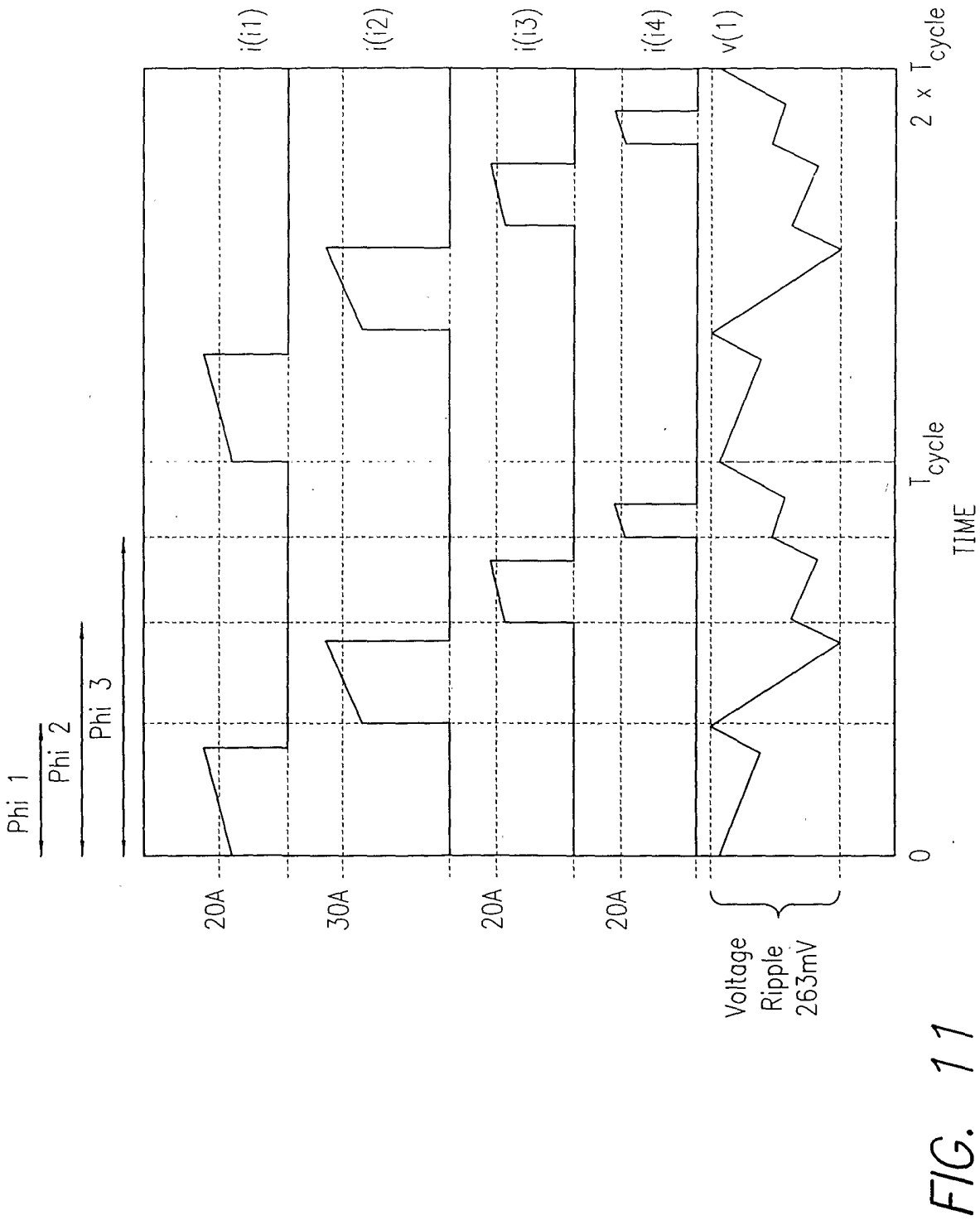
Phi 1
Phi 2
Phi 3
i(i1)
i(i2)
i(i3)
i(i4)
v(1)
20A
30A
20A
20A
Voltage Ripple 263mV
0
Tcycle
2 x Tcycle
TIME

FIG. 11

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/35515

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02J1/10 H02M3/28 H02M3/158

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02J H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 929 618 A (HOCK RICHARD H ET AL) 27 July 1999 (1999-07-27)	1,21
A	abstract the whole document	2-20, 22-26
A	WO 02/31951 A (PRIMARION INC) 18 April 2002 (2002-04-18) abstract page 5 page 13	1-26
A	EP 0 660 487 A (HITACHI LTD) 28 June 1995 (1995-06-28) claim 20	1-26

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 May 2004	21/05/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Marannino, E.

INTERNATIONAL SEARCH REPORT

Information on patent family members

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