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(54) Titre : METHODE D'ATTAQUE POUR LA PROGRAMMATION A TENSION COMPENSEE D'AFFICHAGES DEL ORGANIQUES A MATRICE ACTIVE

(54) Title: DRIVING METHOD FOR COMPENSATED VOLTAGE-PROGRAMMING OF AMOLED DISPLAYS

(57) Abrégé/Abstract:
Disclosed are two techniques for providing a stable current source for active matrix light emitting displays, in particular, active matrix organic light emitting diode (AMOLED) displays. The techniques include a driving method to generate a gate-source voltage independent of the threshold voltage of the drive thin film transistor (TFT) and OLED voltage.

DRIVING METHOD FOR COMPENSATED VOLTAGE-PROGRAMMING OF AMOLED DISPLAYS

ABSTRACT

Disclosed are two techniques for providing a stable current source for active matrix light emitting displays, in particular, active matrix organic light emitting diode (AMOLED) displays. The techniques include a driving method to generate a gate-source voltage independent of the threshold voltage of the drive thin film transistor (TFT) and OLED voltage.

DRIVING METHOD FOR COMPENSATED VOLTAGE-PROGRAMMING OF AMOLED DISPLAYS

FIELD OF THE INVENTION

The present invention generally relates to a light emitting device displays, and particularly, to a driving technique for AMOLED, and to enhance the brightness stability of the OLED by using circuit compensation.

SUMMARY OF INVENTION

This invention provides a simple and highly stable voltage-programmed pixel circuit, suitable for use in AMOLEDs. Each pixel has a driving TFT whose overdrive voltage is generated by applying a waveform independent of its threshold voltage and the OLED voltage.

This also provides another stable driving method based on bootstrapping. Few pixels are presented as examples in which the technique is employed.

Advantages

The pixel circuit provides a stable current independent of the threshold voltage shift of the drive TFT and OLED degradation under prolonged display operation, to efficiently improve the display operating lifetime. Moreover, because of the circuit simplicity, we expect higher production yield, lower fabrication cost and higher resolution than other pixel circuit.

BACKGROUND OF THE INVENTION

The AMOLED display with amorphous silicon (a-si), poly-silicon, organic, or other driving backplane has numerous advantages over the active matrix liquid crystal display (AMLCD). In particular, with a-Si besides its low temperature fabrication that broadens the use of different substrates and makes feasible flexible displays, its low cost fabrication, high resolution, and wide viewing angle are even more attractive. An AMOLED consists of pixelated OLEDs and backplane electronics arranged in an array of

rows and columns. Since the OLED is a current driven device, to achieve a consistent and uniform luminance, the pixel circuit of an AMOLED should be capable of providing an accurate and constant drive current.

FIG. 1 shows a simple pixel as disclosed in U.S. Patent. NO. 5,748,160. It comprises two thin film transistors (TFTs) and an OLED **10** connected to the drain terminal of a driving TFT **11**. The gate terminal of the driving TFT **11** is connected to a column line **12** through a switching TFT **13**. A storage capacitor **14** connected between the gate terminal of the driving TFT **11** and ground is used to maintain the voltage at the gate terminal of the driving TFT when the pixel circuit is disconnected from the column line **12** [1]. For this circuit the current flowing through the OLED strongly depends on the characteristic parameters of the driving TFT **11**. Since the characteristic parameters of the TFT **11**, and in particular, its threshold voltage under bias stress varies with time, and since such changes differ from pixel to pixel, the induced image distortion can be unacceptably high.

Voltage-programmed pixels, disclosed in patents (such as U.S. patent NO. 06229508), provide a current to the OLED independent of the threshold voltage of the driving TFT. The gate-source voltage of the drive TFT in these pixels comprises a programming voltage and the threshold voltage of the driving TFT [2]. The drawback of the disclosed inventions is that the pixel circuit is complex and uses extra transistors.

Current-programmed pixels, disclosed in earlier patents (such as U.S. Patent NO. 6734636), make the circuit less sensitive to shift in the threshold voltage. In these pixels, the gate-source voltage of the drive transistor is self-adjusted based on the current that flows through it in the next frame, so that the OLED current is less dependent on the current-voltage characteristics of the drive transistor [3]. A drawback of the current-programmed pixel is the overhead associated with the low programming current levels arising from the column line charging time due to the large line capacitance.

References:

1- Shieh, Chan-Long, Lee, Hsing-Chung, So, Franky, "U.S. Patent. NO. 5,748,160: Active driven LED matrices," May 5, 1998.

2- Kane, Michael Gillis, "U.S. Patent NO. 6229508: Active matrix light emitting diode pixel structure and concomitant method," May 8, 2001.

3- Sanford, James Lawrence, Libsch, Frank Robert, "U.S. Patent NO. 6734636: OLED current drive pixel circuit," May 11, 2004.

DETAILED DESCRIPTION OF THE INVENTION

The present invention involves a technique for driving a column of pixels to provide stable OLED operation.

FIG. 2 (a-b) shows a pixel circuit along with its control signals. This method is valid with complementary device (p-type transistor) and an example circuit with p-type TFTs is shown in **Fig 8**.

The pixel circuit comprises two transistors **T1** and **T2**, a storage capacitor **21** and an organic light-emitting diode (OLED) **20**. The pixel circuit is connected to a select line (**SEL**), a signal line (**VDATA**), a controllable voltage line (**VDD**), and a common ground.

Transistors **T1**, and **T2** can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology. The source terminal of the drive transistor **T1** is connected to the anode electrode of the OLED **20**. The drain terminal of **T1** is connected to **VDD**, and the gate terminal of **T1** is connected to the signal line (**VDATA**) through **T2**. The storage capacitor is connected between the source and gate of **T1**.

Transistor **T2** is a switch. The gate terminal of **T2** is connected to the select line (**SEL**). The drain terminal of **T2** is connected to the signal line (**VDATA**), and the source terminal is connected to the gate terminal of **T1**. The cathode electrode of OLED **20** is connected to the common ground.

The operation of the pixel presented in **Fig 2 (b)** consists of two operating cycles: programming cycles and driving cycle. During the programming cycles, node **B** is charged to the negative threshold voltage of **T1** and node **A** is charged to a programming voltage (VP) resulting in the gate-source voltage of **T1** as:

$VGS = VP - (-VT) = VP + VT$.

With reference to the waveform shown on **FIG. 2 (b)** we describe the following operating cycles.

The first operating cycle: **VDD** goes to a compensating voltage (VCOMPB), and **VDATA** goes to a high positive compensating voltage (VCOMPA), and **SEL** is high. Therefore, node **A** is charged to VCOMPA and node **B** is charged to VCOMPB.
The second operating cycle: While **VDATA** goes to a reference voltage (VREF), node **B** gets discharged through **T1** until **T1** turns off. As a result, the voltage of node **B** reaches VREF-VT. **VDD** has a positive voltage (VH) to increase the speed of this cycle (for the optimal settling time, VH should be equal to the operating voltage).
The third operating cycle: While **SEL** is high, node **A** is charged to VP +VREF. Because the OLED's capacitance **22** is large, the voltage at node **B** stays at the voltage generated in the previous cycle (VREF-VT). Therefore,

$$VGS = VP + VT,$$

where VGS and VT are the gate-source voltage and threshold voltage of **T1**, respectively.
The fourth operating cycle: **SEL** and **VDATA** are zero and **VDD** goes to the operating voltage. Since the gate-source voltage of **T1** is independent of the voltage of OLED **20** and threshold voltage of **T1**, the OLED degradation and instability of **T1** do not affect the amount of current flowing through **T1** and OLED **20**.

FIG. 3 shows the lifetime test result for the circuit and waveform shown in **FIG. 2 (a)** and **(b)**. The result shows that the OLED current is very stable after 120 hours operation (the VT shift of T1 is 0.7v).

FIG. 4 shows an array structure with pixel **40** of **FIG. 2 (a)**.
The array consists of pixels **40** which are arranged in rows and columns and interconnections **41**, **42**, and **43**. **VDATA** is shared between the common column pixels while **SEL** and **VDD** are shared between common row pixels in an array structure.

FIG. 5 shows a pixel circuit along with its control signals. This method is also valid for the complementary device (p-type transistor).
The pixel circuit comprises three transistors **T1**, **T2**, and **T3**, an organic light-emitting diode (OLED) **50** and two storage capacitors **52, 53**. The pixel circuit is connected to two select lines (**SEL1 and SEL2**), a signal line (**VDATA**), a voltage line (**VDD**), a

controllable voltage line (**VSS**), and a common ground (the ground can be connected to the **VSS**).

Transistors **T1**, **T2** and **T3** can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology. The drain terminal of the drive transistor **T1** is connected to the cathode electrode of the OLED **50**. The source terminal of **T1** is connected to **VSS**, and the gate terminal of **T1** is connected to its drain line through **T2**. The two storage capacitors are in series and connected between the gate of **T1** and ground.

Transistor **T2** is a switch. The gate terminal of **T2** is connected to the first select line (**SEL1**). The drain terminal of **T2** is connected to the drain terminal of **T1**, and the source terminal is connected to the gate terminal of **T1**.

Transistor **T3** is a switch. The gate terminal of **T3** is connected to the second select line (**SEL2**). The drain terminal of **T2** is connected to the signal line (**VDATA**), and the source terminal is connected to the shared terminal of the storage capacitors. The anode electrode of OLED **50** is connected to **VDD**.

The operation of the pixel presented in **Fig 5 (a)** and **(b)** consists of two operating cycles: programming cycles and driving cycle. During the programming cycles, a programming voltage (VP) plus threshold voltage of **T1** (VP+VT) is stored in the first storage capacitor **52**. The source terminal of **T1** goes to zero, and the second storage capacitor **53** is charged to zero, resulting in a gate-source voltage of **T1** as: $VGS = VP + VT$.

With reference to the waveform shown on **FIG. 5 (b)** we describe the following operating cycles.

The first operating cycle: **VSS** goes to a high positive voltage, and **VDATA** is zero, and both select lines are high. Therefore, nodes **B** and **A** are charged to a positive voltage.

The second operating cycle: While **SEL1** is low and **T2** is off, **VDATA** goes to a high positive voltage. Therefore, the voltage at node **B** increases (bootstrapping), and node **A** is charged to the voltage of **VSS**; at this voltage, the OLED **50** is off.

The third operating cycle: **VDATA** goes to VREF –VP, and **VSS** goes to VREF. At the beginning of this cycle, the voltage at node **B** becomes almost equal to the voltage of node **A** because the OLED capacitance **51** is bigger than first storage capacitor **52**. After that, the voltage of node **B** and the voltage of node **A** get discharged through **T1** until **T1**

turns off. Therefore the gate voltage of **T1** is VREF +VT, and the stored voltage in the first storage capacitor **52** is VP+VT.

The fourth operating cycle: Since **SEL2** is high, and **VDATA** is zero, the voltage at node **C** goes to zero.

The fifth operating cycle: **VSS** goes to zero, resulting in a gate-source voltage of **T1** as: VP+VT. Therefore, the current flowing through **T1** is independent of the threshold voltage of **T1**.

FIG. 6 shows a pixel circuit along with its control signals. This method is also valid for the complementary device (p-type transistor).

The pixel circuit comprises three transistors **T1**, **T2**, and **T3**, an organic light-emitting diode (OLED) **60** and two storage capacitors **62**, **63**. The pixel circuit is connected to a select line (**SEL**), a signal line (**VDATA**), a voltage line (**VDD**), a controllable voltage line (**VSS**), and a common ground (the ground can be connected to the **VSS** as well).

Transistors **T1**, **T2** and **T3** can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology.

The drain terminal of the drive transistor **T1** is connected to the cathode electrode of the OLED **60**. The source terminal of **T1** is connected to **VSS,** and the gate terminal of **T1** is connected to its drain line through **T2**. The two storage capacitors are in series, and connected between the gate of **T1** and the ground.

Transistor **T2** is a switch. The gate terminal of **T2** is connected to the select line (**SEL**). The drain terminal of **T2** is connected to the drain terminal of **T1,** and the source terminal is connected to the gate terminal of **T1**.

Transistor **T3** is a switch. The gate terminal of **T3** is connected to the select line (**SEL**). The drain terminal of **T2** is connected to the signal line (**VDATA**), and the source terminal is connected to the shared terminal of the storage capacitors. The anode electrode of OLED **60** is connected to **VDD**.

The operation of the pixel presented in **Fig 6 (a)** and **(b)** consists of two operating cycles: programming cycles and driving cycle. During the programming cycles, a programming voltage (VP) plus threshold voltage of **T1** (VP+VT) is stored in the first storage capacitor

62. The source terminal of **T1** goes to zero, and the second storage capacitor **63** is charged to zero resulting in a gate-source voltage of **T1** as: $VGS = VP + VT$.

With reference to the waveform shown in **FIG. 6 (b)** we describe the following operating cycles.

The first operating cycle: **VSS** goes to a high positive voltage, and **VDATA** is zero, and **SEL** is high. Therefore, node **B** and node **A** are charged to a positive voltage in which the OLED **60** turns off.

The second operating cycle: While **SEL** is high, **VDATA** goes to VREF-VP, and **VSS** goes to VREF. Therefore, the voltage of node **B** and the voltage of node **A** are discharged through **T1** until **T1** turns off. Therefore, the voltage of node **B** is VREF+VT, and the stored voltage in the first storage capacitor **62** is VP+VT.

The third operating cycle: Since **SEL** is VM and **VDATA** is zero, the voltage of node **C** goes to zero. Since VM < VREF+VT(T1) +VT(T2), T2 is off, and the stored voltage in **CS1 62** remains intact .

The fourth operating cycle: **VSS** goes to zero, resulting in the gate-source voltage of **T1** as: VP+VT. Therefore, the current flowing through **T1** is independent of the threshold voltage of **T1.**

FIG. 7 shows a pixel circuit along with its control signals. This method is also valid for the complementary device (p-type transistor).

The pixel circuit comprises three transistors **T1, T2,** and **T3,** an organic light-emitting diode (OLED) **70** and two storage capacitors **72, 73**. The pixel circuit is connected to a select lines **(SEL),** a signal line **(VDATA),** a controllable voltage line **(VDD),** and a voltage line **(VSS).**

Transistors **T1, T2** and **T3** can be amorphous silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology.

The drain terminal of driving transistor **T1** is connected to the cathode electrode of the OLED **70**. The source terminal of **T1** is connected to ground, and the gate terminal of **T1** is connected to its drain line through **T2**. The two storage capacitors are in series and connected between the gate of **T1** and ground.

Transistor **T2** is a switch. The gate terminal of **T2** is connected to the select line (**SEL**). The drain terminal of **T2** is connected to the drain terminal of **T1**, and the source terminal is connected to the gate terminal of **T1**.

Transistor **T3** is a switch. The gate terminal of **T3** is connected to the select line (**SEL**). The drain terminal of **T2** is connected to the signal line (**VDATA**), and the source terminal is connected to the shared terminal of the storage capacitors. The anode electrode of OLED **70** is connected to **VDD**.

The operation of the pixel presented in **Fig 6 (a)** and **(b)** consists of two operating cycles: programming cycles and driving cycle. During the programming cycles, a programming voltage (VP) plus threshold voltage of **T1** is stored in the first storage capacitor **72**. The source terminal of **T1** goes to zero, and the second storage capacitor **73** is charged to zero, resulting in the gate-source voltage of **T1** as: $VGS = VP + VT$.

With reference to the waveform shown on **FIG. 7 (b)** we describe the following operating cycles.

The first operating cycle: While **VDD** is high, node **B** and node **A** are charged to a positive voltage.

The second operating cycle: **SEL** is low, and **VDD** goes to a reference voltage (VREF) in which the OLED **70** is off.

The third operating cycle: **VDATA** goes to –VP, and **SEL** is high. Therefore, the voltage of node **B** and a voltage of node **A** become equal at the beginning of this cycle. The first storage capacitor **72** should be large enough in order that its voltage to become dominant. After that, node **B** gets discharged through **T1** until **T1** turns off. Therefore, the voltage of node **B** is the threshold voltage of **T1**, and the stored voltage in the first storage capacitor **72** is VP+VT.

The fourth operating cycle: Since **SEL** is VM, and **VDATA** is zero, the voltage of node **C** goes to zero resulting in a gate-source voltage of **T1** as: VP+VT. Since VM < VP+VT, T2 is off, and the stored voltage in the first storage capacitor **72** stays at VP+VT.

Fifth operating cycle: **VDD** goes to the operating voltage, and a current independent of the threshold voltage of **T1** flows through the OLED **70**.

FIG. 8 (a-b) shows a pixel circuit along with its control signals.

The pixel circuit comprises two transistors **T1** and **T2**, a storage capacitor **81** and an organic light-emitting diode (OLED) **80**. The pixel circuit is connected to a select line (**SEL**), a signal line (**VDATA**), a controllable ground voltage line (**VSS**), and a common ground.

Transistors **T1** to **T2** can be nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology.

The source terminal of the driving transistor **T1** is connected to the cathode electrode of the OLED **80**. The drain terminal of **T1** is connected to **VSS**, and the gate terminal of **T1** is connected to the signal line (**VDATA**) through **T2**. The storage capacitor is connected between the source and gate of **T1**.

Transistor **T2** is a switch. The gate terminal of **T2** is connected to the select line (**SEL**). The drain terminal of **T2** is connected to the signal line (**VDATA**), and the source terminal is connected to the gate terminal of **T1**. The cathode electrode of the OLED **80** is connected to common ground.

The operation of the presented pixel in **Fig 8** consists of two operating cycles: programming cycles and driving cycle. During the programming cycles, node **B** is charged to positive threshold voltage of T1 and node **A** is charged to negative programming voltage (-VP) resulting in the gate-source voltage of **T1** as:

$$VGS = VP - (-VT) = VP + VT .$$

With reference to **FIG. 8 (b)**, we describe the following operating cycles.

The first operating cycle: **VSS** goes to a positive compensating voltage (VCOMPB) and **VDATA** goes to a negative compensating voltage (-VCOMPA) and **SEL** is negative so **T2** is on; and node **A** is charged to -VCOMPA.

The third operating cycle: **VDATA** goes to a reference voltage (VREF). **SEL** is negative so node **B** gets discharged through **T1** until **T1** turns off. Therefore, the voltage of node **B** reaches the positive threshold voltage of **T1**. **VSS** is a negative voltage (VL) to increase the speed of the circuit. For the optimal settling time, VL should be equal to the operating voltage.

The fourth operating cycle: While **VSS** is zero, and **SEL** is negative, node **A** is charged to negative programming voltage (-VP). Because the OLED's capacitance **82** is large, the voltage of node B stays at the positive threshold voltage. Therefore,

$$V_{GS} = -VP - V_T ,$$

where VGS and VT are the gate-source voltage and threshold voltage of **T1**, respectively.

The fifth operating cycle: **SEL** and **VDATA** are zero, and **VSS** goes to a high negative voltage (operating voltage). Because the gate-source voltage of **T1** is independent of the voltage of the OLED **80** and the threshold voltage of **T1**, the OLED degradation and instability of **T1** do not affect the amount of current flowing through **T1** and the OLED **80**.

FIG. 9 shows an array structure of pixel **90** of **FIG. 8**.

The array consists of pixels **90** which are arranged in rows and columns and interconnections **91**, **92**, and **93**. **VDATA** is shared between the common column pixels while **SEL** and **VSS** are shared between common row pixels in an array structure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is the conventional 2-TFT voltage programmed pixel (prior art). [1]

FIG. 2 (a-b) is a circuit diagram of an embodiment of a pixel circuit and its corresponding waveforms.

FIG. 3 is the lifetime test result for 120 hours.

FIG. 4 is an array structure of the pixel presented in **FIG 2**.

FIG. 5 shows a top emission pixel using n-type transistor.

FIG. 6 shows another top emission pixel using n-type transistor.

FIG. 7 shows a top emission pixel using n-type transistor and patterned OLED.

FIG. 8 (a-b) is circuit diagram of another embodiment of a pixel circuit having a p-channel transistor and its corresponding waveforms.

FIG. 9 is an array structure of the pixel presented in **FIG 8**.

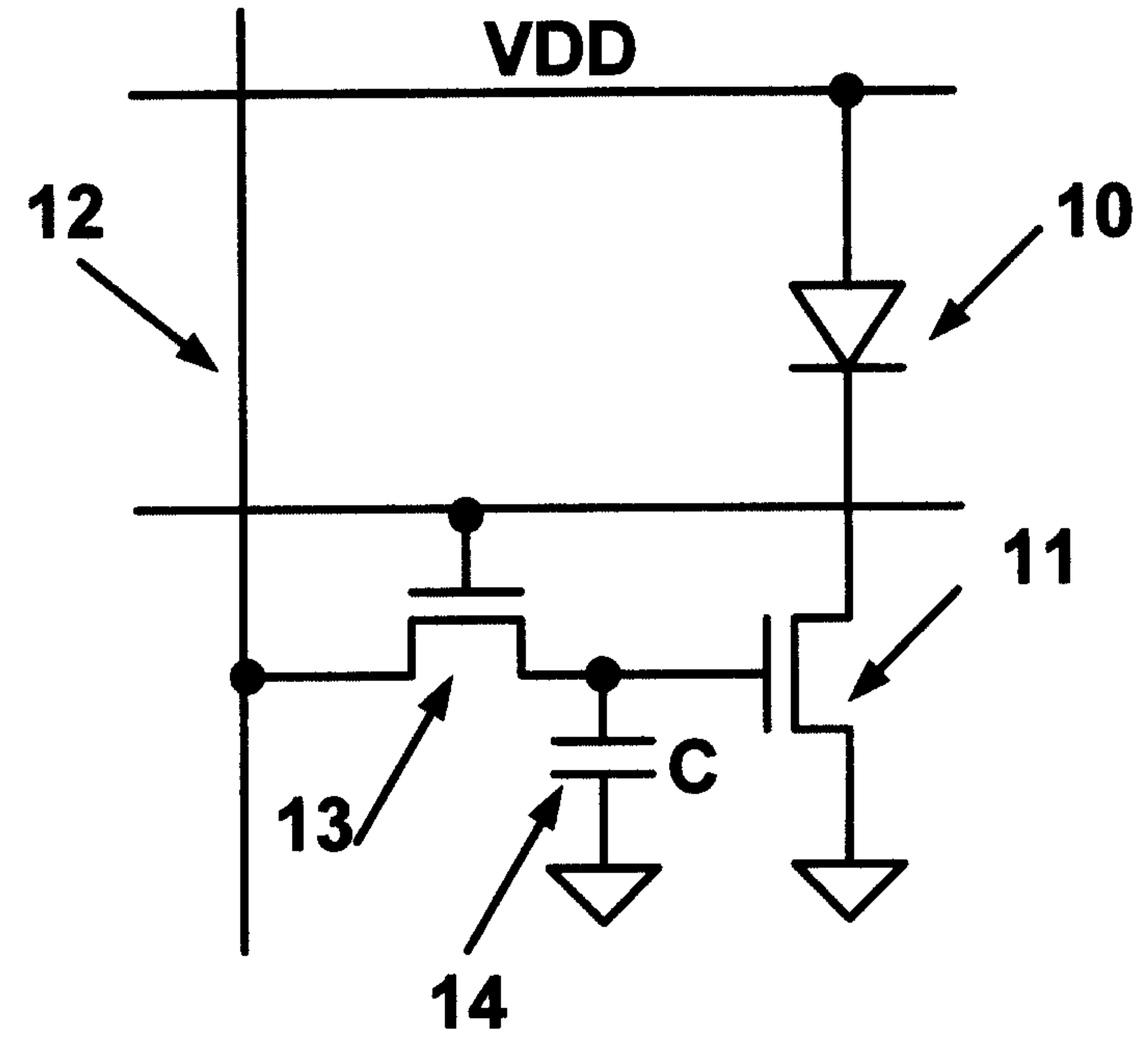
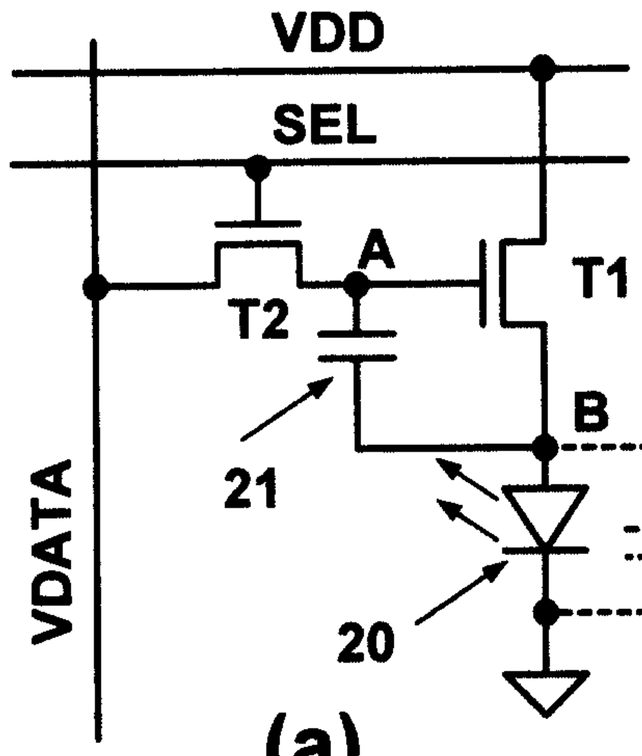
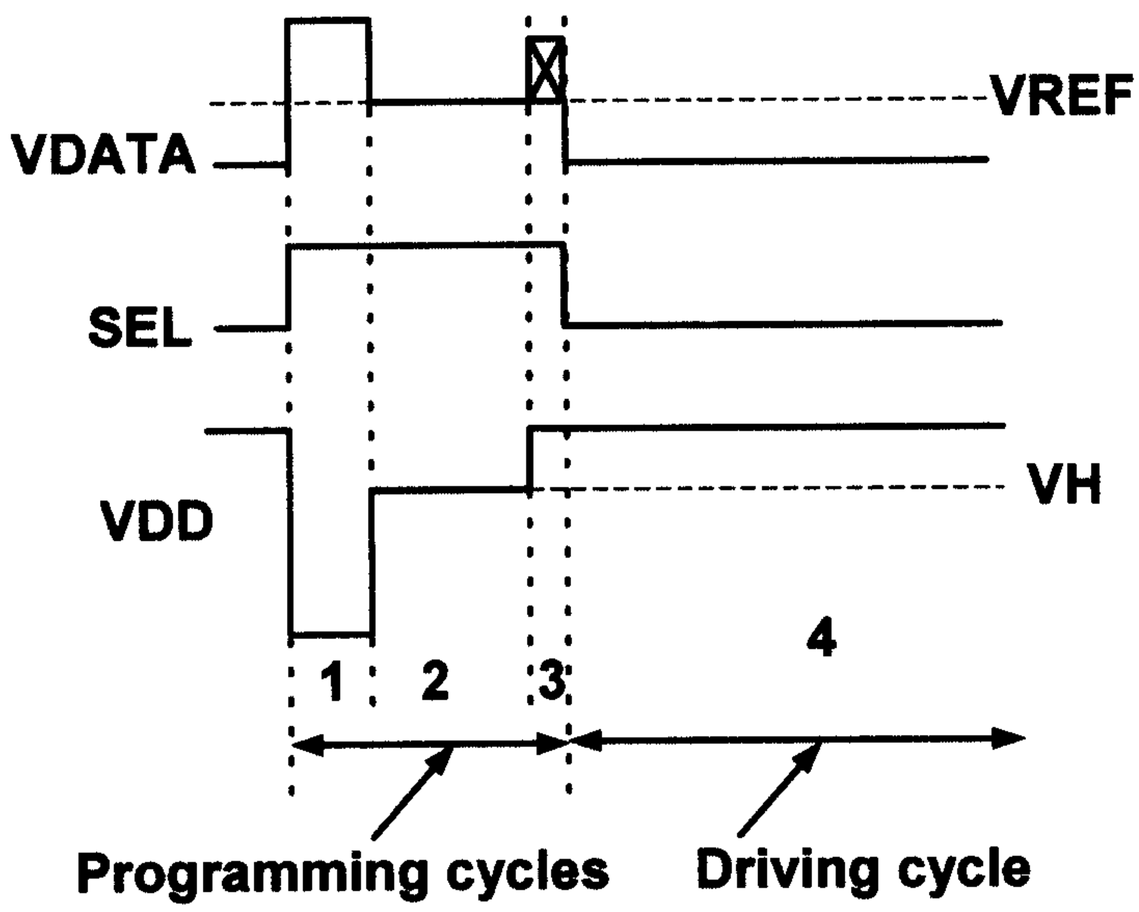


FIG.1


VDD
SEL
A
T1
T2
B
21
VDATA
20
22

(a)


VREF
VDATA
SEL
VH
VDD
4
1
2
3
Programming cycles
Driving cycle

(b)

FIG.2

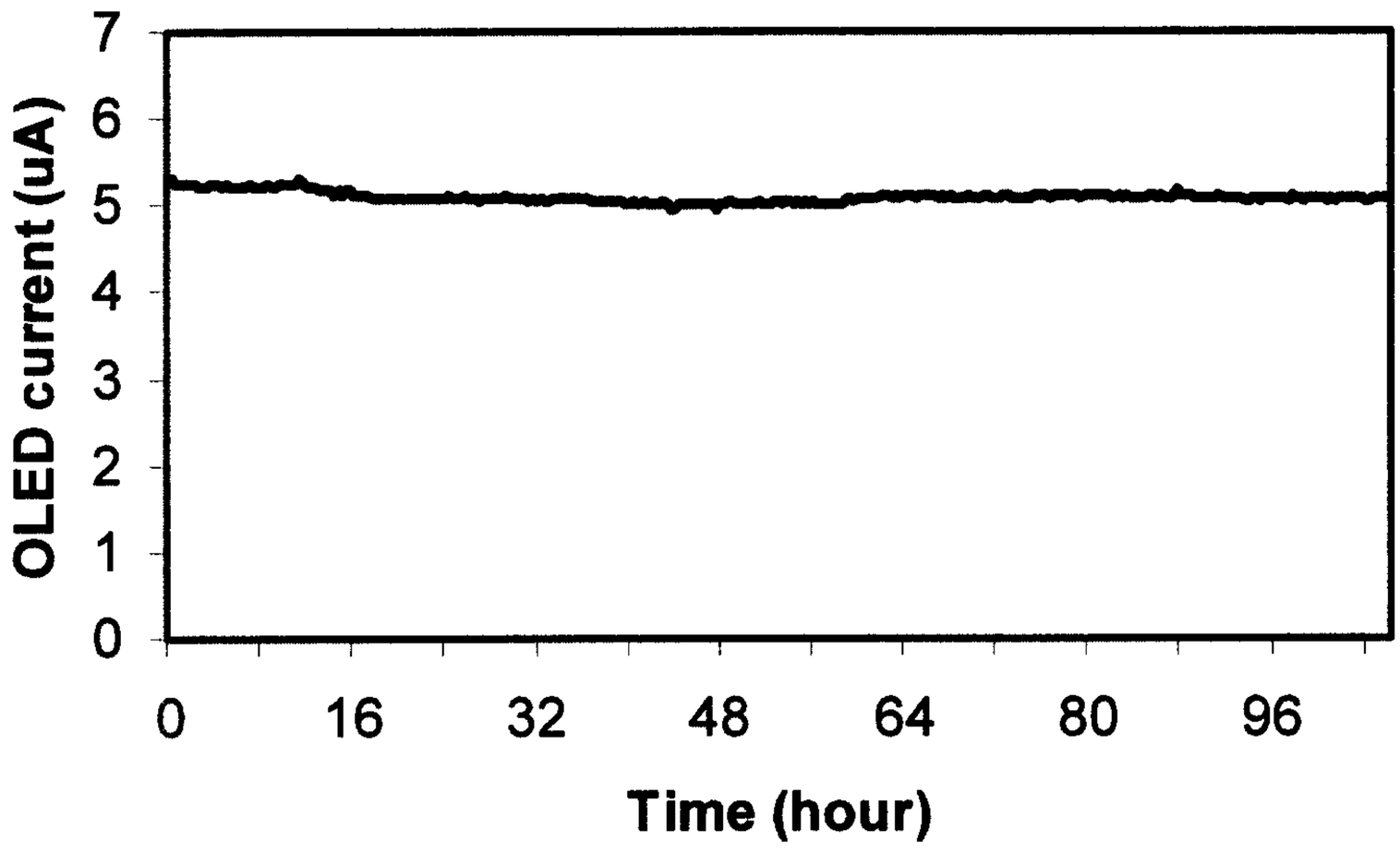


FIG. 3

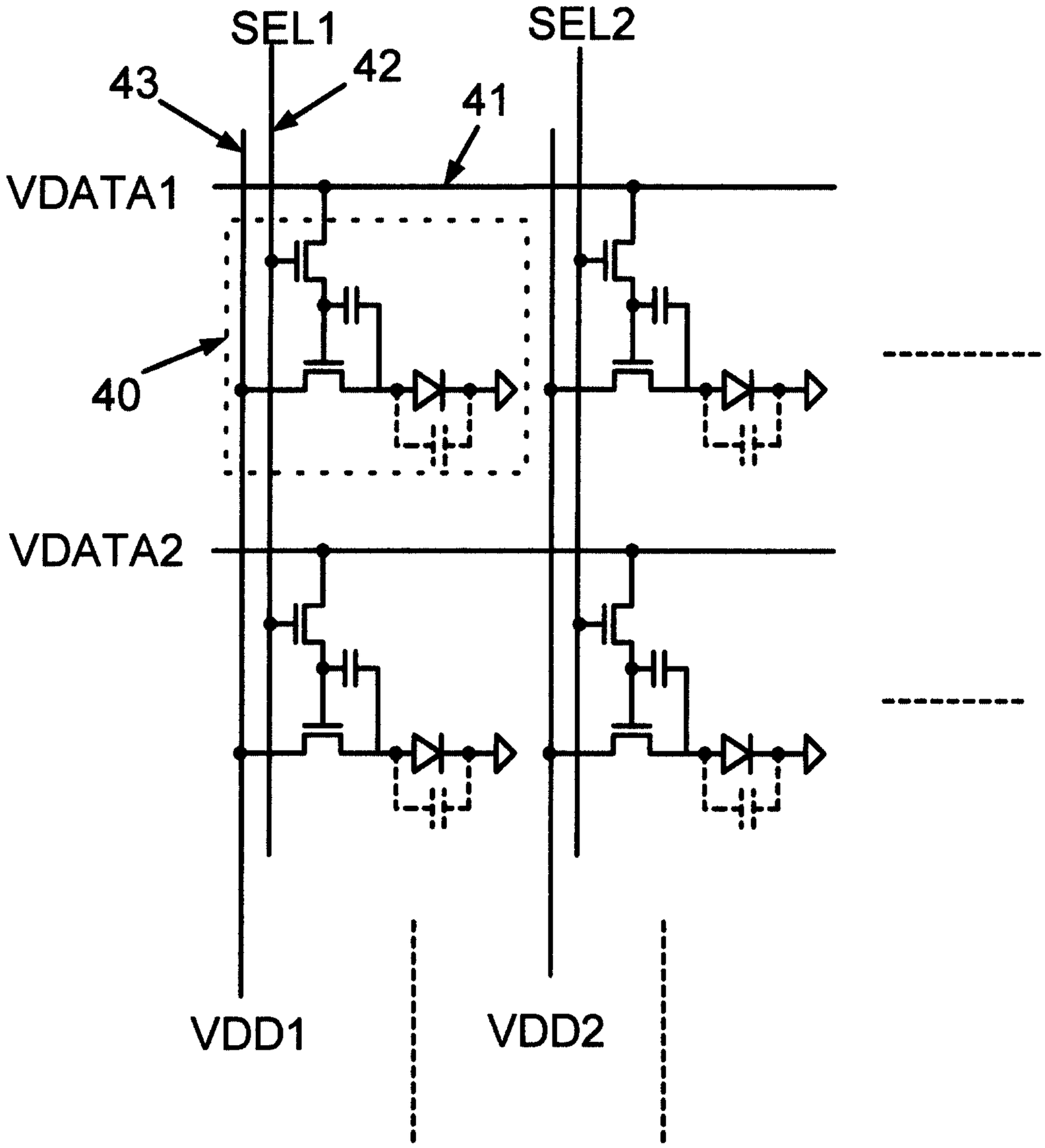


FIG.4

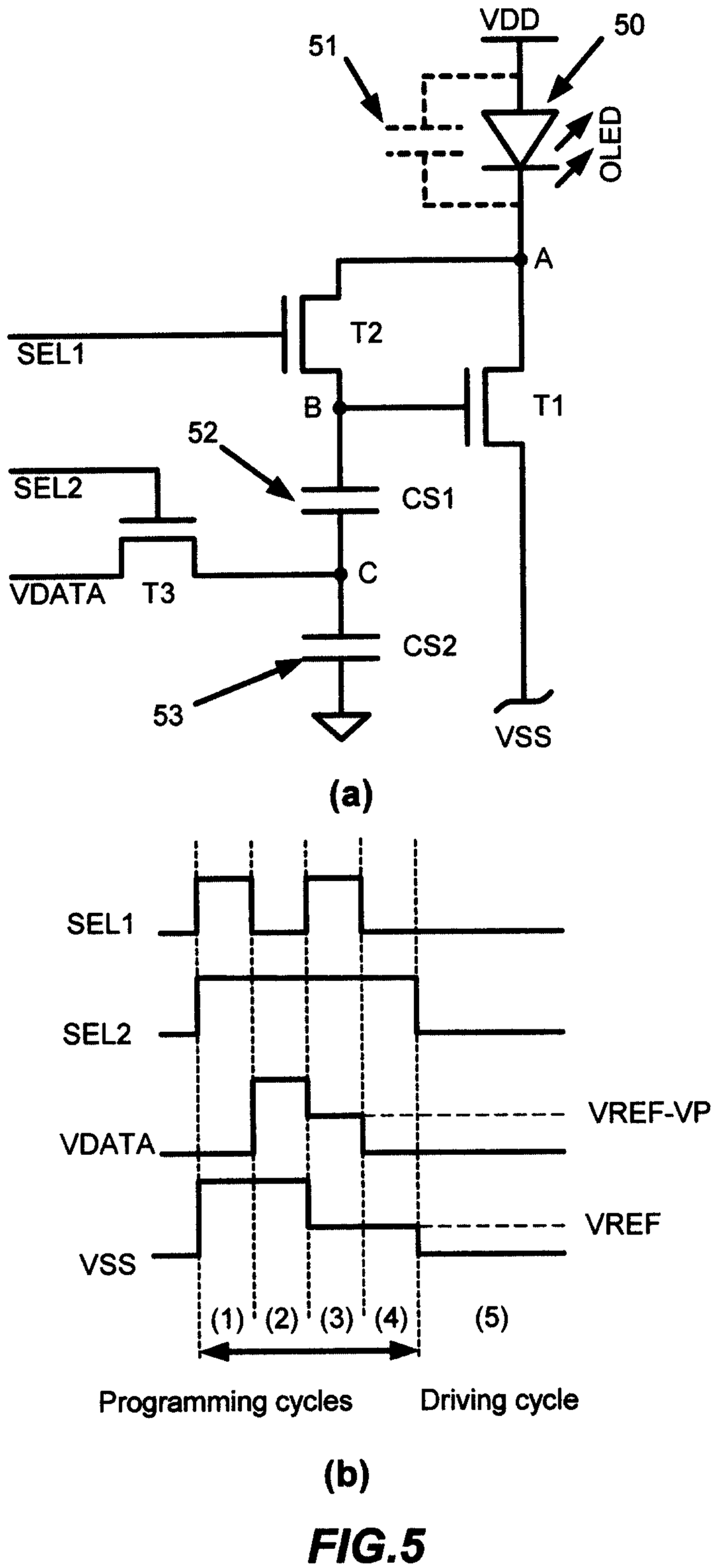
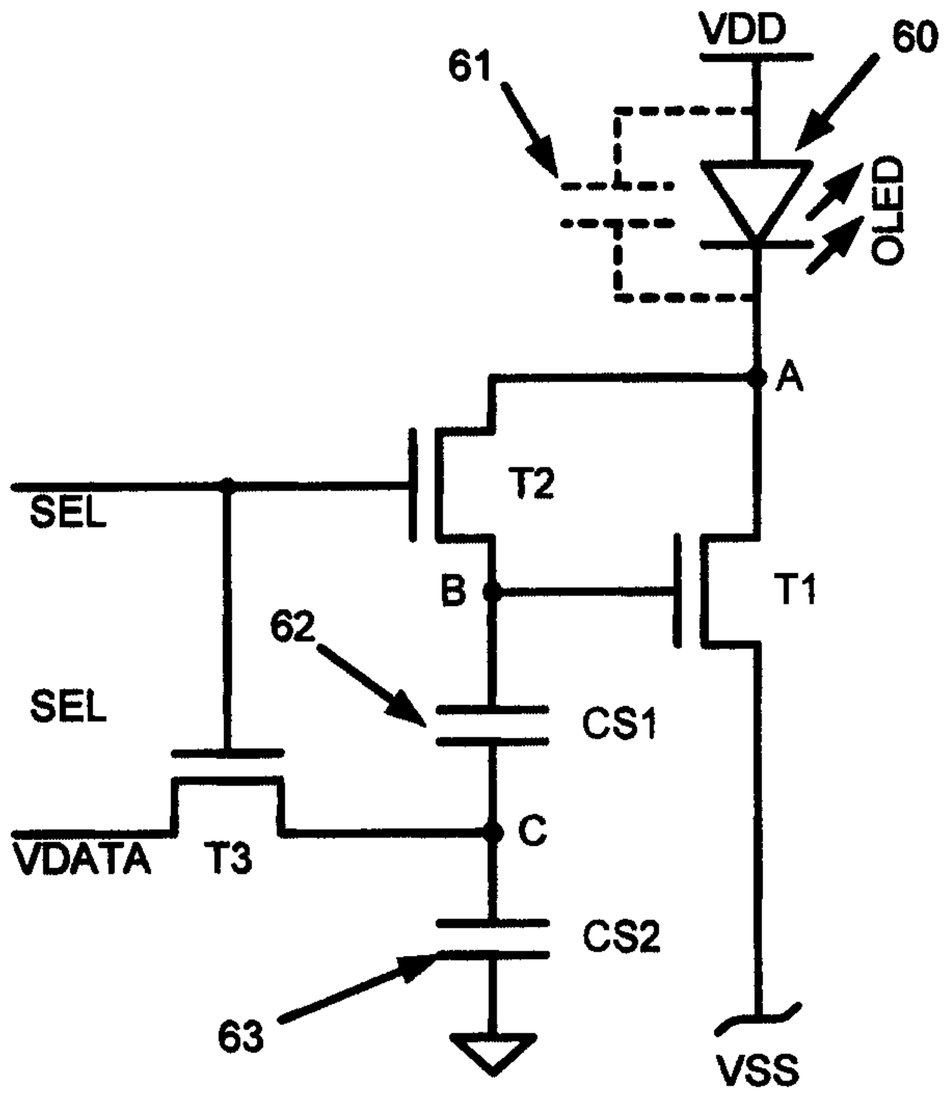
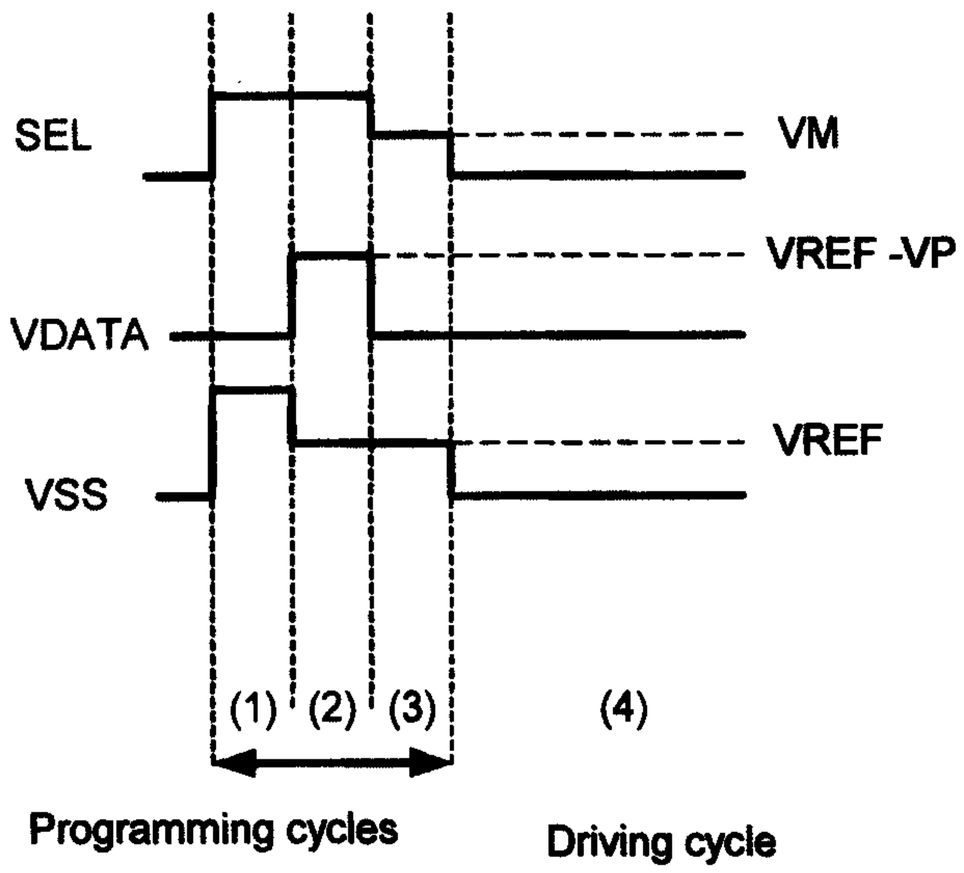

VDD
51
50
OLED
A
T2
SEL1
B
T1
52
SEL2
CS1
C
VDATA
T3
CS2
53
VSS
(a)
SEL1
SEL2
VDATA
VSS
VREF-VP
VREF
(1)
(2)
(3)
(4)
(5)
Programming cycles
Driving cycle
(b)

FIG.5

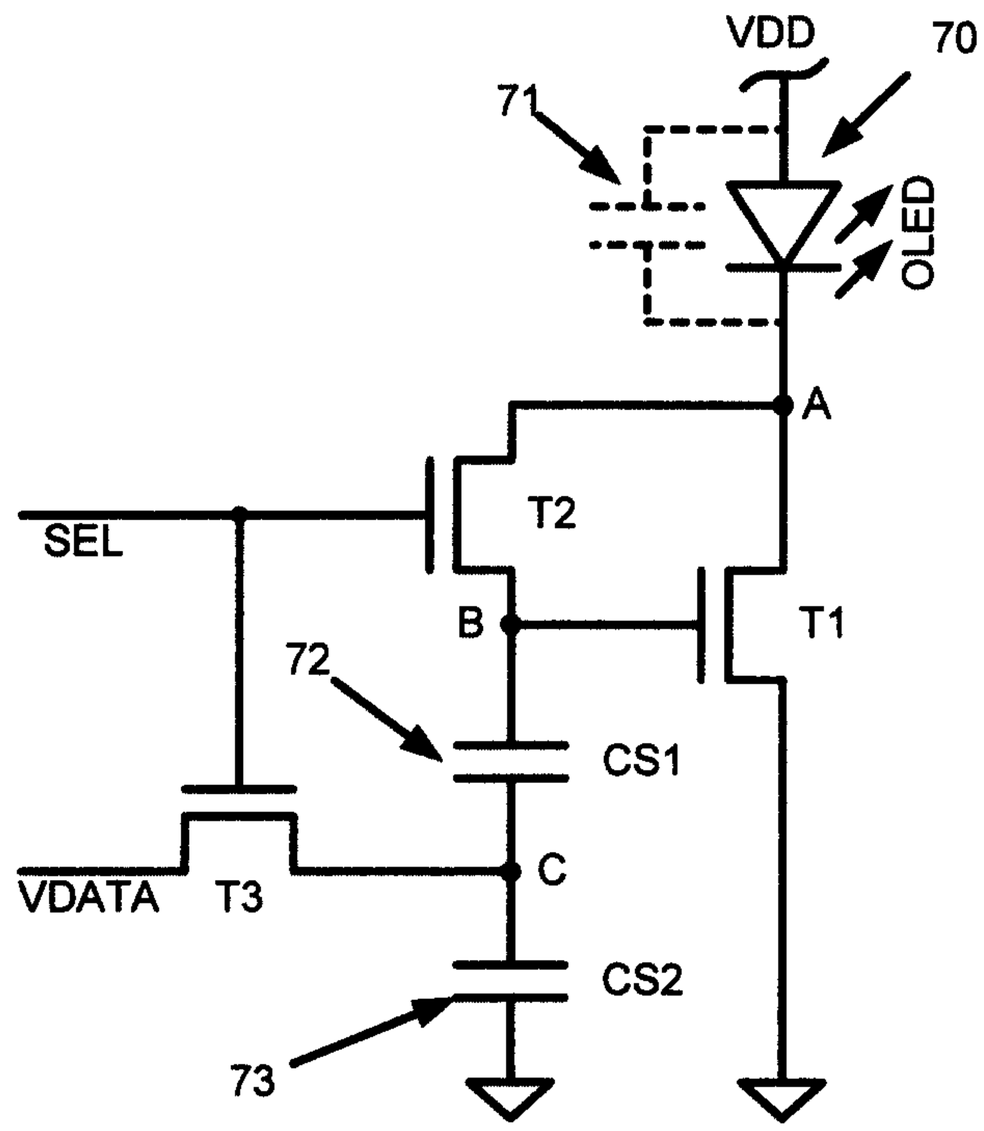

VDD
60
61
OLED
A
T2
SEL
B
T1
62
SEL
CS1
C
VDATA
T3
CS2
63
VSS

(a)

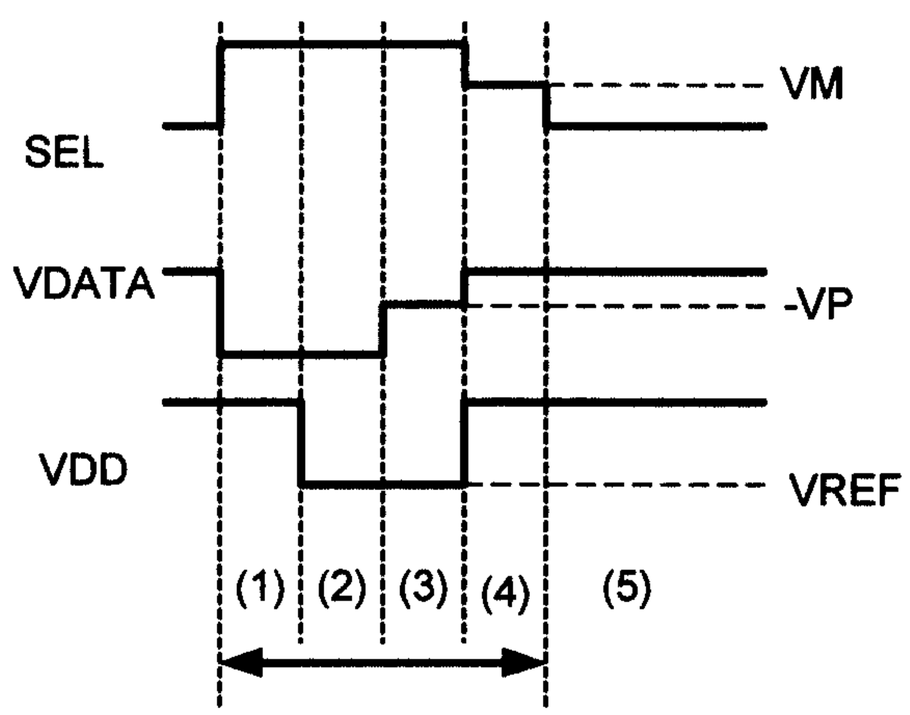

SEL
VM
VREF -VP
VDATA
VREF
VSS
(1)
(2)
(3)
(4)
Programming cycles
Driving cycle

(b)

FIG.6


VDD
70
71
OLED
A
T2
SEL
B
T1
72
CS1
C
VDATA
T3
CS2
73

(a)


SEL
VM
VDATA
-VP
VDD
VREF
(1)
(2)
(3)
(4)
(5)
Programming cycles
Driving cycle

(b)

FIG.7

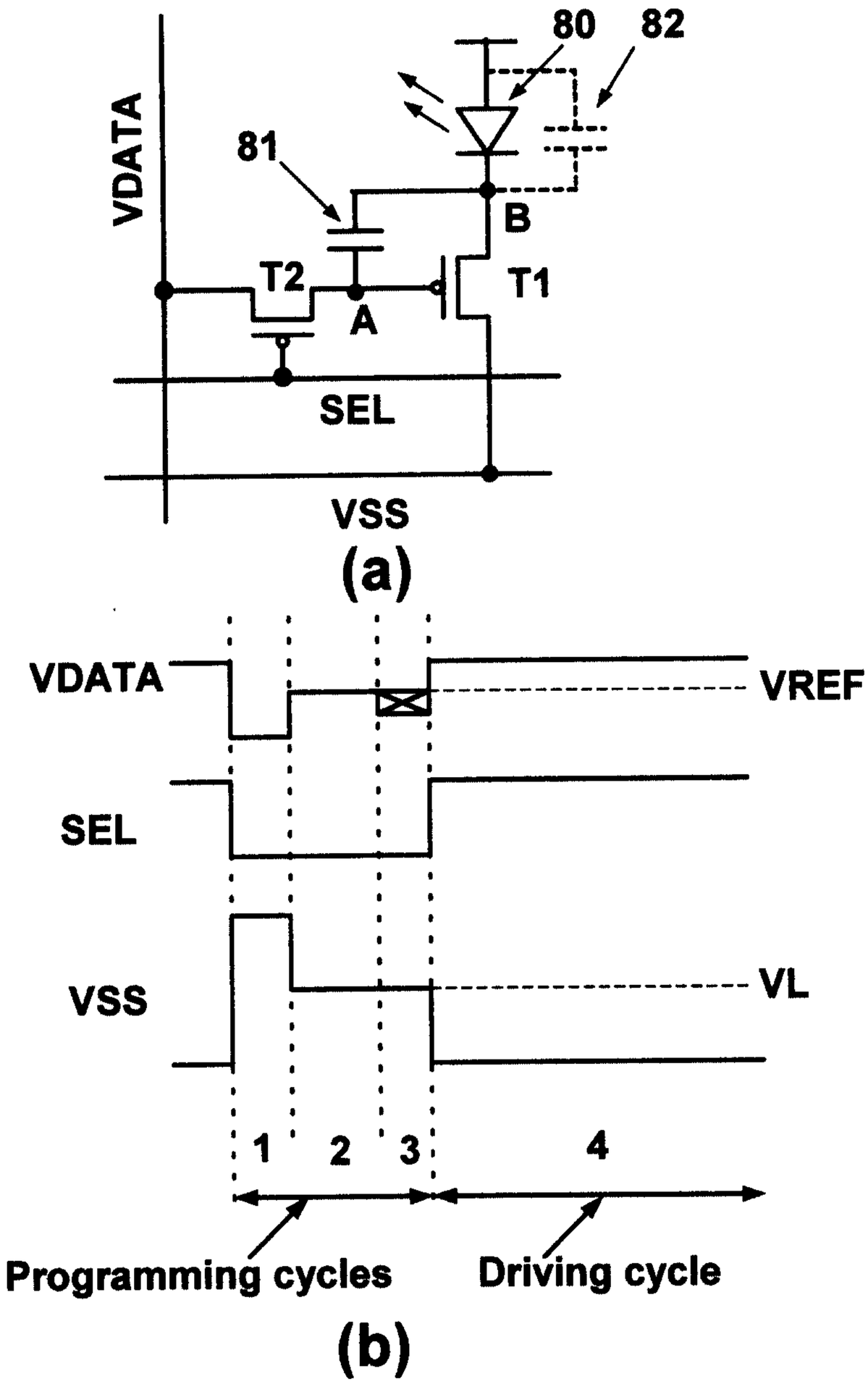

80
82
81
VDATA
B
T2
T1
A
SEL
VSS
(a)
VDATA
VREF
SEL
VSS
VL
1
2
3
4
Programming cycles
Driving cycle
(b)

FIG.8

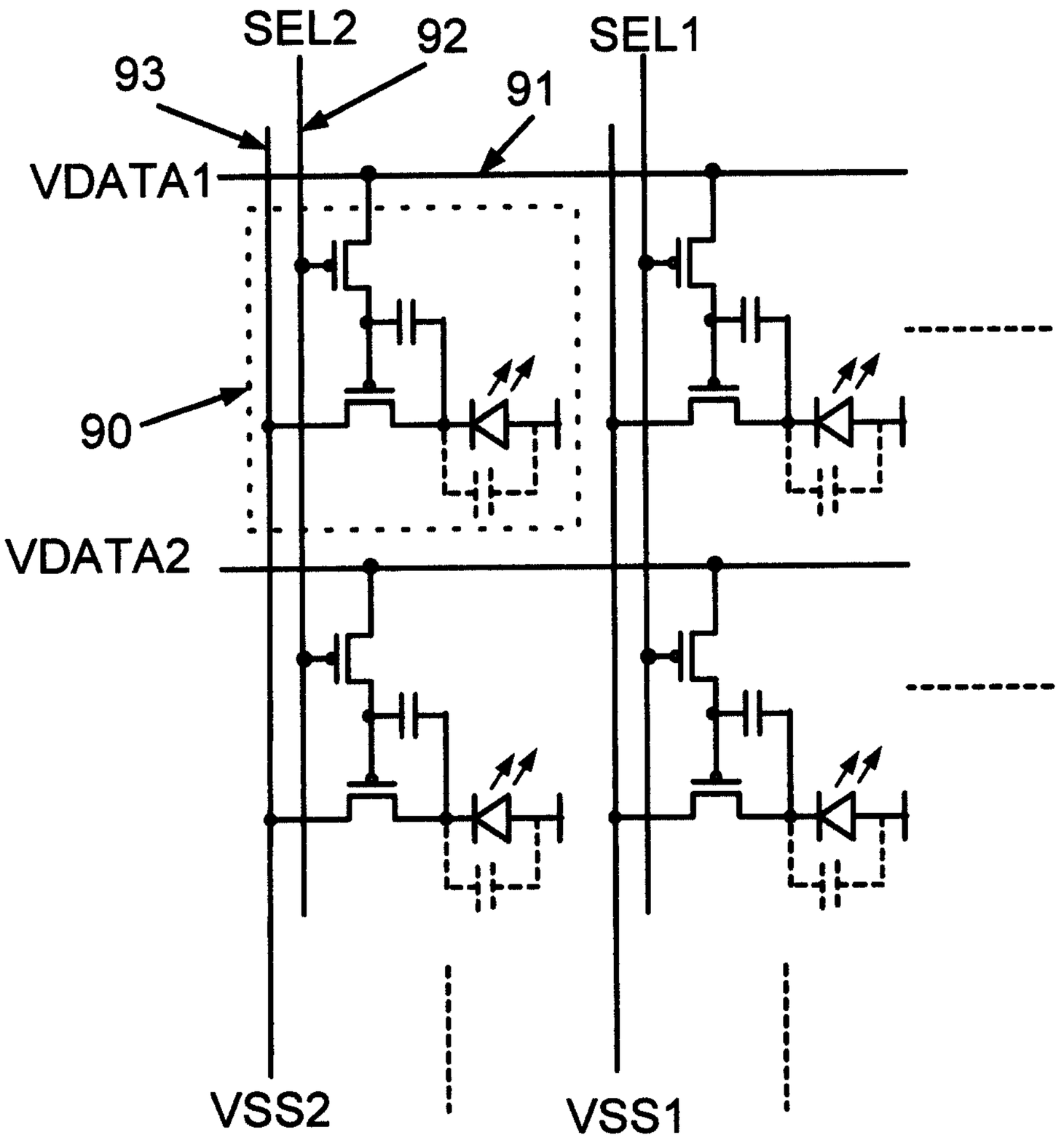


FIG. 9