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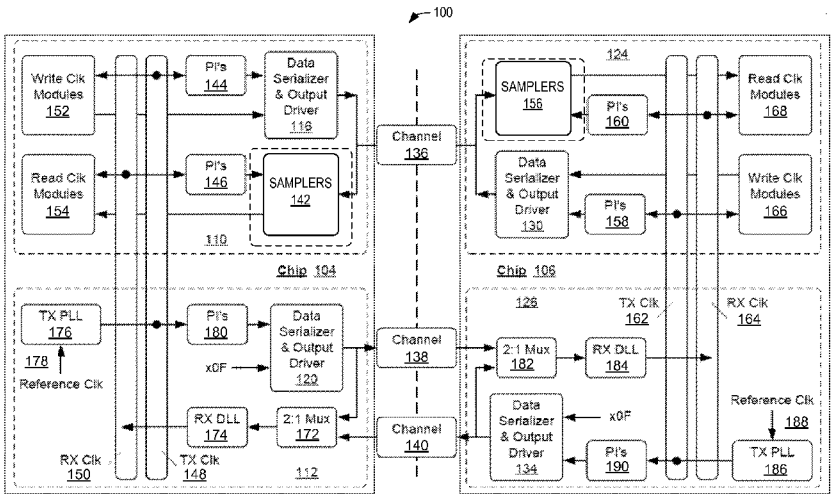

FIG. 1

(57) Abstract: Embodiments are disclosed that relate to multi-phase clock generators (174, 184) and data samplers (142, 156) for use in high speed I/O circuitry (100). One disclosed example provides a multi-phase clock generator (174) including a delay line (fig: 2 202a, b) having a plurality of delay elements, the delay line being configured to receive an input clock signal and output a plurality of output clock signals (fig. 2: CLK0-9) having different phases compared to a phase of the input clock signal. The multi-phase clock generator (fig. 2: 200) further includes a control circuit (fig. 2: 204) configured to control the delay line based at least in part upon rising edges and falling edges of one or more output clock signals (fig. 2: CLK0, 5 and TCLK0, 5) output at one or more locations along the delay line.

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MULTI-PHASE CLOCK GENERATION

BACKGROUND

[0001] High-speed I/O (input/output) data circuits for transferring large volumes of data at high speeds across short distances may suffer from various performance issues. For example, specifications for many commonly used I/O interfaces may be general purpose designs that attempt to meet a wide-range of design constraints, and are not optimal for any one design. Further, I/O data circuits that utilize packet-based communication may have large memory requirements and may come with a significant latency penalty.

SUMMARY

[0002] Embodiments are disclosed that relate to multi-phase clock generators for use in high speed I/O circuitry. One disclosed example provides a multi-phase clock generator comprising a delay line having a plurality of delay elements, the delay line being configured to receive an input clock signal and output a plurality of output clock signals having different phases compared to a phase of the input clock signal. The multi-phase clock generator further includes a control circuit configured to control the delay line based at least in part upon rising edges and falling edges of one or more output clock signals output at one or more locations along the delay line.

[0003] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter. Furthermore, the claimed subject matter is not limited to implementations that solve any or all disadvantages noted in any part of this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 shows a block diagram of an example high-speed I/O data system.

[0005] FIG. 2 shows a block diagram of an example multi-phase clock generator comprising a delay-locked loop for generating multi-phase clock signals.

[0006] FIG. 3 shows example delay elements of the multi-phase clock generator of FIG. 2.

[0007] FIG. 4 shows example inverters for inverting the output of the delay elements from the multi-phase clock generator of FIG. 2.

[0008] FIG. 5 shows an example of the phase detection and charge pump block of FIG. 2.

[0009] FIG. 6 shows an example of the input buffer and crossover control block of FIG. 2.

[0010] FIG. 7 shows an example circuit diagram for the delay element of FIG. 2.

[0011] FIG. 8 shows an example circuit diagram for the crossover block circuit of FIG. 6.

[0012] FIG. 9 shows an example circuit diagram for the crossover control block of FIG. 6.

[0013] FIG. 10 shows an example circuit diagram for the phase detection and current pump blocks of FIG. 5.

[0014] FIG. 11 shows an example circuit diagram for a phase detection circuit of FIG. 10.

DETAILED DESCRIPTION

[0015] In order to maintain synchronization while transmitting signals between electronic components (e.g., system-on-chip [SoC] components, processing cores, etc.), clock signals may be forwarded between the electronic components. In contrast with a phase locked loop (PLL) or an injection locked oscillator (ILO), a delay-locked loop (DLL) may offer enhanced jitter tracking performance and lower self-generated jitter, as a DLL propagates an input signal down a line of delay elements and does not accumulate or integrate input signal jitter over time. Thus, examples are disclosed that relate to the use of DLL circuits to generate multi-phase clock signals for a data sampler at a receiver side of an I/O system. Further, as minimization of phase spacing error in output clock signals from a DLL may be more complicated than with a PLL, examples are disclosed that measure both rising and falling signals at the output of a voltage-controlled delay line to at least reduce or minimize phase spacing error.

[0016] Prior to discussing example DLL circuitry, an example high-speed I/O data system 100 is described with reference to FIG. 1. System 100 includes a first chip 104 having a data circuit 110 and clock circuit 112, and a second chip 106 having a data circuit 124 and clock circuit 126. It is to be understood that chips 104 and 106 may represent any suitable electrical component(s), such as microchips, processing cores, and other circuit elements.

[0017] Data circuit 110 comprises a data serializer and an output driver 116, and data circuit 124 also comprises a data serializer and output driver 130. The data circuit

110 and clock circuit 112 of the first chip 104, and the data circuit 124 and clock circuit 126 of the second chip 106 form a chip-to-chip I/O data interface via data channels 136, 138, and 140.

[0018] System 100 includes data channel 136 for data communication between the data serializer and output driver 116 of the first data circuit 110 and the data serializer and output driver 130 of the second data circuit 124. Data channel 136 may be implemented as a bi-directional data channel, or may have any other suitable implementation. System 100 includes unidirectional clock data channels 138 and 140 for transmitting clock signals between the first chip 104 and the second chip 106.

[0019] The data circuit 110 of the first chip 104 also includes samplers 142, a transmitter clock phase interpolator 144, a receiver clock phase interpolator 146, a transmitter clock distribution 148, and a receiver clock distribution 150. The data circuit 110 further includes write clock modules 152 and read clock modules 154. Likewise, the data circuit 124 of the second chip 106 includes samplers 156, a transmitter clock phase interpolator 158, a receiver clock phase interpolator 160, a transmitter clock distribution 162, and a receiver clock distribution 164. The data circuit 124 further includes write clock modules 166 and read clock modules 168.

[0020] Receiver clock distribution 150 and 164 provide a multi-phase clock signal to samplers 142 and 156, via receiver clock phase interpolators 146 and 160, to enable the sampling of data signals received across channel 136. Examples of circuitry for generating multi-phase clock signals are described in more detail below.

[0021] The clock circuit 112 of the first chip 104 is configured to receive clock signals from clock circuit 126 via a multiplexer 172, and to generate, via a delay locked loop (RX DLL) 174, a multi-phase clock signal from the received clock signals. Multiplexers, such as multiplexer 172, may be used in the circuits for production test and/or for mission-mode operation. The multiplexer enables the use of the locally generated transmit clock (e.g., the clock coupled to channel 138) in place of the incoming receive clock (e.g., via channel 140).

[0022] The multi-phase clock signal generated by RX DLL 174 is then provided to samplers 142 via the receiver clock distribution 150 and the receiver clock phase interpolator 146. The illustrated clock circuit 112 also includes a data transmission clock generator comprising a transmitter phase locked loop (TX PLL) 176 receiving clock data from a reference clock 178, clock phase interpolator 180, and the above-mentioned data

serializer and output driver 120. Clock circuit 112 interfaces with clock circuit 126 via channels 138 and 140.

[0023] As described above, the data circuit 124 of the second chip 106 is symmetric to the data circuit 110 of first chip 104. Similarly, the clock circuit 126 of the second chip 106 is symmetric to the clock circuit 112 of the first chip 104. Thus, the clock circuit 126 of the second chip 106 includes a receiver clock circuit comprising a multiplexer 182 and DLL 184 to generate a multi-phase clock signal for samplers 156 via receiver clock distribution 164 and receiver clock phase interpolators 160. The clock circuit 126 also includes a transmitter clock circuit comprising a transmitter phase locked loop (PLL) 186 that receives a reference clock input 188, phase interpolators 190, and a data serializer and output driver 134 to provide a clock signal for data transmission.

[0024] As mentioned above, the use of a PLL or ILO to generate multi-phase receiver clock signals for data samplers based at least in part upon a clock signal received across channels 138 and/or 140 may suffer from difficulties in jitter tracking and other issues. In contrast, the use of DLLs 174 and 184 may offer better jitter tracking performance. However, accurately controlling phase spacing between the clock signals may be more difficult with a DLL than with a PLL or ILO.

[0025] Accordingly, FIG. 2 illustrates an example delay-locked loop (DLL) suitable for use as DLLs 174 and 184 for generating multi-phase clock signals. The depicted DLL also may be referred to herein as multi-phase clock generator 200. The multi-phase clock generator 200 includes one or more delay lines, illustrated in FIG. 2 as delay line 202a and delay line 202b. While two delay lines are shown, other implementations may utilize a different number of delay lines.

[0026] Each delay line has a plurality of delay elements, illustrated collectively for the two lines as blocks S2-S9 and NS2-NS9, and is configured to output a plurality of output clock signals having different phases compared to the phase of the input clock signal. Delay lines 202a and 202b are arranged in electrically parallel paths and comprise complementary pairs of delay elements. The clock outputs of multi-phase clock generator 200 (e.g., one or more of clk0-clk9) are provided to samplers 156 of chip 106 (e.g. one clock output per sampler) to enable incoming signals to be sampled. By producing 10 clock signals via the multi-phase clock generator, the clock signals INN and INP enter the multi-phase clock generator at $1/10^{th}$ the rate of the data signal entering the sampler.

[0027] The clock signals INN and INP as received may have crossover error, in that clock signal INN and complementary clock signal INP may not at the same time cross

over the midpoint between logic high and logic low levels. In this case, the INN and INP signals may either cross each other high (e.g., closer to a peak of signals) or low (e.g., closer to a trough of the signals). Crossover error may result from errors caused by circuit elements in the clock transmitter from which the clock signals INN and INP are received, and may impact the timing between output clock signals generated by the multi-phase clock generator 200. As such, the clock signals INN and INP are first provided to an input buffer and crossover control block/module 204 configured to reduce the crossover error. Adjusted clock signals INNX and INPX are then output to the delay line(s) and/or the delay elements electrically connected to the delay lines.

[0028] The input buffer and crossover control block 204 may adjust the received complementary clock signals INN and INP in any suitable manner. For example, the depicted input buffer and crossover control block 204 adjusts the clock signals INN and INP based at least in part upon feedback received from the first two blocks electrically connected to each delay line (e.g., fbclk0, nfbclk1, fbclk1, and nfbclk0). In other implementations, other blocks (e.g., delay elements in the delay lines, such as one or more of blocks S2-S9 and/or NS2-NS9) may be utilized for feedback in addition to and/or as an alternative to one or more of the above-described blocks. These feedback signals (e.g., fbclk0, nfbclk0, fbclk1, and nfbclk1) are filtered and converted to DC voltages in the crossover control block such that only the information for influencing crossover control (e.g., the crossover point of fbclk0 and nfbclk0 and the crossover point of fbclk1 and nfbclk1) is maintained, as described in more detail below with respect to FIGS. 6 and 9. Input buffer and crossover control block 204 adjusts the crossover error of feedback signals fbclk0 and nfbclk0 such that it is substantially equal to the crossover error of feedback signals fbclk1 and nfbclk1, and this in turn leads to a crossover error of adjusted clock signals INNX and INPX that is substantially equal to zero in this embodiment.

[0029] Further control of the outputs of the delay lines 202a and 202b is provided by the phase detector and charge pump blocks 206a and 206b, which control the delay lines based at least in part upon the measured rising and falling edges of one or more output clock signals output at one or more locations along the delay lines. The phase detector and charge pump blocks receive signals from delay elements both earlier in the delay line (e.g., NS2 and S2) and later in the delay line (e.g., S7 and NS7).

[0030] In the depicted example, phase detector and charge pump 206a measures the relative phase of signals tclk0 (terminal clock 0, output from delay element S7) and clk0 (clock 0, output from delay element NS2) and sets a voltage proportional to this

relative phase on main control signal MAIN CTRL. Negative feedback enables-the delay-locked loop to lock such that the tclk0 and clk0 signals align and have substantially equal phase. Similarly, phase detector and charge pump 206b measures the relative phase of signals tclk5 and clk5 and sets a voltage proportional to this relative phase on auxiliary control signal AUX CTRL. Negative feedback enables the delay-locked loop to lock such that the tclk5 and clk5 signals align and have substantially equal phase. In this way, multi-phase clock generator 200 maintains phase accuracy of both rising and falling edges.

[0031] As described in more detail below with respect to FIG. 6, the main control and auxiliary control signals are provided to each of the delay elements to control a respective subset of gates of the transistors in the delay elements. In some examples, main control may be connected to more transistors than auxiliary control. In other examples, main control may be connected to a same number of transistors in the delay elements as the auxiliary control, or to a lesser number of transistors.

[0032] The delay lines 202a and 202b are configured such that the relative phases of the clock signals in delay line 202a and the corresponding clock signals in delay line 202b are substantially similar. The phase detector and charge pumps 206a and 206b thus are utilized to detect and substantially correct errors in the relative phases of tclk0 and clk0, and of tclk5 and clk5.

[0033] In some examples, complementary delay elements in delay line 202a and delay line 202b may be cross-coupled, as described in more detail with respect to FIG. 3. In such examples, the main control signal and auxiliary control signal may be connected respectively to delay line 202a and delay line 202b, rather than connecting the main control signal to both delay lines and the auxiliary control signal to both delay lines. In other examples, the main control and auxiliary control signals each may be provided to both delay line 202a and delay line 202b, whether or not complementary delay elements are cross-coupled. Although illustrated as two blocks, it is to be understood that the phase detector and charge pump blocks 206a and 206b may be implemented as a single circuit in some examples.

[0034] FIG. 3 shows an example schematic 300 for delay elements S0-9 and NS0-9 of the multi-phase clock generator 200 of FIG. 2. Block 302a represents the delay elements having even NS labels in FIG. 2 (e.g., NS0, NS2, NS4, NS6, and NS8), and block 302b represents the delay elements having even S labels (e.g., S0, S2, S4, S6, and S8). Further, block 302c represents the delay elements having odd S labels (e.g., S1, S3, S5, S7, and S9), while block 302d represents the delay elements having odd NS labels

(e.g., NS1, NS3, NS5, NS7, and NS9). As illustrated in FIG. 2, each delay element receives input either from the input buffer and crossover control block 204 (e.g., as shown for NS0 and S0) or from an immediately prior delay element. Accordingly, the inputs of each even delay element reflected at the NIN input port are associated with a corresponding output at the OUT output port (e.g., INPX is the input for the delay element that outputs NS0, S1 is the input for the delay element that outputs NS2, etc.).

[0035] As described above, in some examples, each delay element may receive input of the main control signal and auxiliary control signal. Mainp (or ctrlp0) controls an output rising delay, while mainn (or ctrln0) controls an output falling delay. Similarly, auxp (or ctrlp5) controls an output rising delay, while auxn (or ctrln5) controls an output falling delay.

[0036] As further illustrated, the outputs of each even delay element from delay line 202a are coupled to the outputs of each even delay element from delay line 202b via the XNIN input on each delay element. Similarly, the outputs of each odd delay element from delay line 202a are coupled to the outputs of each odd delay element from delay line 202b via the corresponding XNIN input on each delay element. This provides for the cross-coupling of the two delay lines, as mentioned above with respect to FIG. 2.

[0037] FIG. 4 illustrates an example schematic diagram 400 for the inverters connected to the clock output of each delay element of FIG. 2. Inverter IN_LV1 represents the inverters connected to NS0 and NS1, which respectively output fbclk0 and fbclk1 for NS0 and NS1. Similar indicia designate the locations of the other inverters. For example, inverter INV_LV2 corresponds to the inverters connected to S2-S6 and NS2-NS6, which output the clock signals clk0-clk9 for controlling the data samplers.

[0038] FIGS. 5 and 6 illustrate example schematic diagrams for the phase detector and charge pump 206a/206b of FIG. 2 (PDQP circuit 500 in FIG. 5) and the input buffer and crossover control block 204 of FIG. 2 (XOVER CONTROL circuit 602 and XOVER circuits 604a and 604b in FIG. 6). The PDQP 500 receives inputs from tclk0, clk0, tclk5, and clk5 (as described above with respect to FIG. 2) and output control signals ctrlp0, ctrln0, ctrlp5, and ctrln5 utilized as the main control signals and auxiliary control signals, respectively.

[0039] The XOVER CONTROL circuit 602 of Fig. 6 receives feedback clocks and complementary feedback clocks (e.g., fbclk0, fbclk1, nfbclk0, and nfbclk1) and outputs an XOVER output signal indicating relative crossover points of the feedback clocks to control the XOVER circuits 604a and 604b. The XOVER circuit receives respective

complementary transmitted clock input signals as input (e.g., XOVER 604a receives the INN signal illustrated in FIG. 2, while XOVER 604b receives the complementary INP signal illustrated in FIG. 2), and outputs adjusted clock signals INNX or INPX based on control signals received from PDQP (e.g., ctrlp0/mainp and ctrln0/mainn) and XOVER CONTROL (e.g., XOVER). As illustrated, the outputs of each XOVER circuit are coupled to the other XOVER circuit via an XNIN input to provide cross-coupling between delay lines.

[0040] FIG. 7 shows an example circuit diagram for a voltage-controlled delay element 700, such as those of FIGS. 2 and 3. For example, delay element 700 may correspond to any of delay elements 302a-302d of FIG. 3. NIN represents the output of input buffer and crossover control block 204 of FIG. 2, and XNIN provides the cross-coupling from delay elements of another delay line. The diagram illustrated in FIG. 7 is an example of a current-starved inverter. In some examples, transistors that are connected to XNIN may be weaker than other transistors.

[0041] As shown, four transistors (MP2, MP13, MN2, and MN13) have a gate coupled to a main control input (e.g., mainp or mainn), compared to two transistors (MP11 and MN11) that have a gate coupled to an auxiliary control input. Accordingly, the main control input provides approximately two thirds of the control, while the auxiliary control input provides approximately one third of the control in this example. It is to be understood that any suitable ratio of main control to auxiliary control may be utilized without departing from the scope of this disclosure.

[0042] FIG. 8 illustrates an example circuit diagram of an XOVER circuit 800, such as XOVER circuit 604a/604b of FIG. 6. Similarly to the delay element illustrated in FIG. 7, the XOVER circuit performs similarly to a current-starved inverter. Mainp controls the output rising delay, mainn controls the output falling delay, and the XOVER input (e.g., to transistor MP3) controls both delays in a complementary fashion.

[0043] FIG. 9 illustrates an example circuit diagram of XOVER CONTROL circuit 602 of FIG. 6. As illustrated, the four transistors in lower left corner (e.g., MFETs MN1-4) operate similarly to an XOR gate. The eight MFETs in the lower left corner of the figure (e.g., MFETs MN1-4 and MN7 and MN10-12) are utilized to measure the crossover points of the feedback clocks (e.g., to determine if the clocks crossover high/crossover low). If the fbclk0 and nfbclk0 cross over high, fbclk1 and nfbclk1 will crossover low. This control loop adjusts the crossover points until the crossover point of fbclk0 and nfbclk0 is substantially the same as the crossover point fbclk1 and nfbclk1. The four

MFETs on the left (MN1-4) are fbclk/nfbclk1s and the four MFETs on the right (MN7 and MN10-12) are fbclk/nfbclk0s. When the crossover points of each set of feedback clocks are substantially equal, the aggregate pull-down current of the four corresponding transistors (e.g., MN1-4 for fbclk1/nfbclk1 and MN7/MN10-12 for fbclk0/nfbclk0) is substantially equal to the aggregate pull-down current of the other four transistors. When the aggregate pull-down currents are substantially equal, the voltage at FBMX is steady state (e.g., at stable operating point, neither rising nor falling). FBMX is coupled to gate TXG_LV1 and amplified via the inverting amplifier (with feedback compensation) provided by the components to the right of TXG_LV1 in FIG. 9, resulting in the inverted and amplified FBMX being output as the XOVER output signal. In this way, t the crossover control module varies a voltage output as the first signal crossover point deviates from the second signal crossover point, and provides a steady-state voltage output when the first signal crossover point is substantially equal to the second signal crossover point.

[0044] Referring to FIG. 8, in an example scenario, when XOVER is a high voltage, MN3 is stronger and MP3 is weaker. In this case, the output of the input buffer and crossover control block OUT falls faster than it rises. Accordingly, the signals provided delay elements NS0 and S0 crossover low, and outputs from NS0 and S0 (e.g., fbclk0 and nfbclk0 of FIG. 2) crossover high. Since the outputs of NS0 and S0 are inverted to formfbclk0 and nfbclk0, the crossover point of these signals is low. If the crossover point of fbclk0 and nfbclk0is low, a low pull down current exists on FBMX, causing FBMX to pull up, going high. Due to the inverting amplifier illustrated in FIG. 9, FBMX will be inverted and output as XOVER at a low voltage. Accordingly, this feedback enables the response to an XOVER output that is high to pull down the XOVER output.

[0045] FIG. 10 illustrates an example circuit diagram for phase detection and charge pump circuit PDQP 500 of FIG. 5. PDQP includes RXPD circuits 1002a and 1002b, which include phase detectors illustrated in more detail in FIG. 11. The RXPD circuits compare the relative edge positioning of tclk and clk signals (e.g., RXPD 1002a compares tclk0 and clk0, while RXPD 1002b compares tclk5 and clk5) and output a voltage to serve as a delay signal. The output voltage is high if the respective terminal clock (e.g., tclk0/tclk5) leads the clock signal (e.g., clk0/clk5), and low if the terminal clock signal trails the clock signal. The phase detection charge pump, illustrated above the RXPD circuits, generates an output current depending on whether the delay signals are

high or low. For example, the delay signals may be input to switches MP28 and MN29, which are enabled on or off depending upon whether the delay is high or low. The switches selectively short the sources of MP30/MN27, respectively, which are biased such that, when the sources are grounded, the transistors conduct a small amount of current onto or off of the ctrlp0 node. Further, a filter capacitor (MCAP1) may be provided on the output of the charge pump. Ctrlp0 may go to mainn or auxp based on whether the example circuit is utilized in the phase detection and charge pump block 206a of FIG. 2 or the phase detection and charge pump block 206b of FIG. 2 (e.g., utilized in the main or auxiliary control path/block).

[0046] A current mirror formed by MP5/MN1 is utilized to generate ctrln0. Ctrln0 is provided to either mainn or auxn, depending on the block in which the circuit is utilized. The generation of ctrlp5 and ctrln5 is performed similarly to ctrlp0 and ctrln0, with ctrlp5 and ctrln5 providing the auxiliary control signal and ctrlp0/ctrln0 providing the main control signal.

[0047] FIG. 11 illustrates an example circuit diagram of a phase detector RXPD 1100. Phase detector 1100 is utilized in the RXPD circuit 1002a or 1002b of FIG. 10 to generate a logic signal indicating whether the edges of the associated tclk/clk signals are early or late.

[0048] Another example provides a device comprising a delay line having a plurality of delay elements, the delay line being configured to receive an input clock signal and output to a sampler circuit a plurality of output clock signals having different phases compared to a phase of the input clock signal, and a control circuit configured to control the delay line based at least in part upon rising edges and falling edges of one or more output clock signals output at one or more locations along the delay line. In such an example, the delay line may be a first delay line, the plurality of delay elements may be a first plurality of delay elements, and the plurality of output clock signals may be a first plurality of output clock signals, and the multi-phase clock generator may additionally or alternatively comprise a second delay line having a second plurality of delay elements, the second delay line being configured to receive a complement of the input clock signal and to output a second plurality of output clock signals. In such an example, the first delay line and the second delay line may additionally or alternatively be arranged in electrically parallel paths and may comprise complementary pairs of delay elements. In such an example, each complementary pair of delay elements may additionally or alternatively comprise two electrically parallel delay elements communicatively coupled to one another.

In such an example, the device may additionally or alternatively include a crossover control module communicatively coupled to the delay line, the crossover control module being configured to receive clock signals from a clock signal source, receive output signals from a first delay element and a second delay element of the plurality of delay elements, the second delay element being complementary to the first delay element, utilize a signal crossover point for the output signals from the first delay element and the second delay element to determine a crossover error in the complementary clock input signals, and generate the input clock signal for the delay line using the crossover error. In such an example, the signal crossover point may be a first signal crossover point, and the crossover control module may additionally or alternatively be configured to utilize a second signal crossover point for output signals received from a third delay element and a fourth delay element of the plurality of delay elements, the fourth delay element being complementary to the third delay element. In such an example, the crossover control module may additionally or alternatively be configured to vary a control-signal voltage while the first signal crossover point is different from the second signal crossover point and to provide a steady-state control-signal voltage when the first signal crossover point is substantially equal to the second signal crossover point. In such an example, the control circuit may additionally or alternatively be configured to control the delay line based at least in part upon rising and falling edges of delay line output clock signals. In such an example, the device may additionally or alternatively be configured to provide the plurality of output clock signals to a sampler circuit. Any or all of the above-described examples may be combined in any suitable manner in various implementations.

[0049] Another example provides a device comprising a delay line having a plurality of delay elements, and a module electrically coupled to the plurality of delay elements and configured to receive complementary clock input signals from a clock signal source, receive a first output signal and a second output signal from, respectively, a first delay element and a second delay element of the plurality of delay elements, utilize a signal crossover point of the first output signal and the second output signal to determine a crossover error in the complementary clock input signals, and output adjusted complementary clock input signals to the delay line using the crossover error. In such an example, the delay line may be a first delay line, the plurality of delay elements may be a first plurality of delay elements, and the plurality of output clock signals may be a first plurality of output clock signals, and the multi-phase clock generator may additionally or alternatively comprise a second delay line having a second plurality of delay elements

configured to receive a complement of the input clock signal and to output a second plurality of output clock signals. In such an example, the first delay line and the second delay line alternatively or additionally may be arranged in electrically parallel paths and comprise complementary pairs of delay elements. In such an example, the complementary pair of delay elements alternatively or additionally may be electrically coupled to one another. In such an example, the control circuit alternatively or additionally may be configured to control the first delay line and the second delay line based at least in part upon rising and falling edges of one or more output clock signals output at one or more locations along the first delay line and the second delay line. In such an example, the control circuit may alternatively or additionally be configured to output a first control signal for a first subset of electrical components in each delay element and a second control signal for a second subset of electrical components in each delay element. In such an example, the first control signal may alternatively or additionally be provided to a greater number of electrical components in each delay element than the second control signal. In such an example, the one or more locations along the first delay line and the second delay line may alternatively or additionally comprise one or more pairs of electrically parallel delay elements arranged at different locations along the first delay line and the second delay line. In such an example, the signal crossover point may be a first signal crossover point, and the crossover control module may alternatively or additionally be configured to utilize a second signal crossover point for output signals received from a third delay element and a fourth delay element of the plurality of delay elements. In such an example, the crossover control module may alternatively or additionally be configured to generate excess current to vary a control-signal voltage while the first signal crossover point is different from the second signal crossover point and to provide a steady-state control-signal voltage when the first signal crossover point is substantially equal to the second signal crossover point. Any or all of the above-described examples may be combined in any suitable manner in various implementations.

[0050] Another example provides a multi-phase clock generator comprising electrically parallel first and second delay lines having a plurality of complementary delay elements, an input buffer and crossover control module configured to receive a first source clock input signal and a second source clock input signal from a clock signal source, to receive feedback signals from the electrically parallel first and second delay lines, and to output to the electrically parallel first and second delay lines complementary clock input signals by determining crossover error in the first source clock input signal and the second

complementary source input clock signal based at least in part upon the feedback signals received from the electrically parallel first and second delay lines, and a control circuit configured to control the delay line based at least in part upon rising and falling edges of one or more output clock signals output at one or more locations along the electrically parallel first and second delay lines. Any or all of the above-described elements may be combined in any suitable manner in various implementations.

[0051] The above-described examples may be used in combination with sampler circuitry to help enable the samplers to be clocked such that the relative phases are substantially equally distributed across 360 degrees, as the above-described example multi-phase clock generators may provide output signals having increased phase accuracy, and decreased jitter, insertion delay, and crossover error relative to other clock generators (e.g., clock generators using PLLs).

[0052] It will be understood that the configurations and/or approaches described herein are exemplary in nature, and that these specific embodiments or examples are not to be considered in a limiting sense, because numerous variations are possible. The specific routines or methods described herein may represent one or more of any number of processing strategies. As such, various acts illustrated and/or described may be performed in the sequence illustrated and/or described, in other sequences, in parallel, or omitted. Likewise, the order of the above-described processes may be changed.

[0053] The subject matter of the present disclosure includes all novel and non-obvious combinations and sub-combinations of the various processes, systems and configurations, and other features, functions, acts, and/or properties disclosed herein, as well as any and all equivalents thereof.

CLAIMS

1. A device, comprising:

a first delay line having a plurality of delay elements, the delay line being configured to receive a first input clock signal and output to a sampler circuit a first plurality of output clock signals having different phases compared to a phase of the first input clock signal;

a second delay line having a plurality of delay elements, the delay line being configured to receive a second input clock signal and output to a sampler circuit a second plurality of output clock signals having different phases compared to a phase of the second input clock signal; and

a control circuit configured to control the delay lines based at least in part upon a rising or falling edge of at least one output clock signal of the first plurality of output clocks signals and at least one output clock signal of the second plurality of output clock signals.

2. The device of claim 1, wherein the second input clock signal is a complement of the first input clock signal.

3. The device of claim 2, wherein the first delay line and the second delay line are arranged in electrically parallel paths and comprise complementary pairs of delay elements.

4. The device of claim 3, wherein each complementary pair of delay elements comprises two electrically parallel delay elements communicatively coupled to one another.

5. The device of any one of claims 1-4, further comprising a crossover control module communicatively coupled to the delay line, the crossover control module being configured to

receive clock signals from a clock signal source,

receive output signals from a first delay element and a second delay element of the plurality of delay elements, the second delay element being complementary to the first delay element,

utilize a signal crossover point for the output signals from the first delay element and the second delay element to determine a crossover error in the complementary clock input signals and thereby

generate the input clock signal for the delay line using the crossover error.

6. The device of claim 5, wherein the signal crossover point is a first signal crossover point, and wherein the crossover control module is further configured to utilize a second signal crossover point for output signals received from a third delay element and a fourth delay element of the plurality of delay elements, the fourth delay element being complementary to the third delay element.

7. The device of claim 6, wherein the crossover control module is configured to vary a control-signal voltage while the first signal crossover point is different from the second signal crossover point and to provide a steady-state control-signal voltage when the first signal crossover point is substantially equal to the second signal crossover point.

8. The device of any one of claims 1-7, wherein the control circuit is configured to control the delay line based at least in part upon rising and falling edges of delay line output clock signals.

9. The device of any one of claims 1-8, wherein the device is configured to provide the plurality of output clock signals to a sampler circuit.

10. The device of any one of claims 1-9, wherein the control circuit is configured to output a first control signal for a first subset of electrical components in each delay element and a second control signal for a second subset of electrical components in each delay element.

11. The device of claim 10, wherein the first control signal is provided to a greater number of electrical components in each delay element than the second control signal.

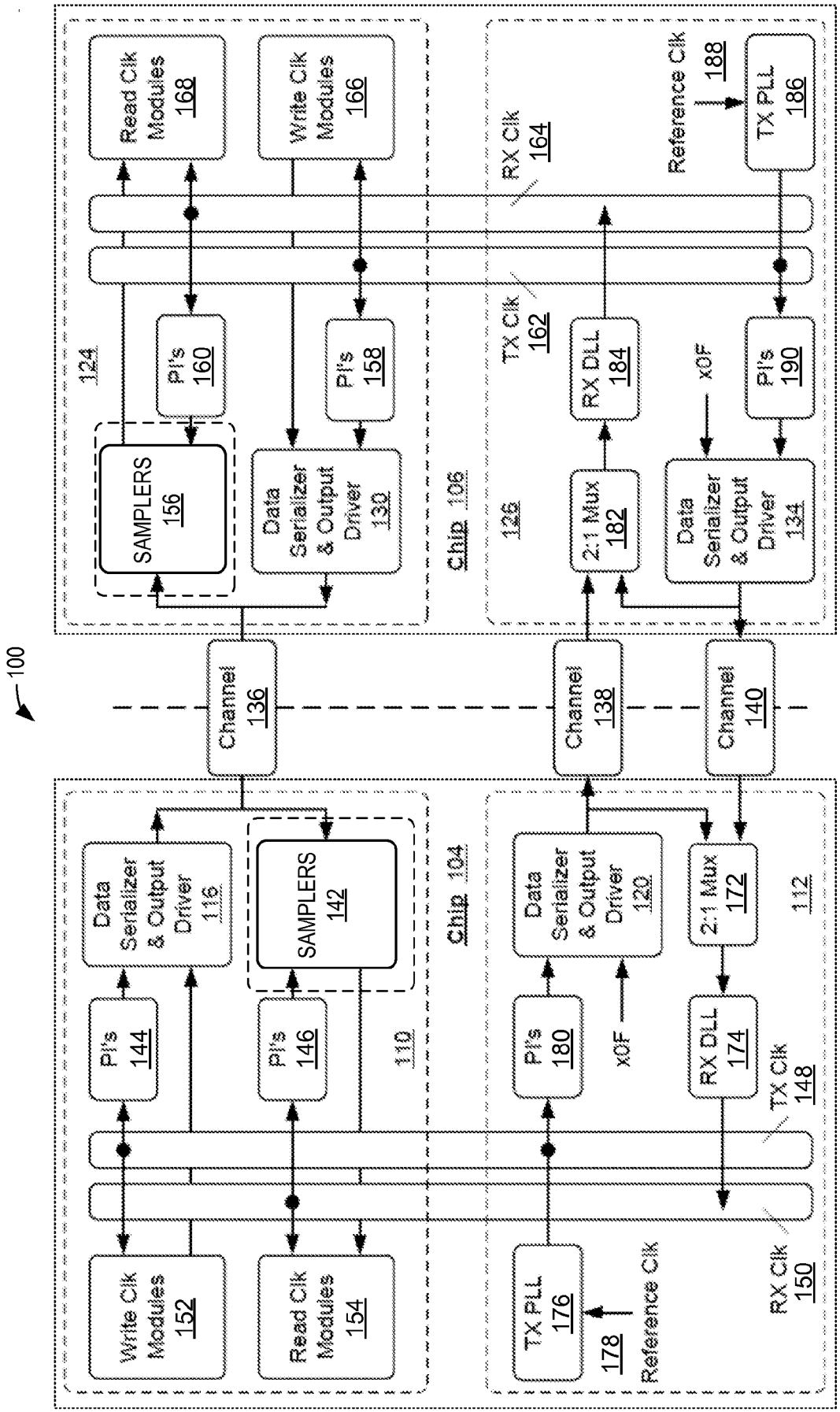

100
Chip 104
Chip 106
110
112
124
126
Read Clk Modules 168
Write Clk Modules 166
Reference Clk 188
TX PLL 186
RX Clk 164
TX Clk 162
PI's 160
PI's 158
RX DLL 184
xOF
PI's 190
SAMPLERS 156
Data Serializer & Output Driver 130
2:1 Mux 182
Data Serializer & Output Driver 134
Channel 136
Channel 138
Channel 140
Data Serializer & Output Driver 116
SAMPLERS 142
PI's 144
PI's 146
Data Serializer & Output Driver 120
2:1 Mux 172
PI's 180
RX DLL 174
TX Clk 148
Write Clk Modules 152
Read Clk Modules 154
TX PLL 176
178
Reference Clk
RX Clk 150

FIG. 1

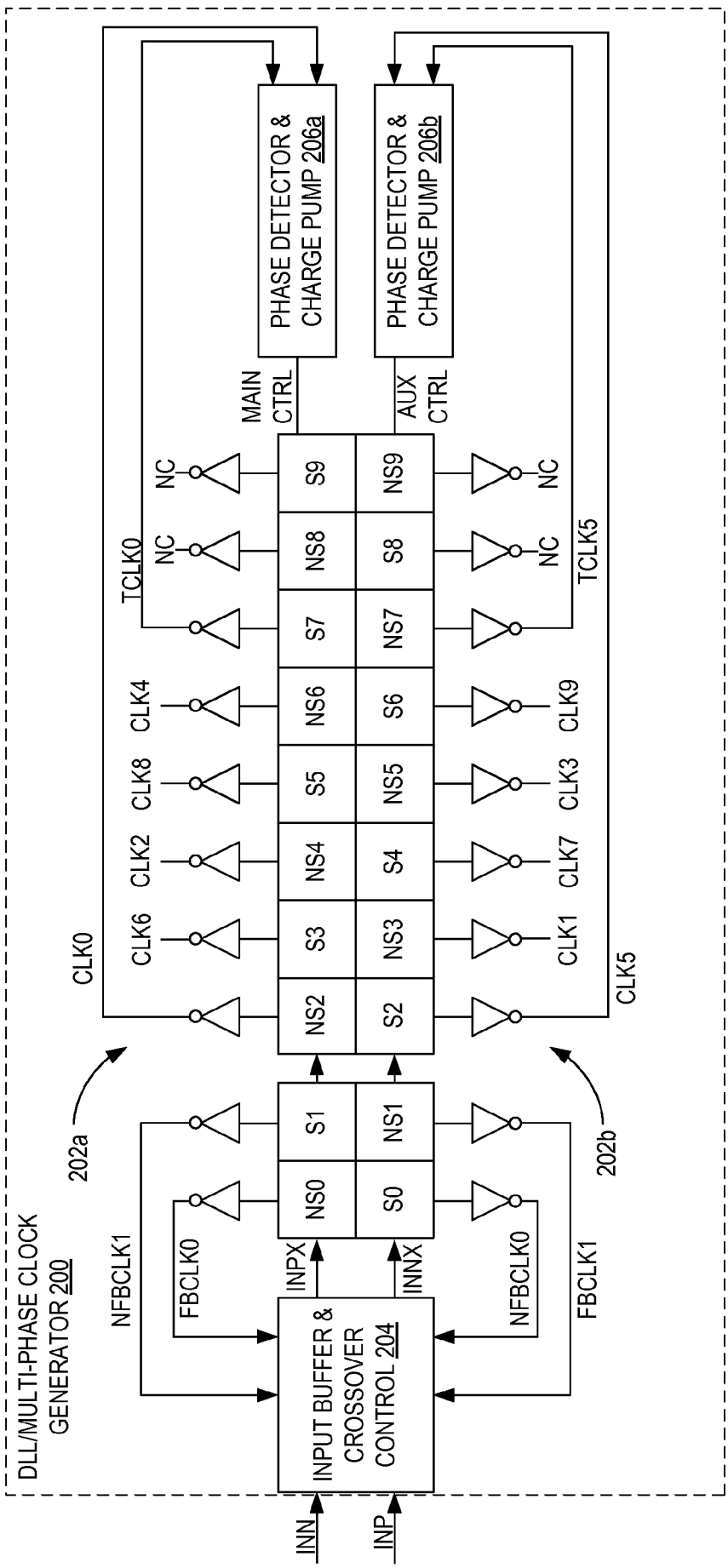

DLL/MULTI-PHASE CLOCK GENERATOR 200
INPUT BUFFER & CROSSOVER CONTROL 204
INN
INP
INPX
INNX
FBCLK0
NFBCLK1
NFBCLK0
FBCLK1
202a
202b
NS0
S0
S1
NS1
NS2
S2
S3
NS3
S4
NS4
S5
NS5
S6
NS6
S7
NS7
NS8
S8
S9
NS9
CLK0
CLK6
CLK2
CLK8
CLK4
TCLK0
NC
NC
NC
NC
NC
CLK1
CLK7
CLK3
CLK9
TCLK5
CLK5
MAIN CTRL
AUX CTRL
PHASE DETECTOR & CHARGE PUMP 206a
PHASE DETECTOR & CHARGE PUMP 206b

FIG. 2

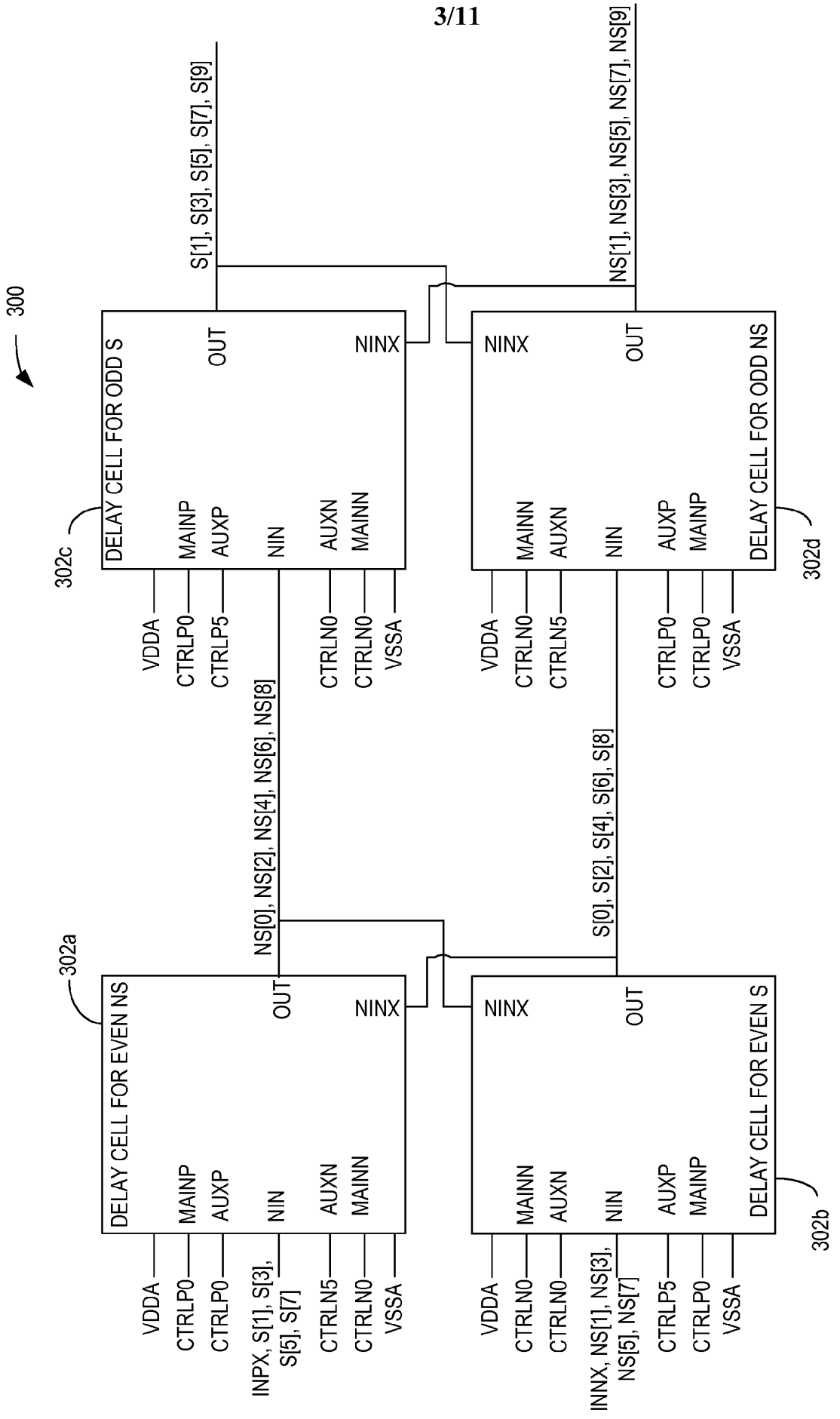

300
302a
DELAY CELL FOR EVEN NS
MAINP
AUXP
NIN
AUXN
MAINN
OUT
NINX
VDDA
CTRLP0
CTRLP0
INPX, S[1], S[3], S[5], S[7]
CTRLN5
CTRLN0
VSSA
NS[0], NS[2], NS[4], NS[6], NS[8]
302b
DELAY CELL FOR EVEN S
MAINN
AUXN
NIN
AUXP
MAINP
OUT
NINX
VDDA
CTRLN0
CTRLN0
INNX, NS[1], NS[3], NS[5], NS[7]
CTRLP5
CTRLP0
VSSA
S[0], S[2], S[4], S[6], S[8]
302c
DELAY CELL FOR ODD S
MAINP
AUXP
NIN
AUXN
MAINN
OUT
NINX
VDDA
CTRLP0
CTRLP5
CTRLN0
CTRLN0
VSSA
S[1], S[3], S[5], S[7], S[9]
302d
DELAY CELL FOR ODD NS
MAINN
AUXN
NIN
AUXP
MAINP
OUT
NINX
VDDA
CTRLN0
CTRLN5
CTRLP0
CTRLP0
VSSA
NS[1], NS[3], NS[5], NS[7], NS[9]

FIG. 3

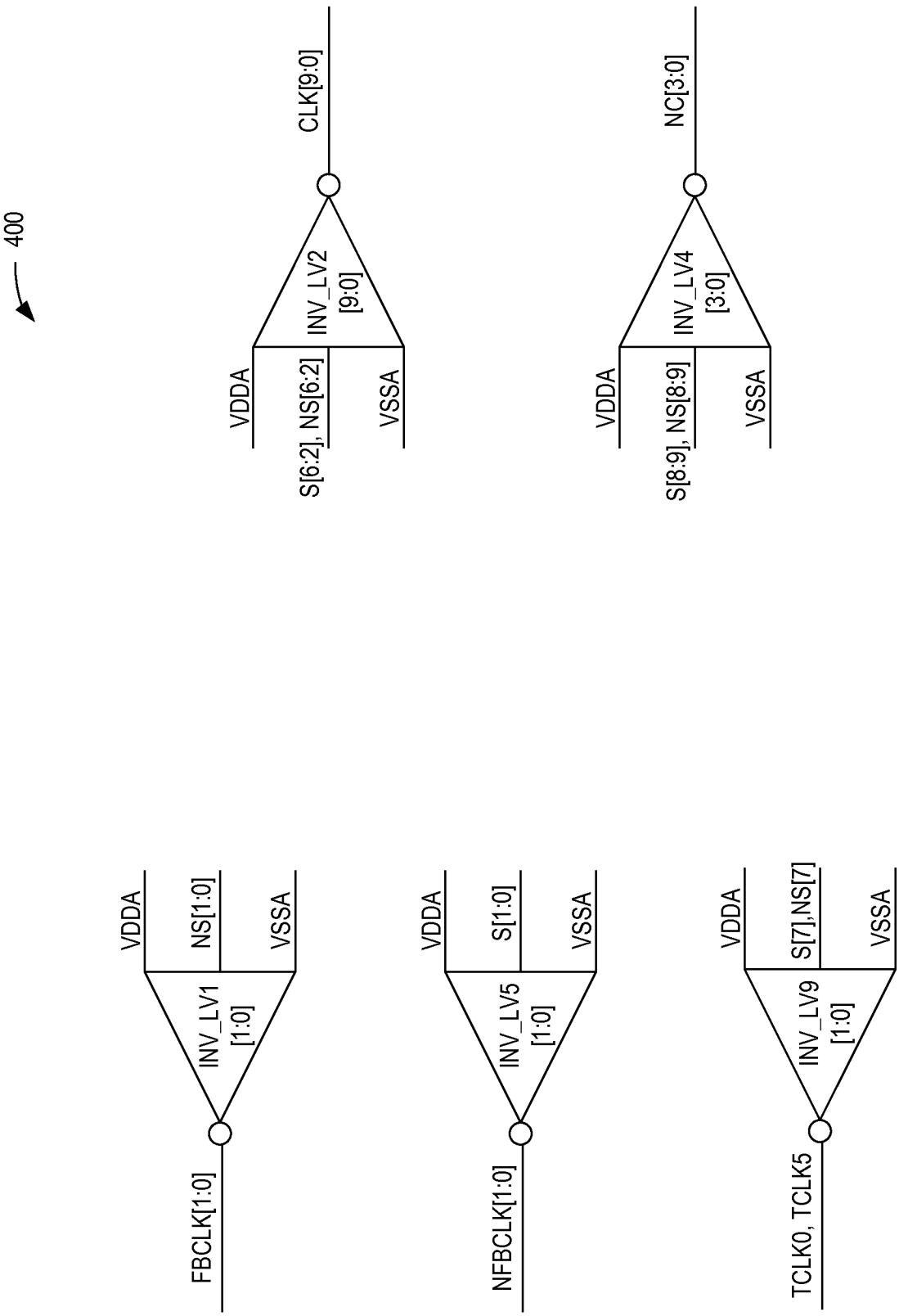

400
CLK[9:0]
INV_LV2
[9:0]
VDDA
S[6:2], NS[6:2]
VSSA
NC[3:0]
INV_LV4
[3:0]
VDDA
S[8:9], NS[8:9]
VSSA
VDDA
NS[1:0]
INV_LV1
[1:0]
VSSA
FBCLK[1:0]
VDDA
S[1:0]
INV_LV5
[1:0]
VSSA
NFBCLK[1:0]
VDDA
S[7],NS[7]
INV_LV9
[1:0]
VSSA
TCLK0, TCLK5

FIG. 4

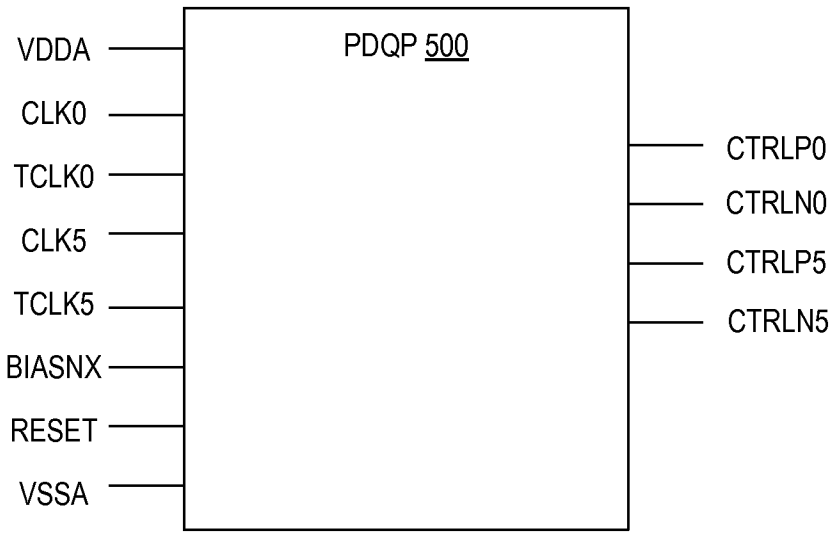

PDQP 500
VDDA
CLK0
TCLK0
CLK5
TCLK5
BIASNX
RESET
VSSA
CTRLP0
CTRLN0
CTRLP5
CTRLN5

FIG. 5

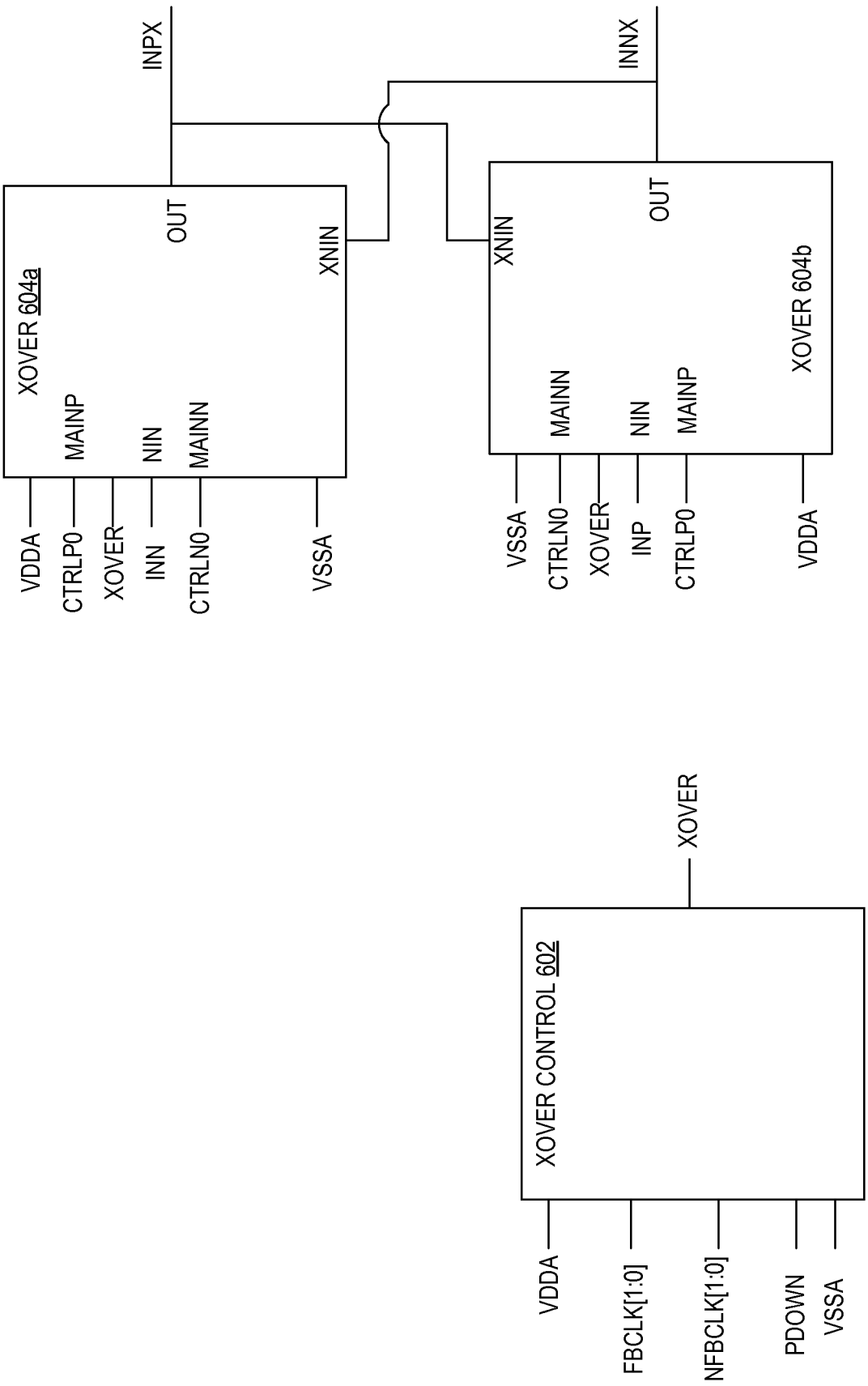

XOVER CONTROL 602
VDDA
FBCLK[1:0]
NFBCLK[1:0]
PDOWN
VSSA
XOVER
XOVER 604a
VDDA
CTRLP0
XOVER
INN
CTRLN0
VSSA
MAINP
NIN
MAINN
OUT
XNIN
INPX
XOVER 604b
VSSA
CTRLN0
XOVER
INP
CTRLP0
VDDA
MAINN
NIN
MAINP
OUT
XNIN
INNX

FIG. 6

FIG. 7

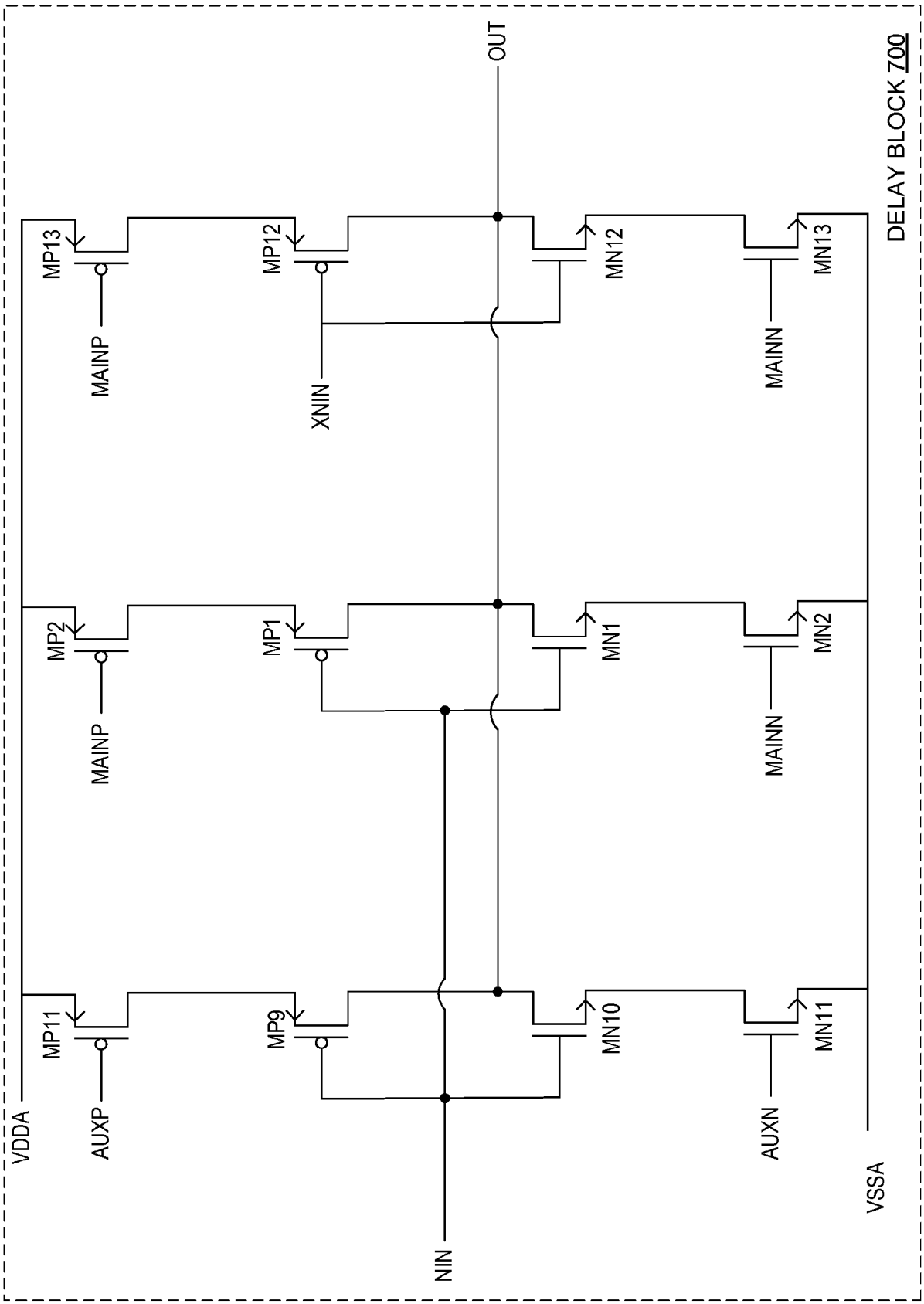

DELAY BLOCK 700
OUT
MP13
MP12
MN12
MN13
MAINP
XNIN
MAINN
MP2
MP1
MN1
MN2
MAINP
MAINN
MP11
MP9
MN10
MN11
VDDA
AUXP
AUXN
VSSA
NIN

FIG. 8

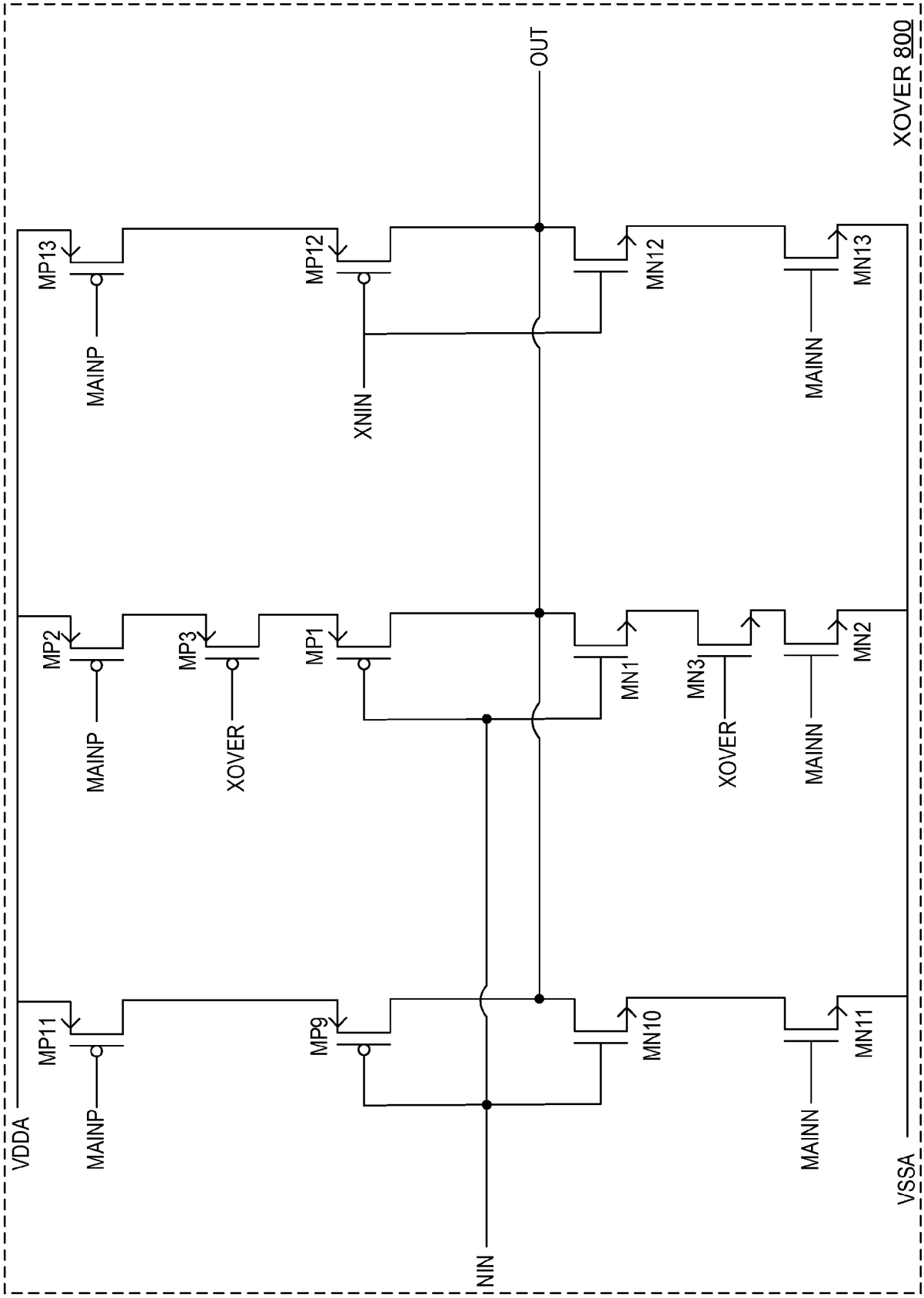

XOVER 800
OUT
MP13
MP12
MN12
MN13
MAINP
XNIN
MAINN
MP2
MP3
MP1
MN1
MN3
MN2
MAINP
XOVER
XOVER
MAINN
MP11
MP9
MN10
MN11
VDDA
MAINP
MAINN
VSSA
NIN

FIG. 9

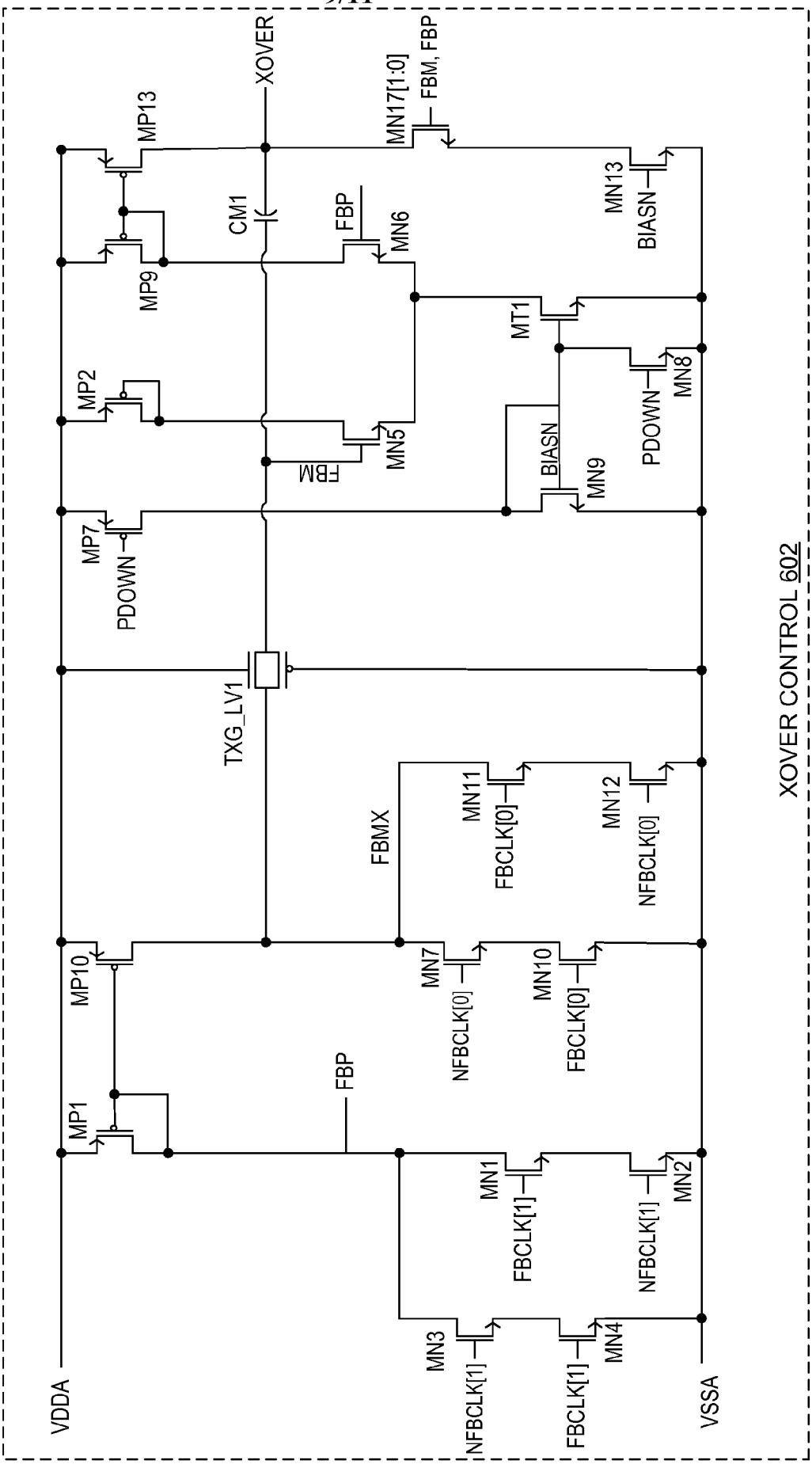
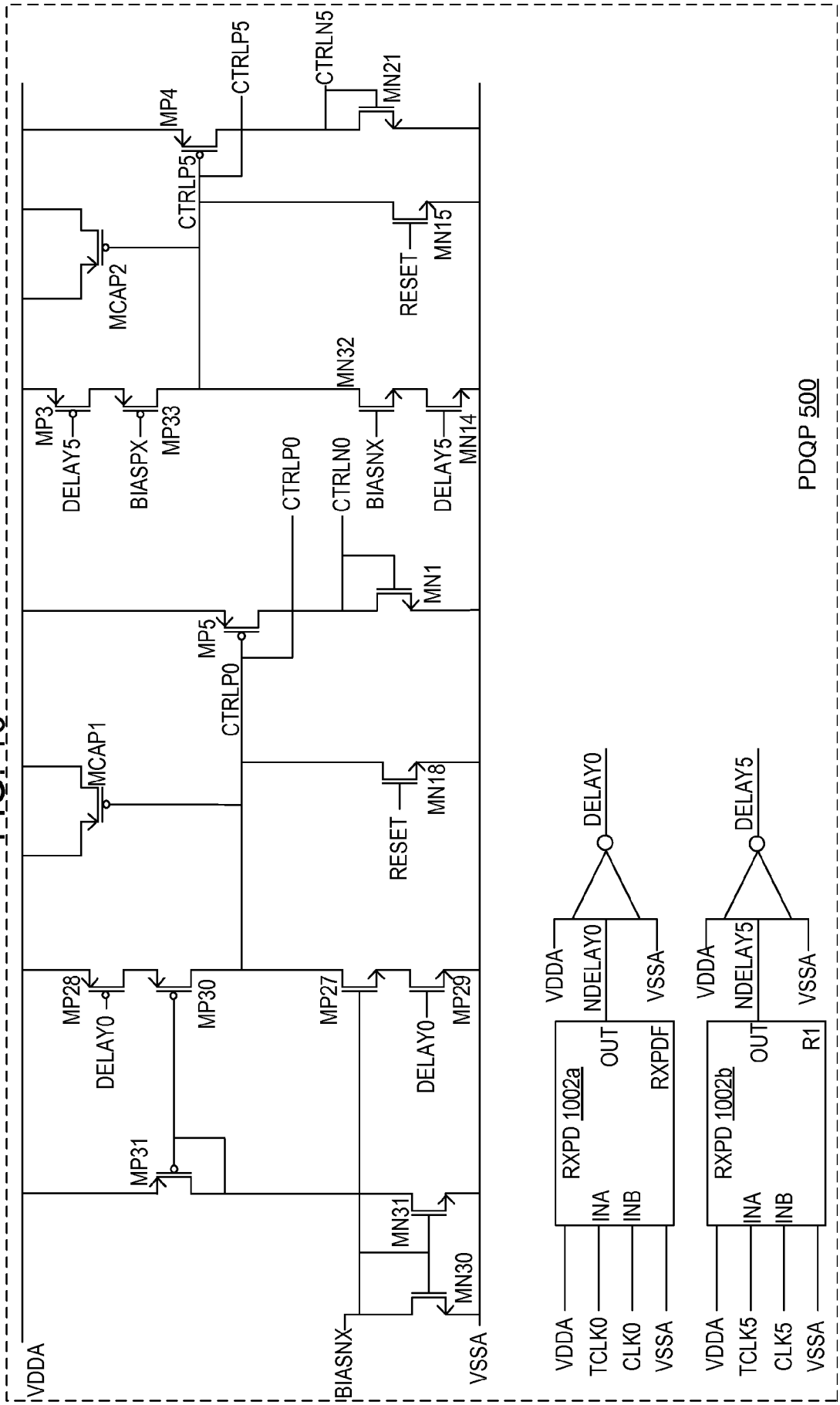

XOVER CONTROL 602
VDDA
VSSA
XOVER
MP13
MP9
MP2
MP7
PDOWN
MP10
MP1
CM1
FBP
MN6
MN17[1:0]
FBM, FBP
MN13
BIASN
MT1
MN8
PDOWN
MN5
FBM
MN9
BIASN
TXG_LV1
FBMX
MN11
FBCLK[0]
MN12
NFBCLK[0]
MN7
NFBCLK[0]
MN10
FBCLK[0]
FBP
MN1
FBCLK[1]
MN2
NFBCLK[1]
MN3
NFBCLK[1]
MN4
FBCLK[1]

FIG. 10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VDDA
BIASNX
VSSA
MP28
DELAY0
MP30
MP31
MP27
DELAY0
MP29
MN31
MN30
MCAP1
MP5
CTRLP0
RESET
MN18
MP3
DELAY5
BIASPX
MP33
CTRLP0
CTRLN0
BIASNX
DELAY5
MN14
MN32
MN1
MCAP2
MP4
CTRLP5
CTRLP5
CTRLN5
MN21
RESET
MN15
VDDA
NDELAY0
VSSA
RXPD 1002a
INA
INB
OUT
RXPDF
DELAY0
VDDA
TCLK0
CLK0
VSSA
VDDA
NDELAY5
VSSA
RXPD 1002b
INA
INB
OUT
R1
DELAY5
VDDA
TCLK5
CLK5
VSSA

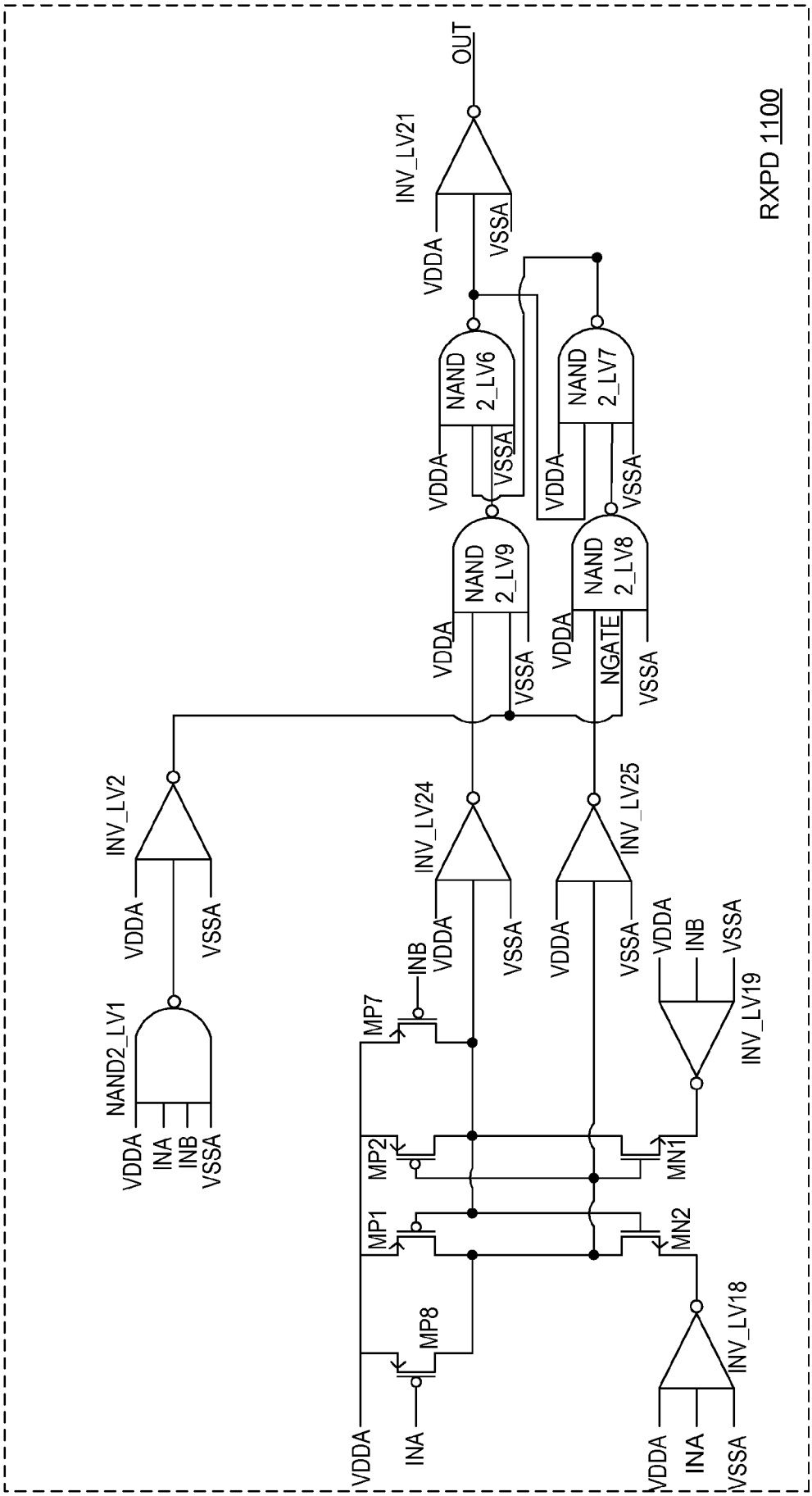
RXPD 1100
OUT
INV_LV21
VDDA
VSSA
NAND 2_LV6
NAND 2_LV7
NAND 2_LV9
NAND 2_LV8
NGATE
INV_LV2
INV_LV24
INV_LV25
INV_LV19
INV_LV18
NAND2_LV1
INA
INB
MP1
MP2
MP7
MP8
MN1
MN2

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/047630

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K5/135 H03L7/081
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2010/103746 A1 (MA YANTAO [US]) 29 April 2010 (2010-04-29) abstract; figures 4,6,7 paragraphs [0017], [0038], [0039] -----	1,2,8,9 10
X A	US 2007/085580 A1 (SINGH RAMESH K [IN] ET AL) 19 April 2007 (2007-04-19) abstract; figures 5,6a,6b,7 paragraphs [0004], [0010], [0014], [0016], [0030], [0032], [0035] - [0039], [0046], [0053], [0055] -----	1,2,8,9 3,10
A	US 2010/253405 A1 (QUAN XIAOHONG [US] ET AL) 7 October 2010 (2010-10-07) abstract; figures 1,5,6,7 paragraphs [0002], [0008], [0022], [0024], [0044], [0047], [0051], [0055] - [0060] -----	1-3,5,9, 10

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 November 2015	26/11/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Mesic, Maté

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/047630

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/169853 A1 (PARK IN-SOO [KR] ET AL) 17 July 2008 (2008-07-17) abstract; figure 1 -----	1,5,8-10

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/047630

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2012119804 A1	17-05-2012
US 2007085580 A1	19-04-2007	NONE	
US 2010253405 A1	07-10-2010	CN 102369669 A	07-03-2012
		EP 2415171 A1	08-02-2012
		JP 5475105 B2	16-04-2014
		JP 2012523181 A	27-09-2012
		JP 2014060729 A	03-04-2014
		KR 20120005013 A	13-01-2012
		KR 20130137051 A	13-12-2013
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		US 2012161837 A1	28-06-2012
		WO 2010115152 A1	07-10-2010
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		US 2008169853 A1	17-07-2008