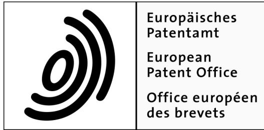
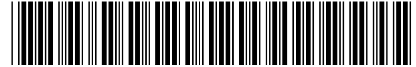
(19) 



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(54) **ULTRASOUND DEVICE**

(57) The present invention relates to an ultrasound device having a piezoelectric micromachined ultrasound transducer comprising at least one piezoelectric element. The ultrasound device also includes a substrate having a first surface and an opposite second surface, and a CMOS control circuit comprising a CMOS metallisation layer on the first surface and a plurality of transistors integrally provided within the first surface. The piezoelectric element comprises a moveable piezoelectric diaphragm having a piezoelectric body, a first electrode and a second electrode each arranged on the first surface. A cavity is defined in part by the moveable piezoelectric diaphragm and in part by the substrate. The moveable piezoelectric diaphragm defines at least part of a wall of the cavity and is configured to deform into the cavity. The CMOS control circuit is configured to control ultrasound transmission by controlling movement of the moveable piezoelectric diaphragm and/or control ultrasound reception by receiving signals resulting from movement of the moveable piezoelectric diaphragm.

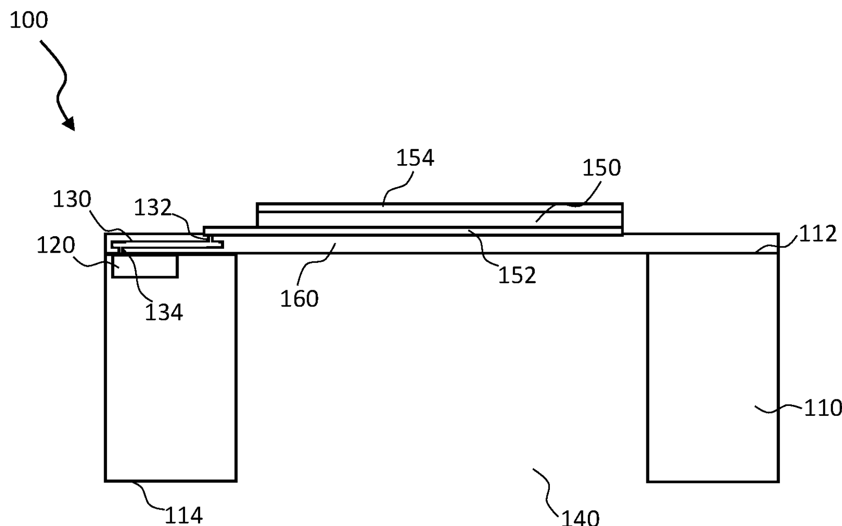

Fig. 1

EP 4 545 191 A1

Description

Field of the invention

[0001] The present invention relates to ultrasound devices, in particular piezoelectric ultrasound transducers, and methods for making these devices.

Background to the invention

[0002] Ultrasound devices are used in many different technical fields including medical imaging, drug delivery devices, non-destructive testing, gesture recognition and fingerprint sensors. For many applications within these technical fields, there is a need for miniaturised ultrasound devices.

[0003] More generally, microelectromechanical system (MEMS) techniques can be used to fabricate miniaturised devices having electrical and mechanical components. Piezoelectric micromachined ultrasonic transducers (PMUTs) are one example of a type of ultrasound transducer fabricated using MEMS processes. PMUTs typically include a thin piezoelectric film sandwiched between two electrodes and arranged above a cavity defined by a substrate. Piezoelectric materials can convert electrical energy into mechanical energy and vice versa. Considering PMUT devices in particular, motion of the piezoelectric film can be used to generate and/or sense ultrasound waves.

[0004] For many applications it would be advantageous to provide PMUTs which are highly integrated with the associated electronics for improved functionality. However, incompatibility with some elements of the desired circuity and the MEMS processing makes the provision of highly integrated devices challenging.

[0005] Accordingly, the invention seeks to improve the integration of PMUT MEMS components and the associated circuitry to provide a compact, highly integrated, ultrasound device.

Summary of the invention

[0006] In accordance with an aspect of the present invention, there is provided an ultrasound device comprising:

a substrate having a first surface and an opposite second surface;
a CMOS control circuit comprising a CMOS metallisation layer on the first surface and
a plurality of transistors integrally provided within the first surface;
a piezoelectric micromachined ultrasound transducer comprising at least one piezoelectric element, wherein the piezoelectric element comprises a moveable piezoelectric diaphragm;
a cavity defined in part by the moveable piezoelectric diaphragm and in part by the substrate;
wherein the moveable piezoelectric diaphragm comprises a piezoelectric body, a first electrode and a second electrode each arranged on the first surface;
wherein the moveable piezoelectric diaphragm defines at least part of a wall of the cavity and is configured to deform into the cavity; and
wherein the CMOS control circuit is configured to control ultrasound transmission by controlling movement of the moveable piezoelectric diaphragm and/or control ultrasound reception by receiving signals resulting from movement of the moveable piezoelectric diaphragm.

[0007] The MEMS components are provided on the same surface of the substrate as the complementary metal-oxide semiconductor (CMOS) control circuit to provide a highly integrated monolithic ultrasound device that is relatively straightforward and cost-effective to manufacture.

[0008] The substrate may comprise a silicon wafer. The substrate may be a semiconductor substrate. The plurality of transistors are integrally provided within the first surface - that is, the plurality of transistors may be formed on the first surface of the substrate and extend into the substrate from the first surface. The CMOS control circuit may be formed using conventional CMOS fabrication techniques. The CMOS metallisation layer may be formed on the first surface after the plurality of transistors are formed.

[0009] The cavity is a hole within the substrate that the moveable piezoelectric diaphragm can deform into - i.e., the cavity provides a space for the moveable piezoelectric diaphragm to flex into. The moveable piezoelectric diaphragm may also deform in the opposite direction - i.e., away from the cavity. Typically, the moveable piezoelectric diaphragm defines one wall of the cavity, and the substrate defines any other wall of the cavity. For example, if the cavity is cuboidal in shape, the substrate may define four walls of the cavity.

[0010] The piezoelectric body may be provided between the first electrode and the second electrode. An electric field between the first and second electrodes can be applied to cause deflection of the moveable piezoelectric diaphragm. In some embodiments, the substrate comprises a buried oxide (BOX) layer. By providing a buried oxide layer, it is possible to operate the CMOS components at a higher voltage - thereby facilitating greater deflection of the moveable piezoelectric diaphragm.

[0011] The piezoelectric body may comprise at least one piezoelectric material processable at a temperature below 450°C. Examples of piezoelectric materials that are processable at temperatures below 450°C include aluminium nitride (AlN), zinc oxide (ZnO), and/or scandium aluminium nitride (ScAlN). CMOS components can be damaged at temperatures greater than 450°C. By using piezoelectric materials that are processable at a temperature below 450°C, it is possible to integrate the

MEMS and CMOS components without causing degradation of the CMOS components, thereby improving the operation and efficiency of the device.

[0012] In some embodiments the piezoelectric element may comprise an inner portion and an outer portion. In these embodiments, the inner portion of the piezoelectric element comprises an inner piezoelectric body and a pair of inner electrodes; and the outer portion of the piezoelectric element comprises an outer piezoelectric body, and a pair of outer electrodes. Each of the inner portion and the outer portion can transmit and/or receive ultrasound. In some embodiments, the ultrasound device is configured so that a first potential difference can be applied between the inner pair of electrodes to cause deflection of the inner piezoelectric body in a first direction and a second potential difference can be applied between the outer pair of electrodes to cause deflection of the outer piezoelectric body in a second direction opposite said first direction.

[0013] In some embodiments, the wall of the cavity defined by the moveable piezoelectric diaphragm is continuous. That is, the moveable piezoelectric diaphragm extends across a full side of the cavity.

[0014] In other embodiments, the moveable piezoelectric diaphragm may be discontinuous - i.e., may not extend across the full side of the cavity. Instead, the moveable piezoelectric diaphragm may have a channel defined therethrough. For example, the piezoelectric diaphragm may be annular. In some embodiments, each electrode, the piezoelectric body, and any other layers which are part of the piezoelectric diaphragm may be annular and arranged concentrically such that a channel is defined through the moveable piezoelectric diaphragm. Providing a discontinuous moveable piezoelectric diaphragm increases the flexibility of the membrane - thereby changing the frequency response of the moveable piezoelectric diaphragm. It will be understood by the skilled person that different ultrasound frequencies are more appropriate for different ultrasound applications. In some embodiments, a channel defined therethrough the moveable piezoelectric diaphragm may be filled with a further material (rather than being left empty). For example, the channel could be filled with benzocyclobutene (BCB). This modification also affects the frequency response of the ultrasound device.

[0015] In some embodiments, the CMOS metallisation layer comprises conductive connections extending from at least one of the plurality of transistors to at least one of the first and second electrodes of the piezoelectric element. These conductive connections may be suitable for conducting digital or analogue information. These conductive connections may be suitable for conducting drive waveforms to actuate the piezoelectric element. In some embodiments the metallisation layer comprises planar structures formed by chemical mechanical planarization to facilitate more straightforward fabrication of the ultrasound device.

Typically, the cavity is formed using an etching process. In some embodiments at least part of at least one of the walls of the cavity is defined by a deep trench isolation structure. The deep trench isolation structure typically comprises a different material compared to the rest of the substrate that is more resistant to the etching process. Accordingly, the deep trench isolation structure can be used to better define the cavity geometry.

[0016] In some embodiments, the moveable piezoelectric diaphragm comprises at least part of the CMOS metallisation layer, and optionally the CMOS metallisation layer comprises a conductive connection extending from at least one of the plurality of transistors to at least one of the first and second electrodes of the piezoelectric element.

[0017] In embodiments where the moveable piezoelectric diaphragm comprises at least part of the CMOS metallisation layer, at least part of the moveable piezoelectric diaphragm that deforms into the cavity comprises at least part of the CMOS metallisation layer. The cavity is required to allow oscillation of the moveable piezoelectric diaphragm. However, the presence of the cavities reduces the space available for electrical routing. By providing at least part of the CMOS metallisation layer in the moveable piezoelectric diaphragm more space is available for metal routing - thereby facilitating device miniaturisation.

[0018] At least one of the plurality of transistors may be connected directly (i.e, without intervening transistors) to at least one electrode of the first electrode or second electrode by one of the conductive connections.

[0019] In some embodiments the ultrasound device further comprises an additional layer on the first surface of the substrate, wherein the moveable piezoelectric diaphragm comprises at least part of the additional layer, wherein the additional layer defines the at least part of the wall of the cavity defined by the moveable piezoelectric diaphragm, and optionally wherein at least part of the CMOS metallisation layer is integrally provided within the additional layer and/or optionally wherein the additional layer comprises CMOS oxide.

[0020] In embodiments where the moveable piezoelectric diaphragm comprises at least part of the additional layer, at least part of the moveable piezoelectric diaphragm that deforms into the cavity comprises at least part of the additional layer.

[0021] The additional layer may be provided directly on the first surface of the substrate. The additional layer may be provided directly on the first surface of the substrate and one of the first and second electrodes provided between the additional layer and the piezoelectric body. The additional layer may define the at least part of the wall of the cavity defined by the moveable piezoelectric membrane. Providing this additional layer facilitates more controlled oscillation of the piezoelectric diaphragm (i.e., an oscillation with a better defined characteristic). In some embodiments, at least part of the CMOS metallisation layer may be integrally provided within the additional layer. The additional layer may comprise oxides,

nitrides, oxynitrides or laminates.

[0022] In some embodiments the additional layer defines a notch in the moveable piezoelectric region. A wall of the notch may be defined by at least part of a CMOS metallisation layer. The presence of a notch in the membrane affects the frequency response of the moveable piezoelectric membrane.

[0023] Providing an additional layer comprising CMOS oxide is particularly advantageous because fewer MEMS manufacturing steps are required. Accordingly, a device having a moveable piezoelectric diaphragm comprising a CMOS oxide layer are relatively straightforward to manufacture.

[0024] In some embodiments the additional layer may consist of CMOS oxide.

[0025] In some embodiments, the metallisation layer is one of a plurality of metallisation layers integrally provided within the additional layer. The combination of an additional layer comprising CMOS oxides, and a plurality of metallisation layers integrally formed within allow for multiple layers of conductive connections, thereby a high level of functionality is provided.

[0026] In some embodiments, the at least one piezoelectric element is one of a plurality of piezoelectric elements arranged in an array,

> wherein each piezoelectric element comprises a moveable piezoelectric diaphragm, wherein each moveable piezoelectric diaphragm comprises a piezoelectric body, a first electrode and a second electrode arranged on the first surface,
> wherein the cavity is one of a plurality of cavities, wherein each moveable piezoelectric diaphragm defines at least part of a wall of a respective cavity of the plurality of cavities.

[0027] In some embodiments each moveable piezoelectric diaphragm comprises at least part of the CMOS metallisation layer.

[0028] For some applications, it is helpful to provide integrated PMUT devices having multiple piezoelectric elements arranged in an array, where each piezoelectric element is connected to corresponding wiring. Subject to cross-talk considerations, it is can be desirable to provide arrays with a high element density. However, providing the high element density together with the required wiring can be technically challenging. Providing high element density is particularly challenging when substrate space is limited by the presence of cavities for allowing deflection of the corresponding moveable piezoelectric diaphragms.

[0029] By providing at least part of the CMOS metallisation layer in each of the moveable piezoelectric diaphragms more space is available for metal routing - thereby facilitating device miniaturisation. Further, the inventors have realised that providing at least part of the CMOS metallisation layer in each of the moveable piezoelectric diaphragms also helps to avoid electrical cross-talk.

[0030] In some embodiments, the CMOS metallisation layer comprises conductive connections extending from at least one of the plurality of transistors to at least one of the first and second electrodes of each respective piezoelectric element.

[0031] In some embodiments, the ultrasound device further comprises an additional layer on the first surface of the substrate, wherein each moveable piezoelectric diaphragm comprises at least part of the additional layer, wherein the additional layer defines the at least part of the wall of each cavity defined by the respective moveable piezoelectric diaphragm, and optionally wherein at least part of the CMOS metallisation layer is integrally provided within the additional layer and/or optionally wherein the additional layer comprises CMOS oxide.

[0032] In some embodiments the CMOS metallisation layer comprises conductive connections extending from at least one of the plurality of transistors to at least one of the first and second electrodes of a respective piezoelectric element, and optionally wherein the lengths of the conductive connections are consistent.

[0033] It is advantageous for the conductive connections to be consistent (i.e., of similar length, thickness and breadth) so that they affected to a similar extent by voltage droop, parasitic capacitance, antenna effects etc. In some embodiments, the length of the conductive connections varies by no more than 1 cm, preferably no more than 0.1 cm. Typically, the length of the conductive connections varies by no more than 10 times the spacing between adjacent piezoelectric elements of the array (i.e., piezoelectric elements adjacent to one another along a row of the array).

[0034] In some embodiments the array comprises a first zone having a first side and a second side opposite to the first side, wherein the plurality of piezoelectric elements are arranged into rows, wherein the conductive connections extend into the array from one or both of the first and second sides between the rows of piezoelectric elements, and optionally wherein the first zone is elongate and the first and second sides correspond to the long sides along the length of the first zone.

[0035] By providing an elongate zone and conductive connections that extend into the array between rows of the piezoelectric elements each of the piezoelectric elements can receive signals transmitted through the conductive connections (e.g., drive waveforms) at very similar times. This improves the uniformity of the ultrasound response when using an array of elements.

[0036] In some embodiments, the first zone comprises at least a first, a second and third row of piezoelectric elements, wherein a first subset of the conductive connections extend between piezoelectric elements of the first and second row to different respective piezoelectric elements along the length of the second row, and optionally,

wherein a second subset of the conductive connections extend between piezoelectric elements of the second

and third row to different respective piezoelectric elements along the length of the second row.

[0037] By providing a wiring arrangement where the first zone comprises at least a first, a second and a third row of piezoelectric elements (typically without other rows in between) wherein a plurality of (and typically at least four) conductive connections extend between piezoelectric elements of the first and second row to different respective piezoelectric elements along the length of the second row, typically wherein a plurality of (and typically at least four) conductive connections extend between piezoelectric elements of the second and third row to different respective piezoelectric elements along the length of the second row a compact wiring arrangements that facilitates device miniaturisation is possible.

[0038] In some embodiments, at least part of the CMOS control circuit is arranged in a column adjacent to at least one of the first and second sides of the first zone.

[0039] By providing at least part of the CMOS control circuit in a column adjacent to at least one of the first and second sides of the first zone in combination with conductive connections extending between piezoelectric elements from the CMOS circuitry it is possible to manufacture an ultrasound device having a small form-factor more conveniently.

[0040] In some embodiments, the CMOS control circuit comprises a drive circuit configured to actuate each moveable piezoelectric diaphragm of at least a subset of the plurality of piezoelectric elements such that an ultrasound signal is transmitted;

wherein the CMOS control circuit comprises a receive circuit for receiving ultrasound signal;
and optionally wherein at least part of the drive circuit and/or at least part of the receive circuit is arranged in the column adjacent to at least one of the first and second sides of the first zone.

[0041] By providing a CMOS control circuit comprising a drive circuit and a receive circuit on the same surface as the MEMS device it is possible to provide a highly integrated and compact ultrasound device. By providing these circuits in a column adjacent to at least one of the first and second sides of the first zone, the size of the ultrasound device can be further reduced.

[0042] In some embodiments, the CMOS control circuit comprises delay circuitry and/or apodisation circuitry;

wherein the delay circuitry is configured to delay the actuator waveform conducted to one of the piezoelectric elements relative to the actuator waveform conducted to another piezoelectric element, and optionally wherein at least part of the apodisation circuitry is arranged in the column adjacent to at least one of the first and second sides of the first zone;
wherein the apodisation circuitry is configured to increase the amplitude of the actuator waveform conducted to one of the piezoelectric elements relative to the actuator waveform conducted to another piezoelectric element, and optionally wherein at least part of the apodisation circuitry is arranged in the column adjacent to at least one of the first and second sides of the first zone.

[0043] By providing delay circuitry it is possible to focus the ultrasound beam transmitted from the ultrasound device. This can provide improved resolution for imaging applications, and improved energy deposition for therapeutic applications. By providing apodisation circuitry, the frequency content of the transmitted pulse can be better controlled - providing improved signal quality for imaging applications. It is particularly advantageous to provide this circuit in the column adjacent at least one of the first and second sides of the first zone because this makes it possible to provide a particularly compact ultrasound device.

[0044] In some embodiments, the CMOS control circuit comprises amplification circuitry for amplifying the received ultrasound signal,

and optionally wherein the amplification circuitry is configured to amplify the received signal based on the depth at which the received signal has been reflected from,
and optionally wherein at least part of the amplification circuitry is arranged in the column adjacent to at least one of the first and second sides of the first zone.

[0045] By providing amplification circuitry the received ultrasound signal is less affected by noise. This amplification may be based on the depth of the received signal (e.g., time-gain amplification). Signal quality is further improved by providing this amplification circuitry in the column adjacent to at least one of the first and second sides of the first zone.

[0046] According to another aspect of the invention there is provided a wearable device comprising any of the ultrasound devices described herein.

[0047] In some embodiments, the wearable device is a patch. For example, a patch that can be worn on a user's arm.

[0048] According to another aspect of the invention there is provided a method of forming any of the ultrasound devices described herein
wherein the ultrasound device comprises a piezoelectric micromachined ultrasound transducer comprising n piezoelectric elements;

forming n cavities within a substrate, wherein the substate has a first surface and an opposite second surface;
forming a plurality of transistors within the first surface;

forming a CMOS metallisation layer on the first surface;
and
forming n moveable piezoelectric diaphragms;
wherein each cavity is defined in part by the substrate and in part by one of the n moveable piezoelectric diaphragms.

[0049] In some embodiments, the method may involve forming the cavities using a deep reactive-ion etching (DRIE) process. The DRIE etching may be carried out from the backside of the substrate, and optionally also from the frontside of the substrate. In some embodiments a deep trench isolation structure is provided in the substrate for defining the walls of the cavity.

[0050] According to another aspect of the invention there is provided a method for using any of the abovementioned ultrasound devices comprising:

transmitting an ultrasound signal and/or receiving an ultrasound signal;
wherein transmitting an ultrasound signal comprises using at least a subset of the plurality of transistors to control the movement of the moveable piezoelectric membrane; and
wherein receiving an ultrasound signal involves receiving a signal generated by movement of the moveable piezoelectric membrane.

[0051] In some embodiments, the CMOS control circuit comprises amplification circuitry and the method involves amplifying the received signal using the amplification circuitry.

[0052] In some embodiments, the ultrasound device comprises a plurality of piezoelectric elements, and the CMOS control circuit comprises beamforming circuitry and the method involves beamforming the received signal using the beamforming circuitry.

[0053] In some embodiments, the ultrasound device comprises a plurality of piezoelectric elements and the CMOS control circuit comprises apodisation circuitry, wherein the method involves transmitting a first ultrasound signal from one piezoelectric element and a second ultrasound signal from a second piezoelectric element, wherein the amplitude of the first ultrasound signal is different from the amplitude of the second ultrasound signal.

[0054] In some embodiments, the ultrasound device comprises a plurality of piezoelectric elements and the CMOS control circuit comprises delay circuitry, wherein the method involves transmitting a first ultrasound signal from one piezoelectric element and a second ultrasound signal from a second piezoelectric element, wherein the first ultrasound signal is delayed relative to the second ultrasound signal.

Description of the Drawings

[0055] An example embodiment of the present invention will now be illustrated with reference to the following Figures in which:

Figures 1-8 are schematic representations of an ultrasound device, each according to a respective embodiment of the invention.
Figure 9 is a schematic representation of an ultrasound device having a plurality of piezoelectric elements, according to another embodiment of the invention;
Figure 10 is a schematic representation of an ultrasound device, according to another embodiment of the invention;
Figure 11 is a schematic representation of part of an ultrasound device, according to another embodiment of the invention;
Figure 12 is a schematic representation of a method of manufacturing an ultrasound device, according to an embodiment of the invention;
Figure 13 is a schematic representation of a method of using an ultrasound device according to an embodiment of the invention; and
Figure 14 is a schematic representation of an ultrasound device according to an embodiment of the invention.

Detailed Description of an Example Embodiment

[0056] Figure 1 is a schematic representation of an ultrasound device 100 having a piezoelectric element. The ultrasound device comprises a semiconductor substrate 110 having a first surface 112 opposite to a second surface 114. The ultrasound device 100 includes a CMOS control circuit comprising a plurality of transistors 120 integrally provided within the first surface 112 and a CMOS metallisation layer 130 provided on the first surface 112. The piezoelectric element comprises a moveable piezoelectric diaphragm including a piezoelectric body 150, a first electrode 152 and a second electrode 154 each arranged on the first surface 112. The moveable piezoelectric diaphragm also includes an additional layer 160 (made from the same material as the rest of the substrate, in this embodiment). A cavity 140 is defined in part by the moveable piezoelectric diaphragm and in part by the semiconductor substrate 110. In this embodiment, the CMOS metallisation layer 130 includes conductive connections 132, 134 extending from the plurality of transistors 120 to the first electrode 152.

[0057] In use, the moveable piezoelectric diaphragm is configured to deform into the cavity 140 in response to control signals from the CMOS control circuit. The motion of the moveable piezoelectric diaphragm generates ultrasound energy, which is transmitted from the ultrasound device 100.
Figure 2 is a schematic representation of an ultrasound

device 200 comprising a substrate 210 having a first surface 212 and an opposite second surface 214. The ultrasound device 200 includes a CMOS control circuit comprising a plurality of transistors 220 integrally provided within the first surface 212 and a CMOS metallisation layer 230 provided on the first surface 212. The ultrasound device 200 comprises a piezoelectric element having a moveable piezoelectric diaphragm. The moveable piezoelectric diaphragm includes a piezoelectric body 250, a first electrode 252, a second electrode 254 and an additional layer 260. The additional layer 260 is a CMOS oxide layer. A cavity 240 is defined in part by the moveable piezoelectric diaphragm and in part by the substrate 210. The ultrasound device includes a protective layer 270 to protect the MEMS components.

[0058] The CMOS metallisation layer 230 is provided integrally with the CMOS oxide layer 260, and comprises conductive connections 232, 234 extending from the plurality of transistors 220 to the first electrode 252. Part of the metallisation layer 230 is provided within the moveable piezoelectric diaphragm, i.e., the part of the piezoelectric element that deforms into the cavity when in use. By providing part of the metallisation layer 230 within the moveable piezoelectric diaphragm it is possible to provide a particularly compact device.

[0059] Figure 3 is a schematic representation of an ultrasound device 300 according to another embodiment of the invention. The ultrasound device 300 comprises a substrate 310 having a first surface 312 and an opposite second surface 314. The ultrasound device 300 includes a CMOS control circuit and a piezoelectric element having a moveable piezoelectric diaphragm. The CMOS control circuit comprises a plurality of transistors 320 integrally provided within the first surface 312 and a CMOS metallisation layer 330. The moveable piezoelectric diaphragm includes a piezoelectric body 350, a first electrode 352, a second electrode 354 and an additional layer 360. A cavity 340 is defined in part by the moveable piezoelectric diaphragm and in part by the substrate 310. The ultrasound device also includes a protective layer 270.

[0060] The CMOS metallisation layer 330 is provided integrally with the additional layer 260, and comprises conductive connections 332, 334 extending from the at least one of the plurality of transistors 320 to the first electrode 352. Part of the metallisation layer 330 is provided within the moveable piezoelectric diaphragm. The metallisation layer 330 is only one of a plurality of metallisation layers 330, 331, 333 provided within the additional layer 360. Providing multiple metallisation layers 330, 331, 333 within the moveable piezoelectric diaphragm makes it possible to provide a device with improved functionality whilst also having a small size. Each of these metallisation layers 330, 331, 333 may be suitable for conducting waveforms between the CMOS control circuit 320 and the first and/or second electrodes 352, 354.

[0061] Figure 4 is a schematic representation of an ultrasound device 400 according to another embodiment of the invention. The ultrasound device 400 comprises a substrate 410 having a first surface 412 and an opposite second surface 414. The ultrasound device 400 includes a CMOS control circuit and a piezoelectric element having a moveable piezoelectric diaphragm. The moveable piezoelectric diaphragm includes a piezoelectric body 450, a first electrode 452, a second electrode 454 and an additional layer 460. The CMOS control circuit comprises a plurality of transistors 420 and a CMOS metallisation layer 430. The CMOS metallisation layer 430 is provided on the first surface 412 and includes conductive connections 432, 434. A cavity 440 is defined in part by the moveable piezoelectric diaphragm and in part by the substrate 410. The ultrasound device also includes a protective layer 470. In this embodiment, the moveable piezoelectric diaphragm does not extend across the full side of the cavity (i.e., it is discontinuous). Each of the first electrode 452, the second electrode 454, and the piezoelectric body 450 are annular and arranged concentrically. The additional layer 460 and protective layer 470 are also discontinuous such that a channel 490 is defined through the moveable piezoelectric diaphragm - thereby increasing the flexibility of the piezoelectric diaphragm.

[0062] Figure 5 is a schematic representation of an ultrasound device 500, which is similar to the ultrasound device 400 shown in Figure 4. In particular, the ultrasound device 500 comprises a substrate 510 having a first surface 512 and an opposite second surface 514. The ultrasound device 500 includes a CMOS control circuit and a piezoelectric element having a moveable piezoelectric diaphragm. The CMOS control circuit comprises a plurality of transistors 520 and a CMOS metallisation layer 530. The moveable piezoelectric diaphragm includes a piezoelectric body 550, a first electrode 552, a second electrode 554 and an additional layer 560. The CMOS metallisation layer 530 is provided on the first surface 512 and includes conductive connections 532, 534. A cavity 540 is defined in part by the moveable piezoelectric diaphragm and in part by the substrate 510. The ultrasound device also includes a protective layer 570. Each of the first electrode 552, the second electrode 554, and the piezoelectric body 550 are annular and arranged concentrically. The additional layer 560 and protective layer 570 are also discontinuous such that a channel 590 is defined through the moveable piezoelectric diaphragm. The main difference between the ultrasound device of Figure 4 compared to the ultrasound device of Figure 5 is that the channel 590 is filled with an additional material, whereas the channel 490 is empty. In this embodiment the additional material is benzocyclobutene (BCB).

[0063] Figure 6 is a schematic representation of an ultrasound device 600, which is similar to the ultrasound device 100 shown in Figure 1. In particular, the ultrasound device 600 comprises a substrate 610 having a first surface 612 and a second surface 614. The ultrasound device 600 includes a protective layer 670 and a CMOS

control circuit including a plurality of transistors 620 and a CMOS metallisation layer 630. The CMOS metallisation layer 630 includes conductive connections 632, 634. The piezoelectric element comprises a moveable piezoelectric diaphragm including a piezoelectric body 650, a first electrode 652, a second electrode 654 and an additional layer 660. A cavity 640 is defined by the moveable piezoelectric diaphragm and the substrate 610. In this embodiment, the ultrasound device 600 further includes a buried oxide layer 680. The buried oxide layer 680 makes it possible to operate the CMOS components at a higher voltage - thereby facilitating greater deflection of the moveable piezoelectric diaphragm.

[0064] Figure 7 is a schematic representation of an ultrasound device 700, which is similar to the ultrasound device 700 shown in Figure 7. The ultrasound device 700 comprises a substrate 710 having a first surface 712 and a second surface 714. The ultrasound device 700 includes a protective layer 770, a plurality of transistors 720, and a CMOS metallisation layer 730 including conductive connections 732, 734. The piezoelectric element comprises a moveable piezoelectric diaphragm including a piezoelectric body 750, a first electrode 752, a second electrode 754 and an additional layer 760. A cavity 740 is defined by the moveable piezoelectric diaphragm and the substrate 710. The ultrasound device 700 also includes a buried oxide layer 780. In this embodiment, the ultrasound device 700 further comprises deep trench isolation structures to define the cavity 740 dimensions. The ultrasound device 700 also includes a notch 790 in the additional layer 760 and having a CMOS metal layer 792 as an etch stop. Having a notch 790, at least partly within the moveable piezoelectric diaphragm, affects the frequency response of the ultrasound device 700.

[0065] Figure 8 is a schematic representation of an ultrasound device 800, according to an embodiment of the invention. The ultrasound device 800 comprises a substrate 810 having a first surface 812 and a second surface 814. The ultrasound device 800 includes a cavity 840, an additional layer 860, a protective layer 870, a plurality of transistors 820, and a CMOS metallisation layer 830 including conductive connections 832, 834. The moveable piezoelectric diaphragm includes a piezoelectric element having an inner portion and an outer portion. The inner portion comprises an inner piezoelectric body 850b, a first inner electrode 852b, and a second inner electrode 854b. The outer portion comprises an outer piezoelectric body 850a, a first outer electrode 852a, and a second outer electrode 854a. In this embodiment, the inner portion is circular and the outer portion is annular. The inner and outer piezoelectric elements are arranged concentrically.

[0066] In use, each of the inner portion and the outer portion can transmit and/or receive ultrasound. A first potential difference can be applied between the inner pair of electrodes 852b, 854b and a second potential difference can be applied between the outer pair of electrodes 852a, 854a to cause deflection of the inner piezoelectric body 850b in a first direction and to cause deflection of the outer piezoelectric body 850a in a second direction opposite said first direction.

[0067] Figure 9 is a schematic representation of an ultrasound device 900 comprising a plurality of piezoelectric elements formed on a semiconductor substrate 910. Each piezoelectric element includes a moveable piezoelectric diaphragm a piezoelectric body 950a-c, a first electrode 952a-c and a second electrode 954a-c arranged on the first surface 912 of the substrate 910. Each piezoelectric element is associated with a cavity 940a-c defined by the substrate 910 and each respective moveable piezoelectric diaphragm. The ultrasound device 900 includes an additional layer 960, a protective layer 970, a plurality of transistors 920, and a CMOS metallisation layer 930 including conductive connections 932, 934. The CMOS metallisation layer 930 is one of a plurality of CMOS metallisation layers 930, 932, 934 integrally provided in the additional layer 960. In this embodiment, each moveable piezoelectric diaphragm comprises at least part of a CMOS metallisation layer. Using the space within the moveable piezoelectric diaphragms for CMOS metallisation layers can facilitate device miniaturisation whilst avoiding electrical crosstalk between elements.

[0068] Figure 10 is a schematic representation of an ultrasound device 1000 according to an embodiment of the invention. The ultrasound device 1000 comprises an array of piezoelectric elements arranged in rows. The array includes an elongate zone 1020 having a first side 1022 and a second side 1024. The ultrasound device comprises a plurality of transistors 1010 is arranged in a column adjacent to the first side 1022 of the elongate zone 1020. Conductive connections 1030 from the plurality of transistors 1010 extend into the array from the first side 1022. In use, waveforms can be conducted between the plurality of transistors 1010 and each piezoelectric element.

[0069] Figure 11 is a schematic representation of part of an ultrasound device 1100 according to an embodiment of the invention. The ultrasound device 1100 comprises an array of piezoelectric elements 1120 arranged in rows 1110a-c. Conductive connections 1130 extend into the array from a first side of the array. It should be understood that Figure 11 is rotated by 90° relative to Figure 10. As show in Figure 11, a subset of the conductive connections extend between the elements of the adjacent rows to different respect piezoelectric elements along the length of each row 1110a-c.

[0070] Figure 12 is a schematic representation of a method 1200 of manufacturing an ultrasound device, according to an embodiment of the invention. The method involves a step 1220 of forming n cavities within a substrate. Typically, the cavities are provided using a DRIE etch procedure from the backside (i.e., the opposite second surface) of the substrate. In other embodiments the method involves etching from the frontside (i.e., the first surface) and the backside. Buried oxide and deep

trench isolation structures can be used to define the cavity dimensions.

[0071] The method includes a step 1220 of forming a plurality of transistors within the first surface. The transistors are formed by standard CMOS processing methodologies including ion implantation on a p-type or n-type substrate.

[0072] The method also includes a step 1230 of forming a CMOS metallisation layer on the first surface. The CMOS metallisation layer is also formed by standard processes such as ion implantation chemical vapour deposition, physical vapour deposition, etching, chemical-mechanical planarization and/or electroplating.

[0073] The method involves a step 1240 of forming n moveable piezoelectric diaphragms - i.e., the MEMS components. Forming each moveable piezoelectric diaphragms involves forming the respective electrodes and intervening piezoelectric body. Typically this step involves using successive thin film deposition techniques. Preferably, each piezoelectric body is formed of a material such as AIN or ScAIN which may be deposited at a temperature below 450°C by physical vapour deposition (including low-temperature sputtering). The electrodes are formed of, for example titanium, platinum, aluminium, tungsten or alloys thereof.

[0074] Figure 13 is a schematic representation of a method of using an ultrasound device according to an embodiment of the invention. Figure 13 shows a method involving transmitting an ultrasound signal and receiving an ultrasound signal (e.g., an ultrasound signal generated by reflection of the transmitted ultrasound signal from another structure).

[0075] The method involves a step of generating drive waveforms 1310 using at least a subset of the plurality of transistors. Typically, one drive waveform is generated for each piezoelectric element of the ultrasound device. The method also includes a step of introducing delays to the drive waveforms 1320. The drive waveforms are delayed based on the relative positions of the piezoelectric elements on the array so that a focussed ultrasound beam is transmitted from the ultrasound device. In other embodiments, no such focussing is provided and plane waves are transmitted from the ultrasound device. The method also involves an apodisation step 1330. This step comprises weighting the drive waveforms such that the amplitude of the ultrasound signal transmitted from the piezoelectric elements arranged at the edges of the array is less than the ultrasound signal transmitted from the more central piezoelectric elements. The amplitude variation from the central elements to the outer elements is smooth such that unwanted lobes of the transmitted ultrasound pulse are suppressed, thereby providing improved signal quality (reduced clutter). The variation may be determined based on Hanning, Hamming, or Blackman functions, for example. The method then involves a step of actuating the moveable piezoelectric diaphragms 1340. This involves varying the voltage applied over the first and second electrodes of each piezoelectric element based on the drive waveforms to cause the moveable piezoelectric diaphragms to move in and out of the cavity in a controlled way.

[0076] Turning now to the reception, the method involves a step of sensing the membrane movement 1350. Ultrasound signal incident on each moveable piezoelectric diaphragm causes that diaphragm to move. An electrical signal is generated based on the movement of the diaphragm. The method further involves an amplification step 1360. This step involves amplification of the electrical signal received from each piezoelectric element. By providing the amplification circuitry on the same surface as the MEMs components, noise propagation through the electrical circuitry is limited. The method also involves a beamforming step 1370. It will be understood that various beamforming methods can be used. Those beamforming method may involve weighting of the signals received based on the position of the piezoelectric element receiving each signal (i.e., receive apodisation) and/or delaying the signals received from each element based on their relative positions. The method also involves a further filtering step 1380 to reduce noise.

[0077] Figure 14 is a schematic representation of an ultrasound device 1400 according to an embodiment of the invention. In particular, Figure 14 includes a highly schematic representation of some of the control circuitry of the ultrasound device 1400. In this embodiment, the control circuitry is distributed between a machine controller 1430 and the CMOS control circuit 1420 provided on and integrally within a surface of the substrate 1410. The circuitry associated with the machine controller 1430 and CMOS control circuitry 1420 are connected in part by conductors 1440 extending through a flexible cable 1460.

[0078] Individual piezoelectric elements 1450 of the ultrasound device 1400 are each connected to respective amplification circuitry 1422, drive circuitry 1424, and an analogue to digital converter (ADC) 1426. In this embodiment, each piezoelectric element is connected to further control circuitry 1428. The further control circuitry comprises switching circuitry to control which piezoelectric elements are able to transmit/receive during a given sequence. In alternative embodiments the switching circuitry may be between the piezoelectric elements and amplification/ADC circuitry. In these alternative embodiments there may be fewer amplification/ADC modules than piezoelectric elements so that only a subset of the piezoelectric elements are simultaneously operable.

[0079] In use, in a transmit mode, drive waveforms generated by the drive circuitry 1424 are conducted through conductive connections to at least one electrode of each piezoelectric element 1450 which is in operation. In a receive mode, ultrasound energy incidence on each piezoelectric element 1450 generates signal which is conducted through respective conductive connections, amplified by the respective amplification circuit 1422 and converted by the respective ADC.

[0080] The machine controller 1430 comprises at least one waveform generator 1470 and a voltage amplifier

1475 which provides control pulses to the ultrasound CMOS control circuitry 1420 through conductors 1440. The machine controller also comprises a processor 1480 connected to further amplification circuitry 1482 for amplifying the received signals. In this embodiment the processor comprises memory 1484 for storing system settings/received signals. The processor further comprises a beamforming module 1486 for beamforming the received signals. The beamforming module 1486 may also carry out filtering/other image processing functions.

[0081] In this embodiment the machine controller is connected to a display device 1490 for displaying the beamformed (and/or non-beamformed) data.

[0082] Throughout the description and claims of this specification, the words "comprise" and "contain" and variations of them mean "including but not limited to", and they are not intended to and do not exclude other components, integers, or steps. Throughout the description and claims of this specification, the singular encompasses the plural unless the context otherwise requires. In particular, where the indefinite article is used, the specification is to be understood as contemplating plurality as well as singularity, unless the context requires otherwise.

[0083] Features, integers, characteristics, or groups described in conjunction with a particular aspect, embodiment, or example of the invention are to be understood to be applicable to any other aspect, embodiment or example described herein unless incompatible therewith. All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive. The invention is not restricted to the details of any foregoing embodiments. The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. An ultrasound device comprising:

a substrate having a first surface and an opposite second surface;
a CMOS control circuit comprising a CMOS metallisation layer on the first surface and
a plurality of transistors integrally provided within the first surface;
a piezoelectric micromachined ultrasound transducer comprising at least one piezoelectric element, wherein the piezoelectric element comprises a moveable piezoelectric diaphragm;
a cavity defined in part by the moveable piezoelectric diaphragm and in part by the substrate;
wherein the moveable piezoelectric diaphragm comprises a piezoelectric body, a first electrode and a second electrode each arranged on the first surface;
wherein the moveable piezoelectric diaphragm defines at least part of a wall of the cavity and is configured to deform into the cavity; and
wherein the CMOS control circuit is configured to control ultrasound transmission by controlling movement of the moveable piezoelectric diaphragm and/or control ultrasound reception by receiving signals resulting from movement of the moveable piezoelectric diaphragm.

2. The ultrasound device according to claim 1 wherein the moveable piezoelectric diaphragm comprises at least part of the CMOS metallisation layer, and optionally wherein the CMOS metallisation layer comprises a conductive connection extending from at least one of the plurality of transistors to at least one of the first and second electrodes of the piezoelectric element.

3. The ultrasound device according to claim 1 or claim 2, further comprising an additional layer on the first surface of the substrate, wherein the moveable piezoelectric diaphragm comprises at least part of the additional layer, wherein the additional layer defines the at least part of the wall of the cavity defined by the moveable piezoelectric diaphragm, and optionally wherein at least part of the CMOS metallisation layer is integrally provided within the additional layer and/or optionally wherein the additional layer comprises CMOS oxide.

4. The ultrasound device according to claim 1,

wherein the at least one piezoelectric element is one of a plurality of piezoelectric elements arranged in an array,
wherein each piezoelectric element comprises a moveable piezoelectric diaphragm, wherein each moveable piezoelectric diaphragm comprises a piezoelectric body, a first electrode and a second electrode arranged on the first surface,
wherein the cavity is one of a plurality of cavities,
wherein each moveable piezoelectric diaphragm defines at least part of a wall of a respective cavity of the plurality of cavities.

5. The ultrasound device according to claim 4, wherein each moveable piezoelectric diaphragm comprises at least part of the CMOS metallisation layer.

6. The ultrasound device according to claim 4 or claim

5, further comprising an additional layer on the first surface of the substrate, wherein each moveable piezoelectric diaphragm comprises at least part of the additional layer, wherein the additional layer defines the at least part of the wall of each cavity defined by the respective moveable piezoelectric diaphragm, and optionally wherein at least part of the CMOS metallisation layer is integrally provided within the additional layer and/or optionally wherein the additional layer comprises CMOS oxide.

7. The ultrasound device according to claim 5 or claim 6 wherein the CMOS metallisation layer comprises, conductive connections extending from at least one of the plurality of transistors to at least one of the first and second electrodes of a respective piezoelectric element, and optionally wherein the lengths of the conductive connections are consistent.

8. The ultrasound device of claim 7, wherein the array comprises a first zone having a first side and a second side opposite to the first side, wherein the plurality of piezoelectric elements are arranged into rows, wherein the conductive connections extend into the array from one or both of the first and second sides between the rows of piezoelectric elements, and optionally wherein the first zone is elongate and the first and second sides correspond to the long sides along the length of the first zone.

9. The ultrasound device of claim 8, wherein the first zone comprises at least a first, a second and third row of piezoelectric elements, wherein a first subset of the conductive connections extend between piezoelectric elements of the first and second row to different respective piezoelectric elements along the length of the second row, and optionally,
wherein a second subset of the conductive connections extend between piezoelectric elements of the second and third row to different respective piezoelectric elements along the length of the second row.

10. The ultrasound device of claim 8 or claim 9, wherein at least part of the CMOS control circuit is arranged in a column adjacent to at least one of the first and second sides of the first zone.

11. The ultrasound device according to claim 10

wherein the CMOS control circuit comprises a drive circuit configured to actuate each moveable piezoelectric diaphragm of at least a subset of the plurality of piezoelectric elements such that an ultrasound signal is transmitted;
wherein the CMOS control circuit comprises a receive circuit for receiving ultrasound signal;
and optionally wherein at least part of the drive circuit and/or at least part of the receive circuit is arranged in the column adjacent to at least one of the first and second sides of the first zone.

12. The ultrasound device according to claim 11,

wherein the CMOS control circuit comprises delay circuitry and/or apodisation circuitry;
wherein the delay circuitry is configured to delay the actuator waveform conducted to one of the piezoelectric elements relative to the actuator waveform conducted to another piezoelectric element, and optionally wherein at least part of the apodisation circuitry is arranged in the column adjacent to at least one of the first and second sides of the first zone;
wherein the apodisation circuitry is configured to increase the amplitude of the actuator waveform conducted to one of the piezoelectric elements relative to the actuator waveform conducted to another piezoelectric element, and optionally wherein at least part of the apodisation circuitry is arranged in the column adjacent to at least one of the first and second sides of the first zone.

13. The ultrasound device according to claim 11 or 12,

wherein the CMOS control circuit comprises amplification circuitry for amplifying the received ultrasound signal,
and optionally wherein the amplification circuitry is configured to amplify the received signal based on the depth at which the received signal has been reflected from,
and optionally wherein at least part of the amplification circuitry is arranged in the column adjacent to at least one of the first and second sides of the first zone.

14. A wearable device comprising the ultrasound device of any preceding claim.

15. A method of forming an ultrasound device according to any preceding claim, wherein the ultrasound device comprises a piezoelectric micromachined ultrasound transducer comprising n piezoelectric elements;

forming n cavities within a substrate, wherein the substate has a first surface and an opposite second surface;
forming a plurality of transistors within the first surface;
forming a CMOS metallisation layer on the first surface;
and
forming n moveable piezoelectric diaphragms;
wherein each cavity is defined in part by the substrate and in part by one of the n moveable

piezoelectric diaphragms.

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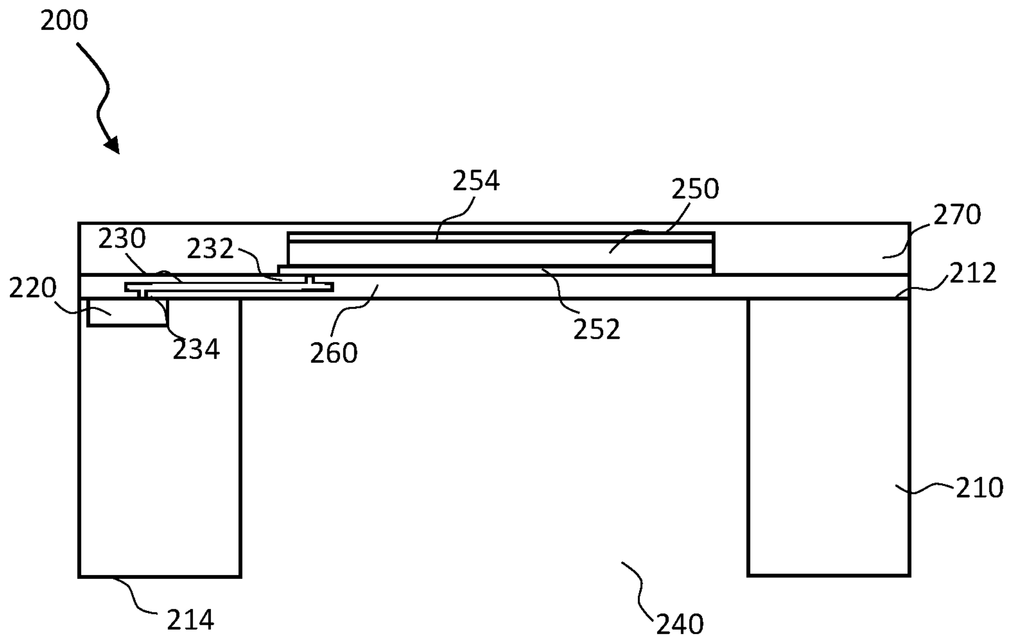

Fig. 2

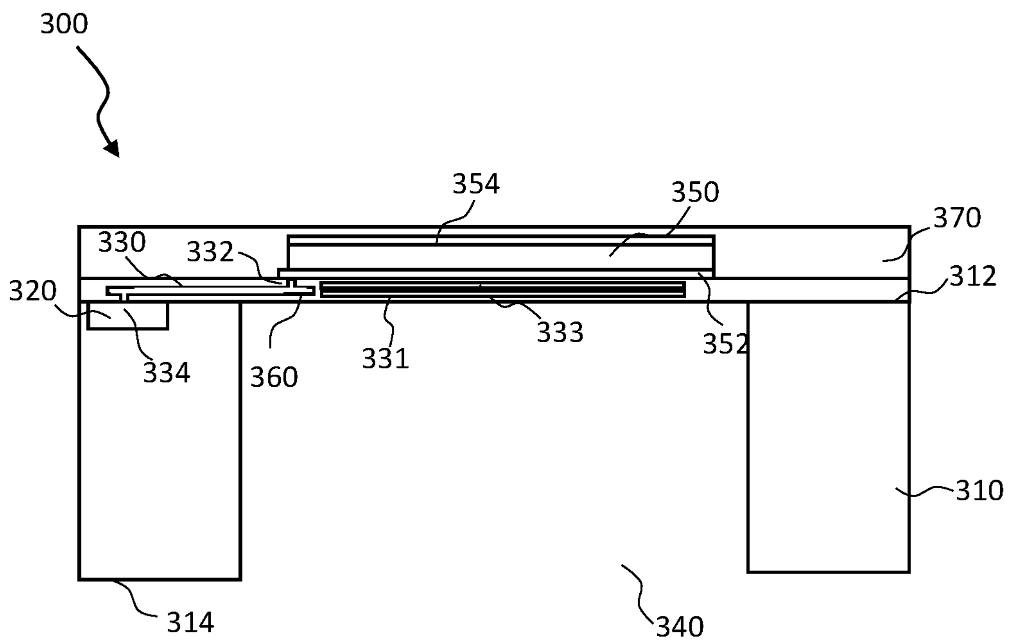

Fig. 3

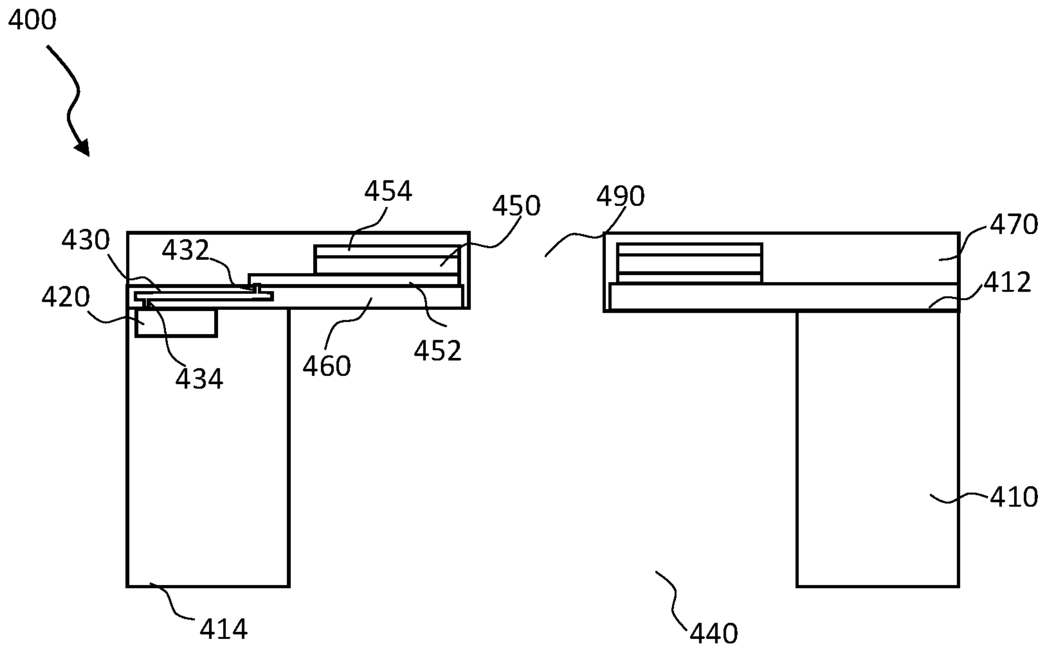

Fig. 4

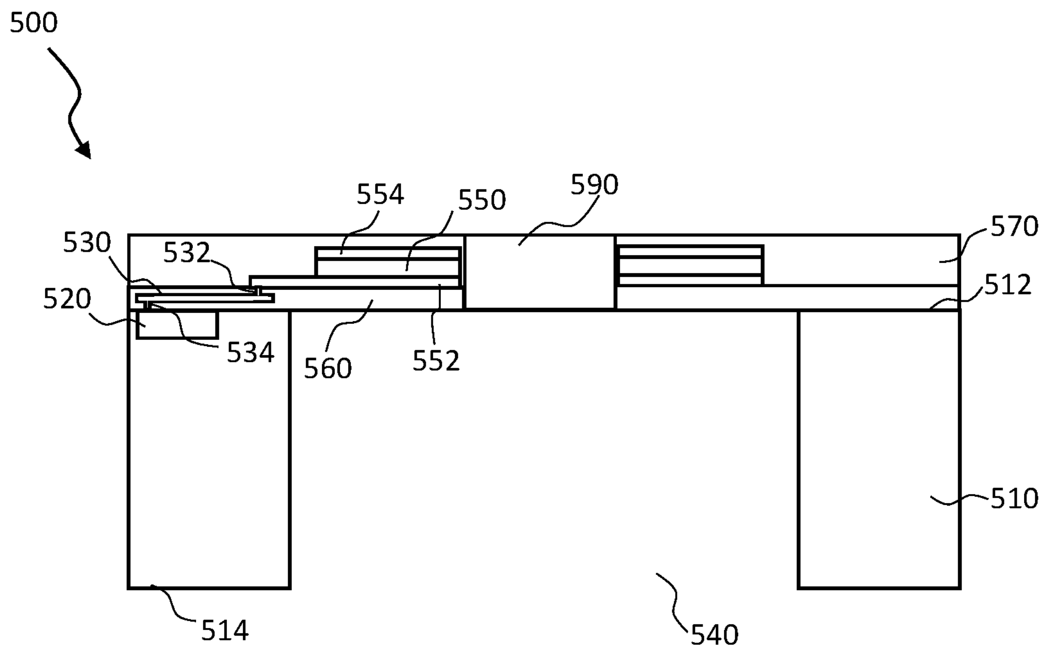

Fig. 5

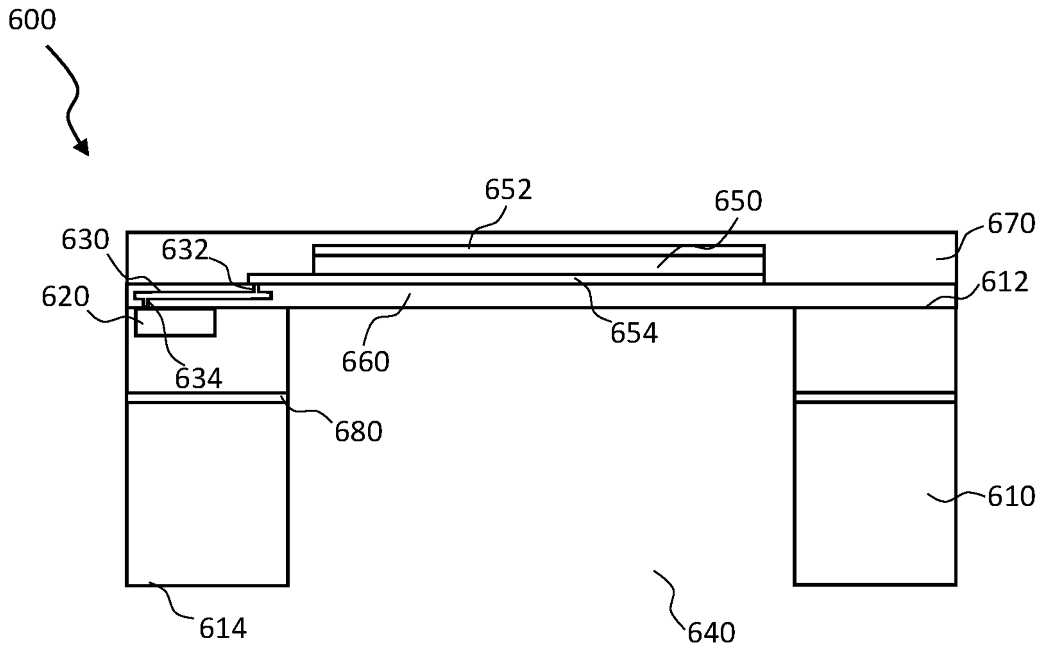

Fig. 6

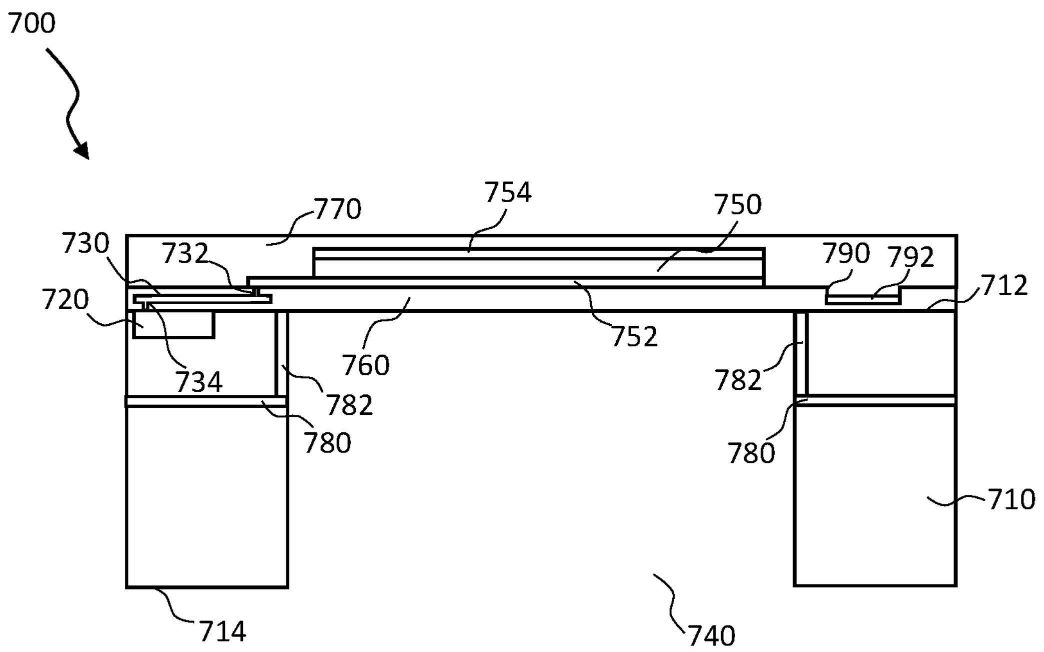

Fig. 7

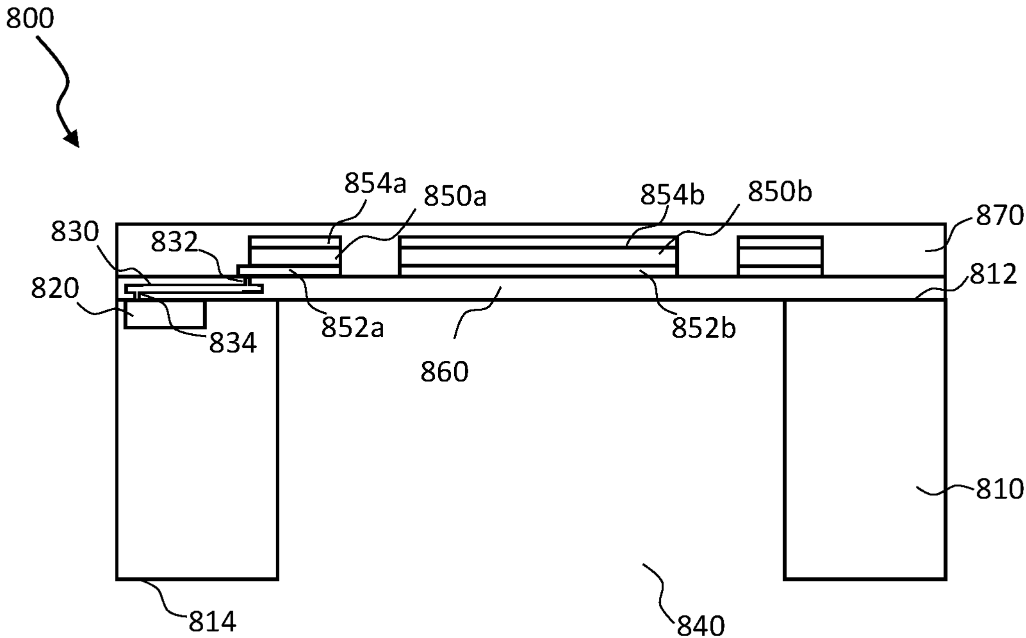

Fig. 8

Fig. 9

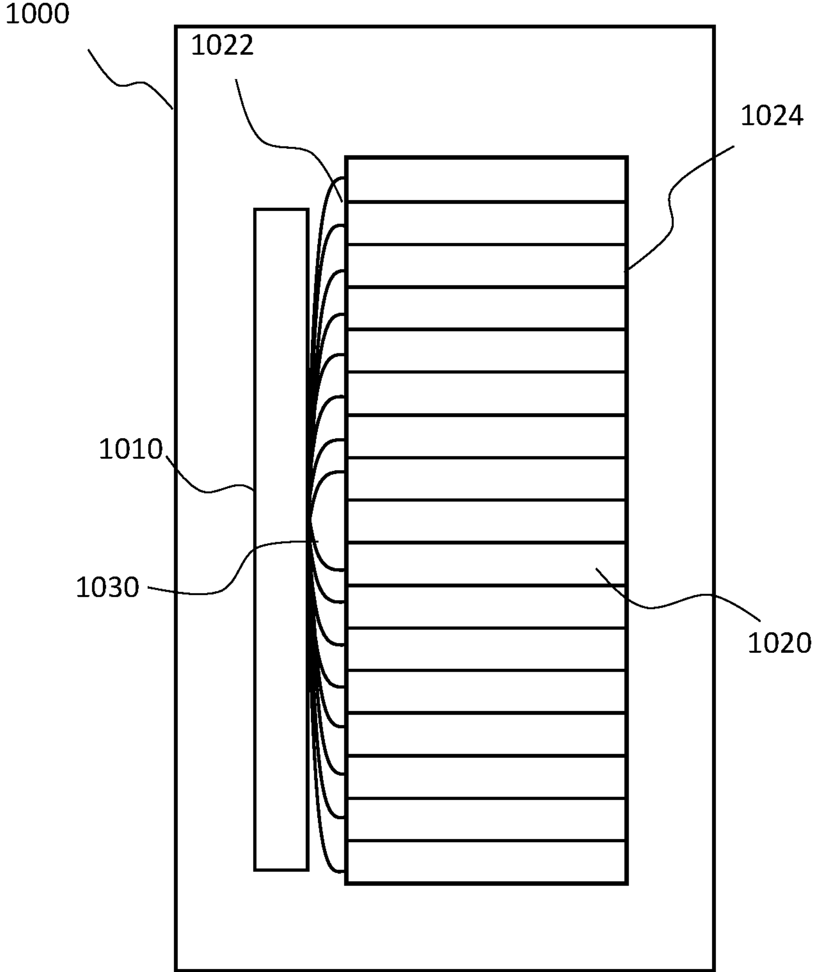

Fig. 10

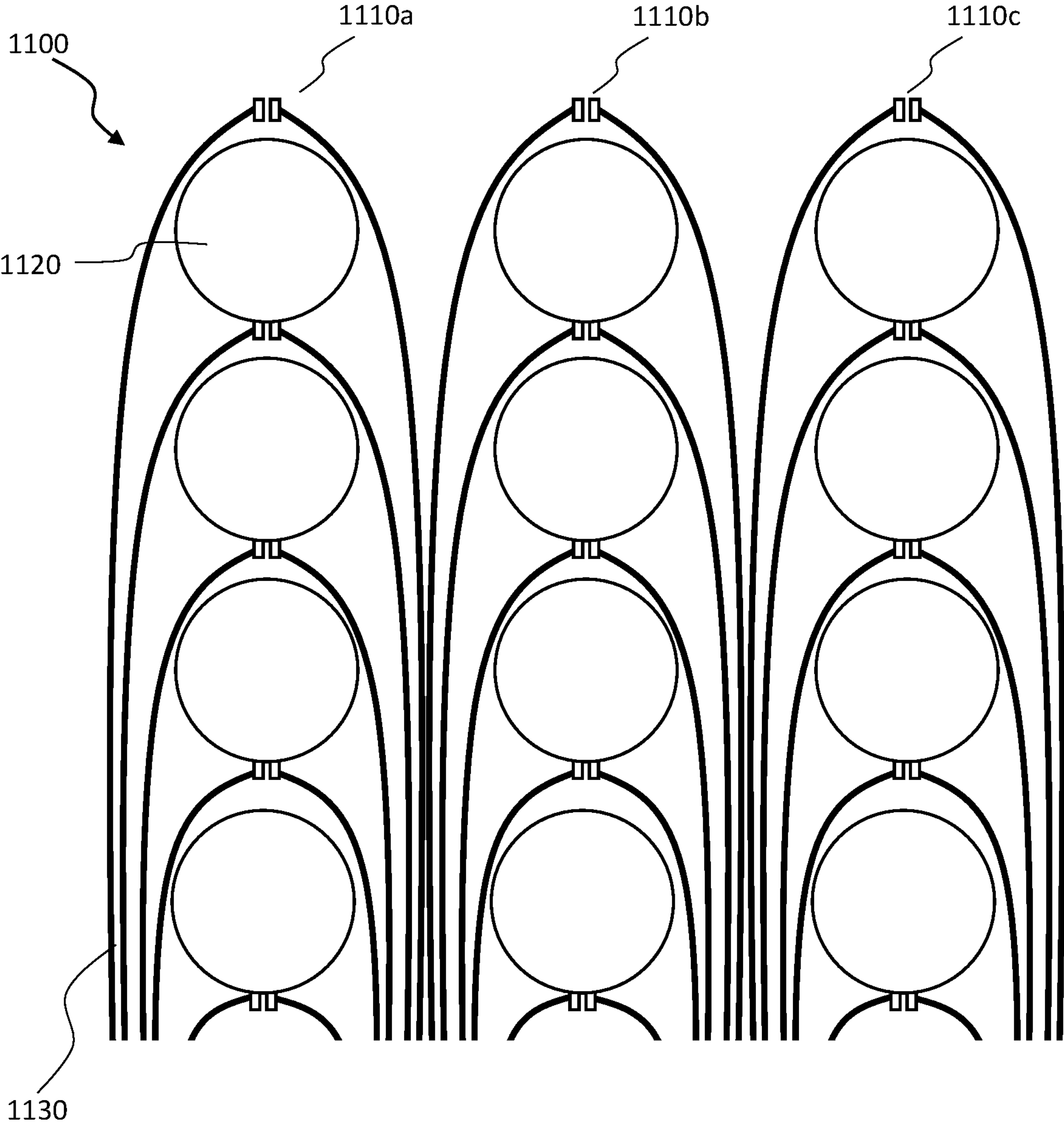

Fig. 11

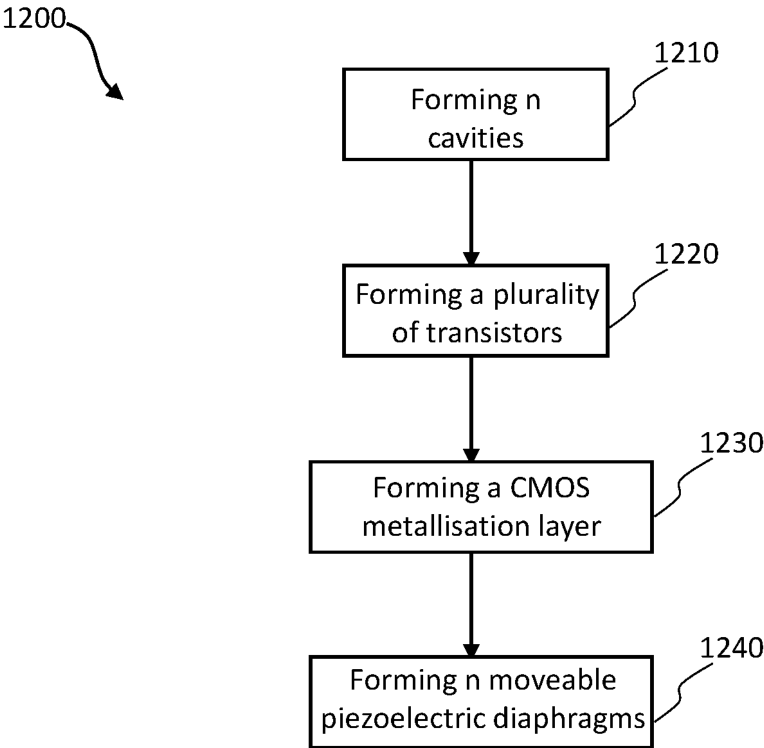

Fig. 12

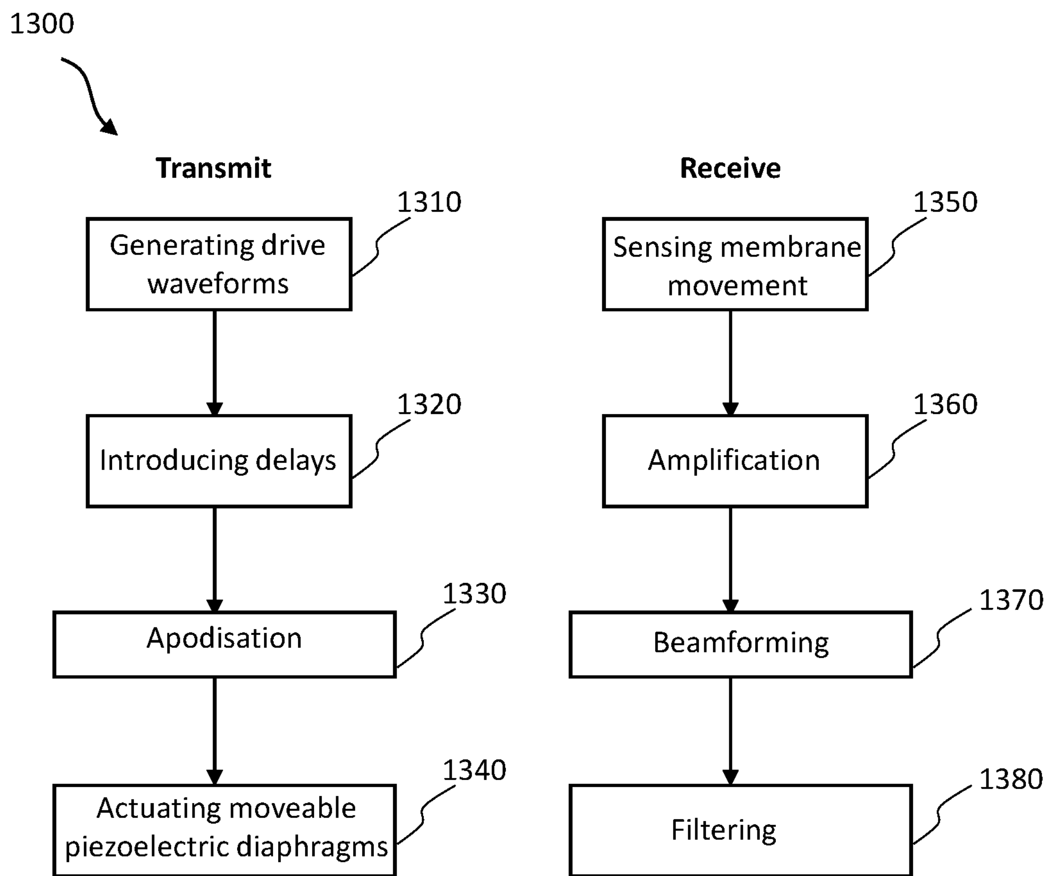

Fig. 13

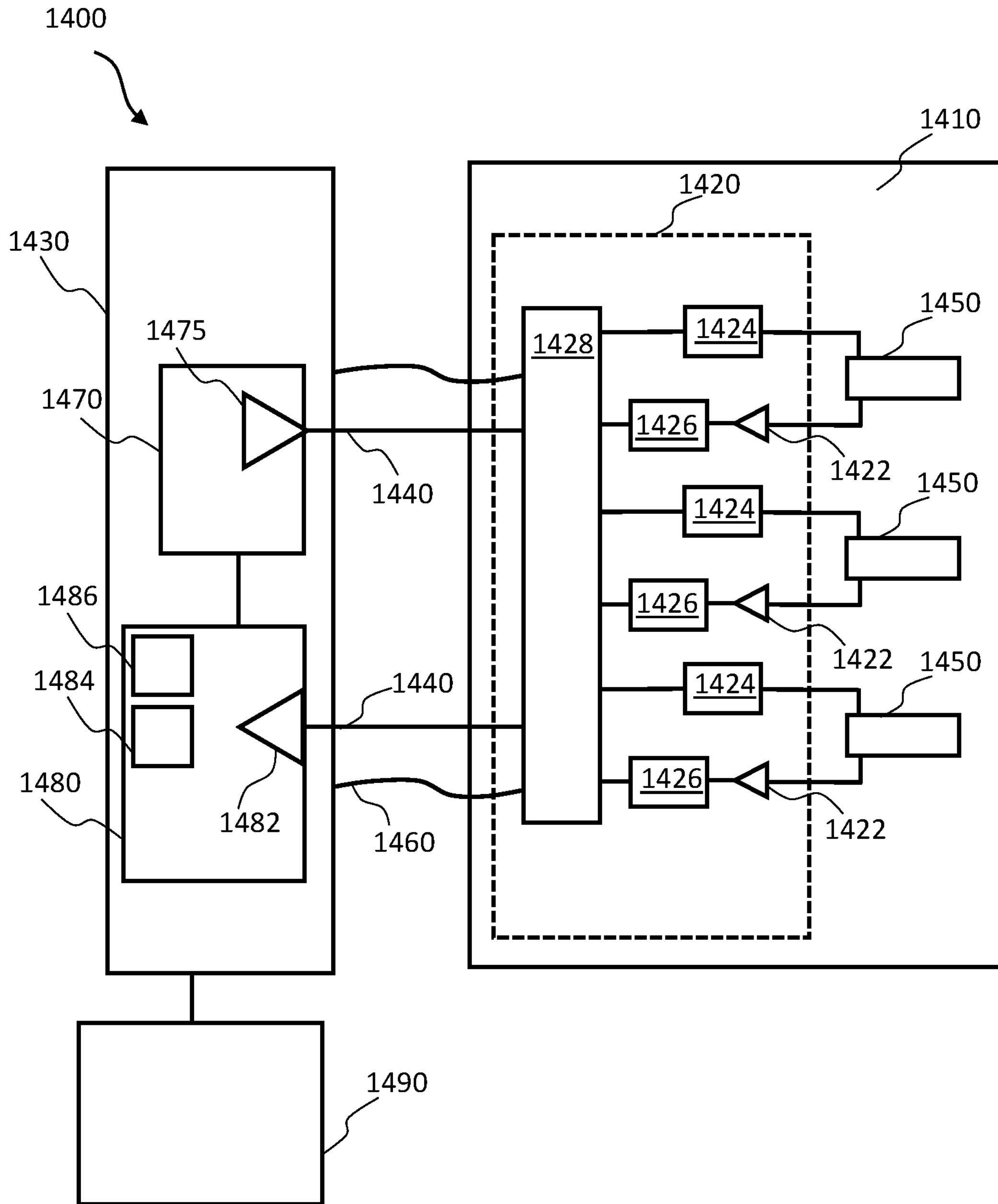

Fig. 14

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Application Number
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	11 March 2024	Meyer, Matthias

CATEGORY OF CITED DOCUMENTS

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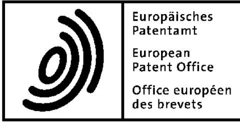

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page 2 of 2

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