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(54) **PRINTED CIRCUIT BOARD**

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(52) **U.S. Cl.** **174/261**

(57) **ABSTRACT**

A printed circuit board having an insulating layer; circuit patterns formed on both surfaces of the insulating layer in order to be embedded in the insulating layer; and a bump formed to pass through the insulating layer in order to electrically connect the circuit patterns formed on both surfaces of the insulating layer.

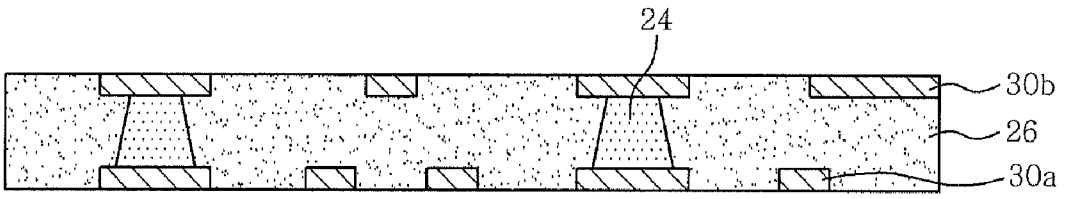


FIG. 1A

Prior Art

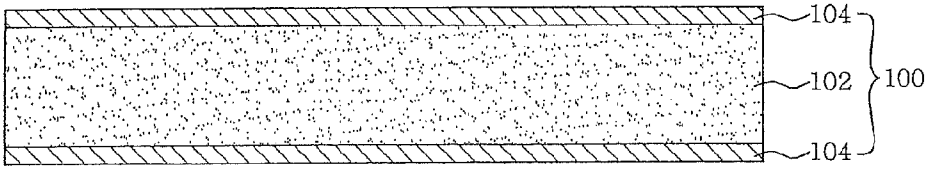


FIG. 1B

Prior Art

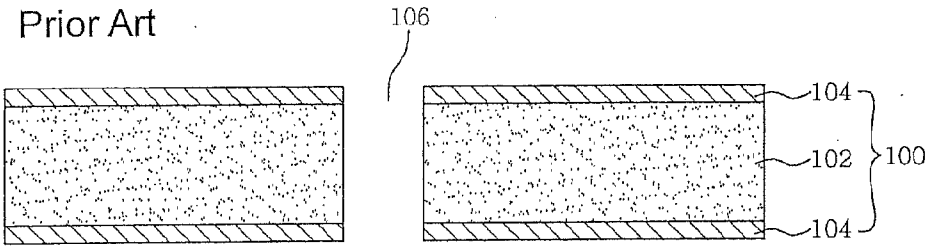


FIG. 1C

Prior Art

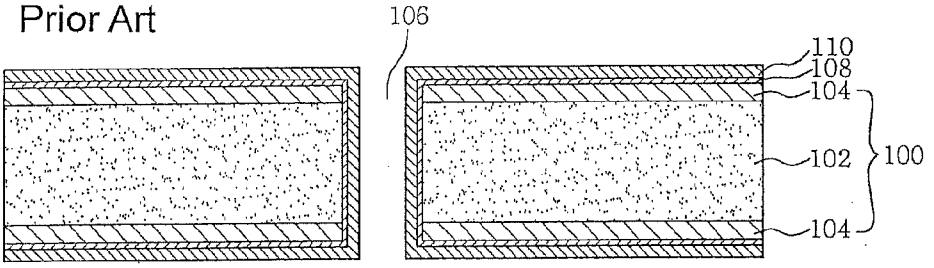


FIG. 1D

Prior Art

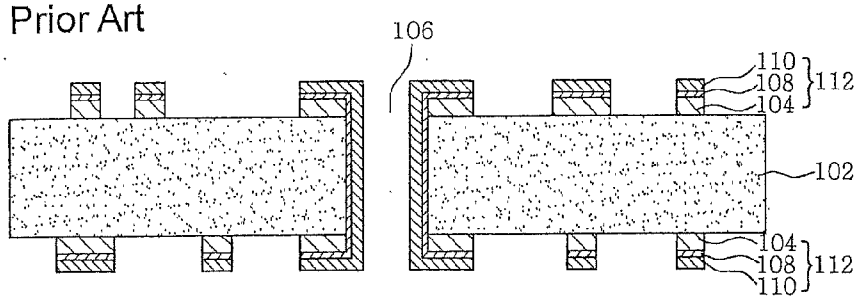


FIG. 2

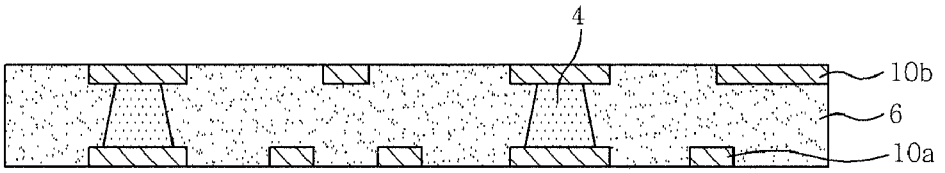


FIG. 3A

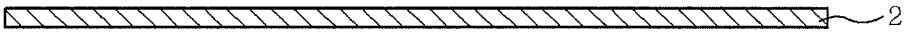


FIG. 3B

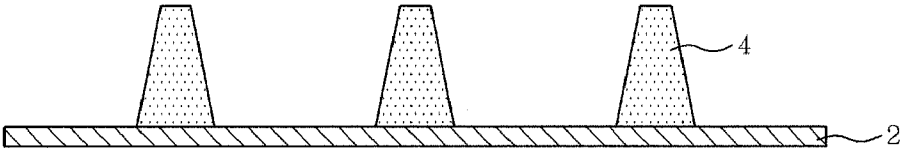


FIG. 3C

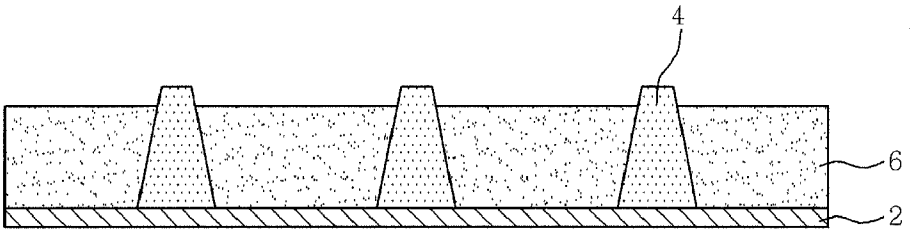


FIG. 3D

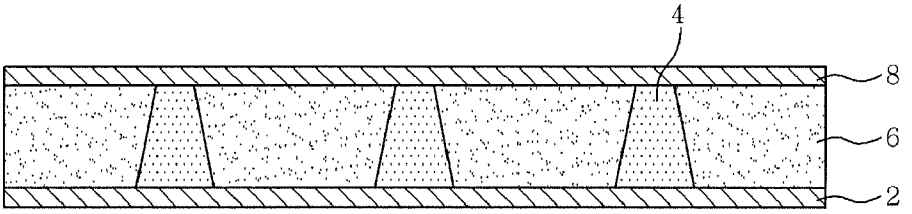


FIG.3E

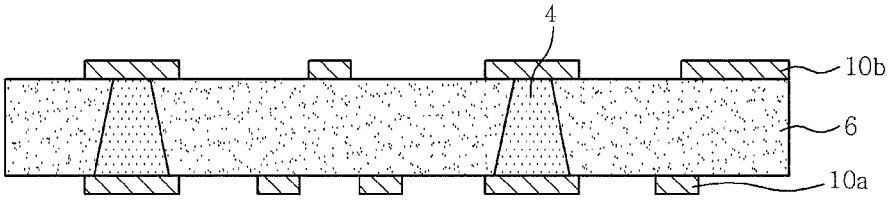


FIG.3F

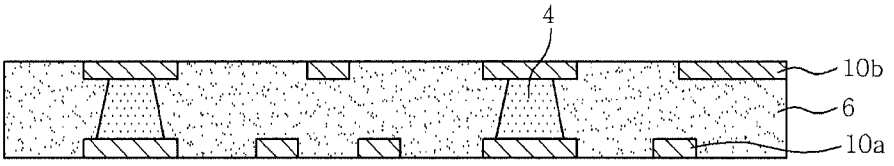


FIG.4A

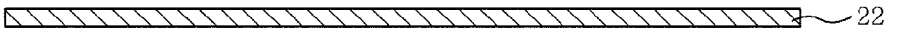


FIG.4B

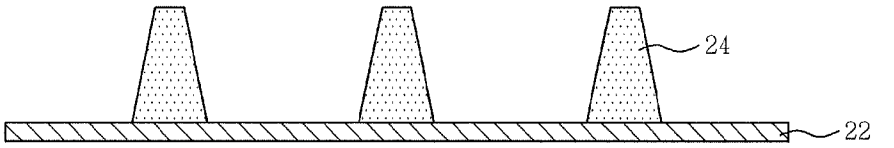


FIG.4C

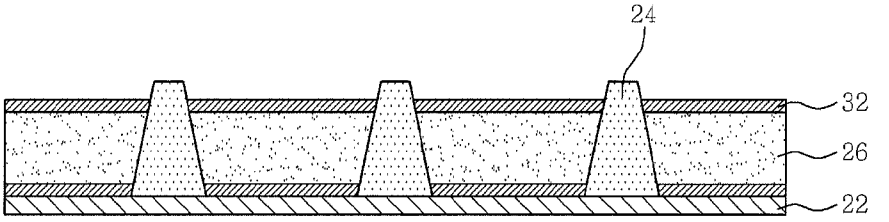


FIG. 4D

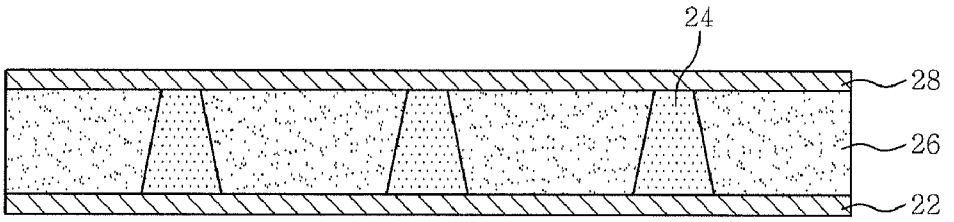


FIG. 4E

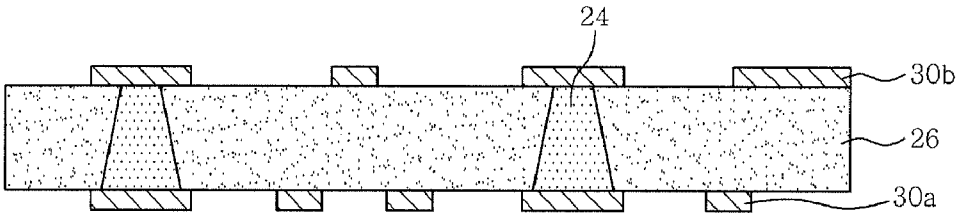
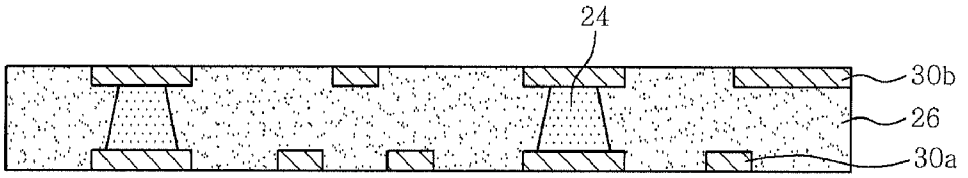


FIG. 4F



PRINTED CIRCUIT BOARD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a U.S. divisional application filed under 37 USC 1.53(b) claiming priority benefit of U.S. Ser. No. 12/073,712 filed in the United States on Mar. 7, 2008, which claims earlier priority benefit to Korean Patent Application Nos. 10-2007-0052162, filed on May 29, 2007, entitled "Fabricating Method of Printed Circuit Board" and 10-2007-0121026, filed on Nov. 26, 2007, entitled "Printed circuit board and method for fabricating thereof", which are hereby incorporated by reference in their entirety into this application.

BACKGROUND

[0002] 1. Field

[0003] The present invention relates, in general, to a printed circuit board (PCB) and a method of fabricating the same, and more particularly, to a PCB and a method of fabricating the same, in which the thickness of a circuit pattern is decreased to thus realize a fine circuit, the circuit pattern is embedded in an insulating layer to thus decrease the thickness of a PCB, and the time and cost required for the process of fabricating a PCB are decreased.

[0004] 2. Description of the Related Art

[0005] According to the trend in which an electronic product is fabricated to be light, slim, short and small and to have multiple functions, a package mounted to the electronic product need be thin. Thus, a substrate, which is an important component of the package, is required to be thin and to have high density.

[0006] FIGS. **1**A to **1**D are sectional views sequentially illustrating the process of fabricating a PCB according to a conventional technique.

[0007] As illustrated in FIG. **1**A, a metal layer laminate **100**, in which a metal layer **104** is laminated on both surfaces of an insulating layer **102**, is prepared.

[0008] Next, as illustrated in FIG. **1**B, a via hole **106** is formed through the metal layer laminate by drilling.

[0009] After the formation of the via hole **106**, an electroless copper plating layer **108** and a copper electroplating layer **110** are formed on the inner wall of the via hole **106** and on the metal layer **104** through electroless copper plating and copper electroplating, as illustrated in FIG. **1**C.

[0010] After the formation of the electroless copper plating layer **108** and the copper electroplating layer **110**, a dry film (not shown) is applied on the copper electroplating layer **110**, and the portion of the dry film other than the portion of the dry film corresponding to a circuit pattern is removed through exposure and development.

[0011] Next, the copper electroplating layer **110**, exposed by removing the portion of the dry film, the electroless copper plating layer **108**, and the metal layer **104** are etched using an etchant, thus forming a circuit pattern **112** on both surfaces of the insulating layer **102**, as illustrated in FIG. **1**D.

[0012] However, the method of fabricating the PCB according to the conventional technique is disadvantageous because the circuit pattern **112**, composed of the metal layer **104**, the electroless copper plating layer **108**, and the copper electroplating layer **110**, is formed on both surfaces of the insulating layer **102**, and thus the circuit pattern **110** is thick, and also, the circuit pattern **112** is formed to be exposed on both surfaces of the insulating layer **102**, undesirably increasing the thickness of the PCB.

[0013] Further, the method of fabricating the PCB according to the conventional technique is disadvantageous because the circuit pattern **112** is composed of the metal layer **104**, the electroless copper plating layer **108** and the copper electroplating layer **110**, and thus, upon the formation of the circuit pattern **112**, the over-etching of the outer portion of the circuit pattern **112** or the under-etching of the inner portion of the circuit pattern **112** may occur, making it difficult to realize a predetermined width, that is, a pitch, between adjacent circuit patterns, with the result that a fine circuit is not realized.

[0014] Furthermore, the method of fabricating the PCB according to the conventional technique is disadvantageous because the circuit pattern is formed using electroless copper plating and copper electroplating, undesirably increasing the time required for the process of fabricating a PCB.

SUMMARY

[0015] Therefore, the present invention provides a PCB and a method of fabricating the same, in which the thickness of a circuit pattern is decreased, thus realizing a fine circuit, and the circuit pattern is embedded in an insulating layer, thus decreasing the thickness of the PCB.

[0016] In addition, the present invention provides a PCB and a method of fabricating the same, in which the time and cost required for the process of fabricating a PCB are decreased.

[0017] According to the present invention, a PCB may include an insulating layer; circuit patterns formed on both surfaces of the insulating layer in order to be embedded in the insulating layer; and a bump formed to pass through the insulating layer in order to electrically connect the circuit patterns formed on both surfaces of the insulating layer.

[0018] In the PCB according to the present invention, the circuit patterns and the insulating layer may be adhered using an adhesive.

[0019] In the PCB according to the present invention, the adhesive may have a glass transition temperature lower than that of the insulating layer.

[0020] In addition, according to the present invention, a method of fabricating a PCB may include a) forming a bump on a first metal layer; b) laminating an insulating layer on the bump so that the bumps passes through the insulating layer; c) placing a second metal layer on the insulating layer and then conducting heating and pressing, thus laminating the second metal layer on the insulating layer; d) etching the first metal layer and the second metal layer, thus forming circuit patterns on both surfaces of the insulating layer; and e) heating and pressing both surfaces of the insulating layer, thus embedding the circuit patterns in the insulating layer.

[0021] In the method of fabricating the PCB according to the present invention, the a) may include a-1) preparing the first metal layer; a-2) placing a mask having a hole on the first metal layer to be in close contact therewith, in which the hole is formed at a position corresponding to an area to which the bump is to be formed; a-3) filling the hole with a conductive paste using a squeegee; a-4) removing the mask; and a-5) drying the conductive paste, thus forming the bump.

[0022] In the method of fabricating the PCB according to the present invention, the c) may be conducted by heating and pressing both surfaces of the PCB under conditions of 50~150° C. and 1~30 kgf/cm^2.

[0023] In the method of fabricating the PCB according to the present invention, the e) may be conducted by heating and pressing the circuit patterns under conditions of temperature and pressure which are higher than in the c), thus embedding the circuit patterns in the insulating layer.

[0024] In the method of fabricating the PCB according to the present invention, the e) may be conducted by heating and pressing the circuit patterns under conditions of 150~300° C. and 30~50 kgf/cm^2.

[0025] In the method of fabricating the PCB according to the present invention, the b) may include b-1) applying an adhesive on both surfaces of the insulating layer; and b-2) laminating the insulating layer having the adhesive applied on both surfaces thereof on the bump so that the bump passes through the adhesive and the insulating layer.

[0026] In the method of fabricating the PCB according to the present invention, the c) may include melting the adhesive using heat applied to both surfaces of the PCB to thus adhere the first metal layer and the second metal layer to both surfaces of the insulating layer.

[0027] In the method of fabricating the PCB according to the present invention, the e) may include curing the insulating layer and the adhesive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0029] FIGS. **1**A to **1**D are sectional views sequentially illustrating the process of fabricating a PCB according to a conventional technique;

[0030] FIG. **2** is a view illustrating the PCB according to the present invention;

[0031] FIGS. **3**A to **3**F are sectional views sequentially illustrating the process of fabricating a PCB according to a first embodiment of the present invention; and

[0032] FIGS. **4**A to **4**F are sectional views sequentially illustrating the process of fabricating a PCB according to a second embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0033] Hereinafter, a detailed description will be given of the preferred embodiments of the present invention, with reference to the appended drawings.

[0034] FIG. **2** is a view illustrating the PCB according to the present invention.

[0035] With reference to FIG. **2**, the PCB according to the present invention includes an insulating layer **6**, circuit patterns **10***a*, **10***b* formed on both surfaces of the insulating layer **6** in order to be embedded in the insulating layer, and bumps **4** formed to pass through the insulating layer **6** in order to electrically connect the circuit patterns **10***a*, **10***b* formed on both surfaces of the insulating layer **6**.

[0036] The insulating layer **6** is formed of an epoxy resin, and plays a role in electrically isolating the circuit patterns **10***a*, **10***b* formed on both surfaces thereof.

[0037] The circuit patterns **10***a*, **10***b* are formed on both surfaces of the insulating layer **6** so that they are embedded in the insulating layer **6**.

[0038] The circuit patterns **10***a*, **10***b* are formed from a metal layer.

[0039] The insulating layer **6** and the circuit patterns **10***a*, **10***b* are adhered using an epoxy-based adhesive having Tg (glass transition temperature) lower than that of the insulating layer **6**.

[0040] The bumps **4** are formed to pass through the insulating layer **6**, thus electrically connecting the circuit patterns **10***a*, **10***b*, which are formed on both sides of the insulating layer **6**.

[0041] FIGS. **3**A to **3**F are sectional views sequentially illustrating the process of fabricating a PCB according to a first embodiment of the present invention.

[0042] As illustrated in FIG. **3**A, a first metal layer **2** is prepared.

[0043] As the first metal layer **2**, a copper foil is used.

[0044] Next, bumps **4** are formed on the first metal layer **2**, as illustrated in FIG. **3**B.

[0045] Useful for interlayer connection, the bumps **4** are formed by placing a mask having holes on the first metal layer **2** to be in close contact therewith, in which the holes are formed at positions corresponding to areas to which the bumps **4** are to be formed, printing a conductive paste using a squeegee to thus fill the holes with the conductive paste, and then removing the mask.

[0046] Because the conductive paste has high viscosity, when the conductive paste is printed and is then dried, the bumps **4** are formed.

[0047] When the bumps **4** are formed, the printing and drying of the conductive paste are repeated several times (e.g., three or four times), thus adjusting the height of the bumps **4**.

[0048] After the formation of the bumps **4**, an insulating layer **6** is laminated on the bumps **4**, as illustrated in FIG. **3**C.

[0049] As the insulating layer **6**, a prepreg or an epoxy resin in a semi-cured state is used, and the insulating layer **6** is laminated on the bumps **4** so that the bumps **4** pass through the insulating layer **6**.

[0050] After the lamination of the insulating layer **6**, a second metal layer **8** is placed on the insulating layer **6**, and is then heated and pressed using a first press, by which the second metal layer **8**, for example, a copper foil, is laminated on the insulating layer **6**, as illustrated in FIG. **3**D.

[0051] As such, the insulating layer **6** is maintained in a semi-cured state.

[0052] When the second metal layer **8** is laminated using the first press, both surfaces of the PCB, that is, the first metal layer **2** and the second metal layer **8**, are heated and pressed under conditions of 50~150° C. and 1~30 kgf/cm^2, by which the second metal layer **8** is laminated on the insulating layer **6**.

[0053] After the lamination of the second metal layer **8**, a dry film (not shown) is applied on the first metal layer **2** and the second metal layer **8**, and the portion of the dry film other than the portion of the dry film corresponding to a circuit pattern is removed through exposure and development.

[0054] Next, the first metal layer **2** and the second metal layer **8** are etched using an etchant, thus forming circuit patterns **10***a*, **10***b* on both surfaces of the insulating layer **6**, as illustrated in FIG. **3**E.

[0055] After the formation of the circuit patterns **10***a*, **10***b*, the dry film, remaining on the circuit patterns **10***a*, **10***b*, is removed.

[0056] Next, the PCB having the circuit patterns **10***a*, **10***b* is heated and pressed using a second press, thus embedding the circuit patterns **10***a*, **10***b* in the insulating layer **6**.

[0057] As such, the outer surfaces of the circuit patterns **10***a*, **10***b* are flush with the insulating layer **6**.

[0058] Specifically, the circuit patterns **10***a*, **10***b* are embedded in the insulating layer **6** so that the outer surfaces of the circuit patterns **10***a*, **10***b* embedded in the insulating layer **6** are flush with the surface of the insulating layer **6**.

[0059] The circuit patterns **10***a*, **10***b* are heated and pressed using the second press under conditions of 150~300° C. and 30~50 kgf/cm^2, which are higher than when using the first press, thus embedding the circuit patterns **10***a*, **10***b* in the insulating layer **6**.

[0060] As such, the insulating layer **6** in a semi-cured state is cured.

[0061] In the method of fabricating the PCB according to the first embodiment of the present invention using B2it (Buried Bump Interconnection Technology), because the circuit patterns **10***a*, **10***b* are composed exclusively of the metal layers **2**, **8**, the thickness of the circuit patterns **10***a*, **10***b* may be decreased. Hence, when the metal layers **2**, **8** are etched to form the circuit patterns **10***a*, **10***b*, it is possible to prevent the over-etching of the outer portions of the circuit patterns **10***a*, **10***b* and the under-etching of the inner portions of the circuit patterns **10***a*, **10***b*, thereby realizing a fine circuit.

[0062] In the method of fabricating the PCB according to the first embodiment of the present invention, the circuit patterns **10***a*, **10***b* are embedded in the insulating layer **6**, thus decreasing the thickness of the PCB.

[0063] In the method of fabricating the PCB according to the first embodiment of the present invention, electroless copper plating and copper electroplating are not conducted upon the formation of the circuit patterns **10***a*, **10***b*, thus decreasing the time and cost required for the process of fabricating the PCB.

[0064] FIGS. **4**A to **4**F are sectional views sequentially illustrating the process of fabricating a PCB according to a second embodiment of the present invention.

[0065] As illustrated in FIG. **4**A, a first metal layer **22** is prepared.

[0066] As the first metal layer **22**, a copper foil is used.

[0067] Next, bumps **24** are formed on the first metal layer **22**, as illustrated in FIG. **4**B.

[0068] Useful for interlayer connection, the bumps **24** are formed by placing a mask having holes on the first metal layer **22** to be in close contact therewith, in which the holes are formed at positions corresponding to areas to which the bumps **24** are to be formed, printing a conductive paste using a squeegee to thus fill the holes with the conductive paste, and then removing the mask.

[0069] Because the conductive paste has high viscosity, when the conductive paste is printed and is then dried, the bumps **24** are formed.

[0070] When the bumps **24** are formed, the printing and drying of the conductive paste are repeated several times (e.g., three or four times), thus adjusting the height of the bumps **24**.

[0071] After the formation of the bumps **24**, an insulating layer **26**, both surfaces of which are coated with an adhesive **32**, is laminated on the bumps **24**, as illustrated in FIG. **4**C.

[0072] Specifically, the adhesive **32** is applied on both surfaces of the insulating layer **26**, after which the insulating layer **26** having the adhesive **32** applied on both surfaces thereof is laminated on the bumps **24**.

[0073] The adhesive **32** is exemplified by an epoxy-based product having Tg lower than that of the insulating layer **26**, in order to increase the force of adhesion between a circuit pattern, which is subsequently formed, and the insulating layer **26**. The insulating layer **26** is formed of an epoxy resin in a semi-cured state.

[0074] In the lamination of the insulating layer **26** of FIG. **4**C, the bumps **24** are formed to pass through the insulating layer **26** and the adhesive **32**.

[0075] After the lamination of the insulating layer **26**, a second metal layer **28** is placed on the insulating layer **26**, and is then heated and pressed using a first press, by which the second metal layer **28** is laminated on the insulating layer **26**, as illustrated in FIG. **4**D.

[0076] As such, the insulating layer **26** is maintained in a semi-cured state.

[0077] When the second metal layer **28** is laminated using the first press, both surfaces of the PCB, that is, the first metal layer **22** and the second metal layer **28**, are heated and pressed under conditions of 50~150° C. and 1~30 kgf/cm^2, by which the second metal layer **28** is laminated on the insulating layer **26**.

[0078] At this time, the adhesive **32** applied on both surfaces of the insulating layer **26** is melted by heat from the first press, such that the first metal layer **22** and the second metal layer **28** are adhered to both surfaces of the insulating layer **26**.

[0079] The force of adhesion between the insulating layer **26** and the first metal layer **22** or the second metal layer **28** is increased thanks to the adhesive **32**.

[0080] After the lamination of the second metal layer **28**, a dry film (not shown) is applied on the first metal layer **22** and the second metal layer **28**, and the portion of the dry film other than the portion of the dry film corresponding to circuit patter electroless copper plating and copper electroplating n is removed through exposure and development.

[0081] Next, the first metal layer **22** and the second metal layer **28** are etched using an etchant, thus forming circuit patterns **30***a*, **30***b* on both surfaces of the insulating layer **26**, as illustrated in FIG. **4**E.

[0082] After the formation of the circuit patterns **30***a*, **30***b*, the dry film, remaining on the circuit patterns **30***a*, **30***b*, is removed.

[0083] Next, the PCB having the circuit patterns **30***a*, **30***b* is heated and pressed using a second press, thus embedding the circuit patterns **30***a*, **30***b* in the insulating layer **26**.

[0084] As such, the outer surfaces of the circuit patterns **30***a*, **30***b* are flush with the insulating layer **26**.

[0085] Specifically, the circuit patterns **30***a*, **30***b* are embedded in the insulating layer **26** so that the outer surfaces of the circuit patterns **30***a*, **30***b* embedded in the insulating layer **26** are flush with the surface of the insulating layer **26**.

[0086] The circuit patterns **30***a*, **30***b* are heated and pressed using the second press under conditions of 150~300° C. and 30~50 kgf/cm^2, which are higher than when using the first press, thus embedding the circuit patterns **30***a*, **30***b* in the insulating layer **26**.

[0087] As such, the insulating layer **26** in a semi-cured state and the adhesive **32** applied on both surfaces of the insulating layer are cured.

[0088] In the method of fabricating the PCB according to the second embodiment of the present invention using B2it, because the circuit patterns **30***a*, **30***b* are composed exclusively of the metal layers **22**, **28**, the thickness of the circuit patterns **30***a*, **30***b* may be decreased. Thus, when the metal layers **22**, **28** are etched to form the circuit patterns **30***a*, **30***b*,

it is possible to prevent over-etching of the outer portions of the circuit patterns **30***a*, **30***b* and under-etching of the inner portions of the circuit patterns **30***a*, **30***b*, thereby realizing a fine circuit.

[0089] In the method of fabricating the PCB according to the second embodiment of the present invention, because the insulating layer **26** and the circuit patterns **30***a*, **30***b* are adhered using the adhesive **32** applied on both surfaces of the insulating layer **26**, the force of adhesion between the insulating layer **26** and the circuit patterns **30***a*, **30***b* is greater than that of the PCB formed through the method of fabricating a PCB according to the first embodiment of the present invention.

[0090] In the method of fabricating the PCB according to the second embodiment of the present invention, the circuit patterns **30***a*, **30***b* are embedded in the insulating layer **26**, thus decreasing the thickness of the PCB, and furthermore, the force of adhesion between the circuit patterns **30***a*, **30***b* and the insulating layer **26** may be increased thanks to the adhesive **32**, which is applied on both surfaces of the insulating layer **26**.

[0091] In the method of fabricating the PCB according to the second embodiment of the present invention, electroless copper plating and copper electroplating are not conducted upon the formation of the circuit patterns **30***a*, **30***b*, thus decreasing the time and cost required for the process of fabricating a PCB.

[0092] As described hereinbefore, the present invention provides a PCB and a method of fabricating the same. According to the present invention, because a circuit pattern is composed solely of a metal layer, the thickness of the circuit pattern can be decreased. Thus, when the metal layer is etched to form the circuit pattern, over-etching of the outer portion of the circuit pattern and under-etching of the inner portion of the circuit pattern can be prevented, thereby realizing a fine circuit.

[0093] Further, according to the present invention, because the circuit pattern is embedded in an insulating layer, the thickness of the PCB can be decreased and the force of adhesion between the circuit pattern and the insulating layer can be increased thanks to the adhesive, which is applied on both surfaces of the insulating layer.

[0094] Furthermore, according to the present invention, because electroless copper plating and copper electroplating are not conducted upon the formation of the circuit pattern, the time and cost required for the process of fabricating a PCB can be reduced.

[0095] Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible within the technical spirit of the invention.

What is claimed is:

1. A printed circuit board, comprising:

an insulating layer;

circuit patterns formed on both surfaces of the insulating layer in order to be embedded in the insulating layer; and

a bump formed to pass through the insulating layer in order to electrically connect the circuit patterns formed on both surfaces of the insulating layer.

2. The printed circuit board as set forth in claim **1**, wherein the circuit patterns and the insulating layer are adhered using an adhesive.

3. The printed circuit board as set forth in claim **2**, wherein the adhesive has a glass transition temperature lower than that of the insulating layer.

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