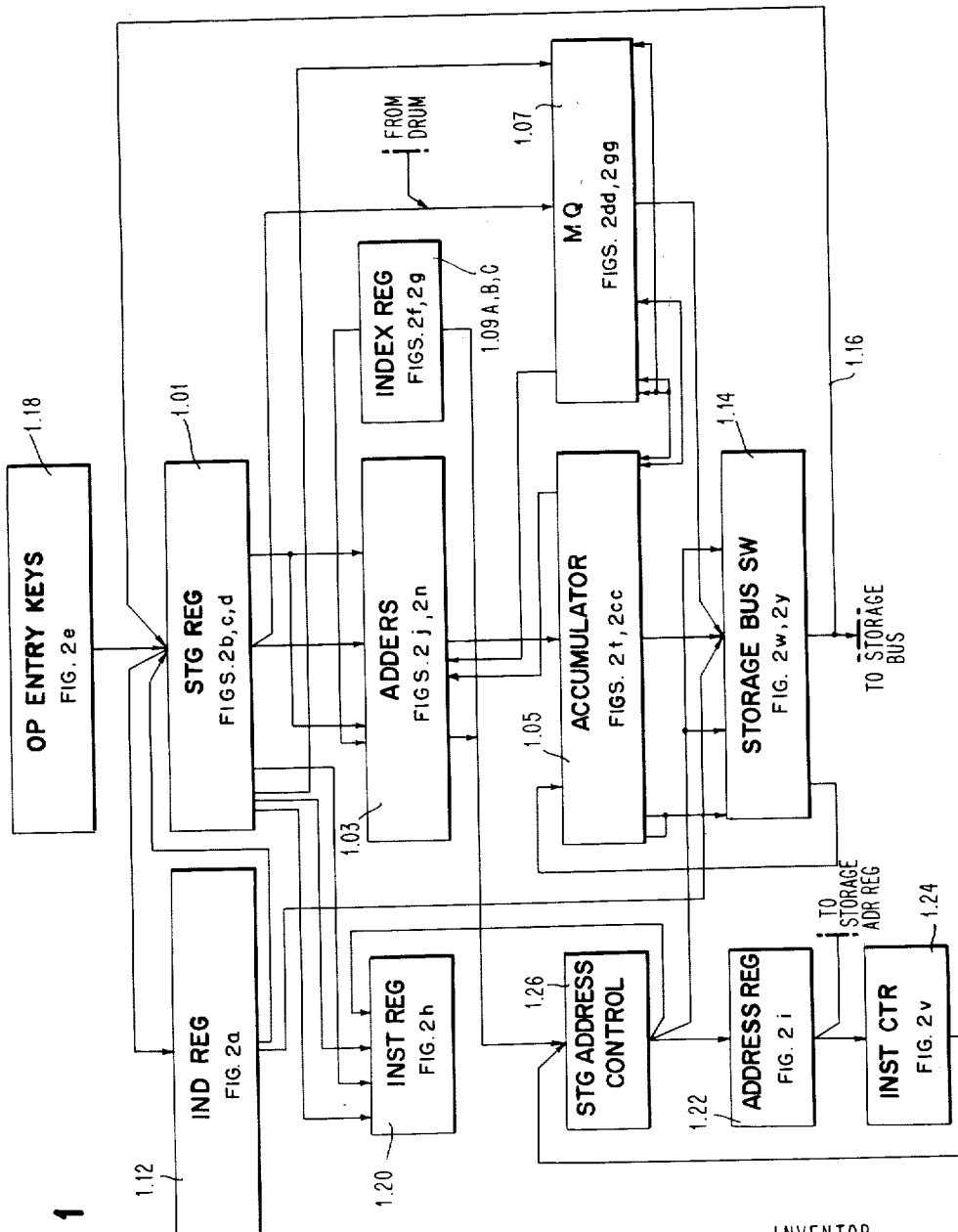


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**FIG. 1**



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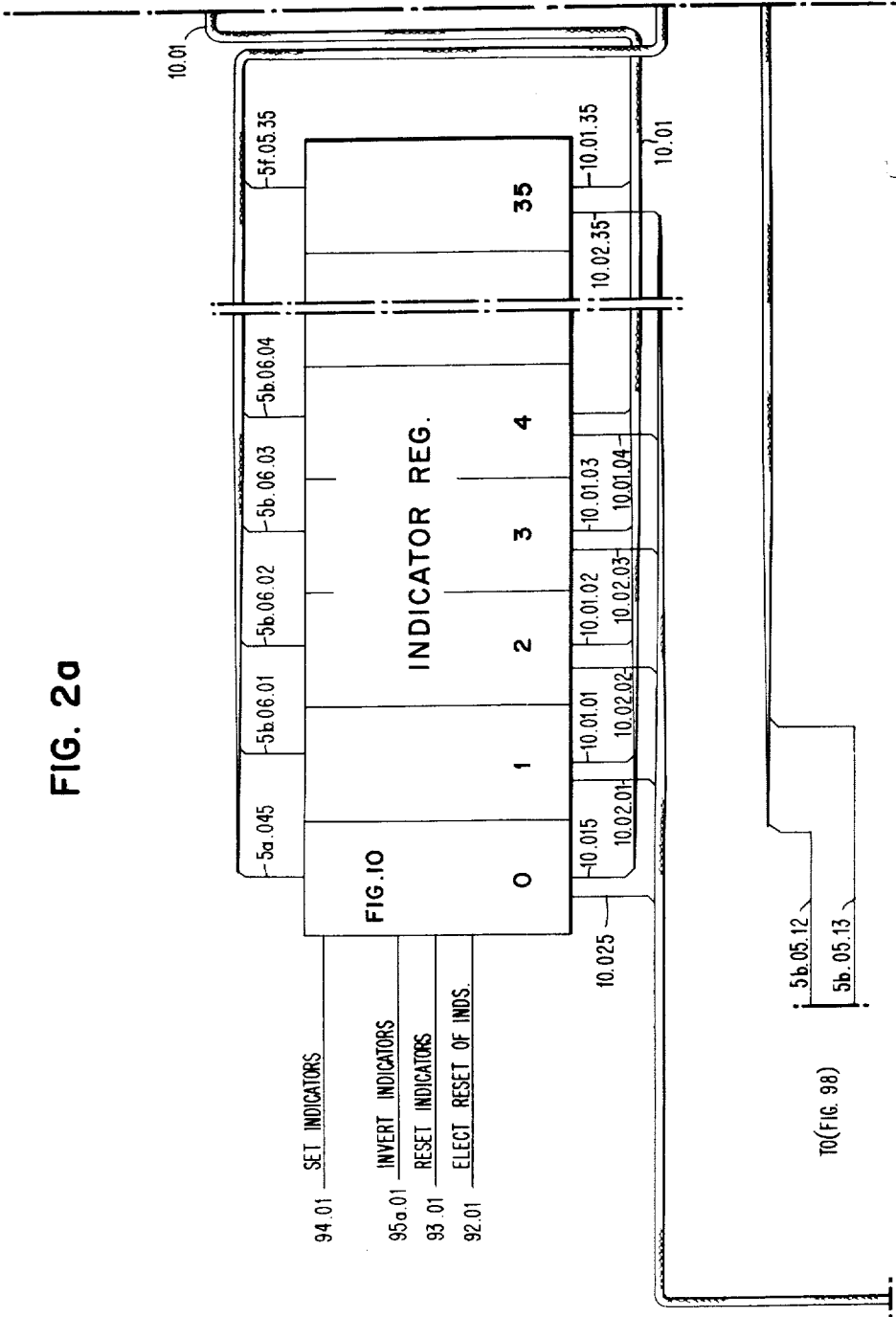
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FIG. 2a



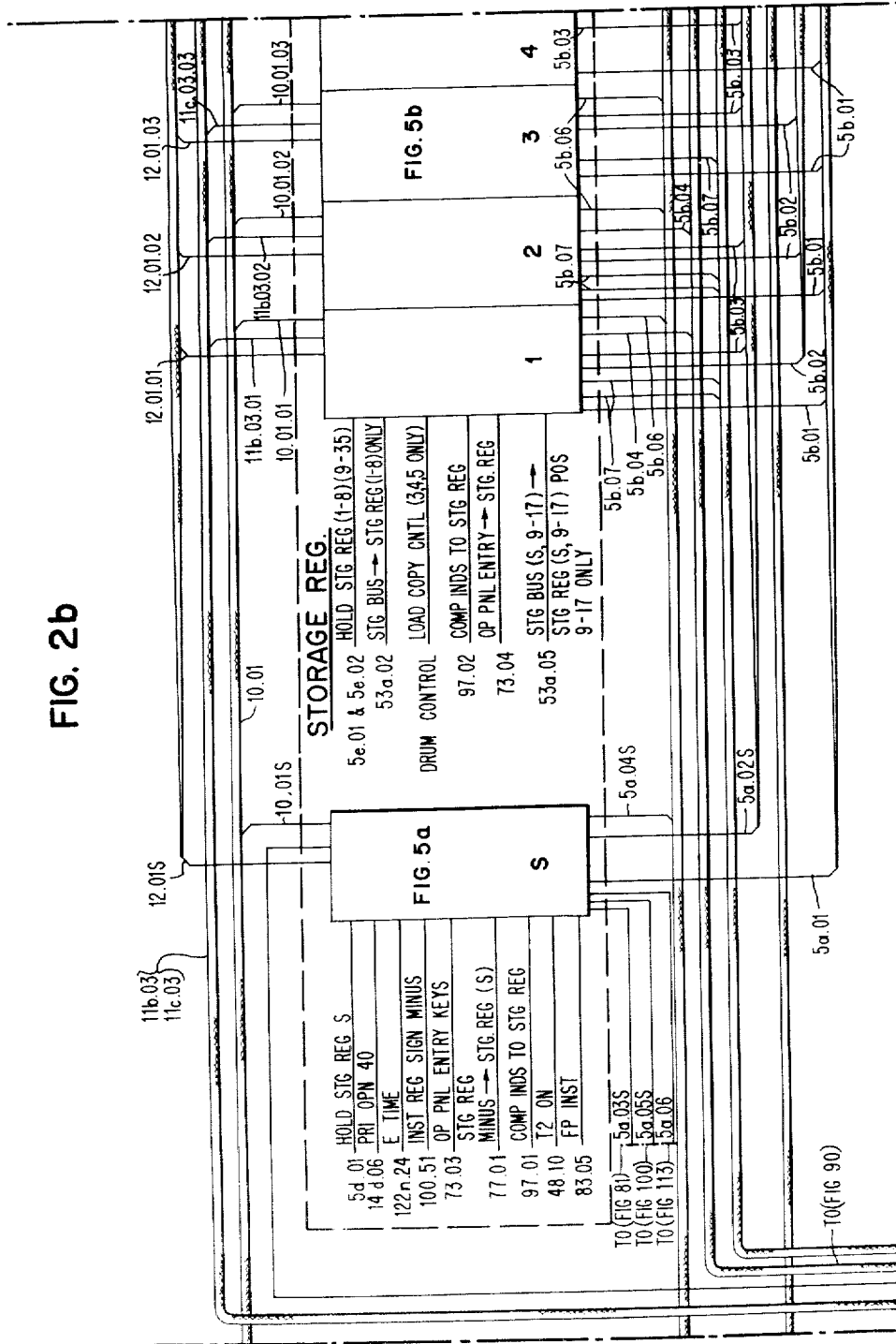
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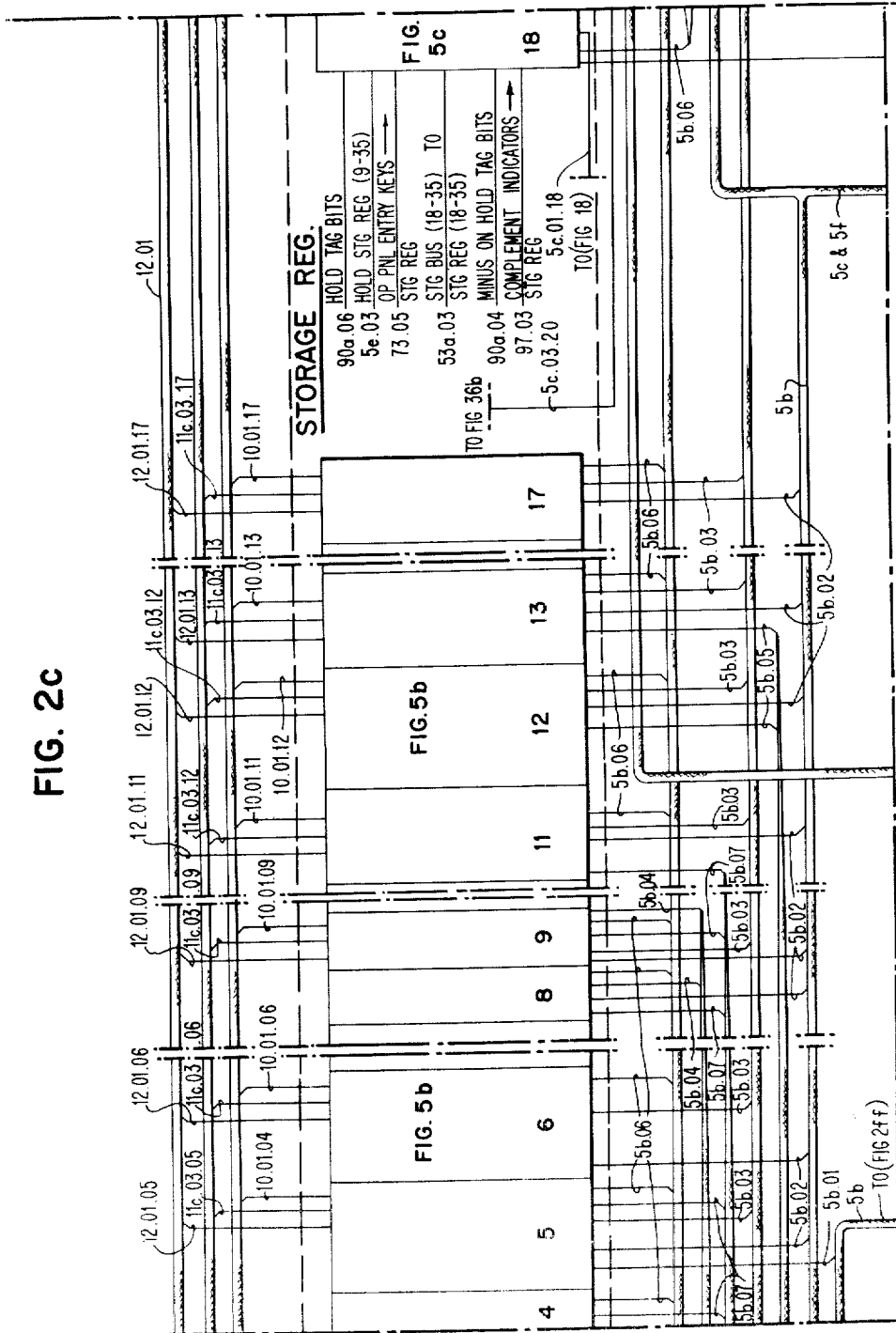
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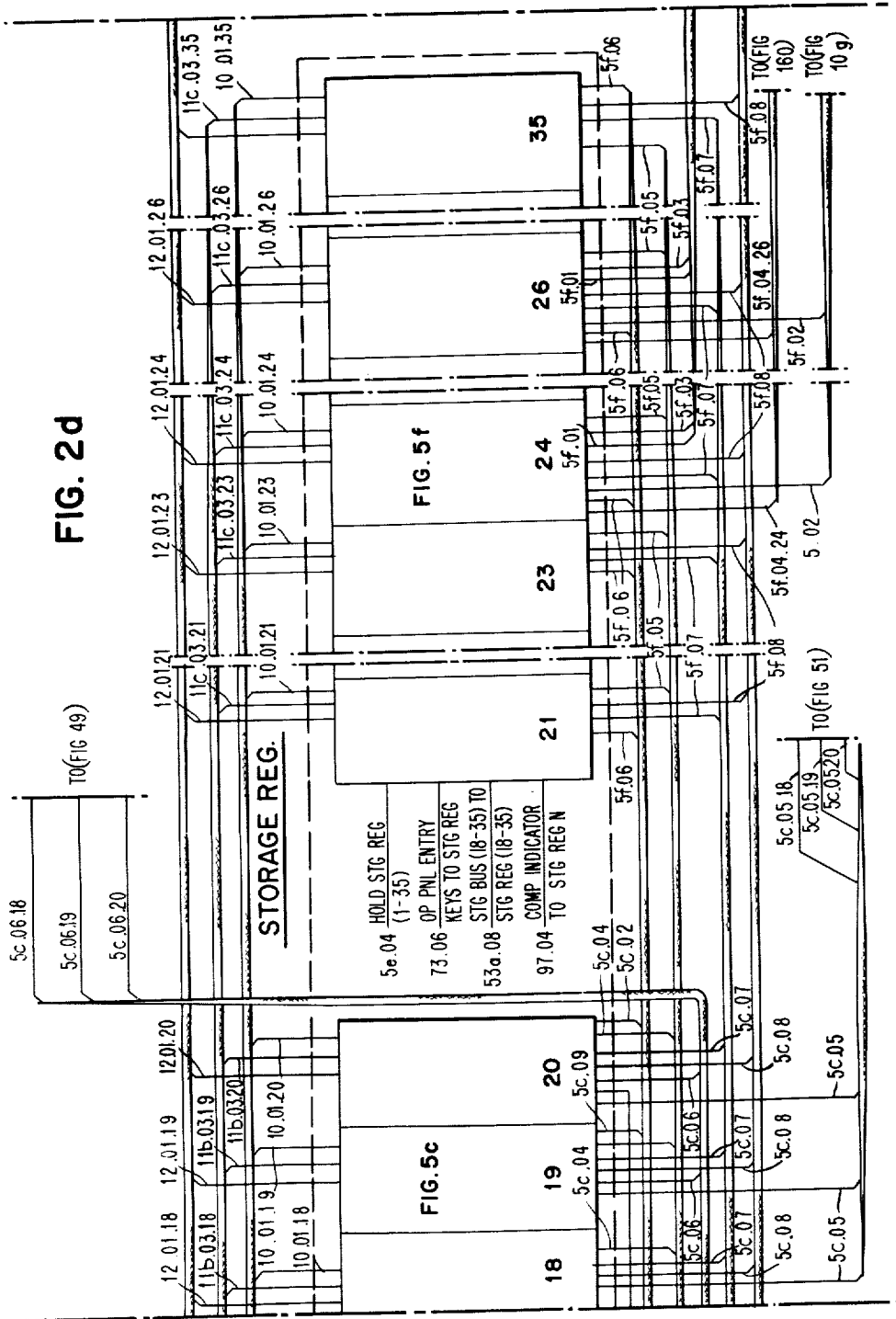
Feb. 6, 1962

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AN INDICATING REGISTER

3,019,976

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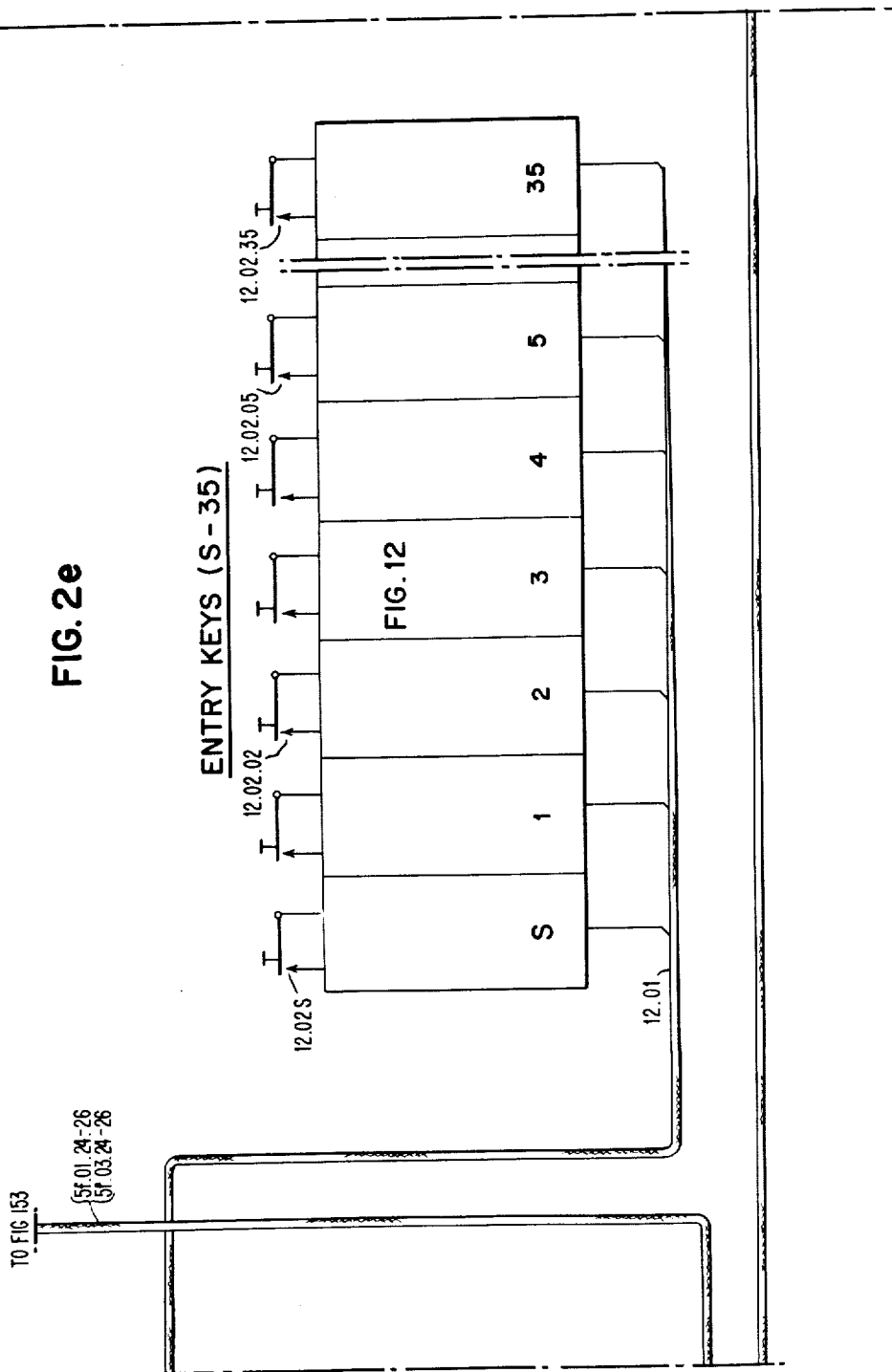
247 Sheets-Sheet 5



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**FIG. 2e**



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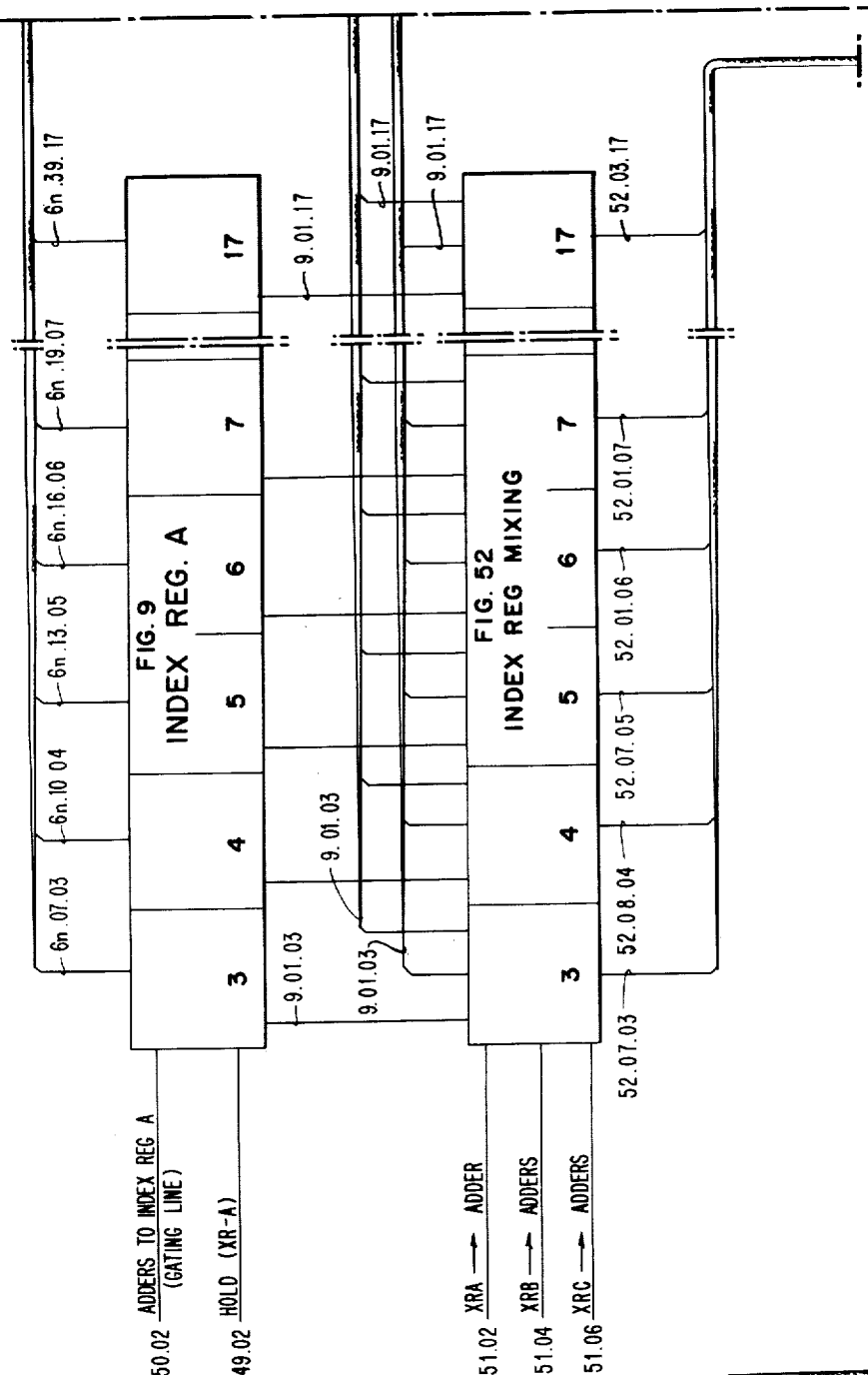
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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FIG. 2f



Feb. 6, 1962

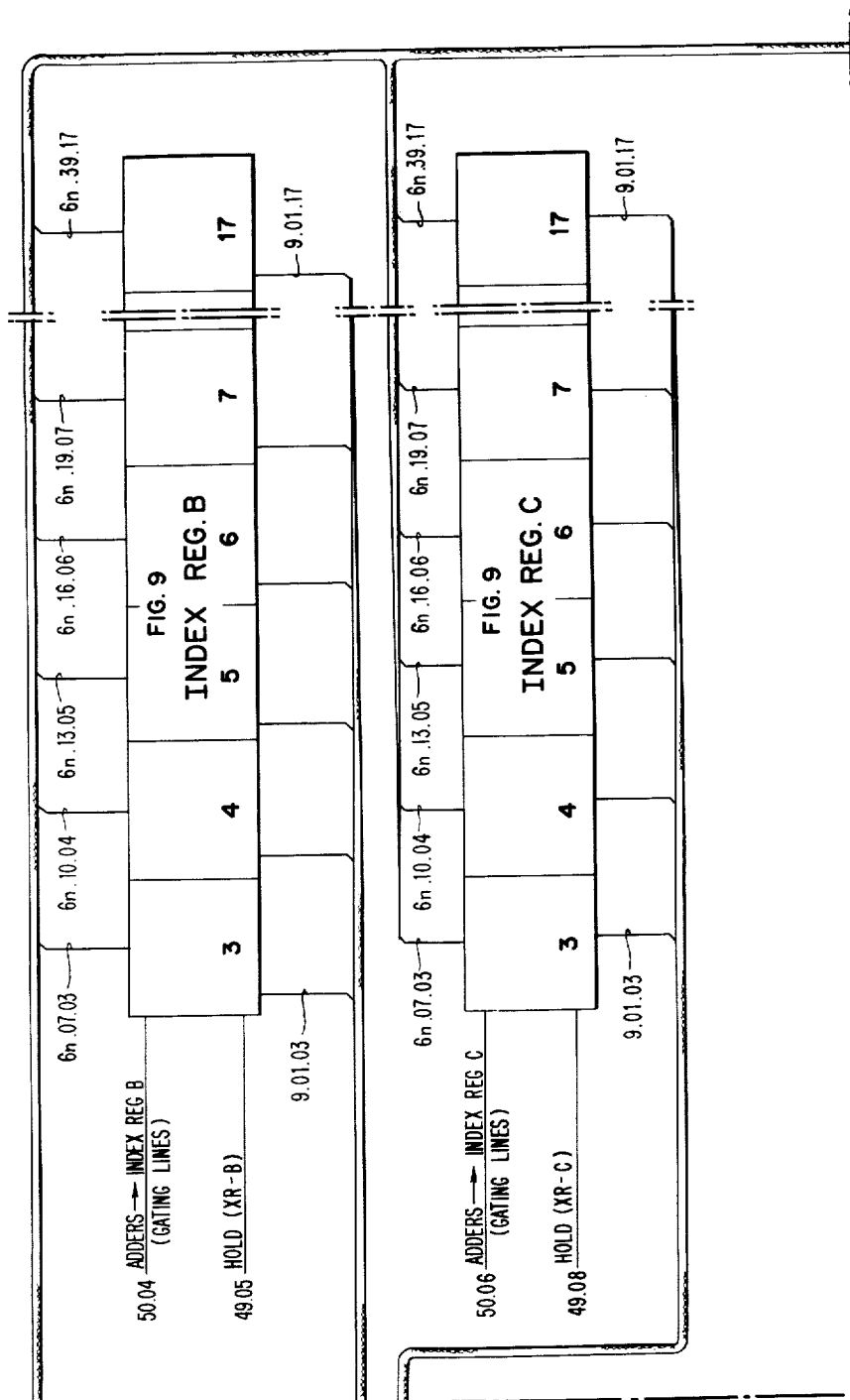
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AN INDICATING REGISTER

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FIG. 2g



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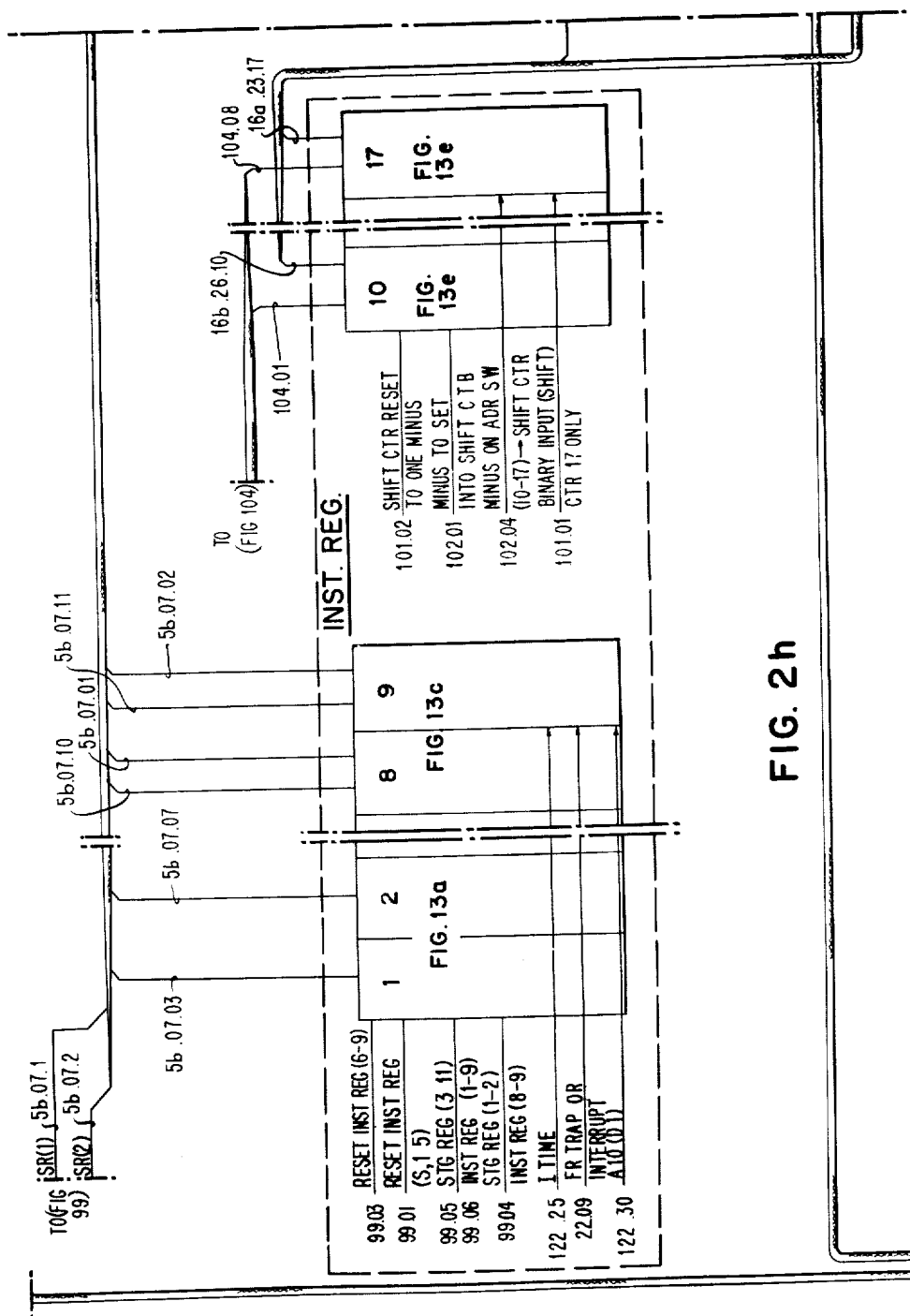


FIG. 2h

Feb. 6, 1962

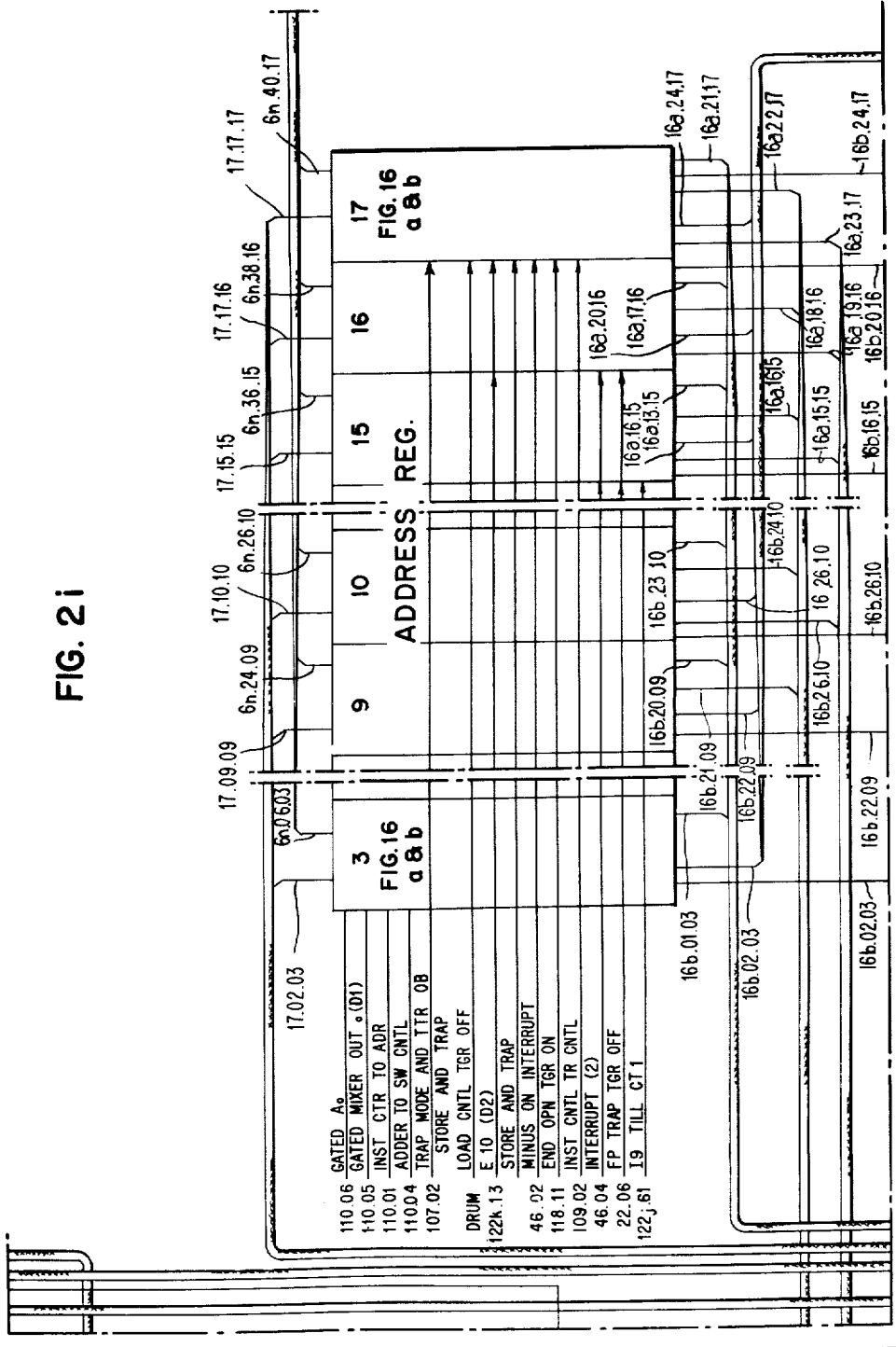
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247 Sheets-Sheet 10

FIG. 2i



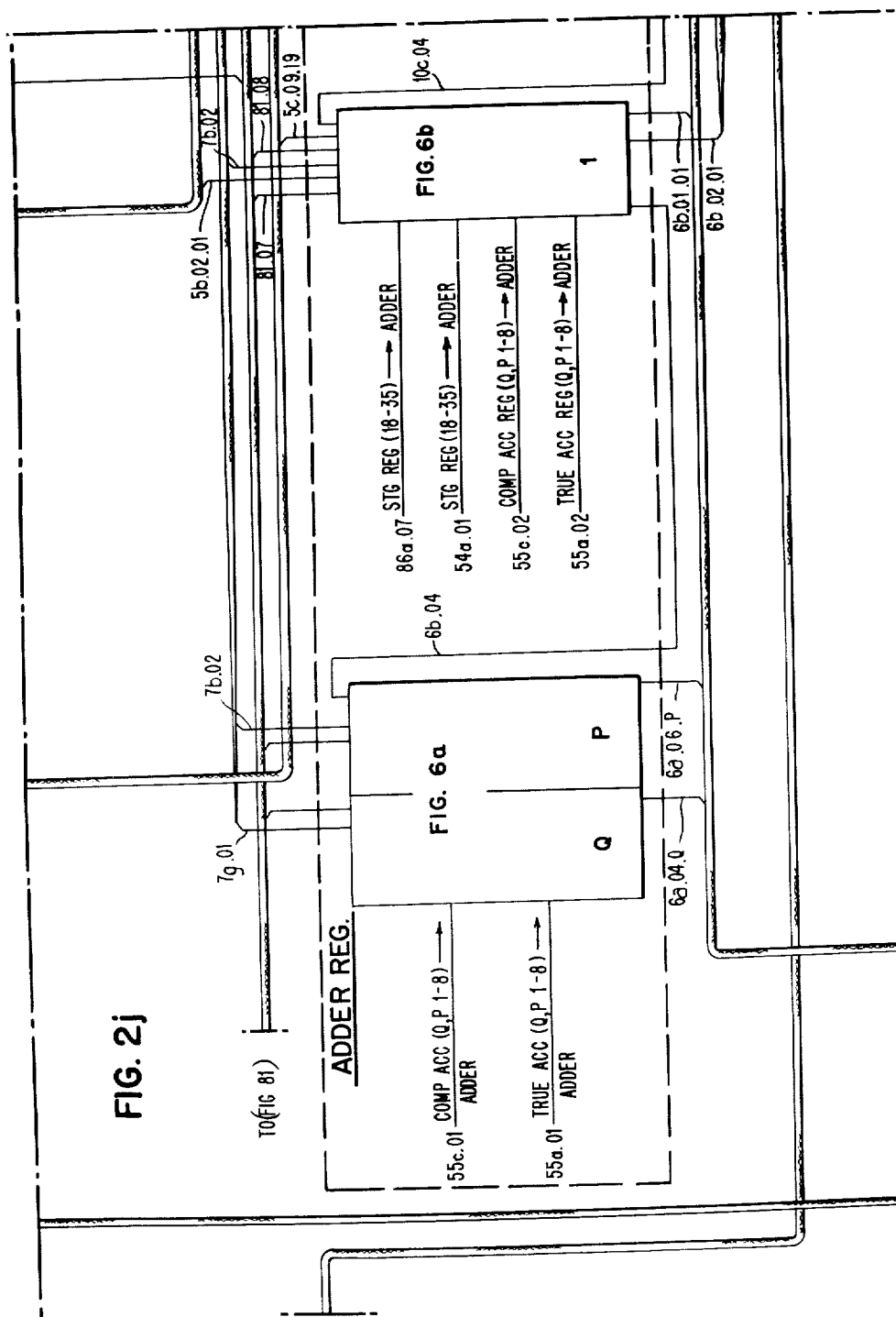
Feb. 6, 1962

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AN INDICATING REGISTER

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247 Sheets-Sheet 11



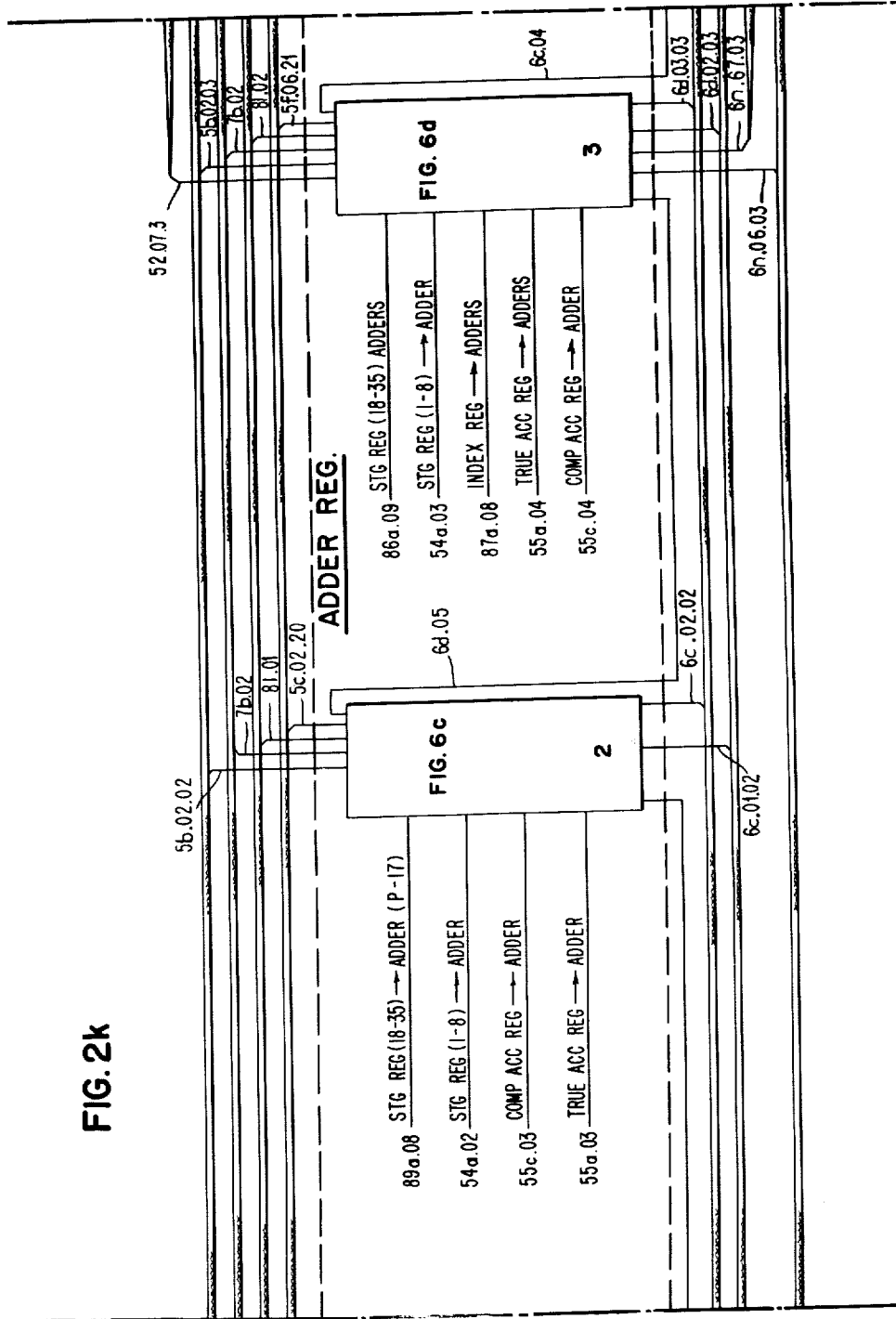
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AN INDICATING REGISTER

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Feb. 6, 1962

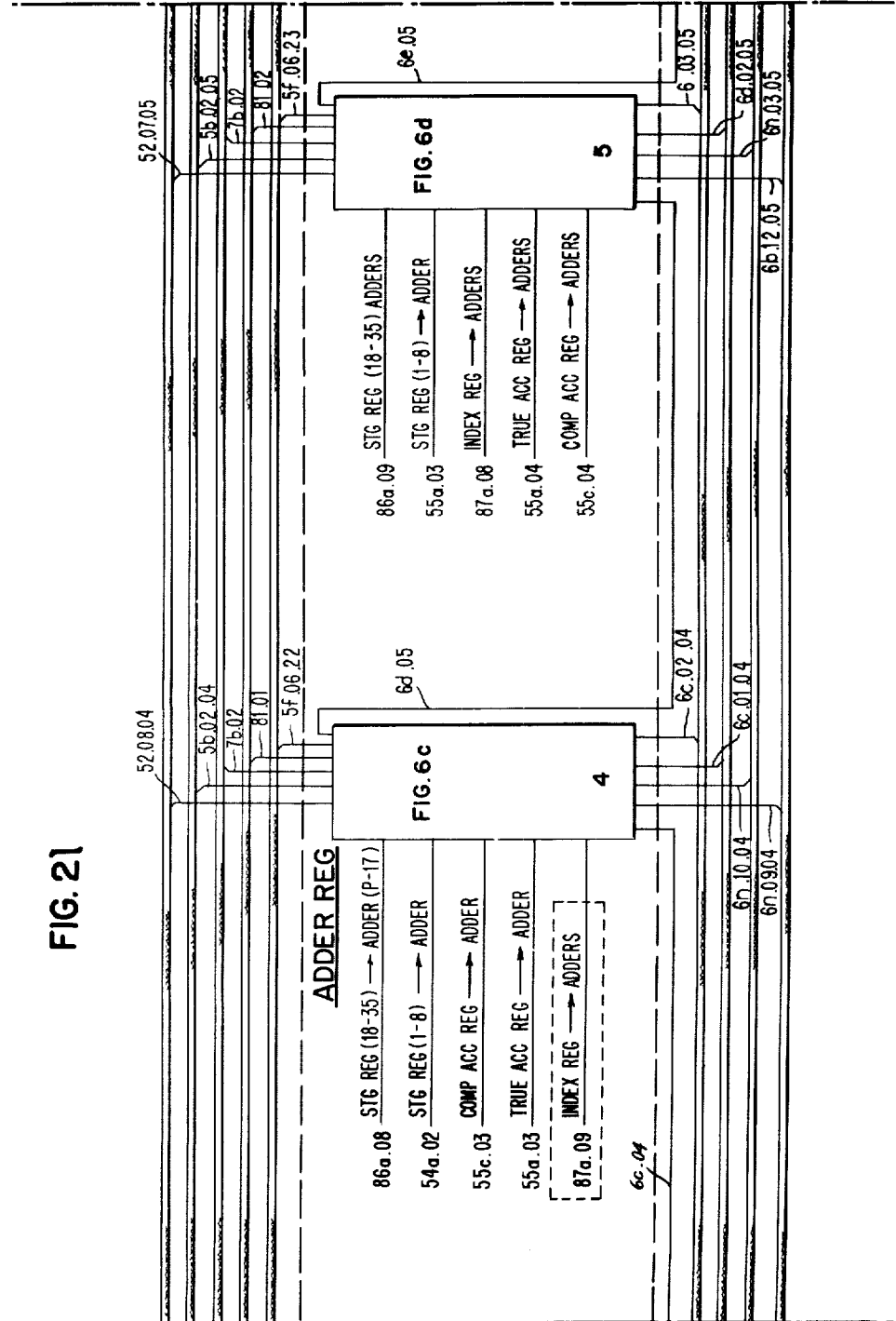
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AN INDICATING REGISTER

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FIG. 21



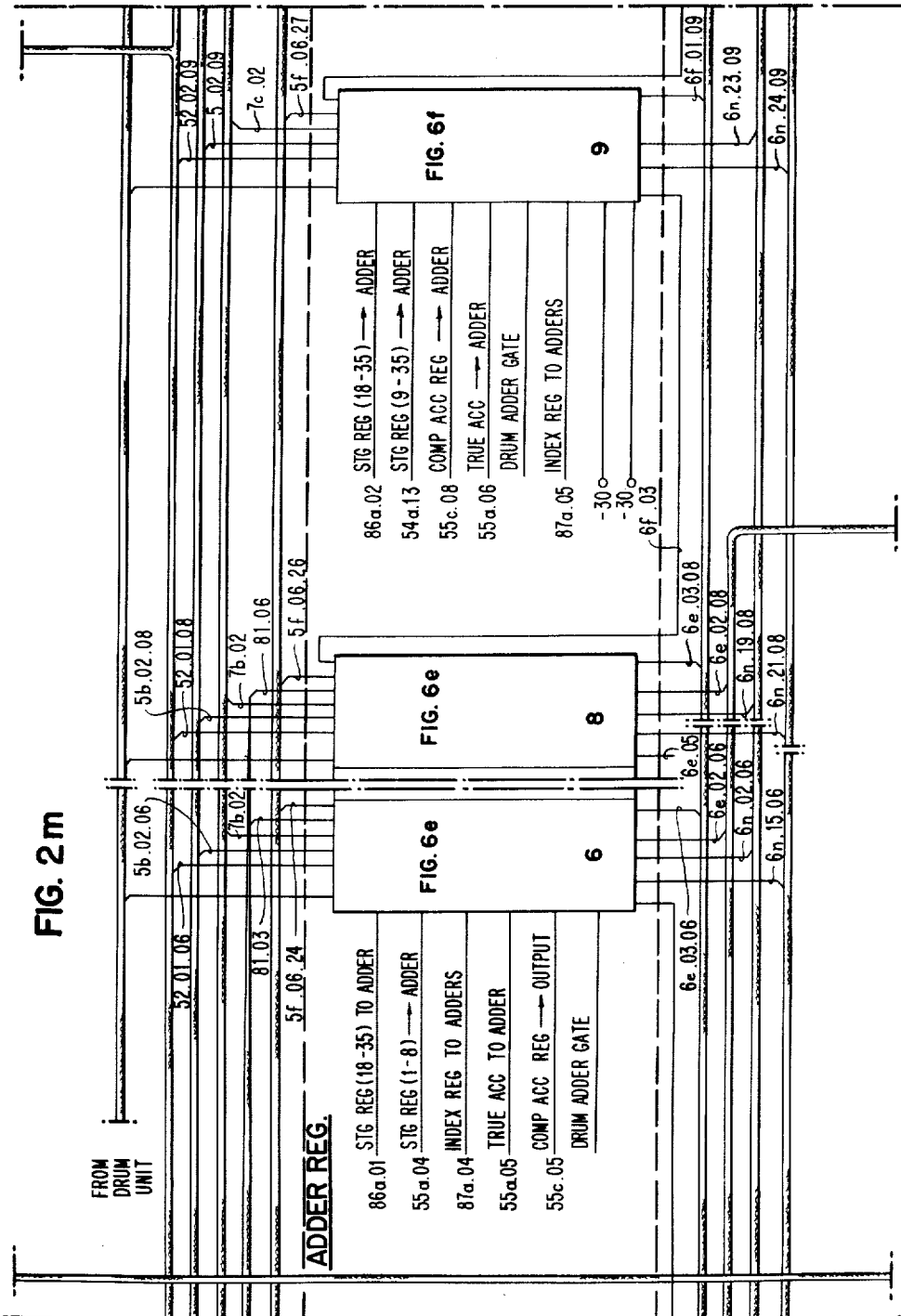
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AN INDICATING REGISTER

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247 Sheets-Sheet 14



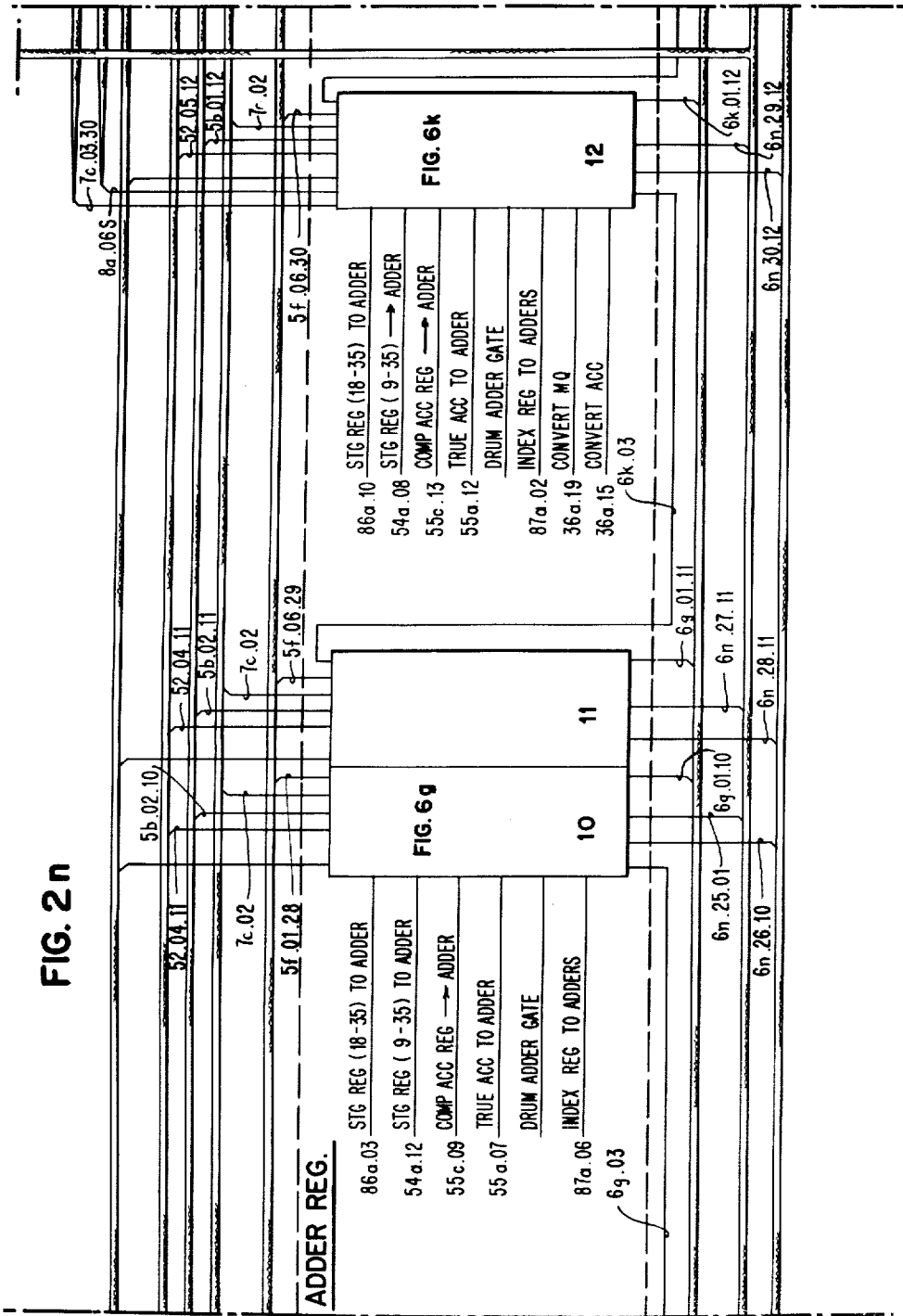
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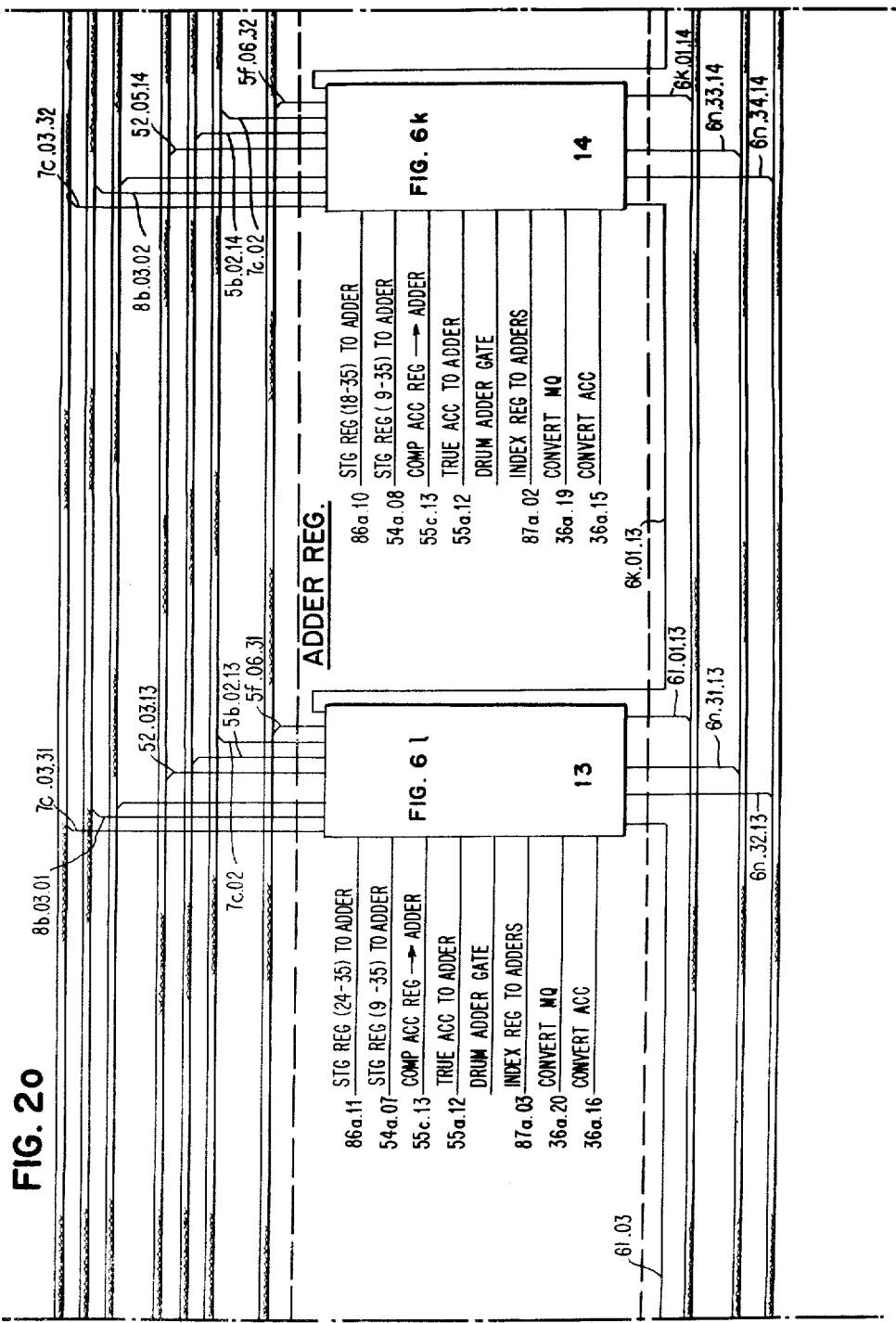
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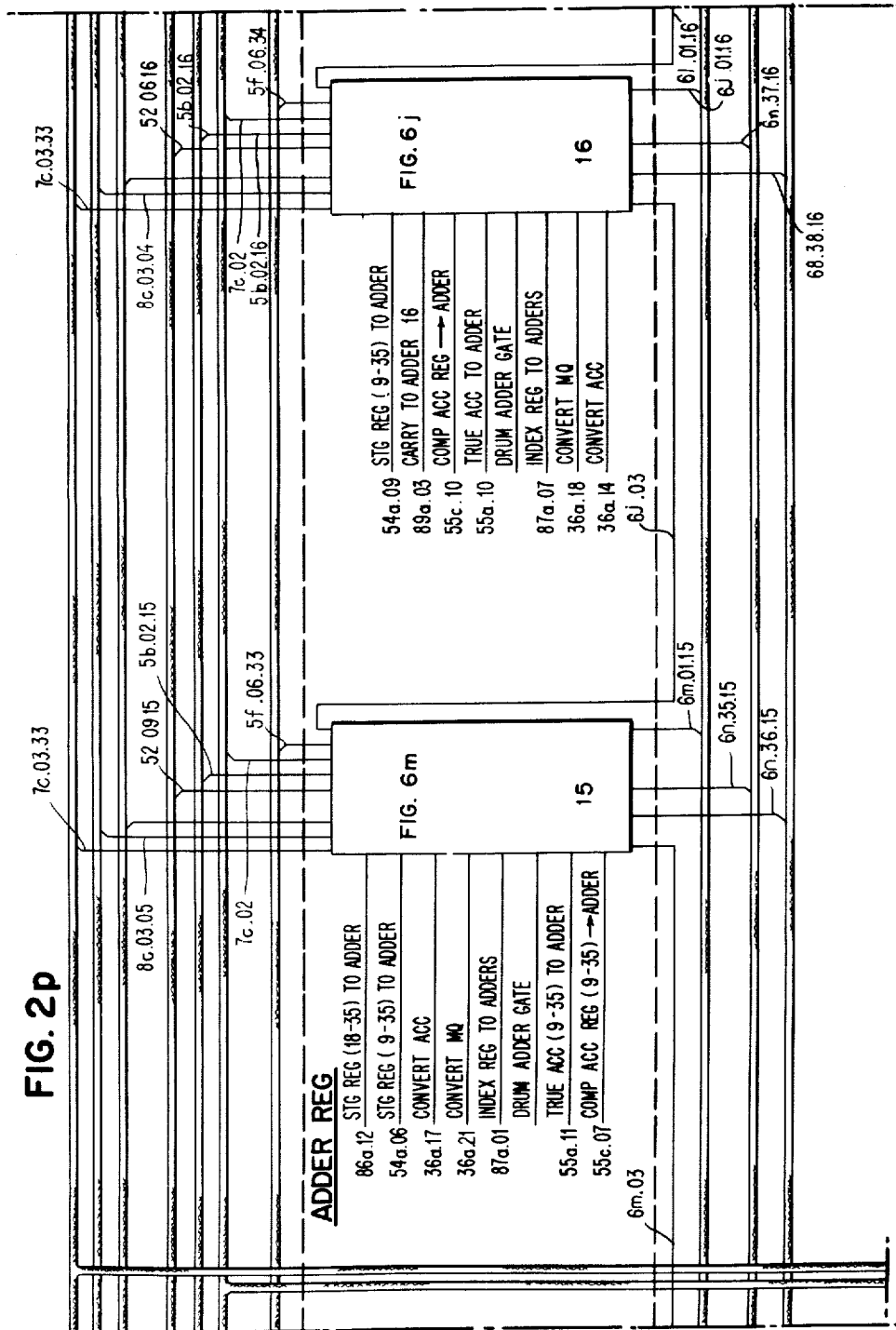
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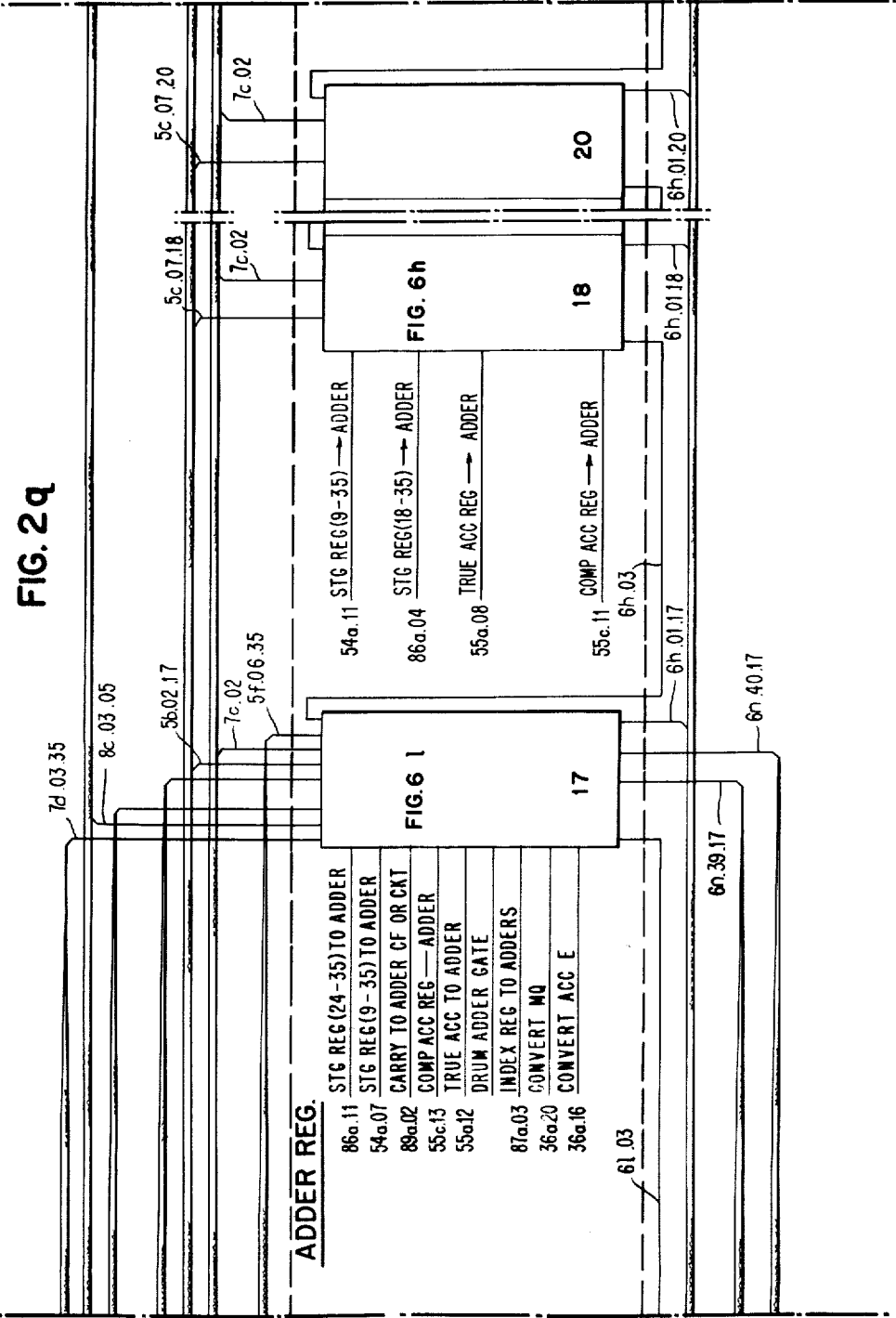
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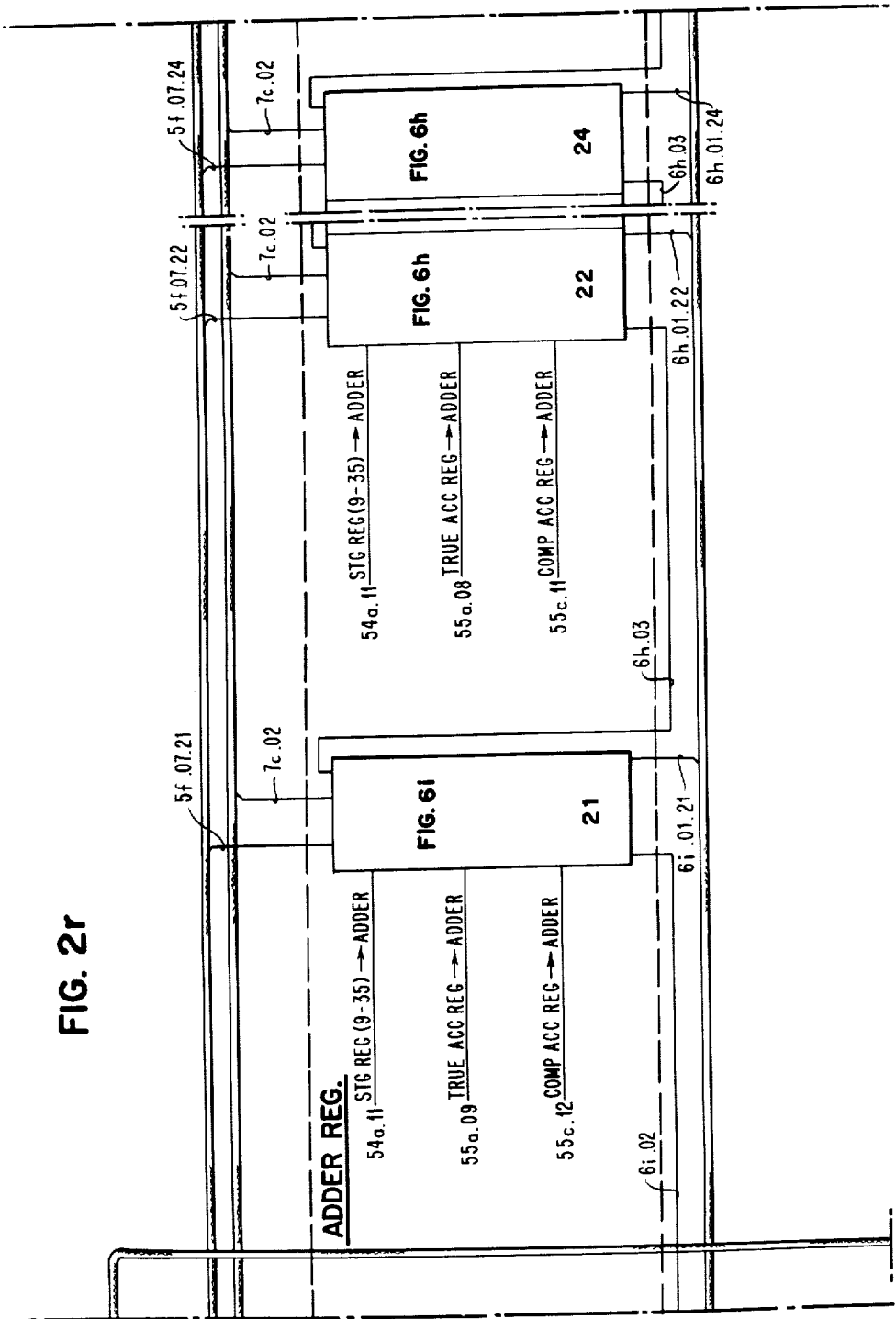
247 Sheets-Sheet 18

FIG. 2q



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**247 Sheets-Sheet 19**



Feb. 6, 1962

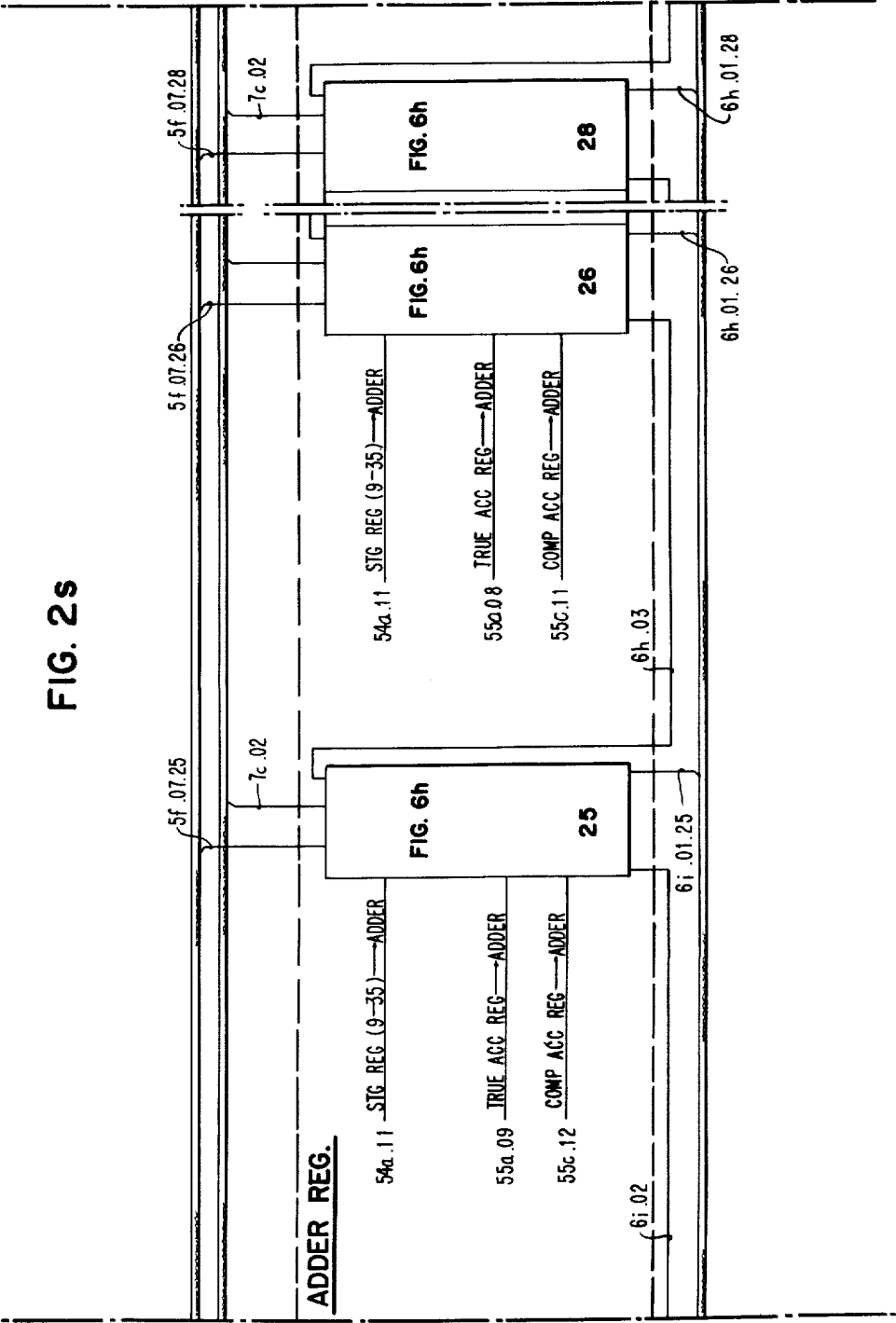
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AN INDICATING REGISTER

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FIG. 2s



Feb. 6, 1962

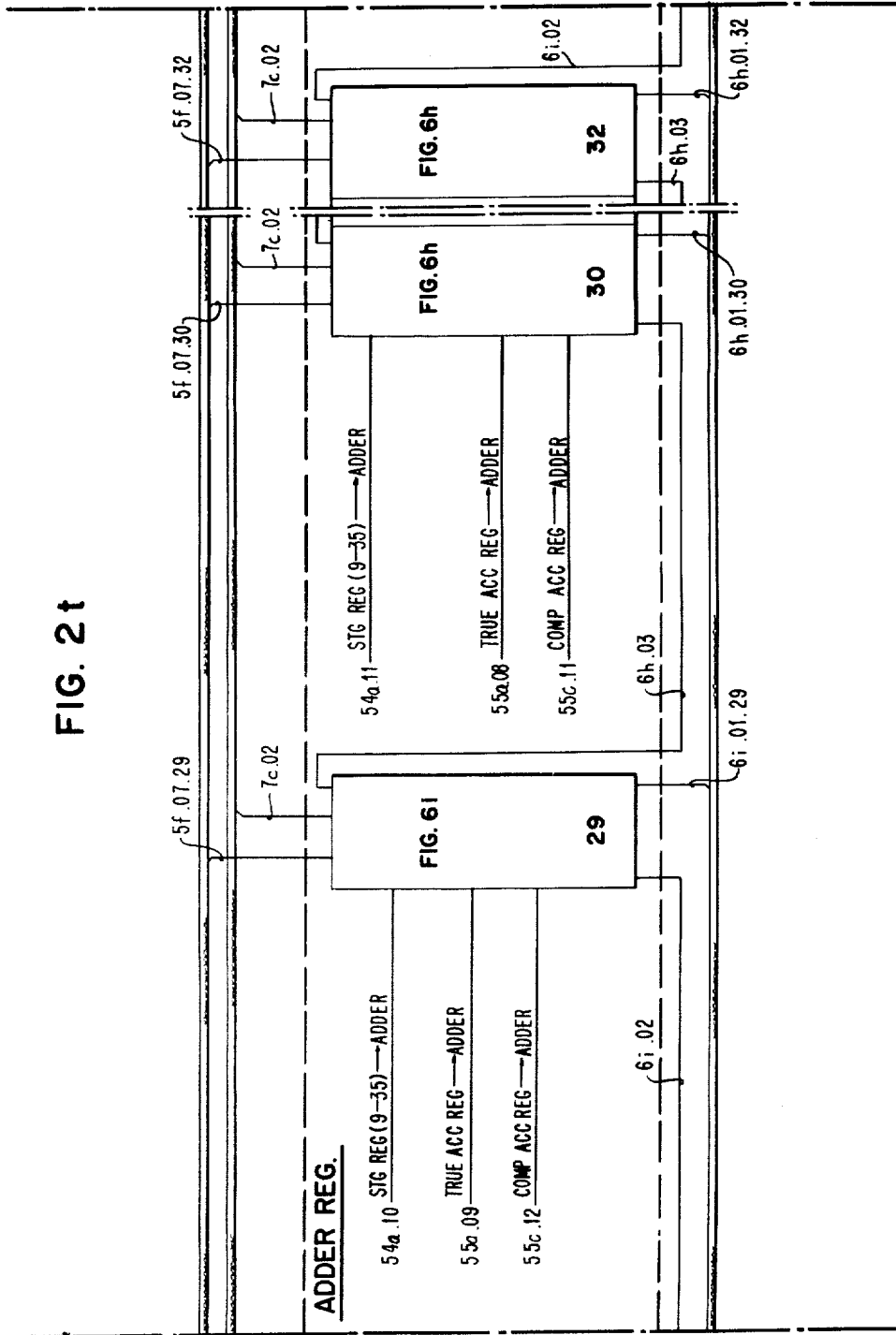
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FIG. 2t



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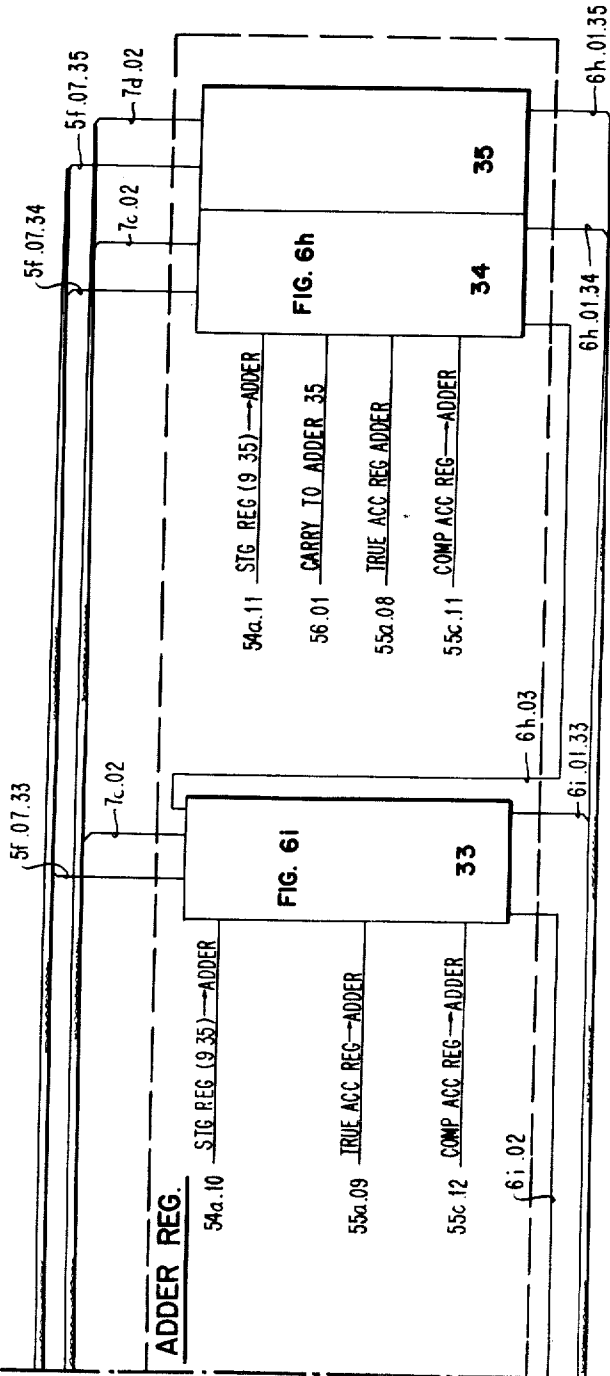
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AN INDICATING REGISTER

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FIG. 2u



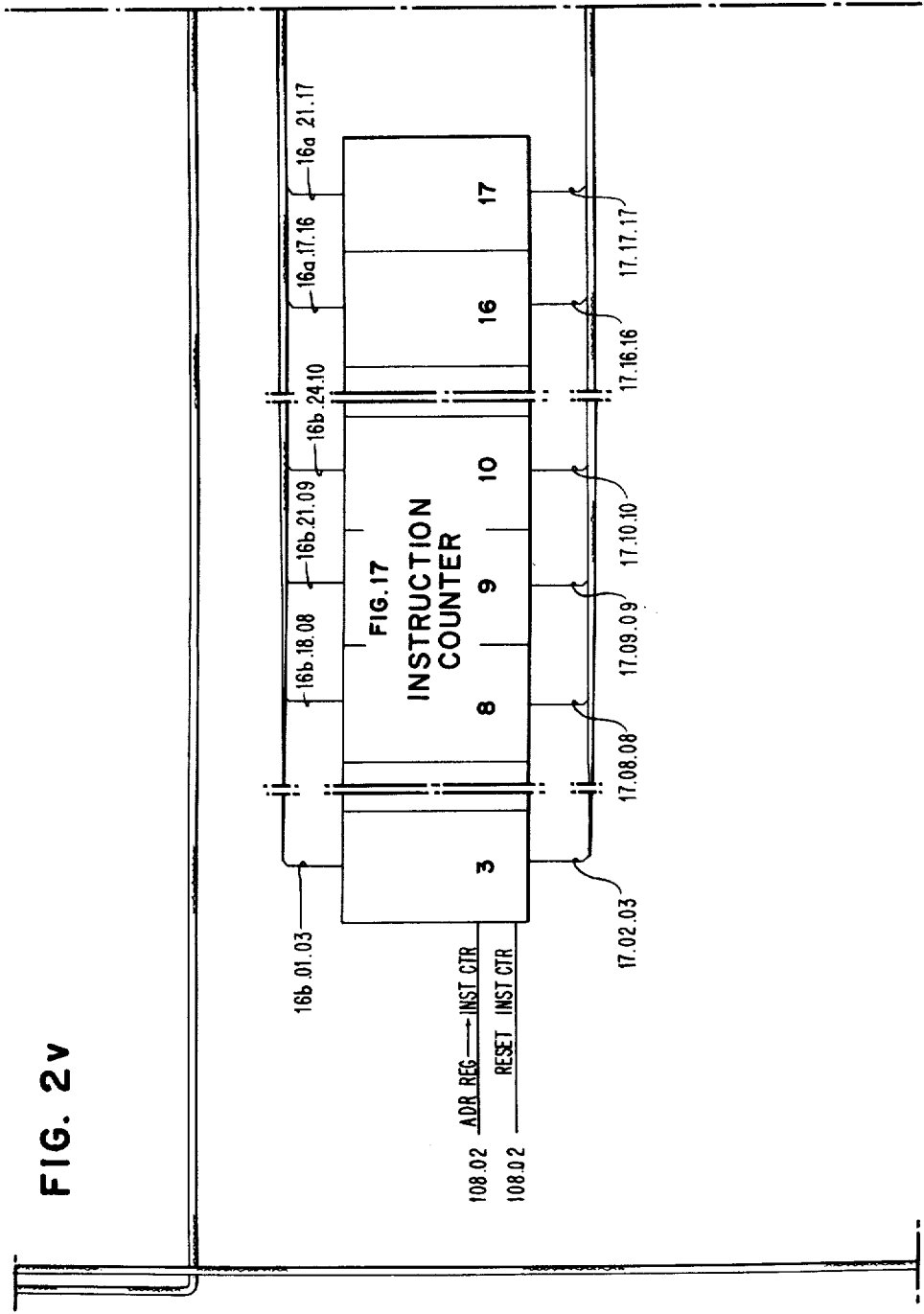
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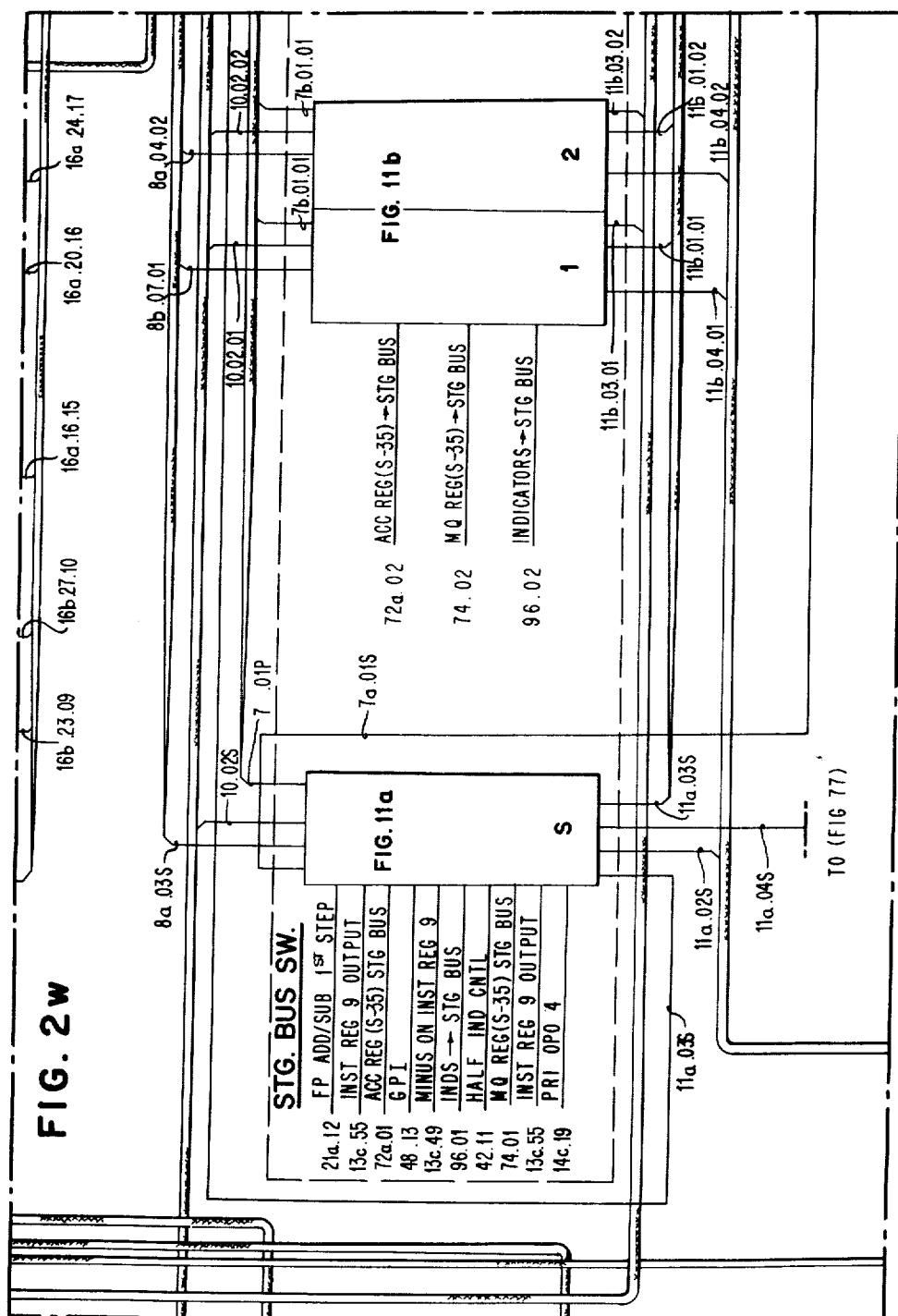
Filed Dec. 26, 1957

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Filed Dec. 26, 1957

**247 Sheets-Sheet 24**



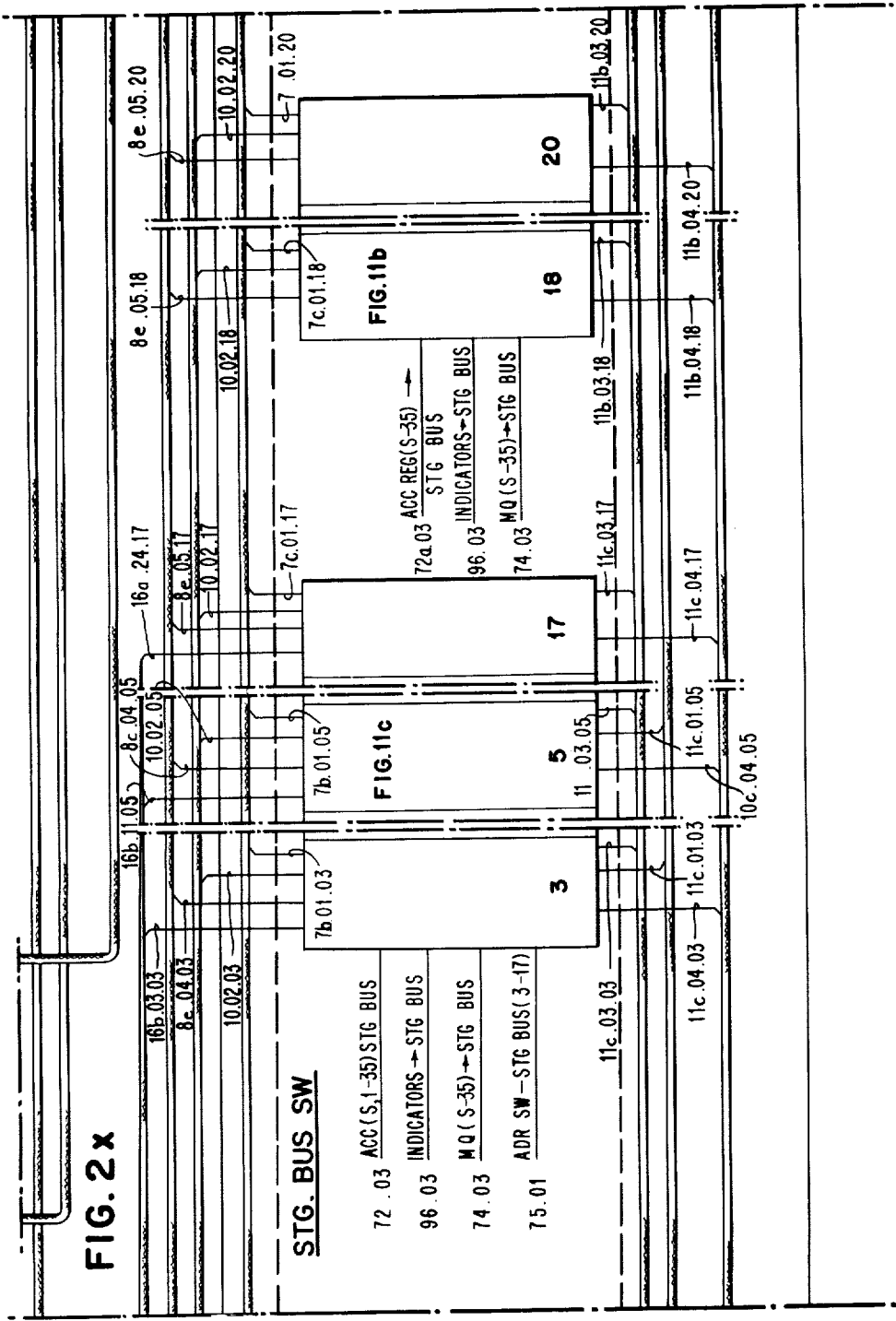
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AN INDICATING REGISTER

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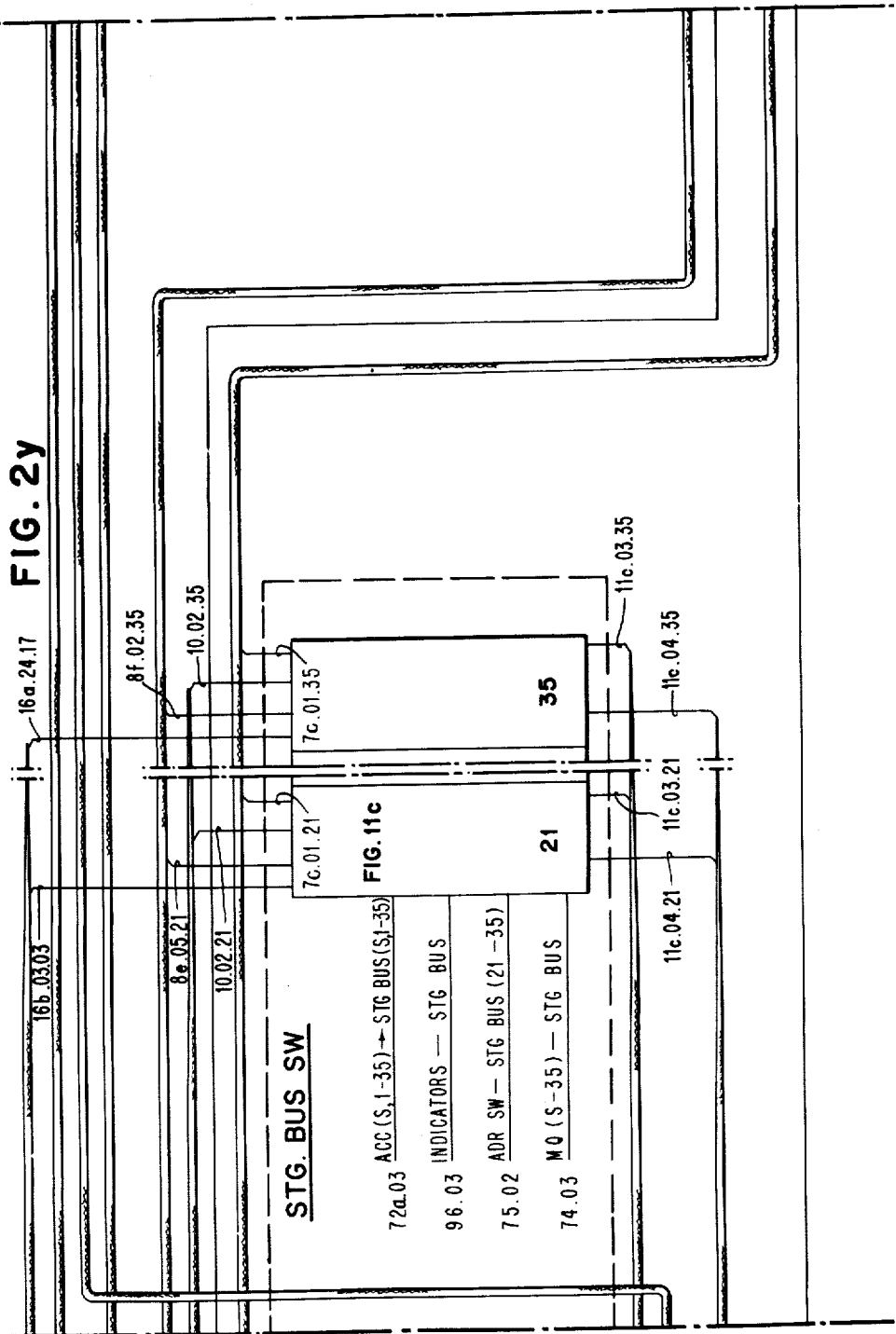
Feb. 6, 1962

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AN INDICATING REGISTER

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247 Sheets-Sheet 26



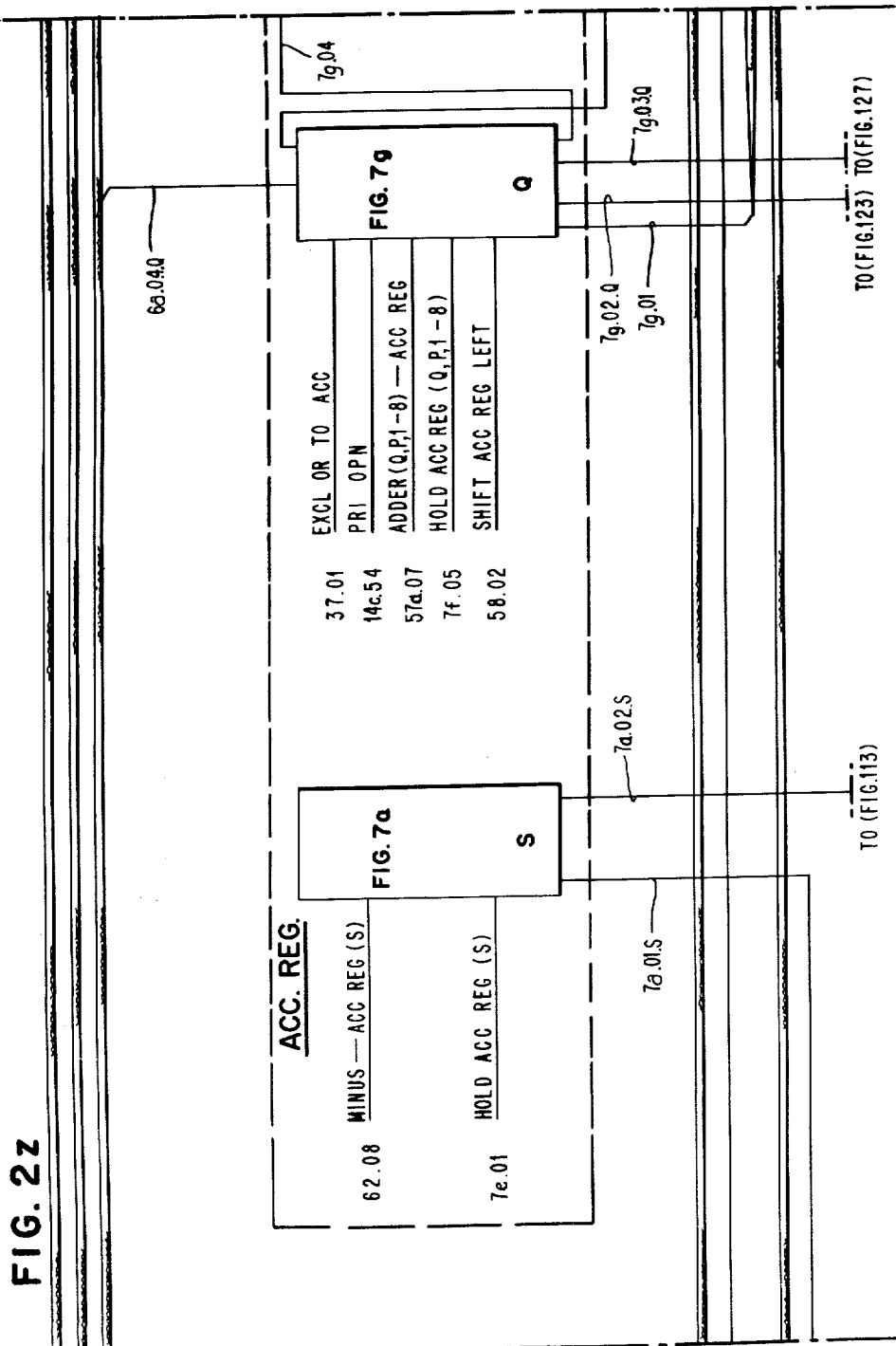
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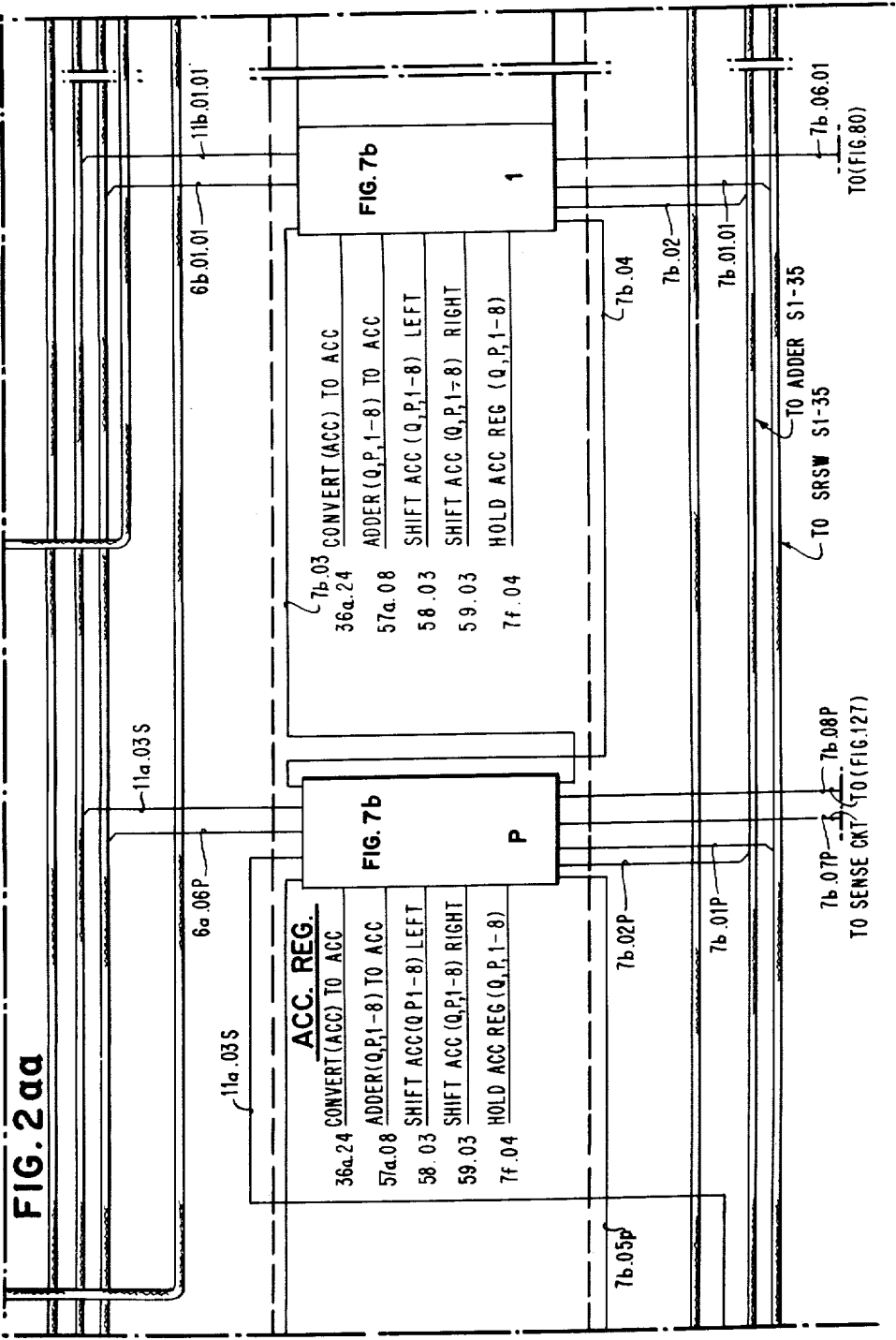
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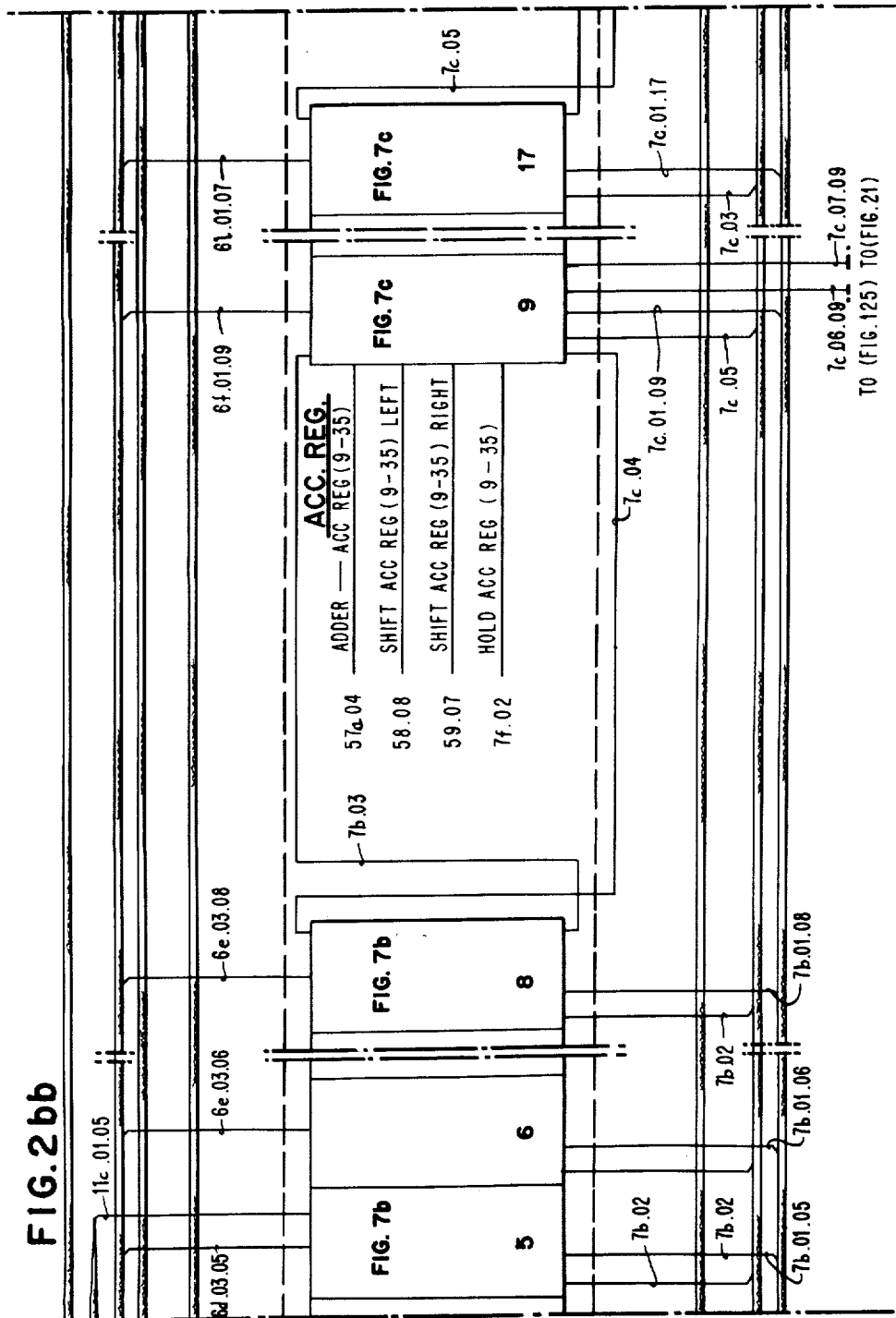
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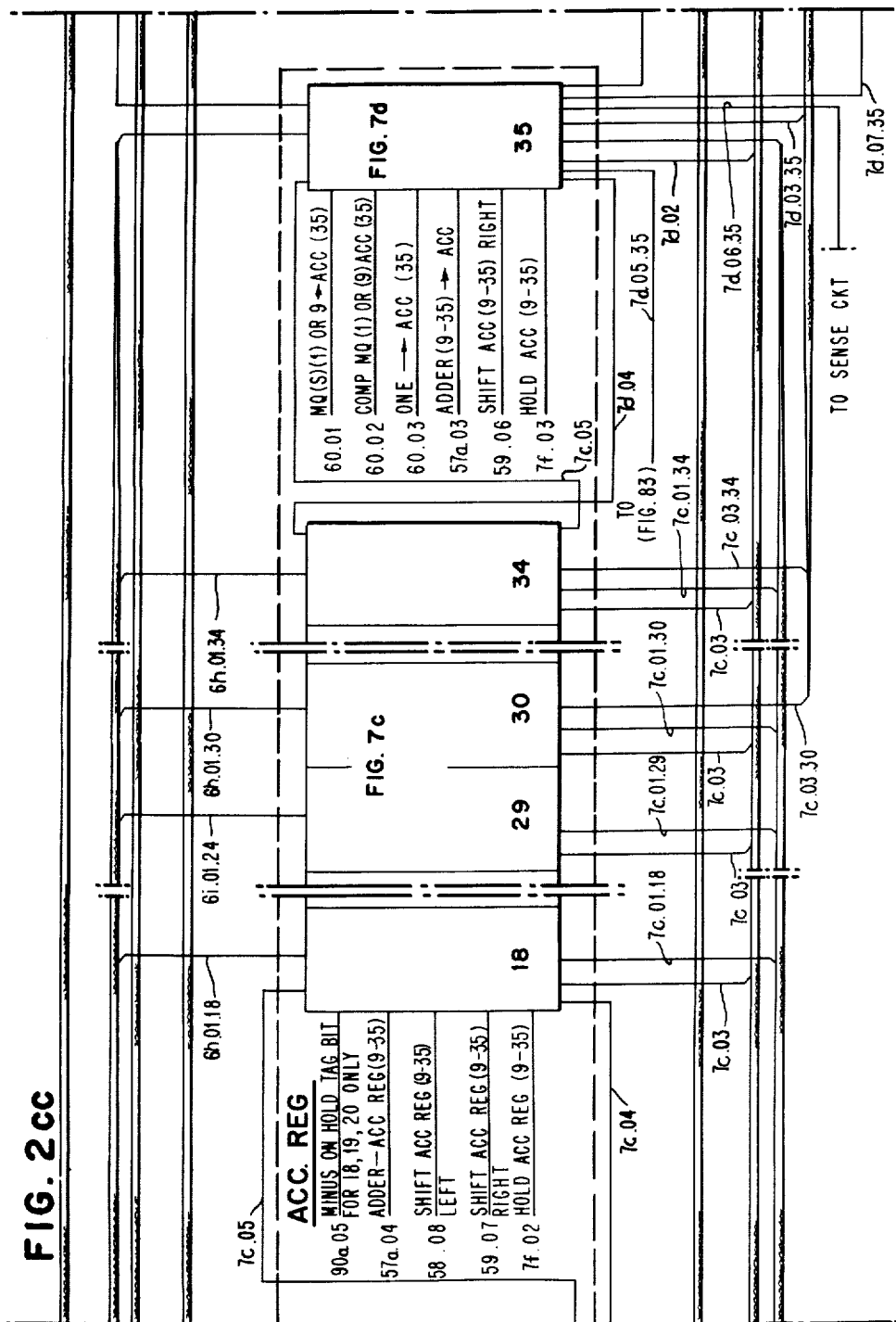
Filed Dec. 26, 1957

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Filed Dec. 26, 1957

247 Sheets-Sheet 30



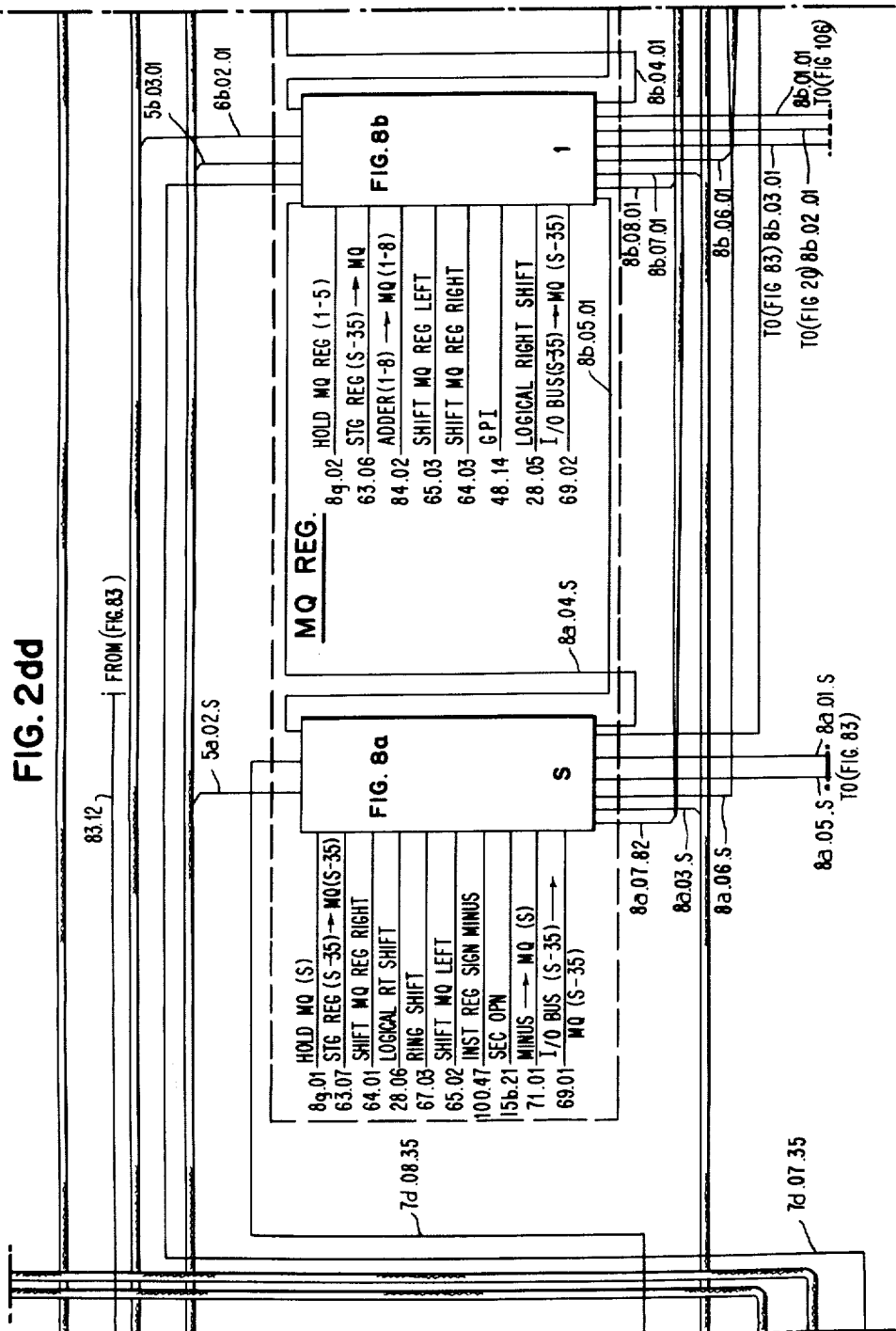
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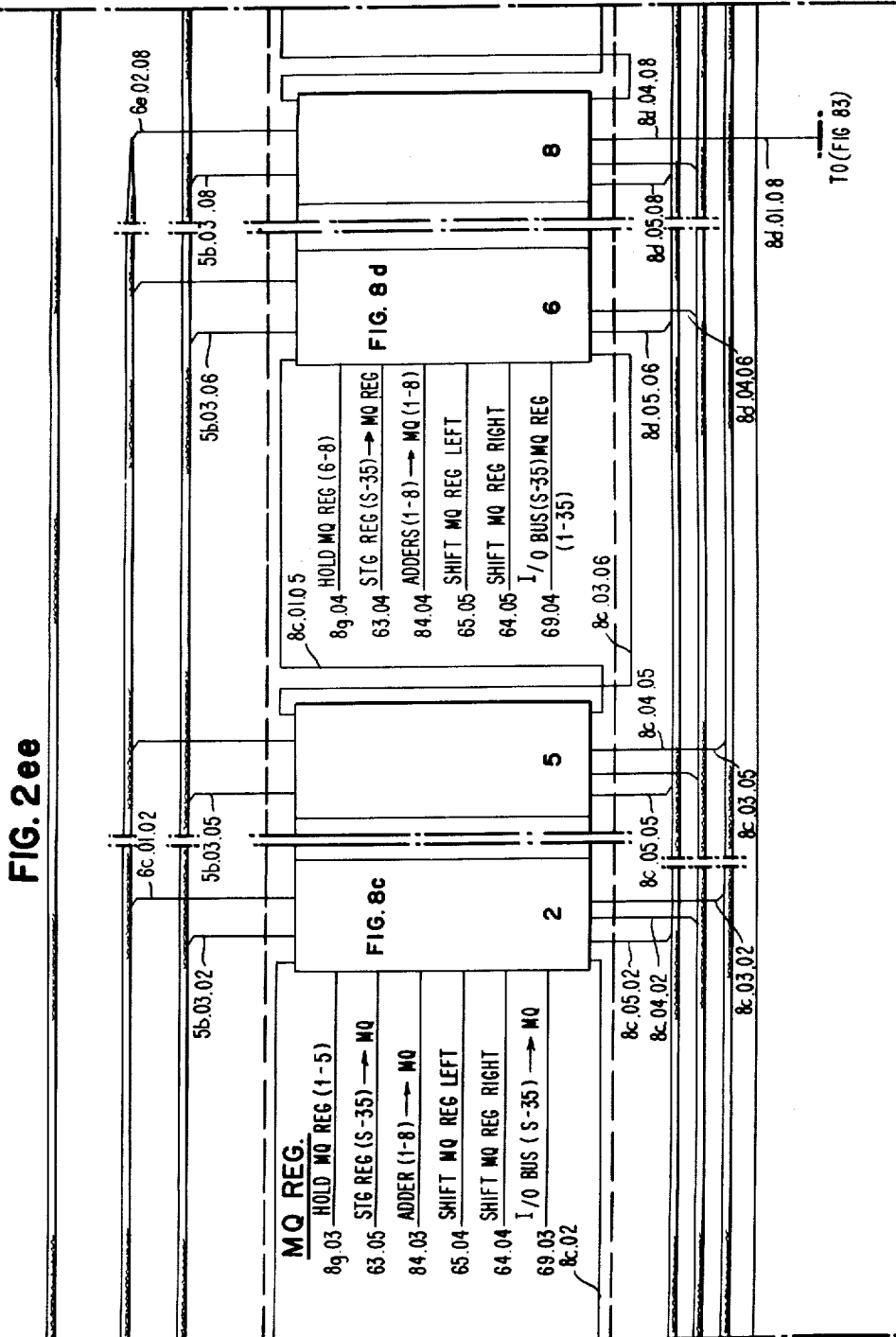
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AN INDICATING REGISTER

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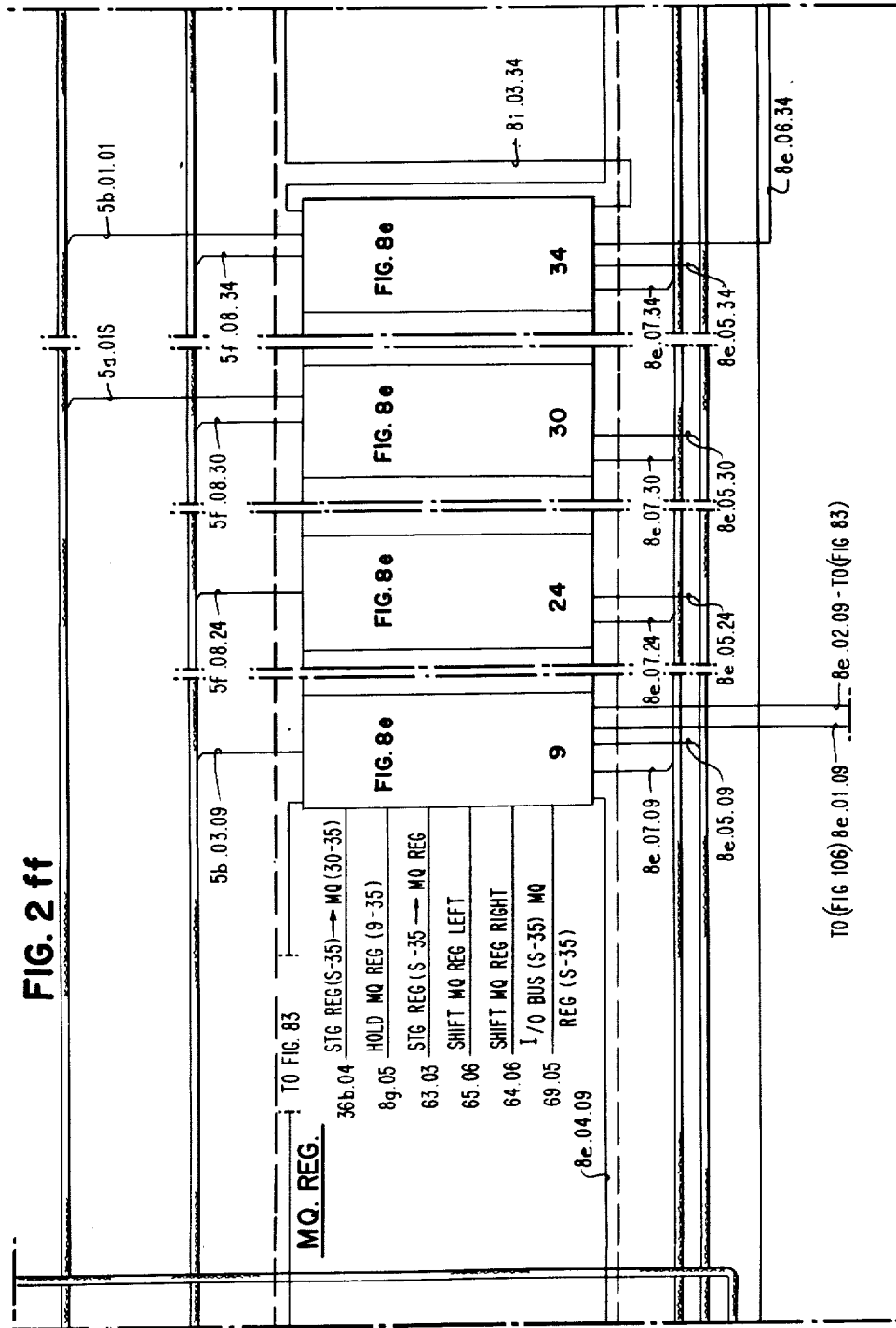
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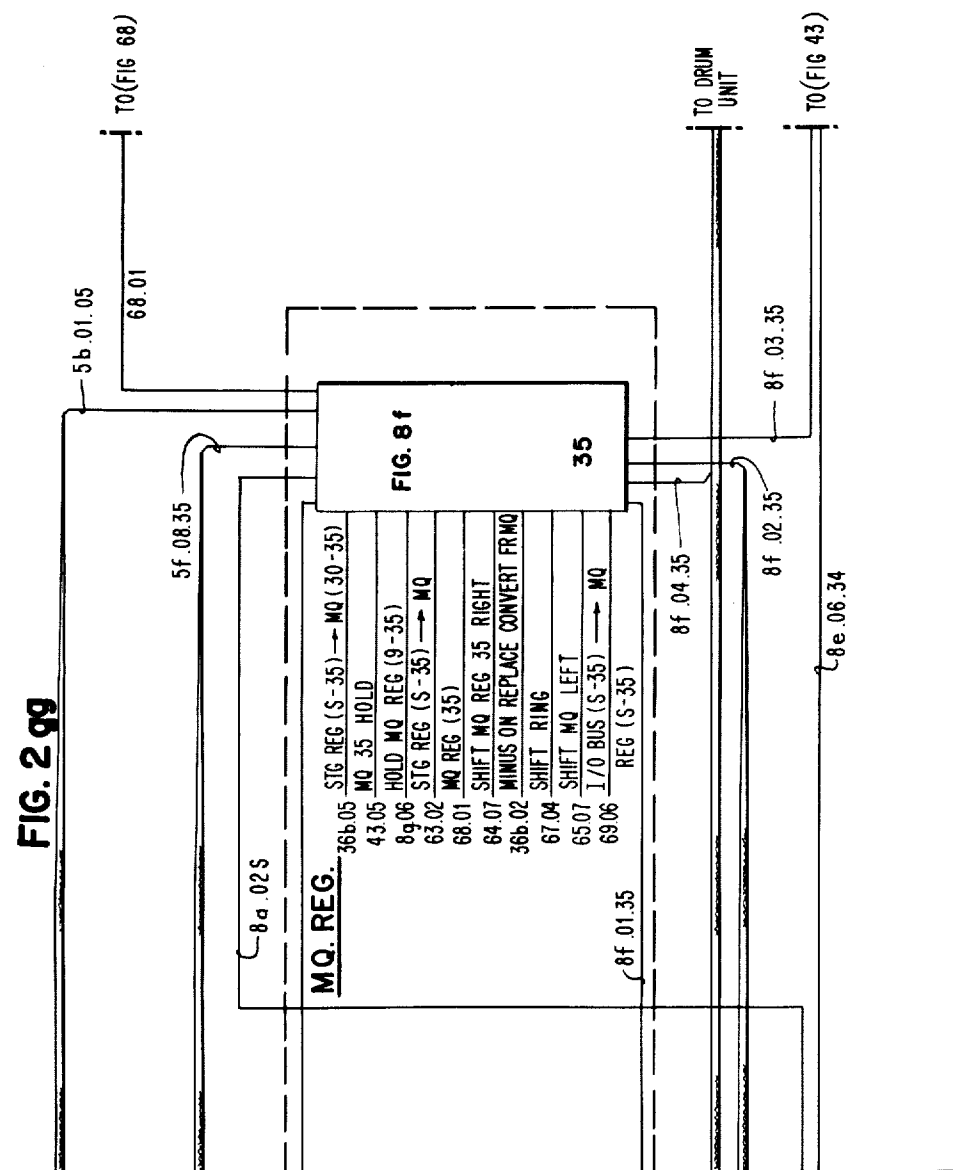
247 Sheets-Sheet 33



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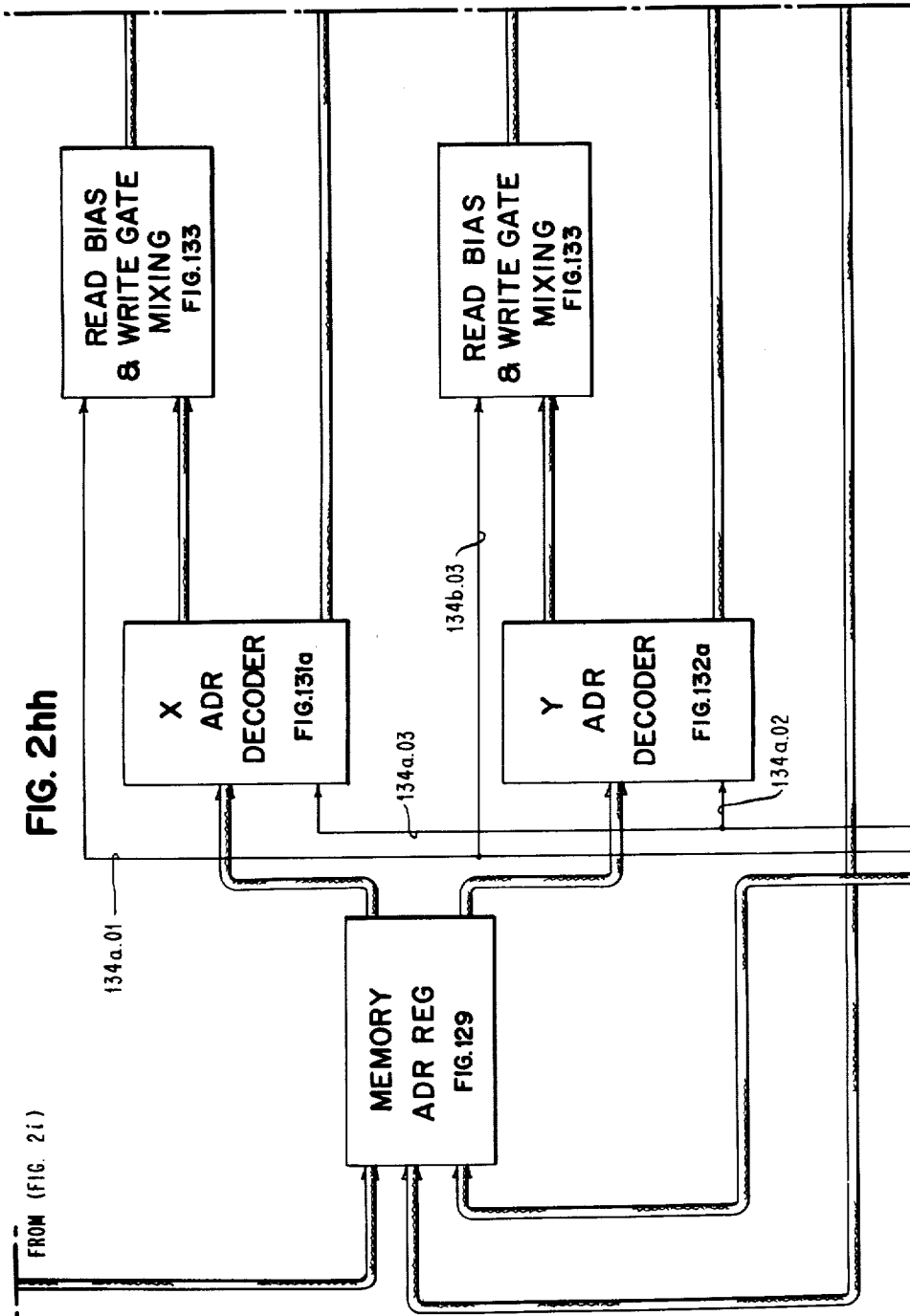
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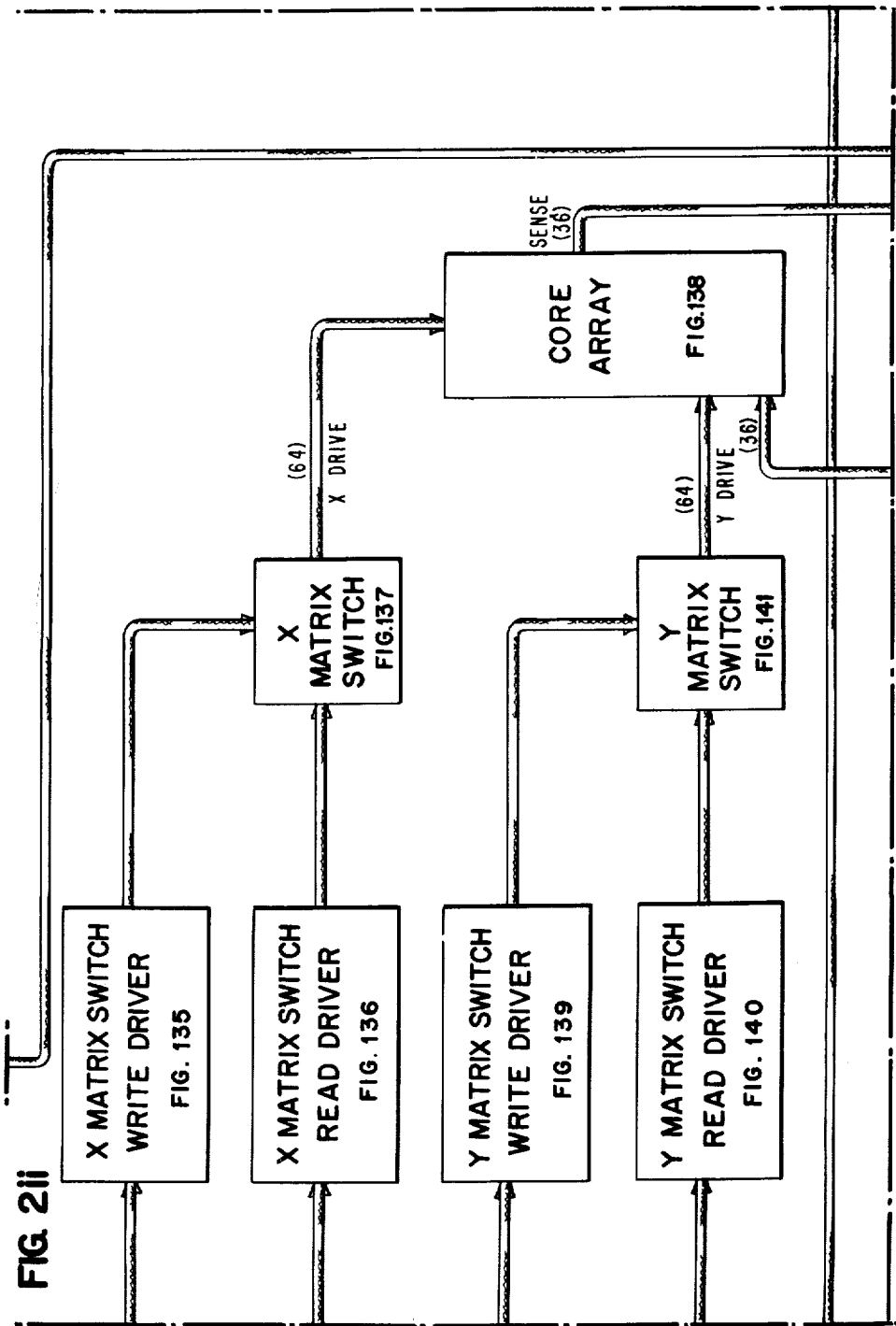
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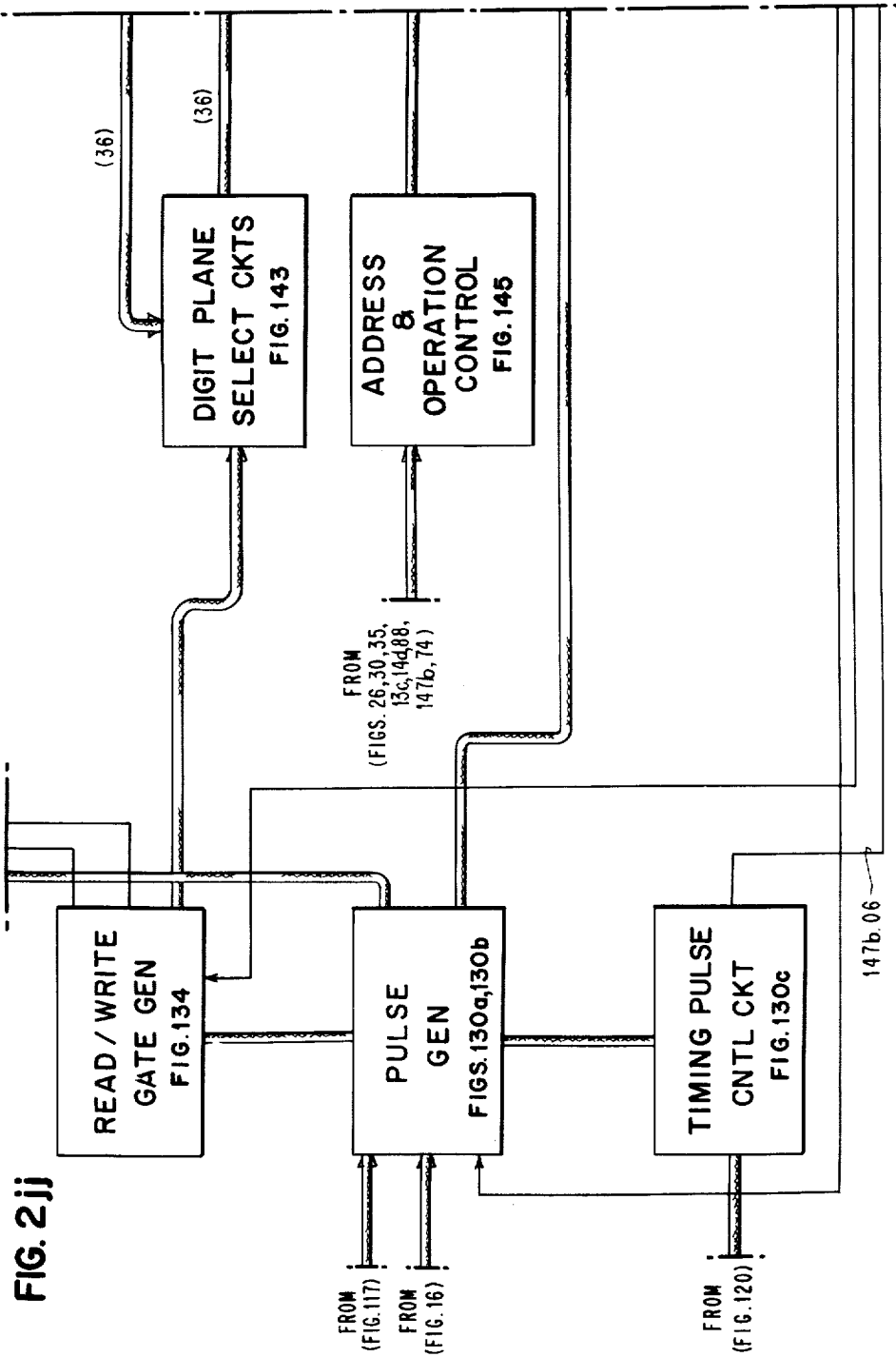
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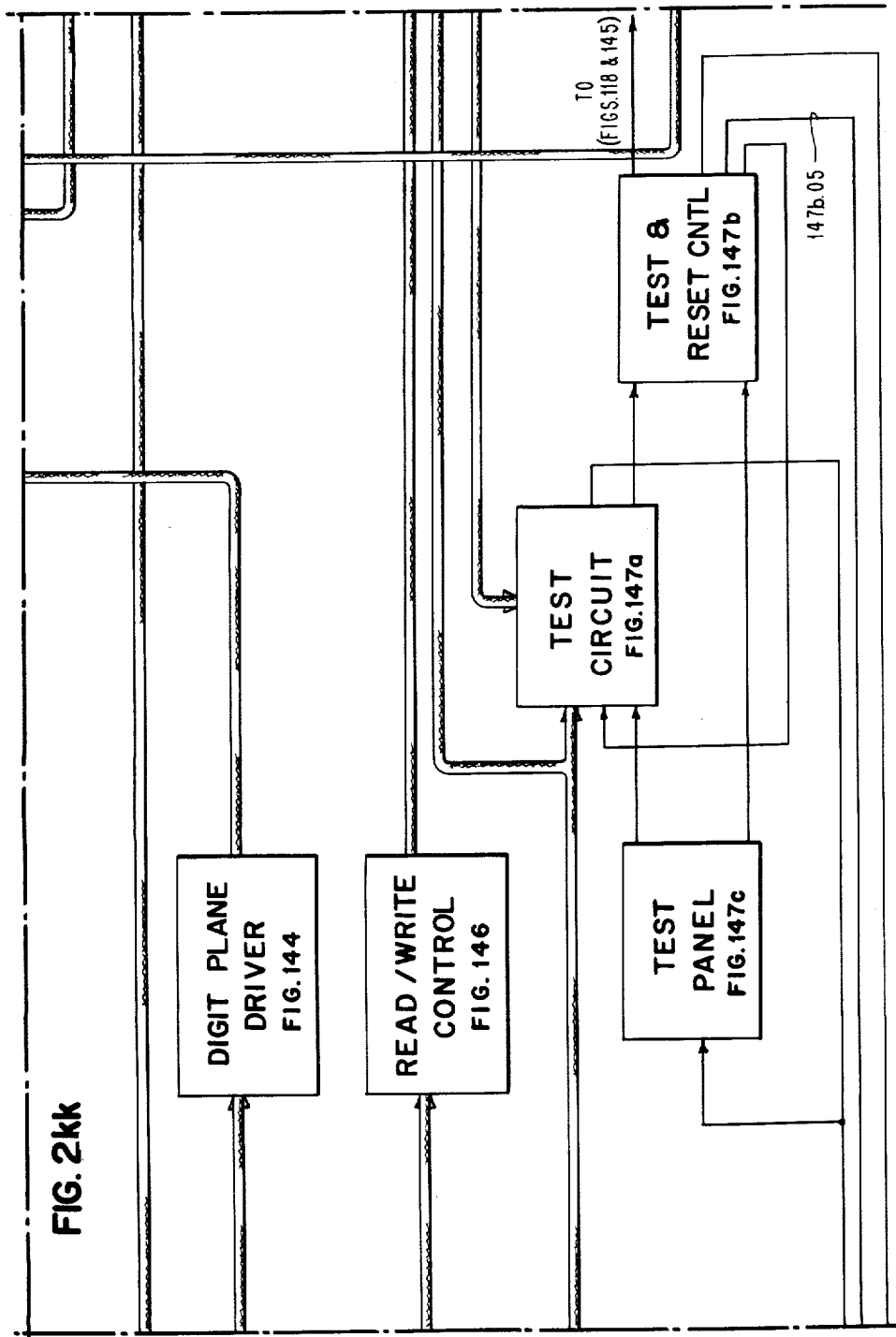
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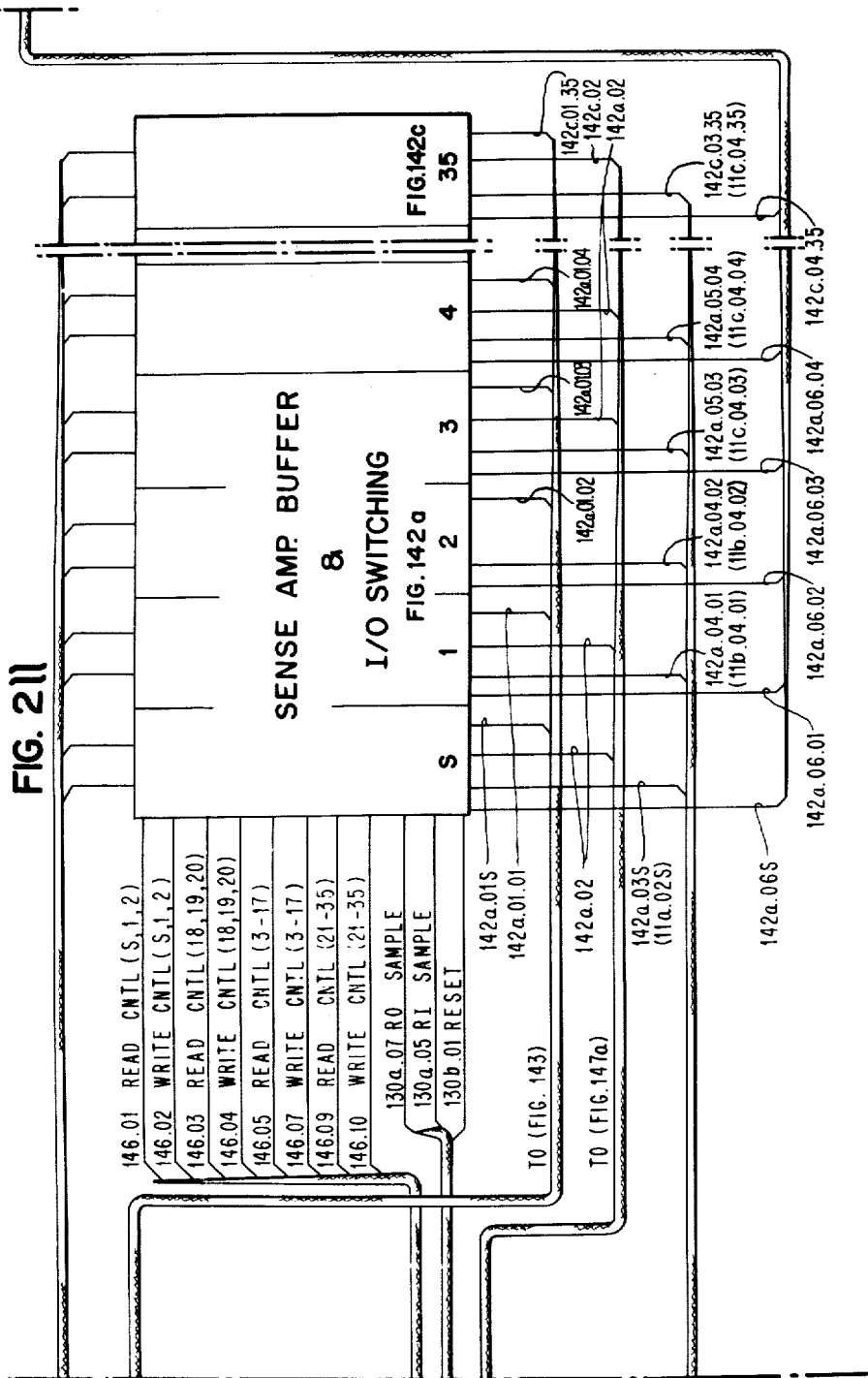
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FIG. 3a

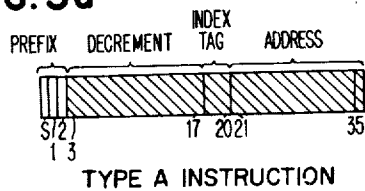


FIG. 3b

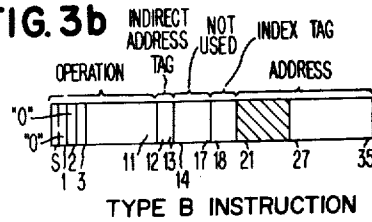


FIG. 3c

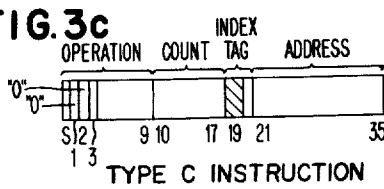


FIG. 3d

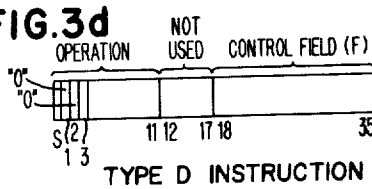


FIG. 3e

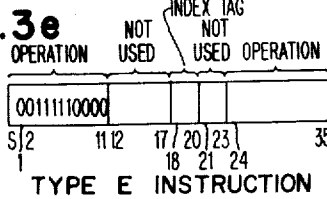


FIG. 3f

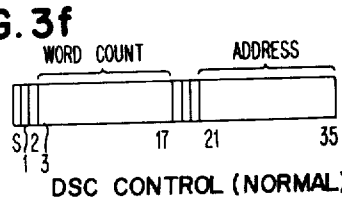


FIG. 3g

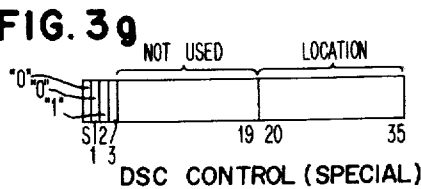


FIG. 3h

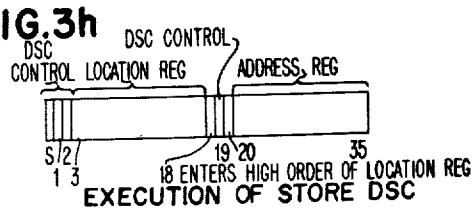


FIG. 3i

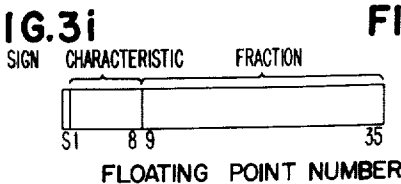


FIG. 3j

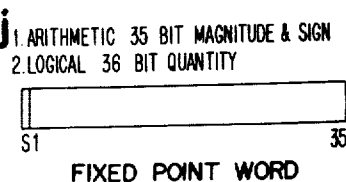
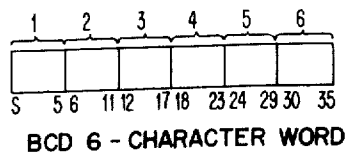


FIG. 3k



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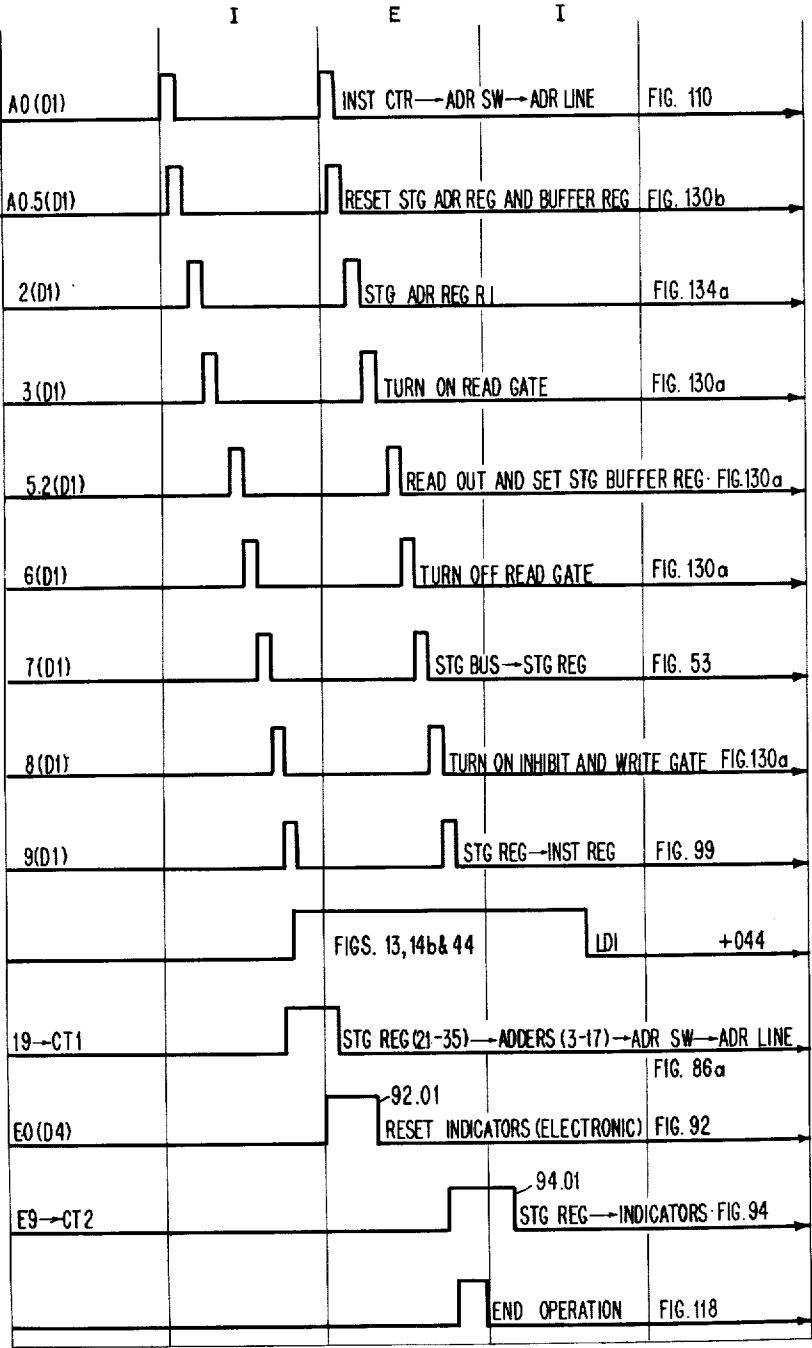
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FIG. 4a  
LOAD INDICATORS +044I  
LDI



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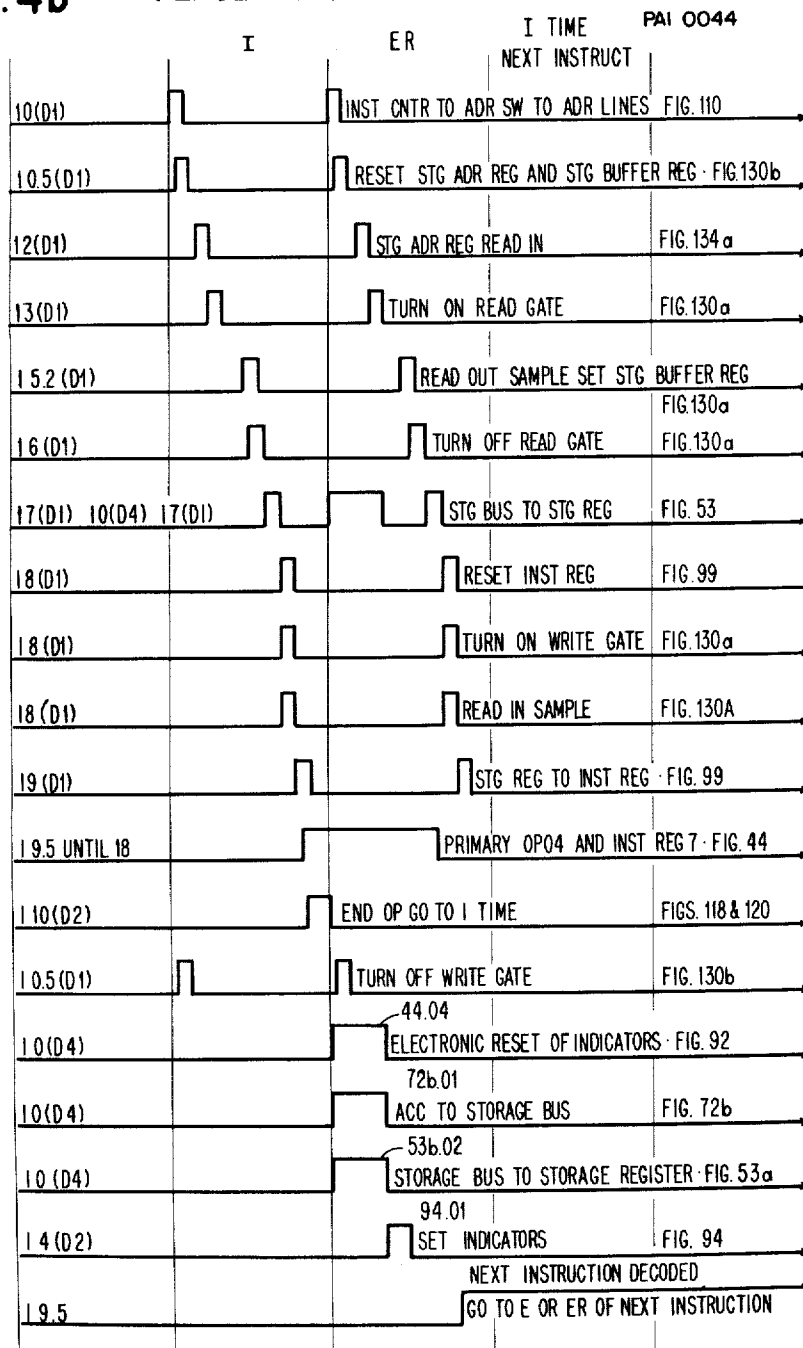
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# FIG. 4b PLACE ACCUMULATOR IN INDICATOR



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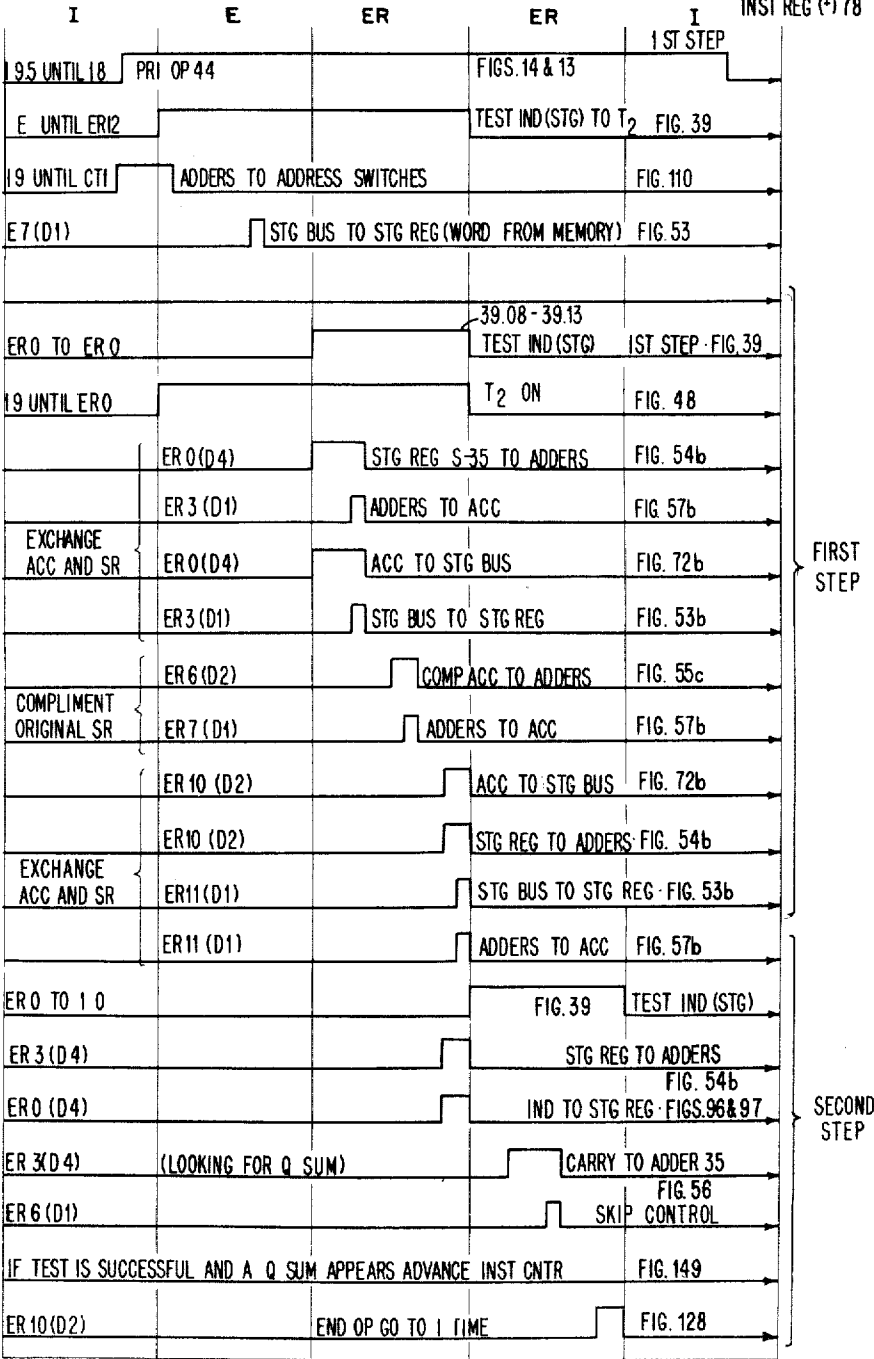
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FIG. 4c

ON TEST FOR INDICATORS  
1ST STEP 2ND STEP

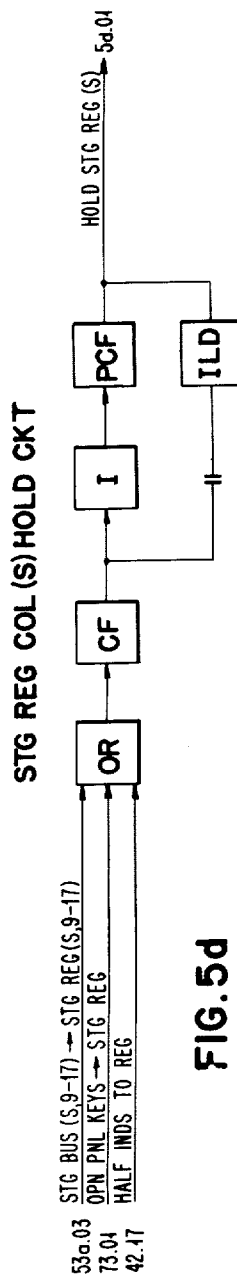
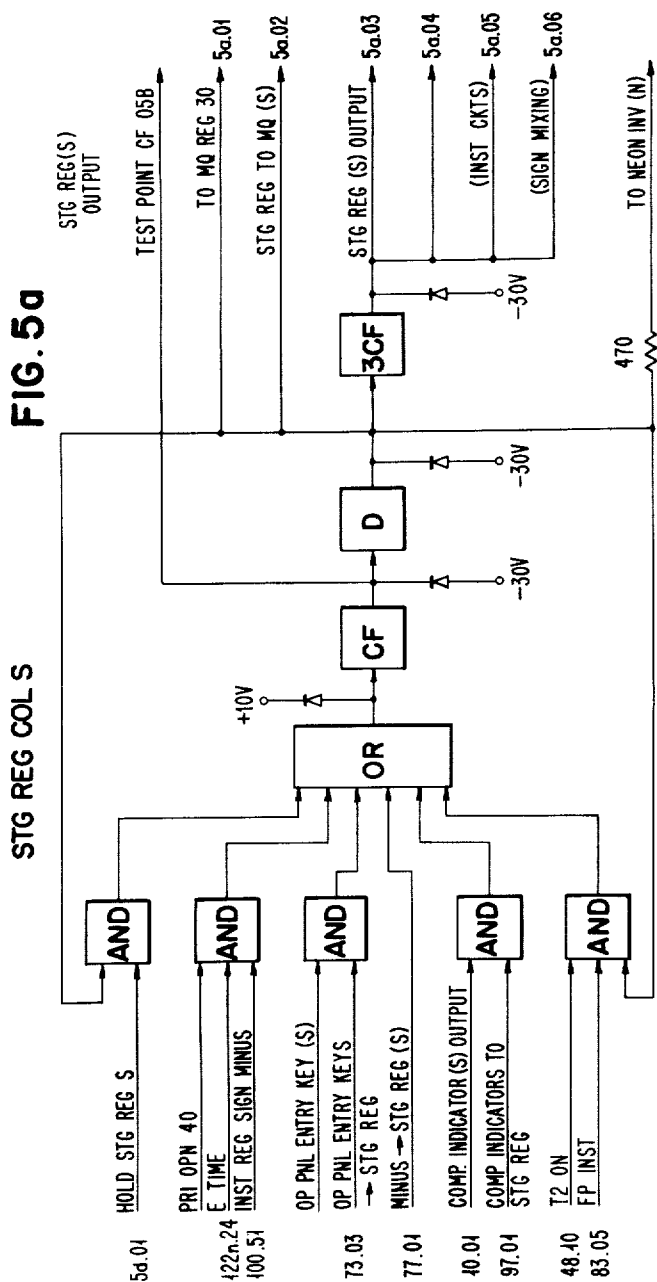
ONT-0446  
PRI OP 44  
INST REG (\*) 78



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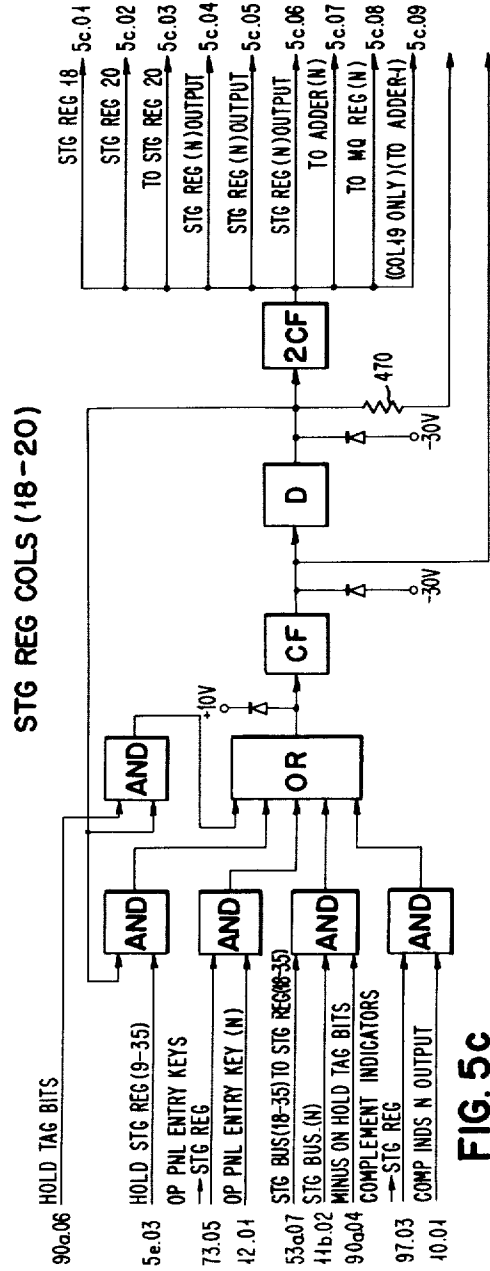
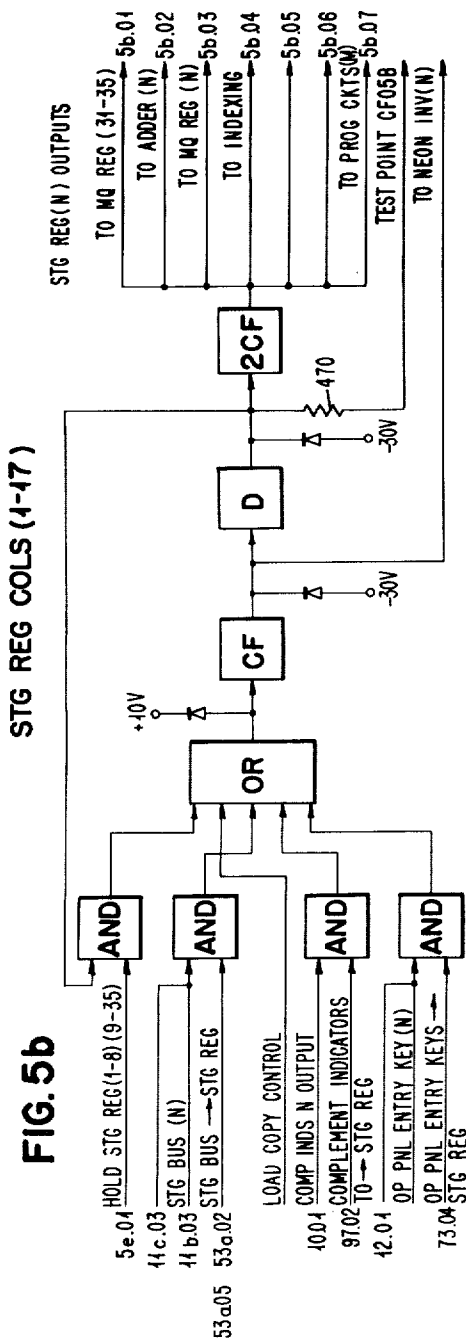
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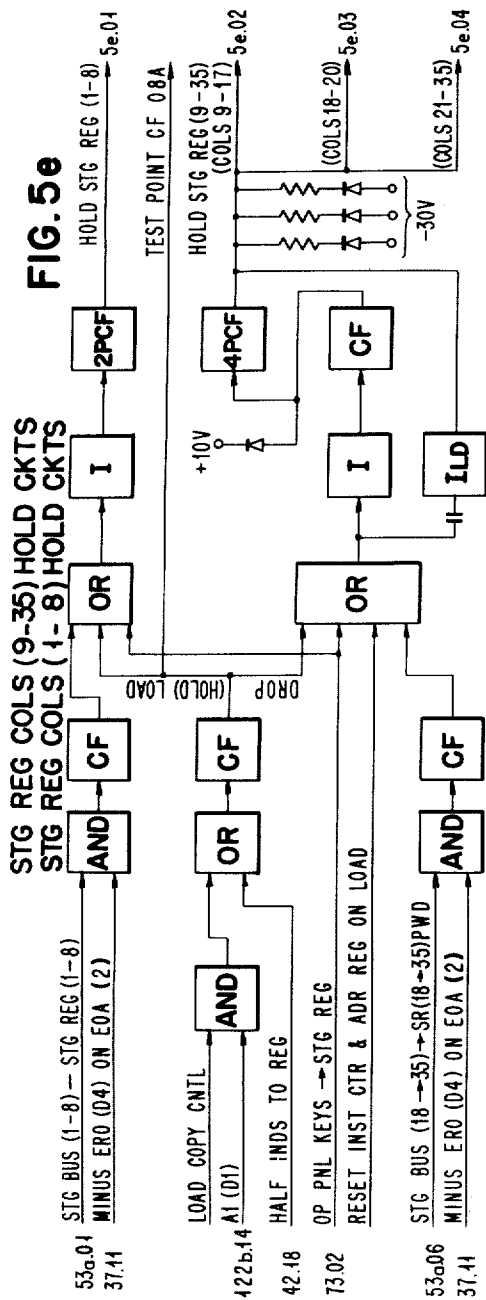
247 Sheets-Sheet 46



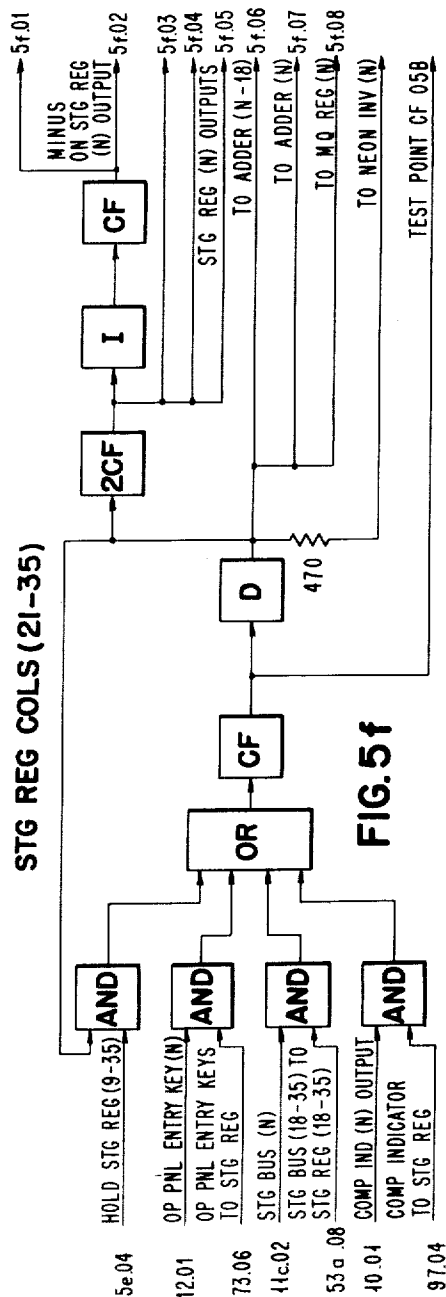
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AN INDICATING REGISTER

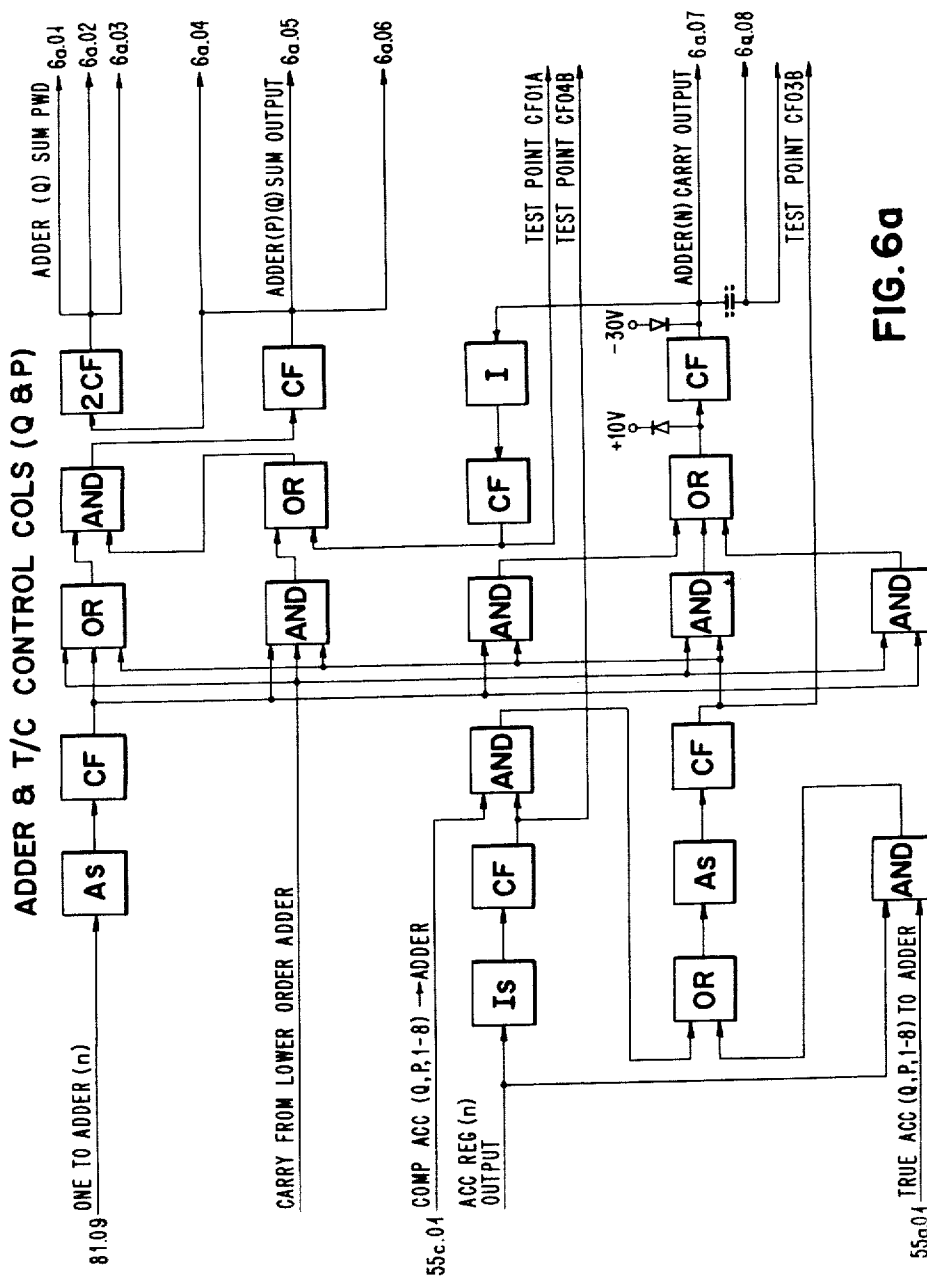
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**FIG. 5e**



STG REG COLS (21-35)





**FIG. 6a**

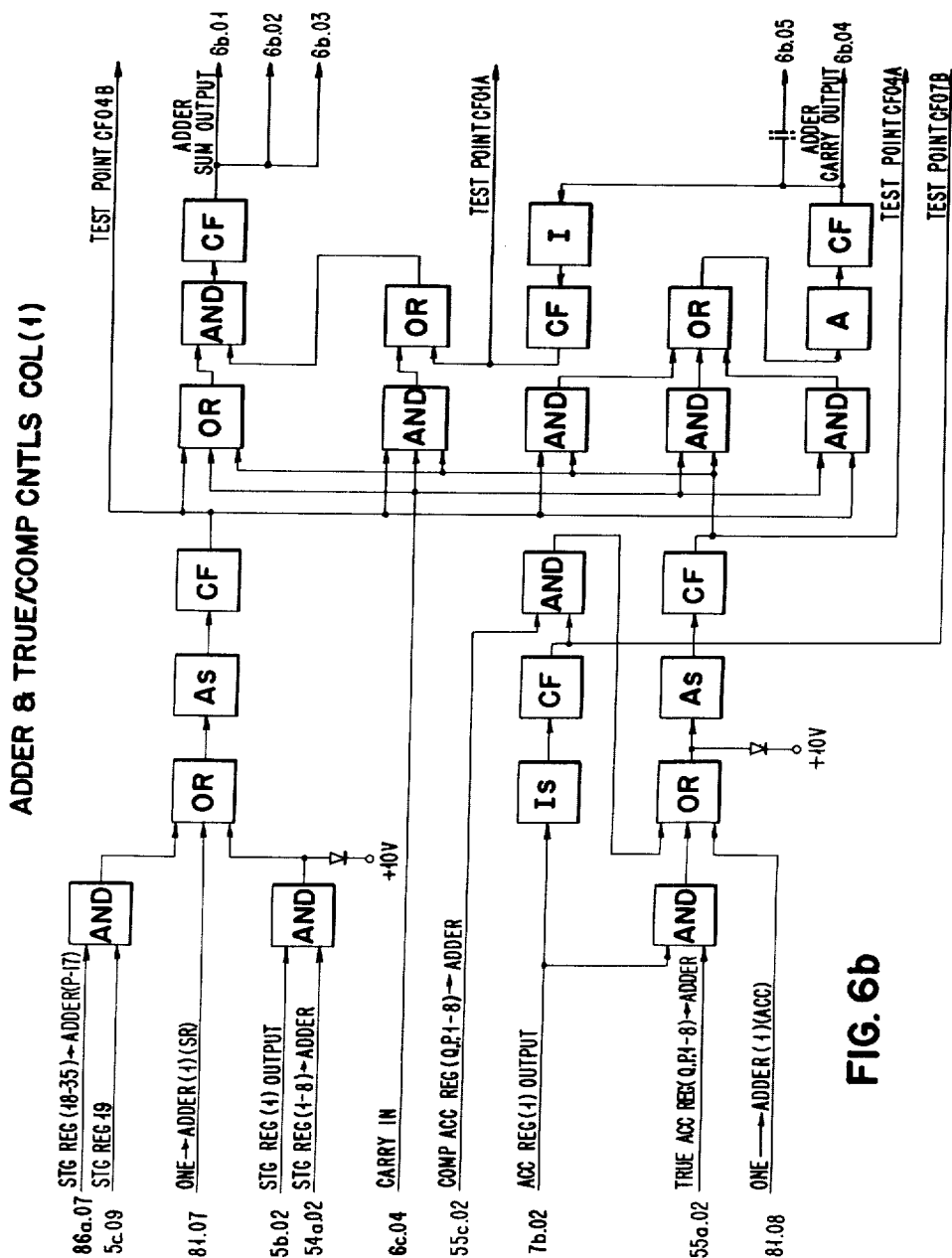
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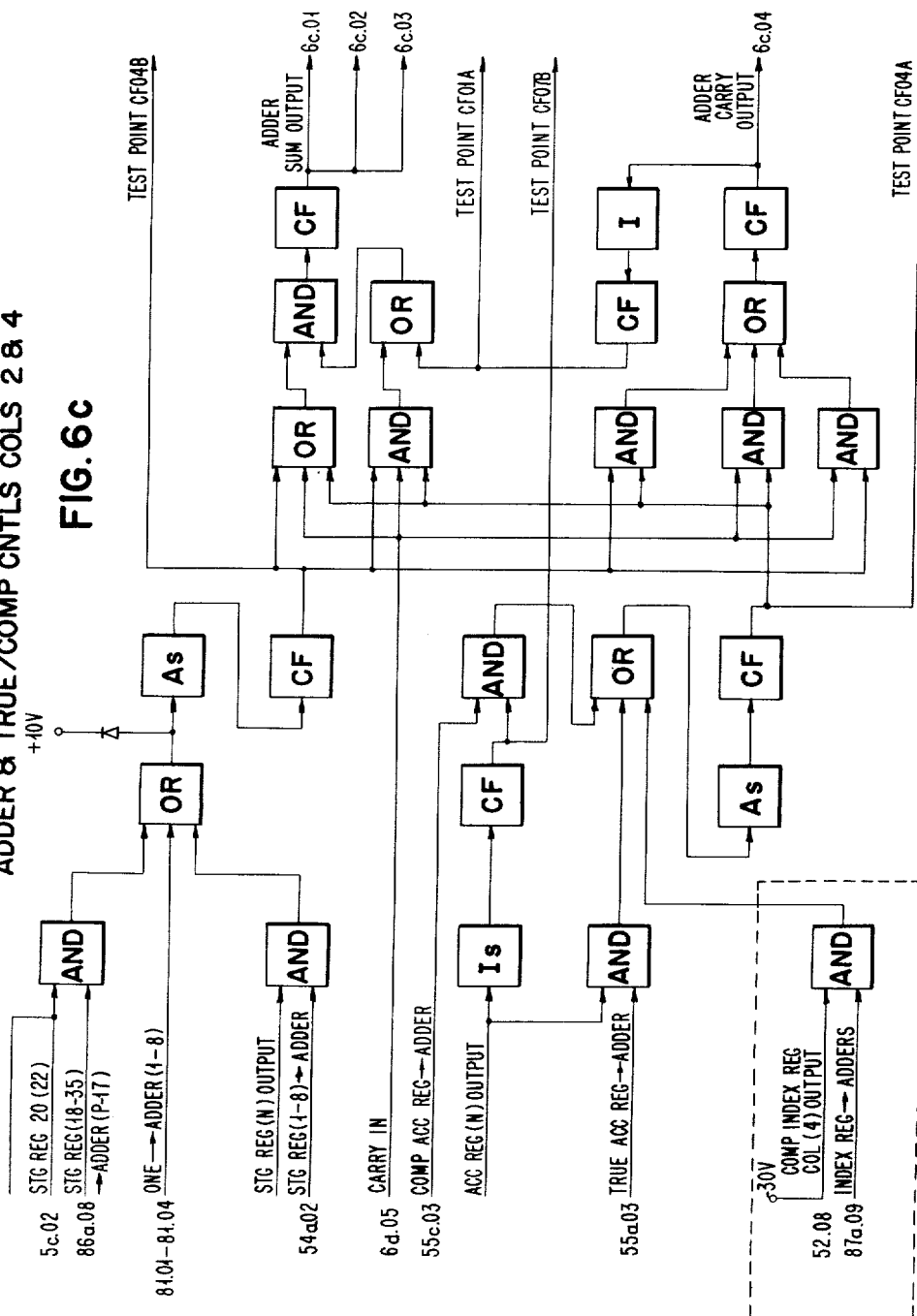
**FIG. 6b**

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ADDER &amp; TRUE/COMP CNTLS COLS 2 &amp; 4

**FIG. 6c**



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ADDER & TRUE /COMP CNTLS COLS 3 & 5

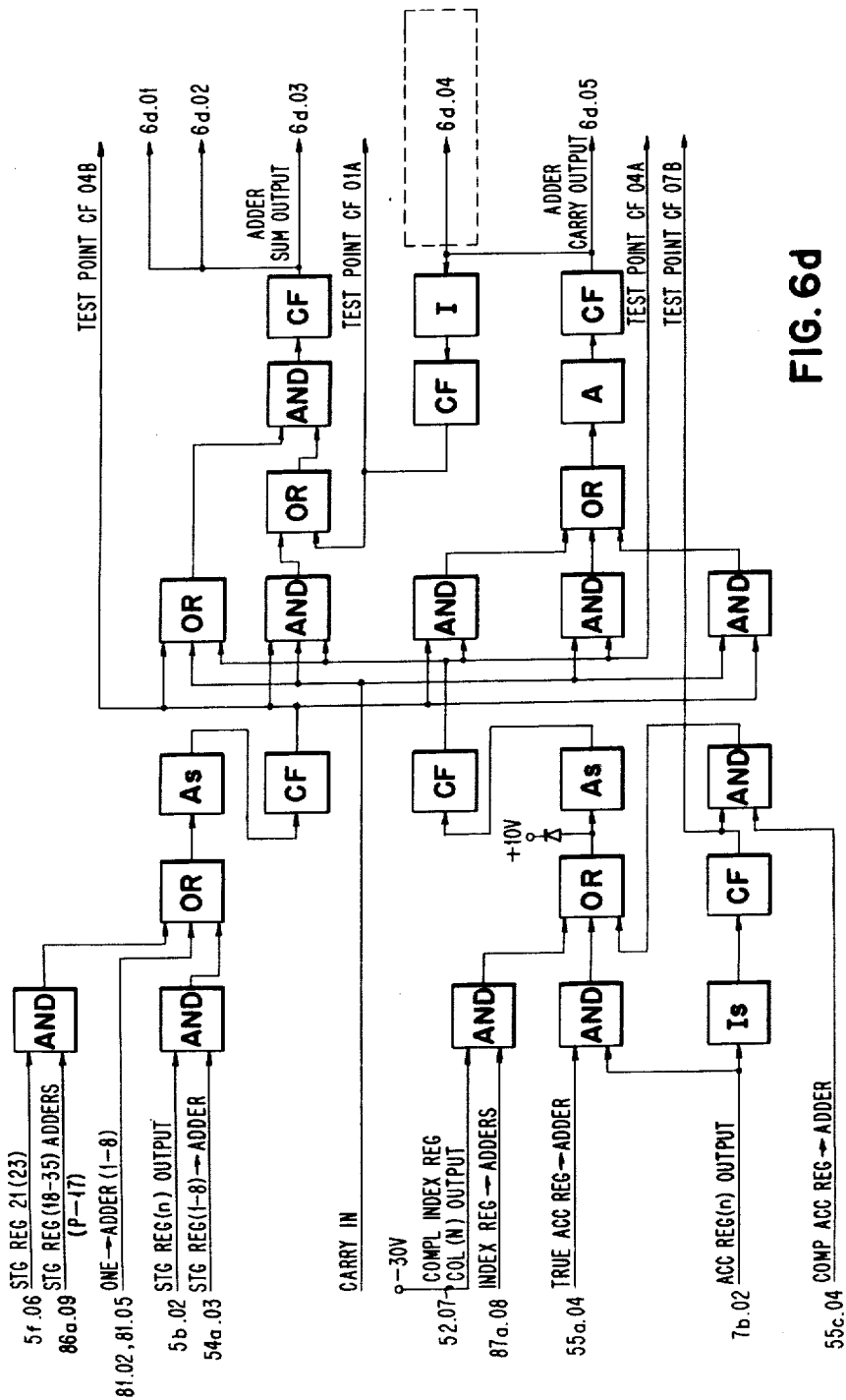
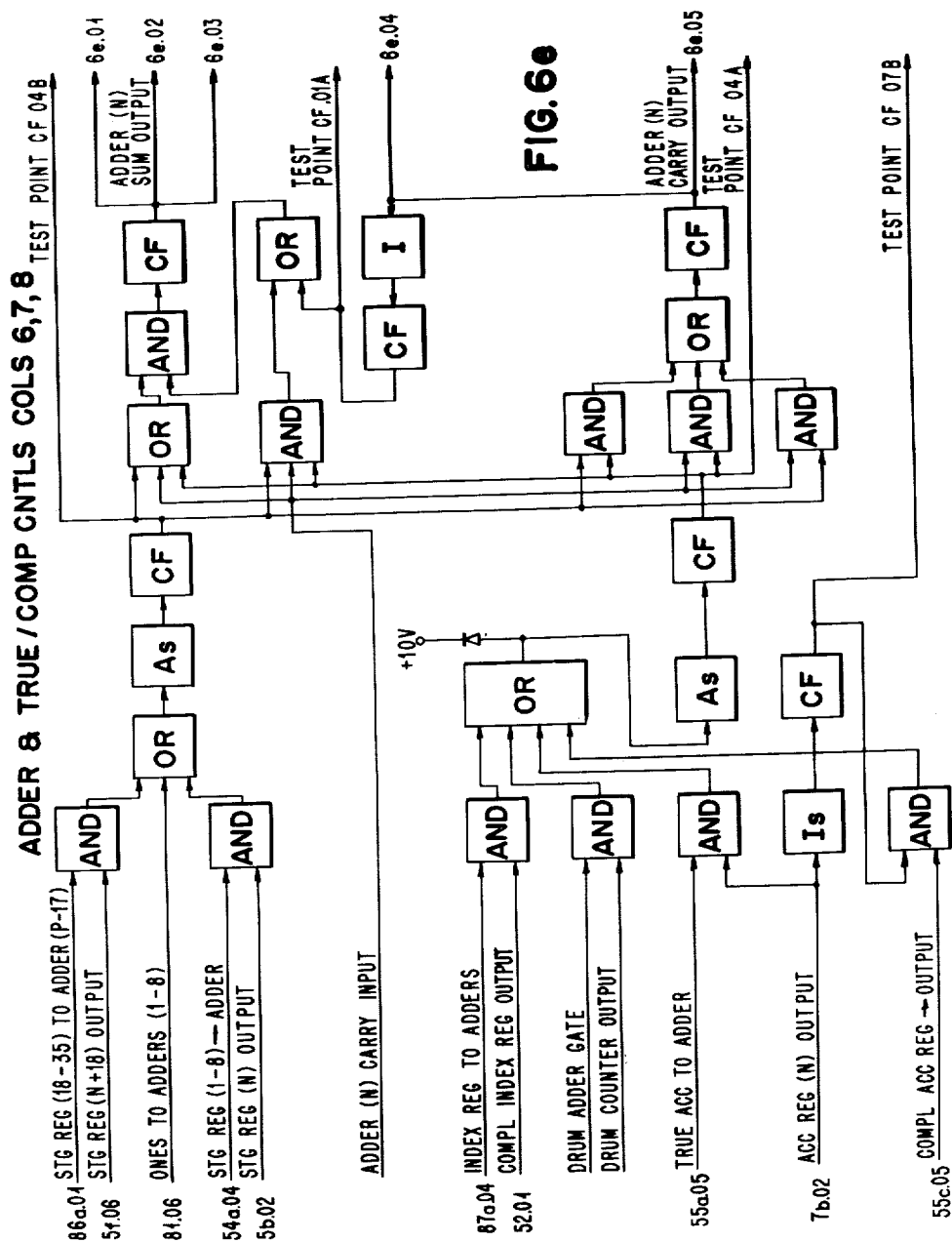


FIG. 6d

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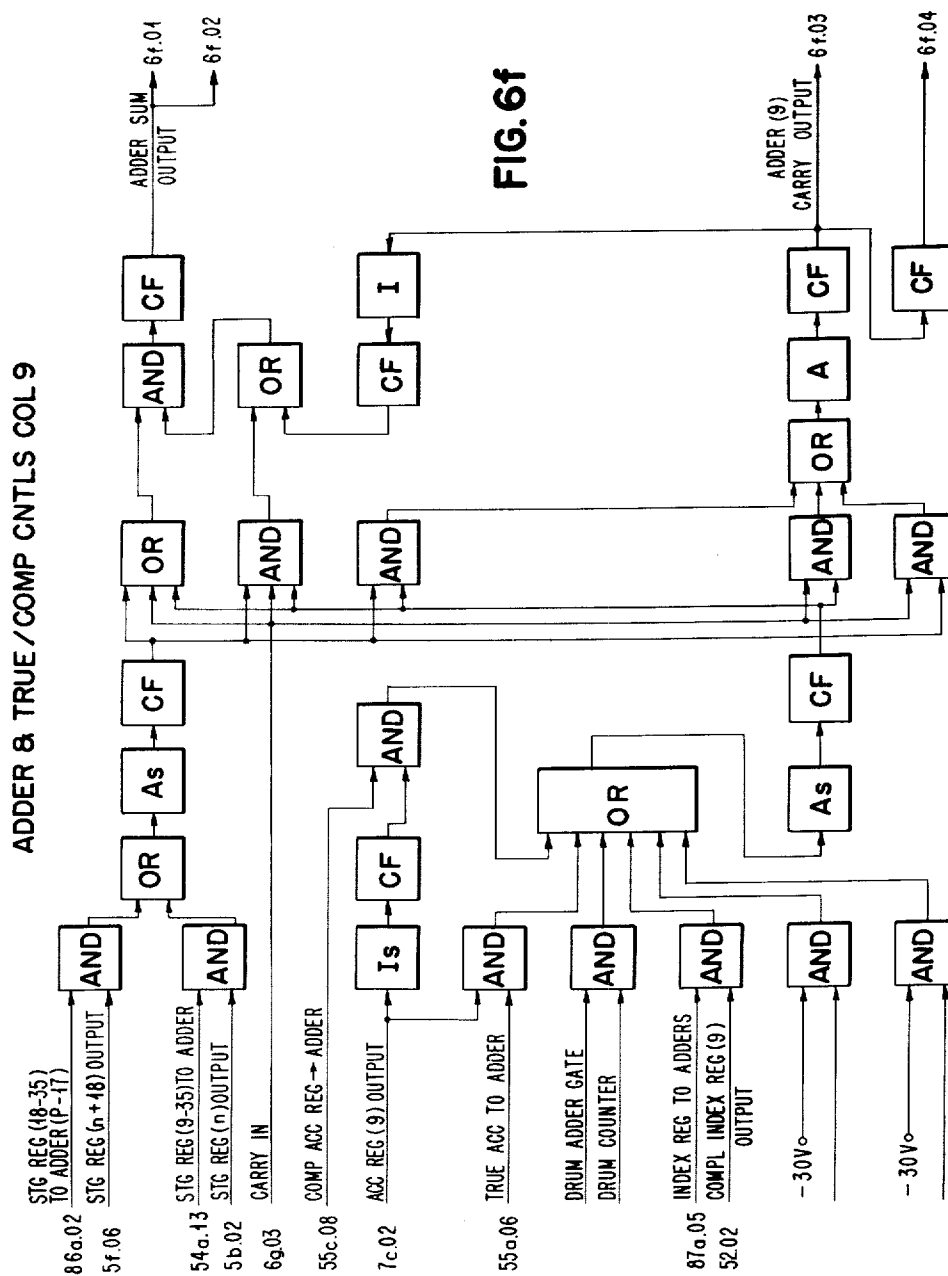
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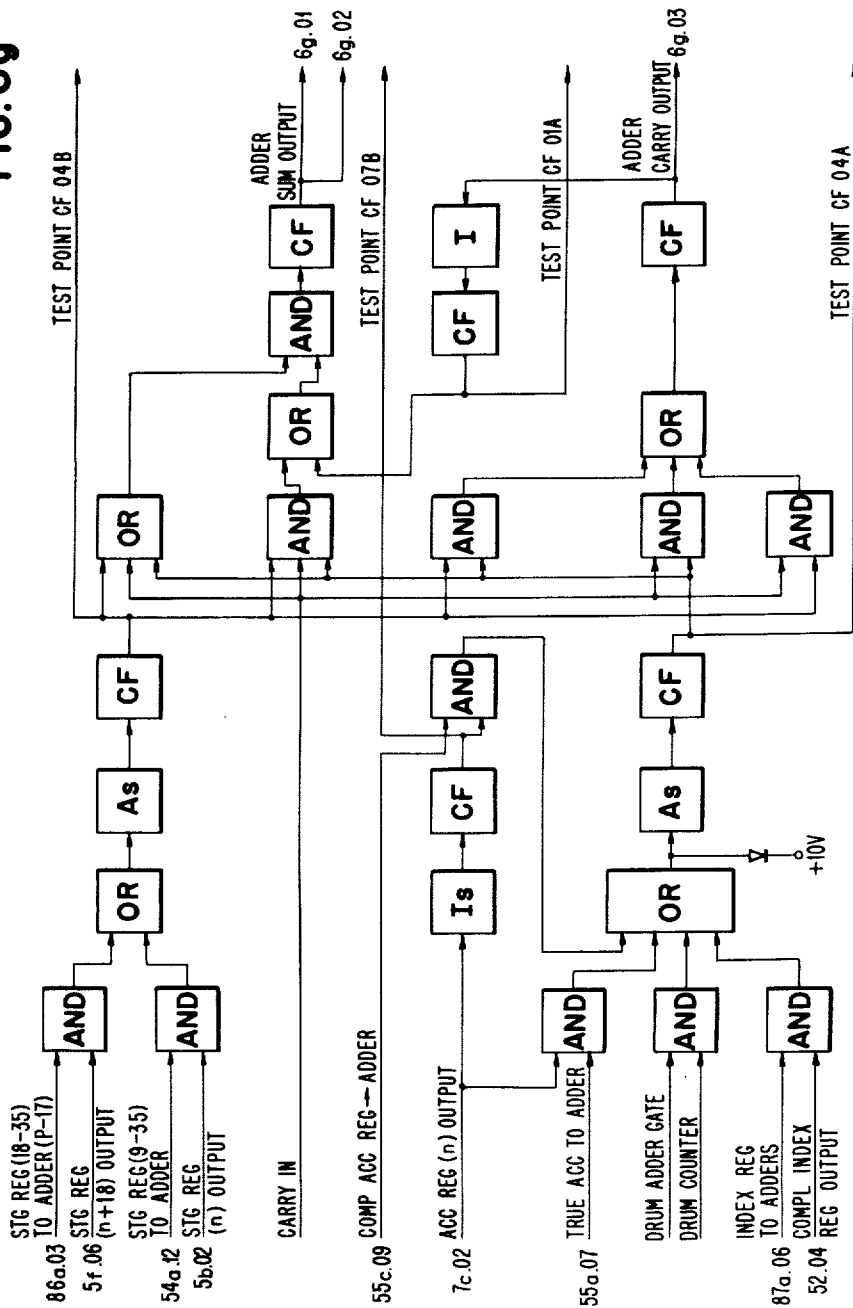
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247 Sheets-Sheet 54

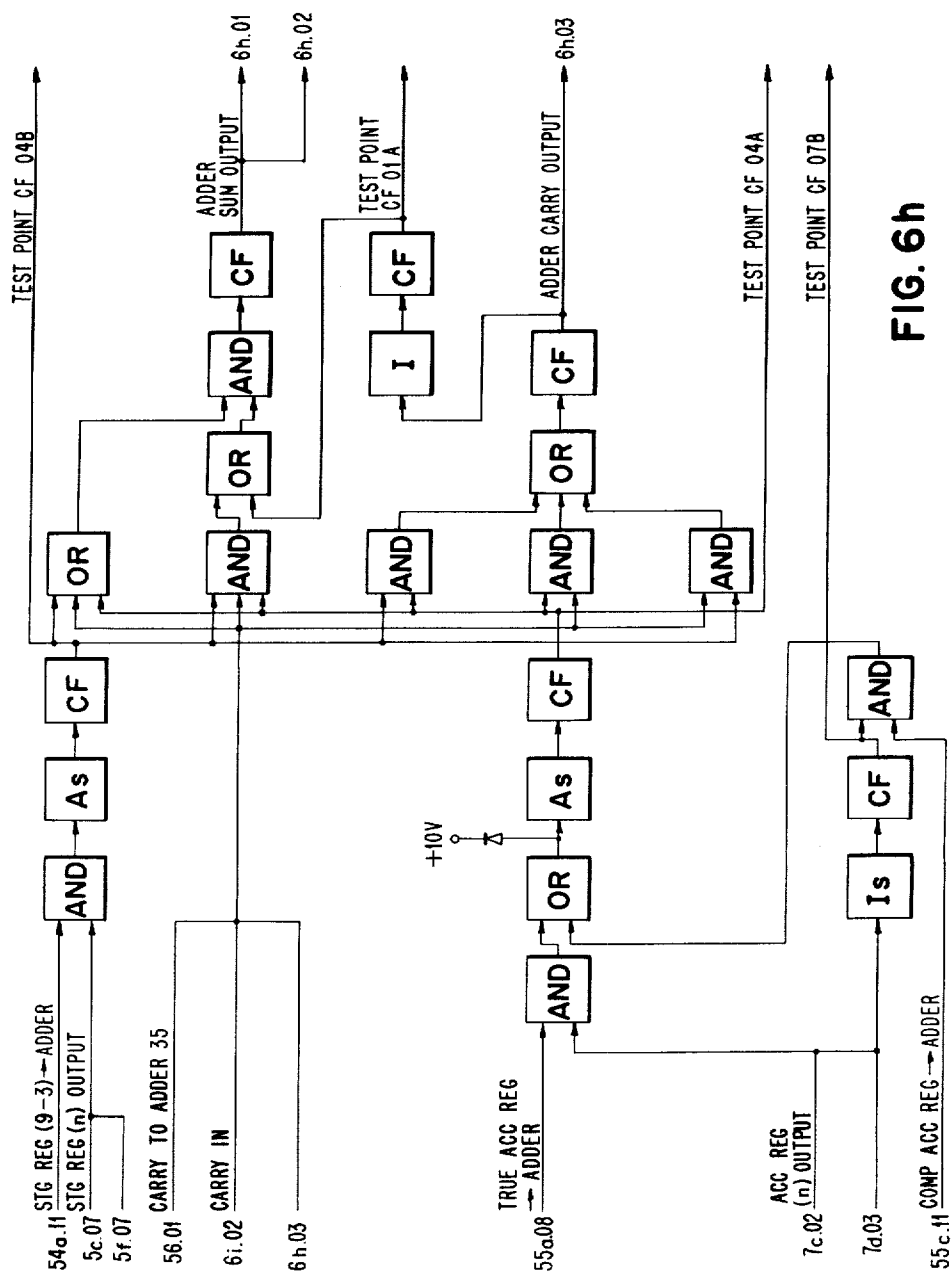
ADDER & TRUE/COMP CNTLS COLS 10, 11 **FIG. 6g**



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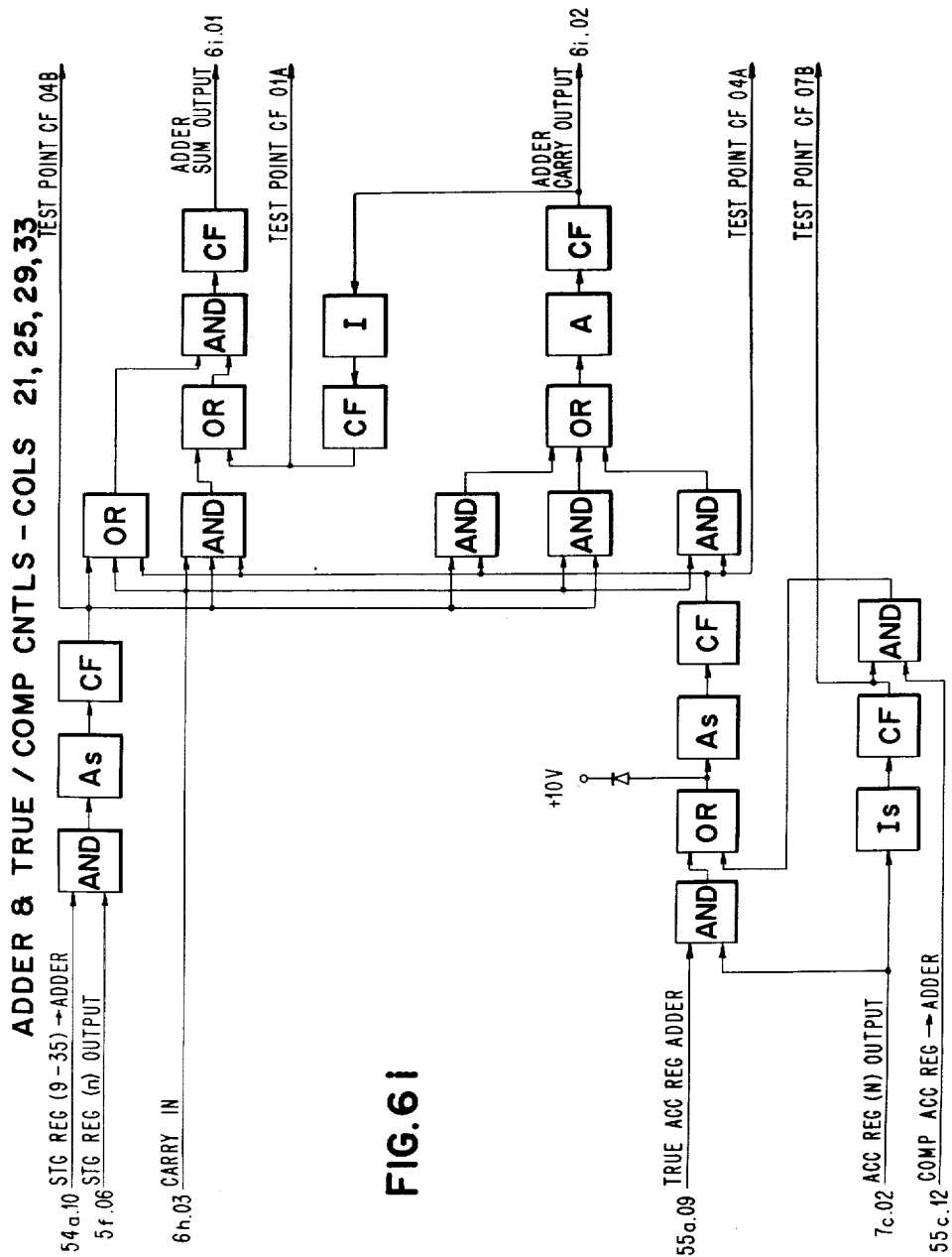
**FIG. 6h**

ADDER & TRUE/COMP CNTL COLS 18-20,22-24,26-28,30-32,34,35

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ADDER & TRUE / COMP CNTLS COL 16

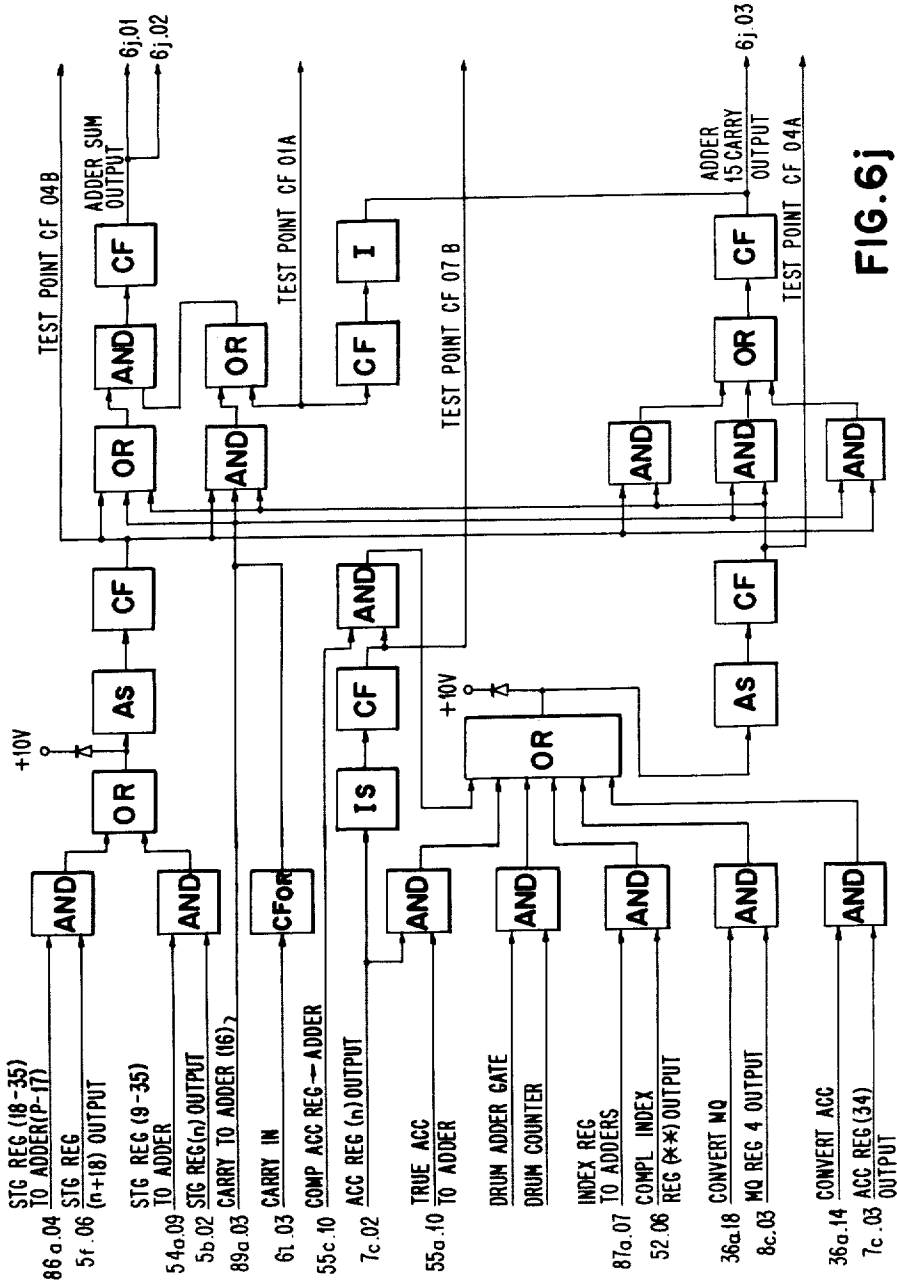
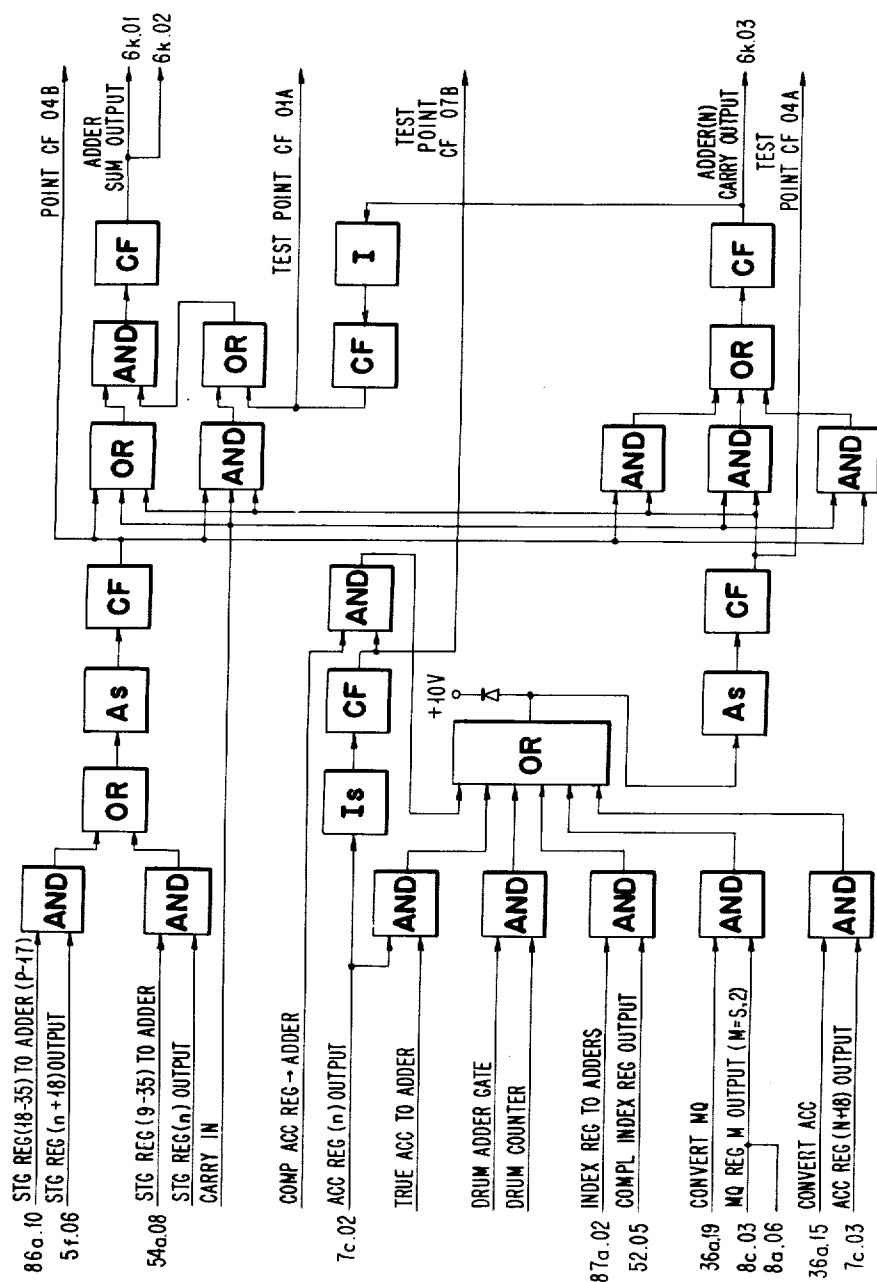


FIG. 6j

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**FIG. 6k**



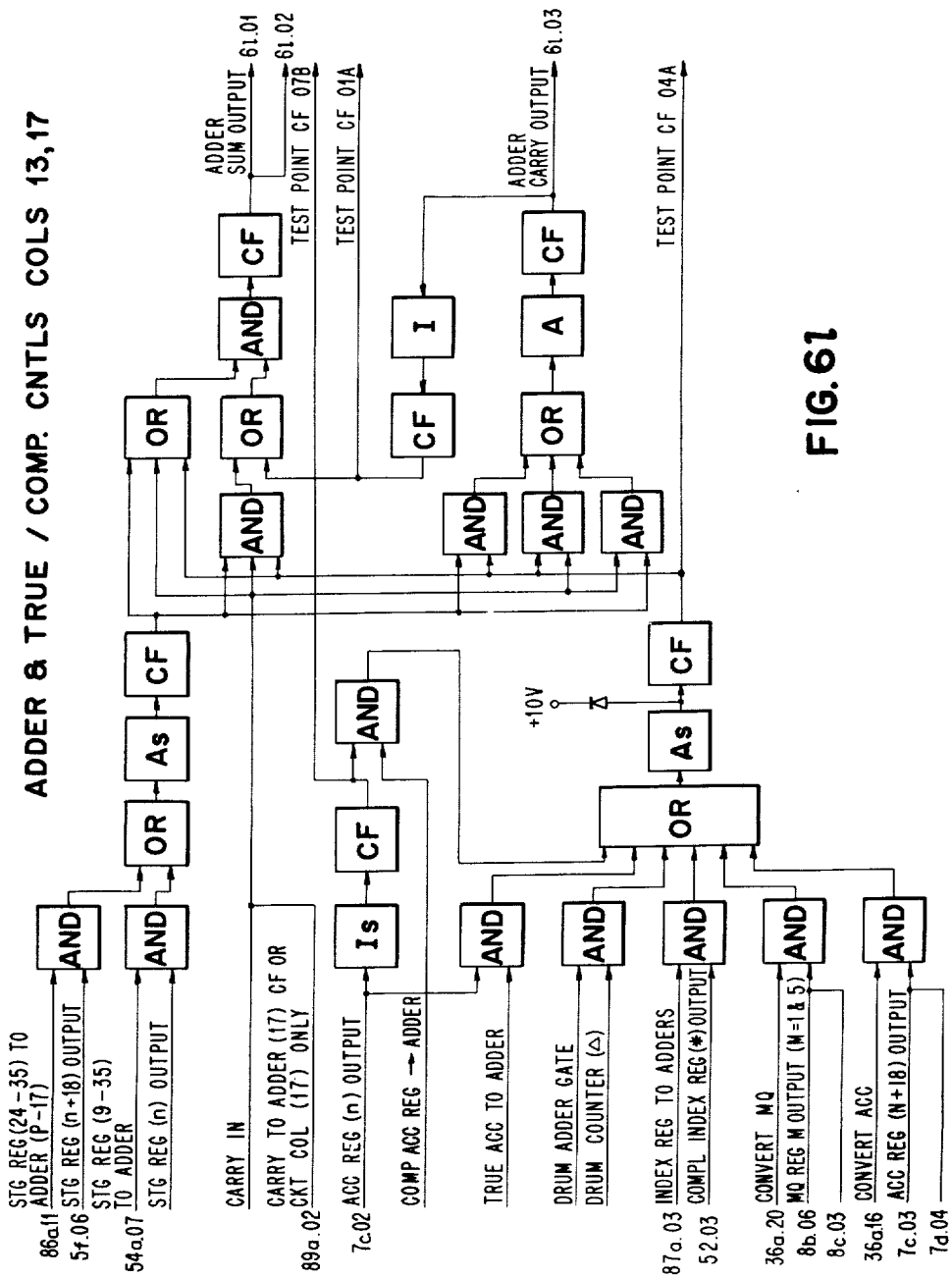
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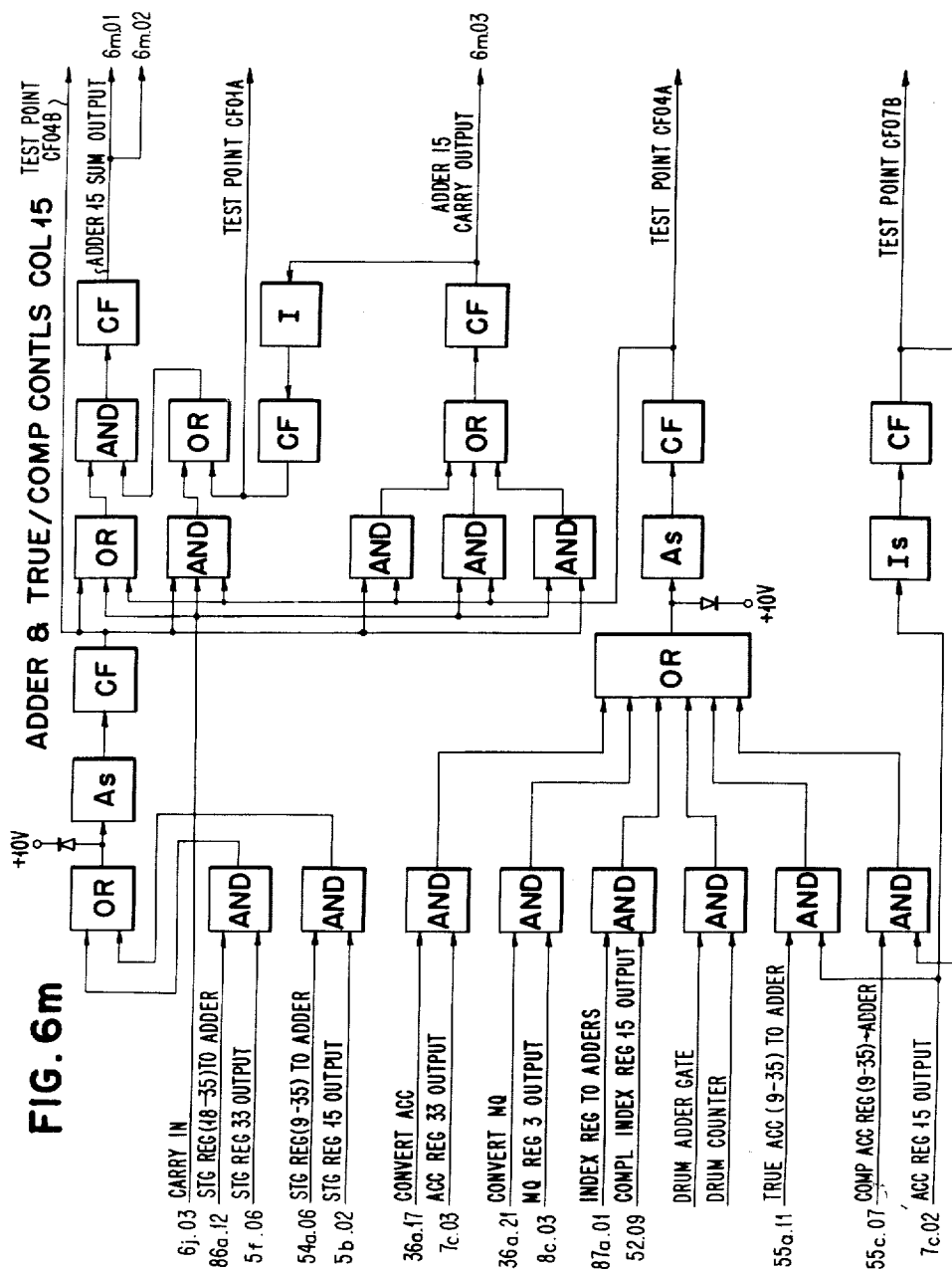
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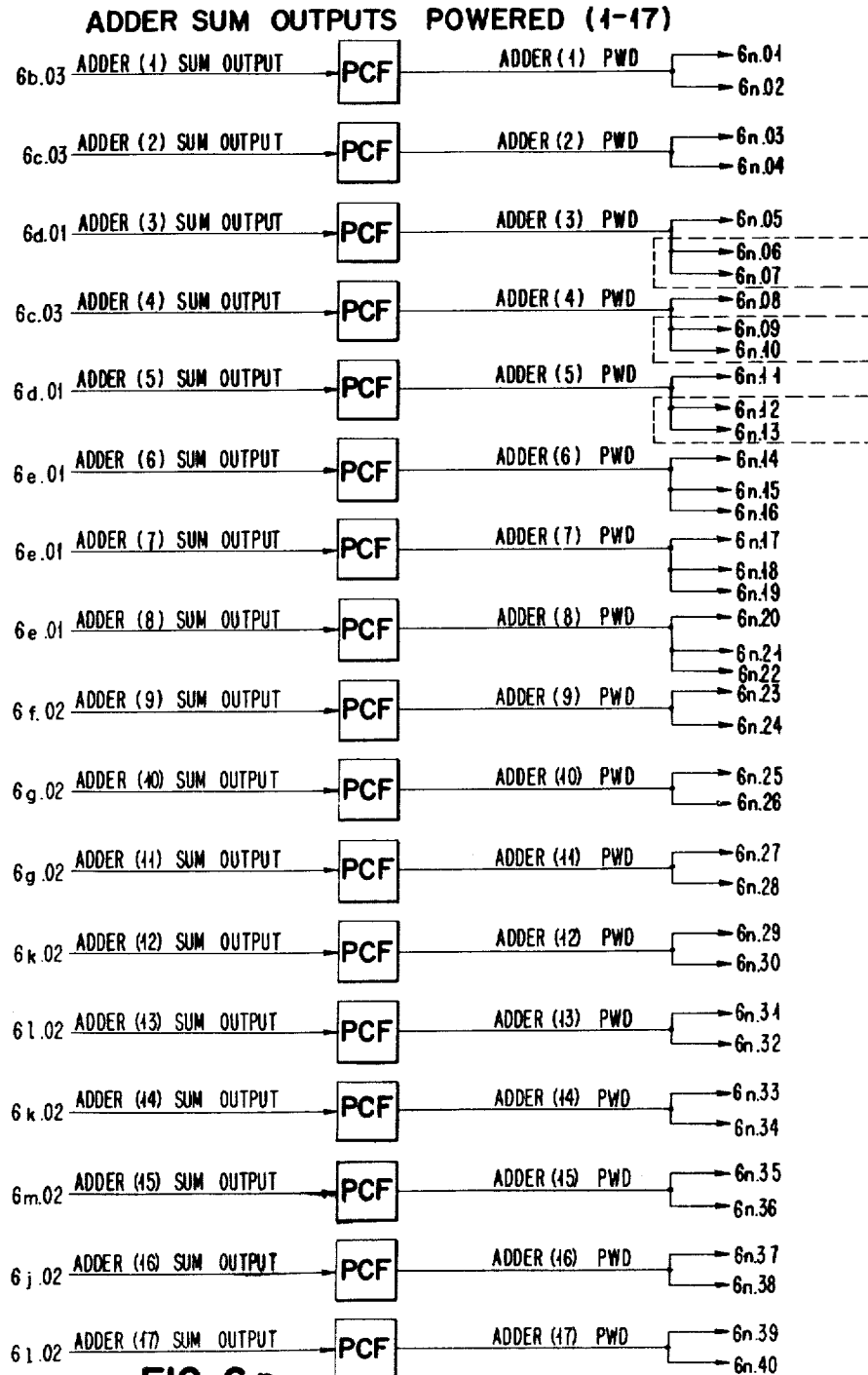
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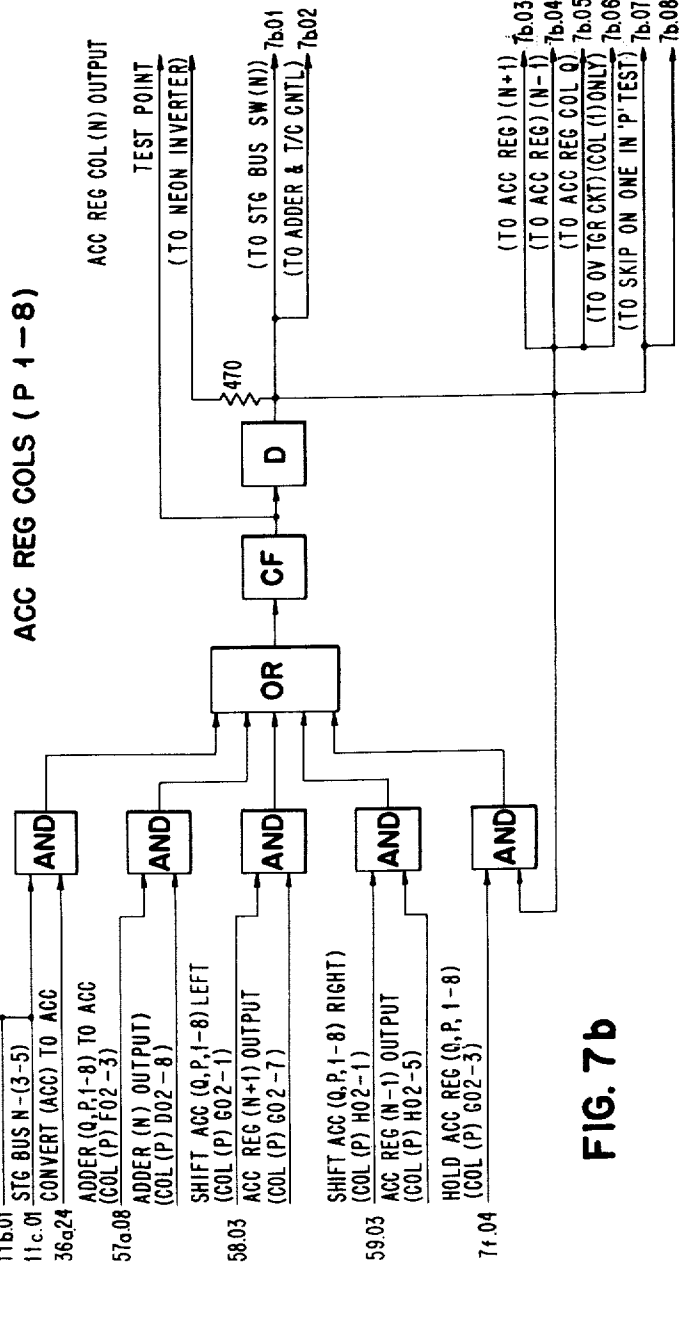
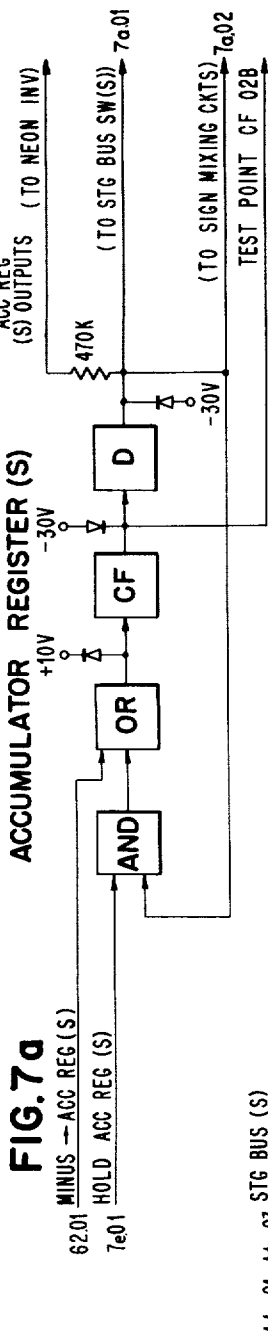
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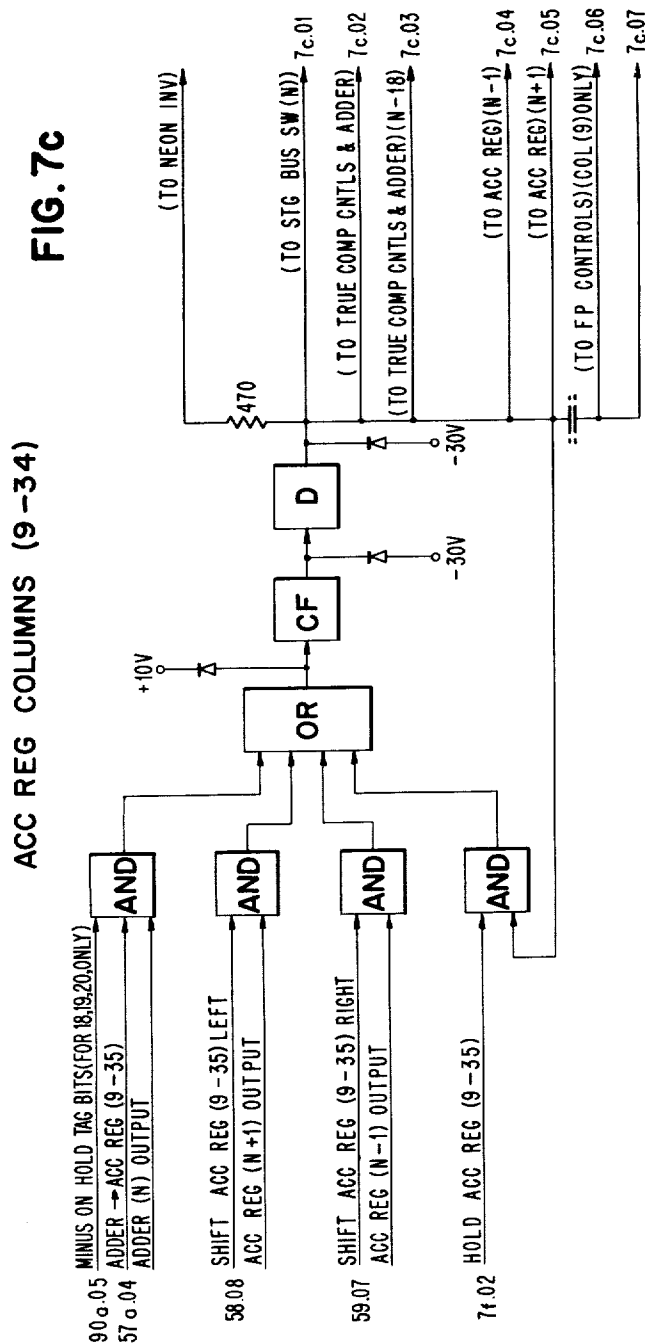
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247 Sheets-Sheet 62

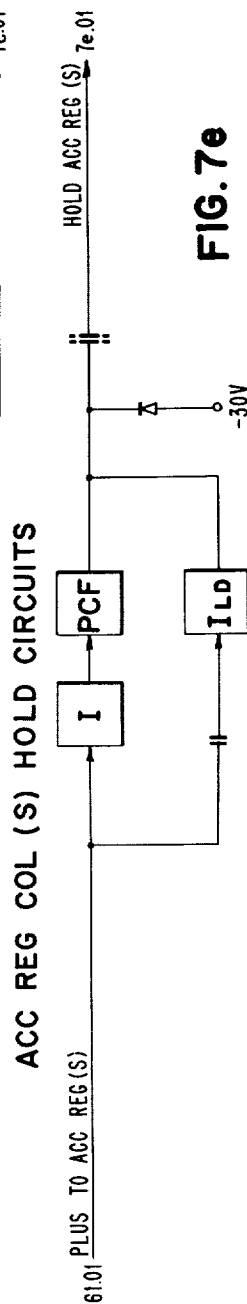


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**FIG. 7c**



**FIG. 7e**



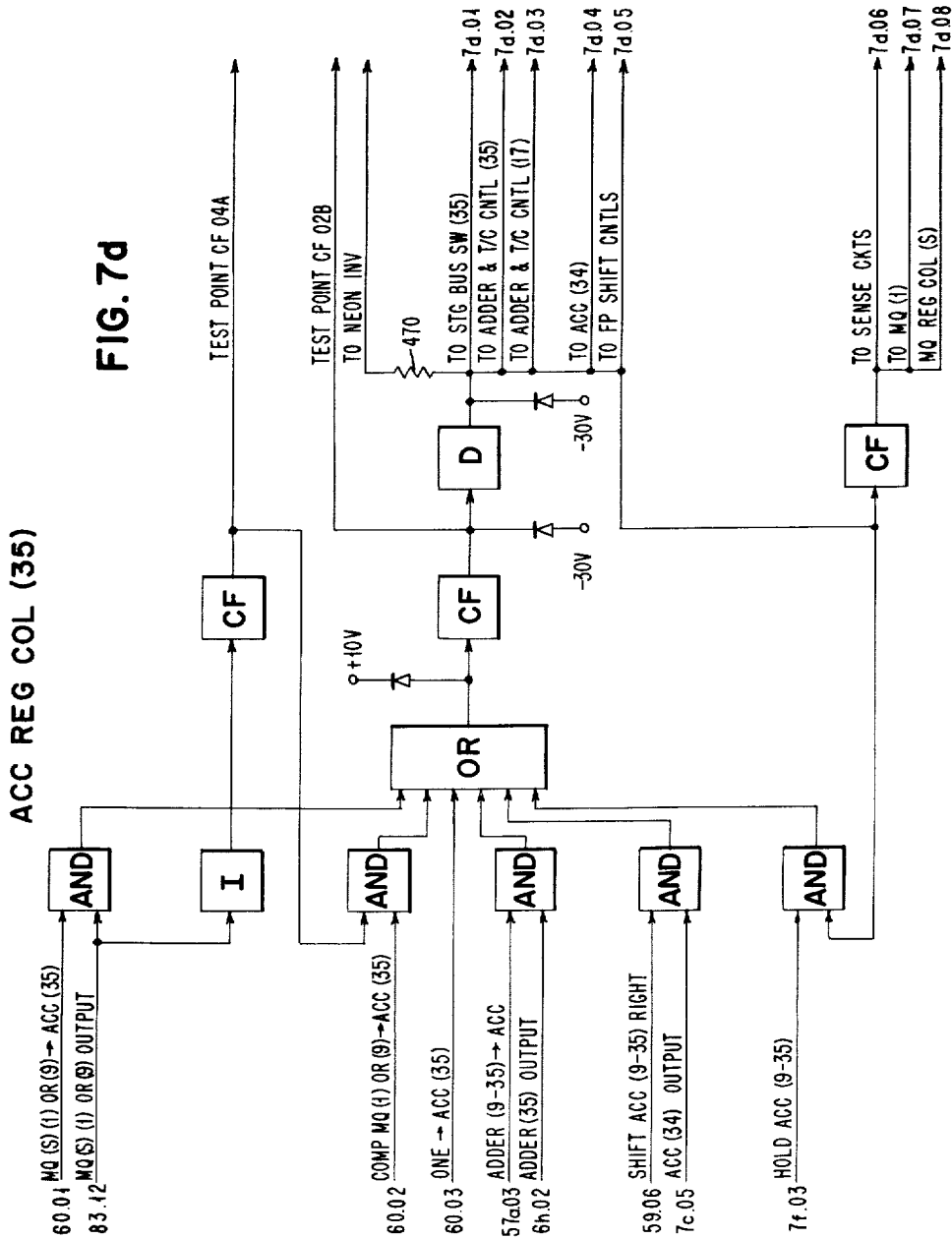
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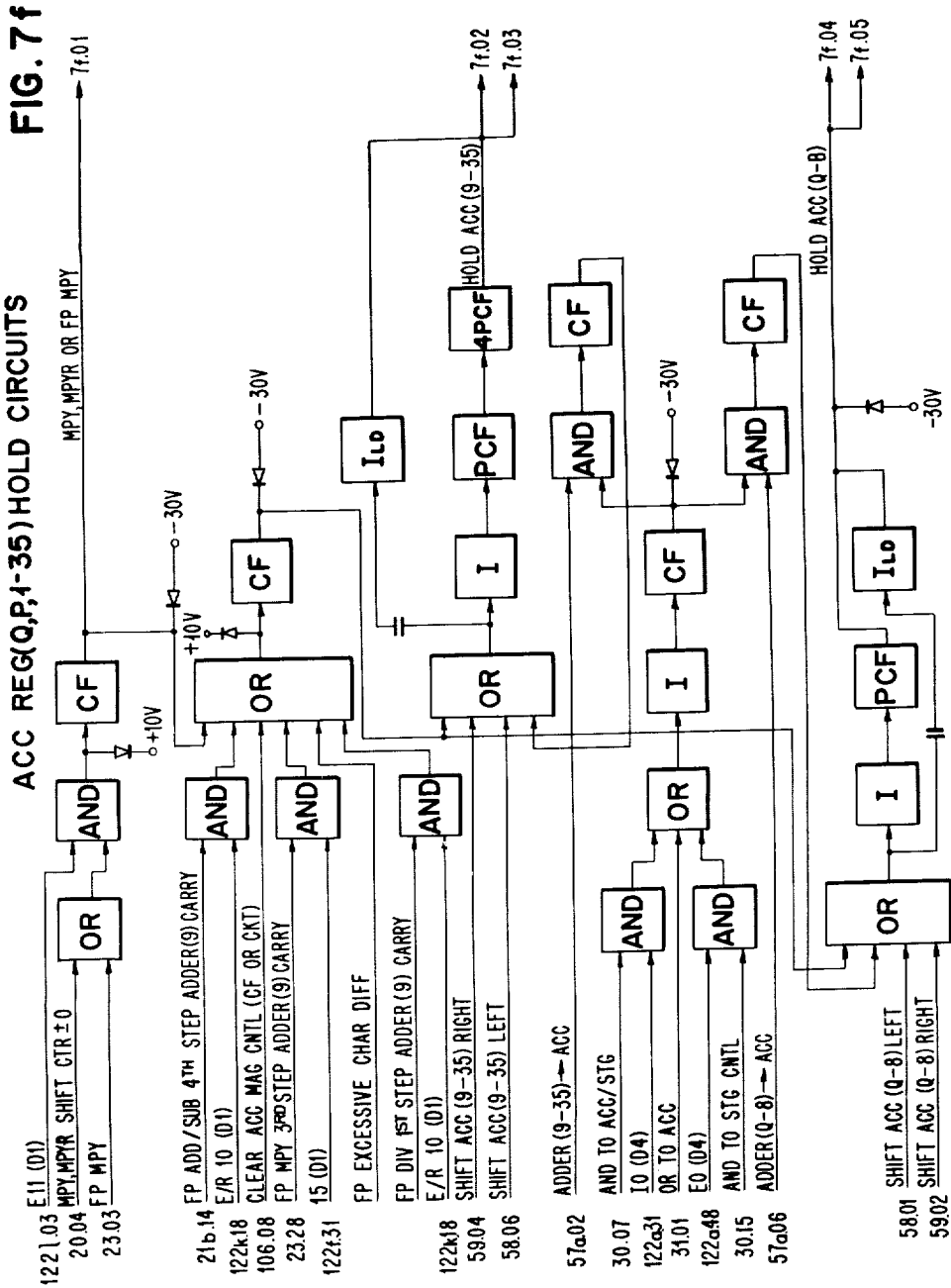
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AN INDICATING REGISTER

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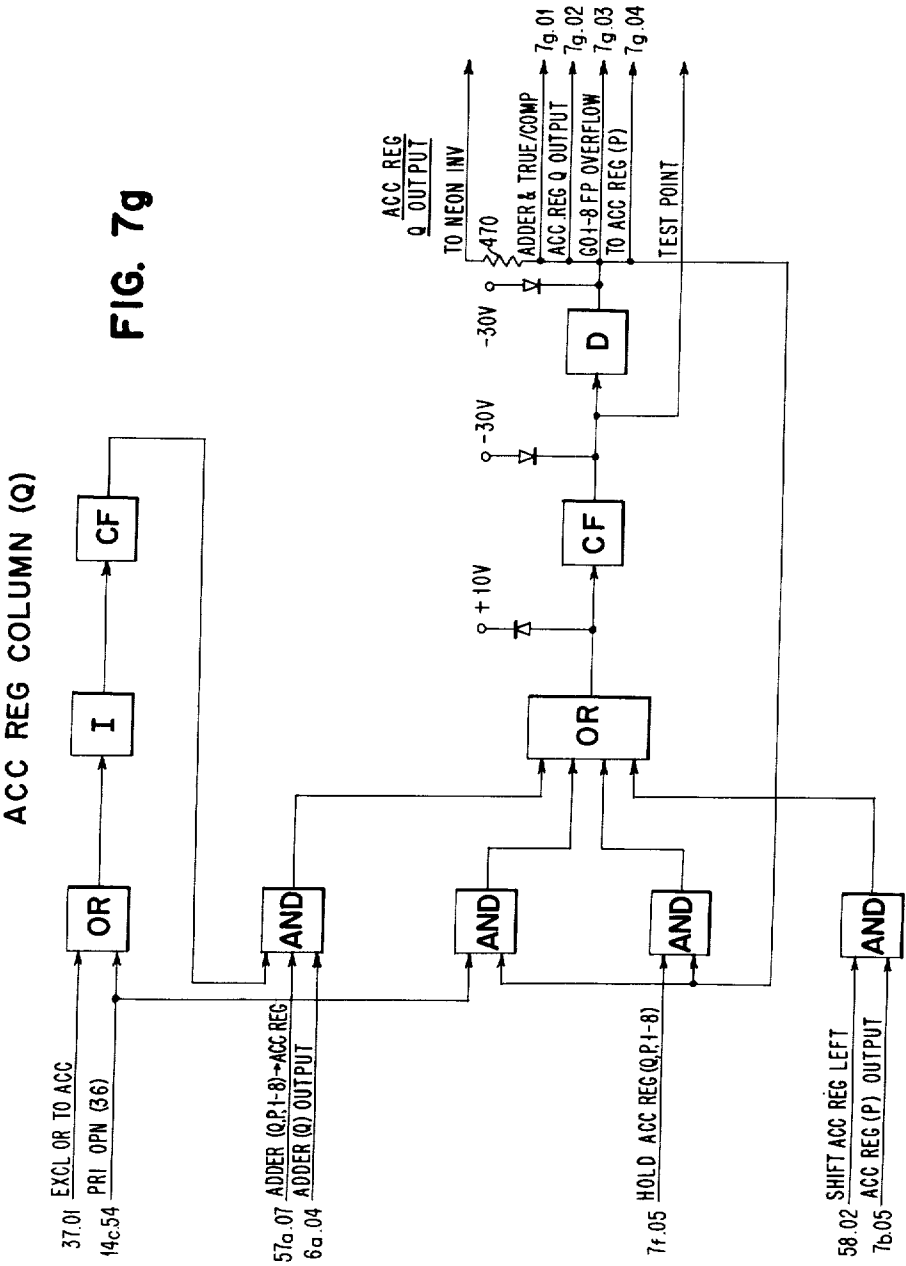
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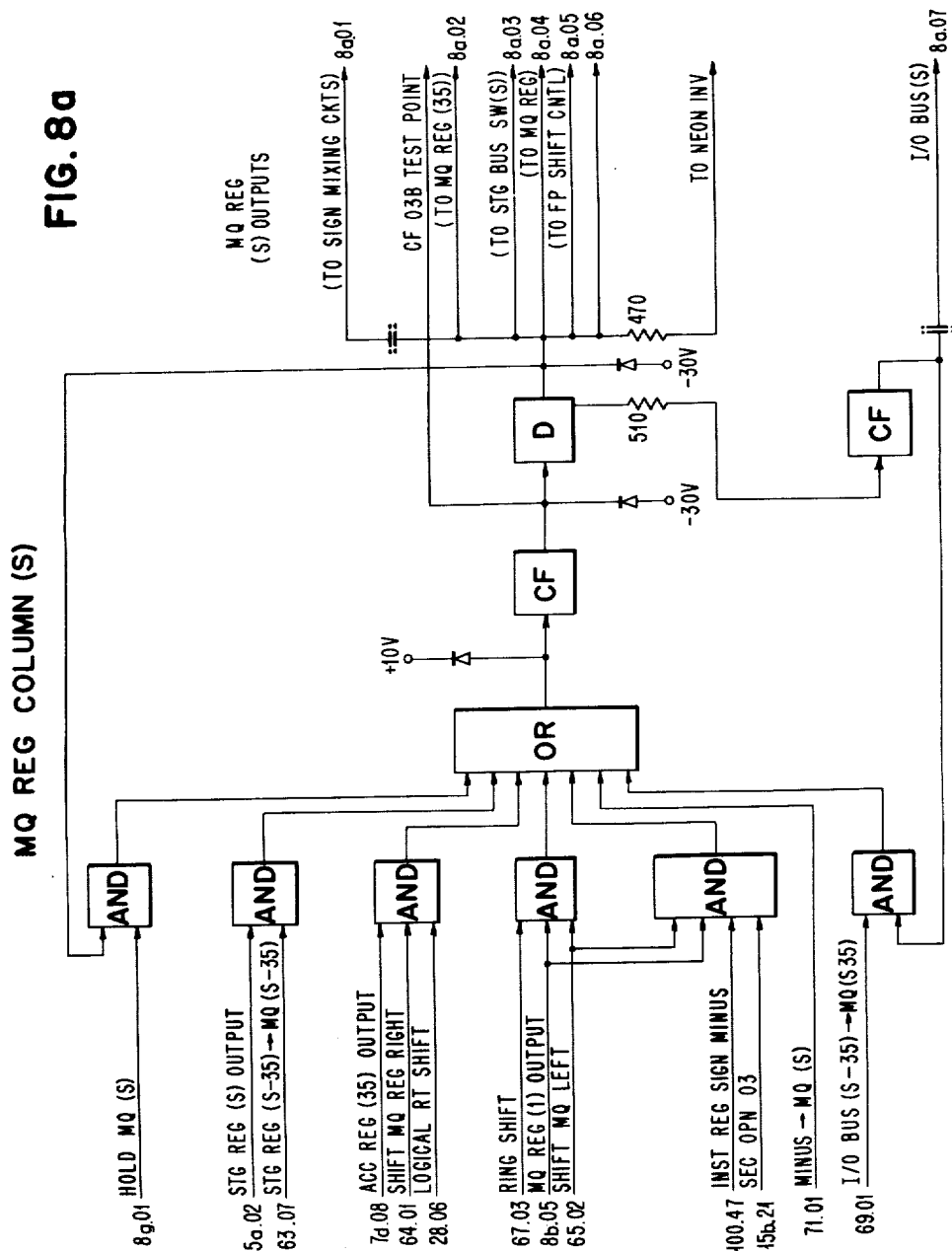
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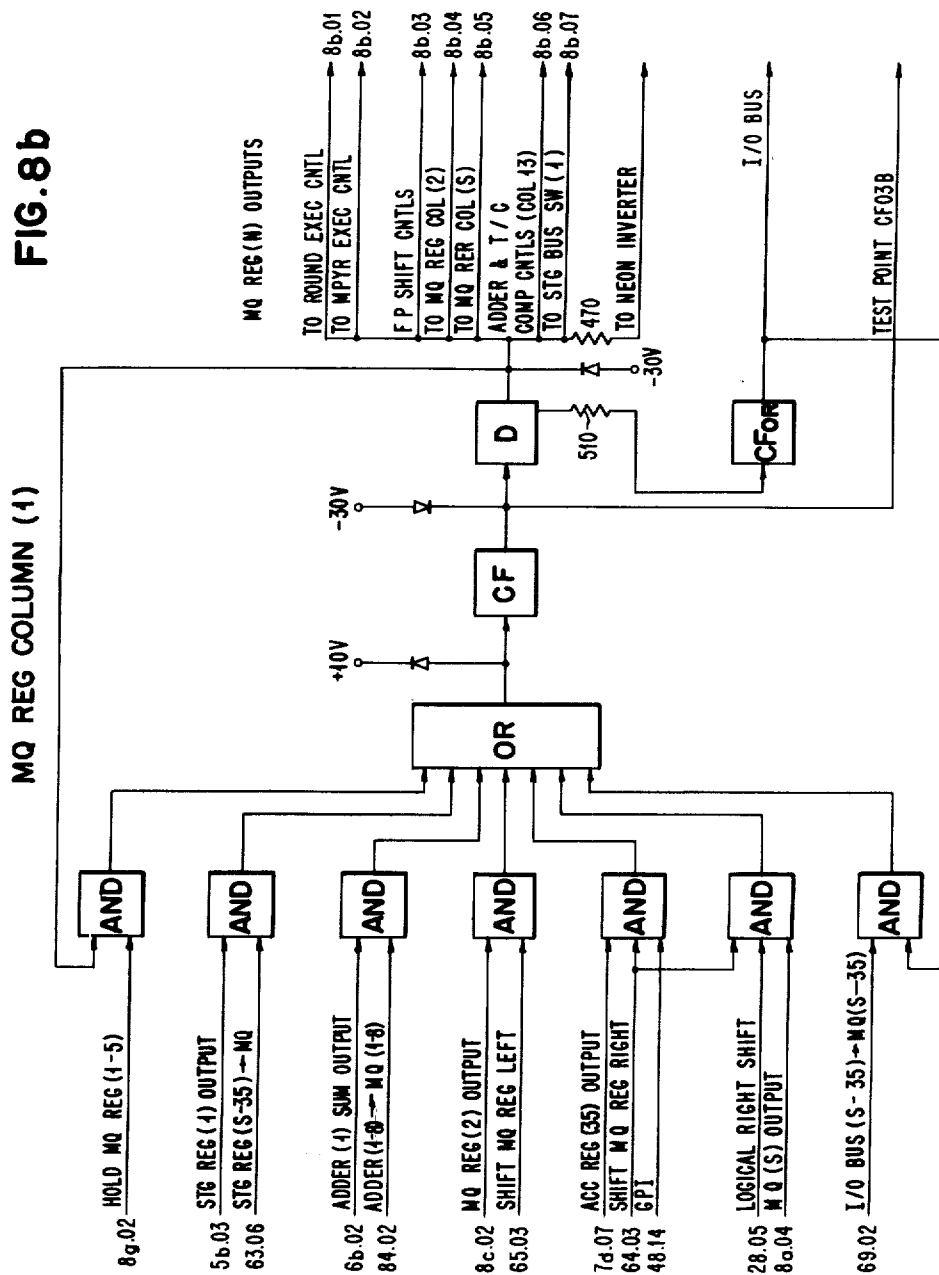
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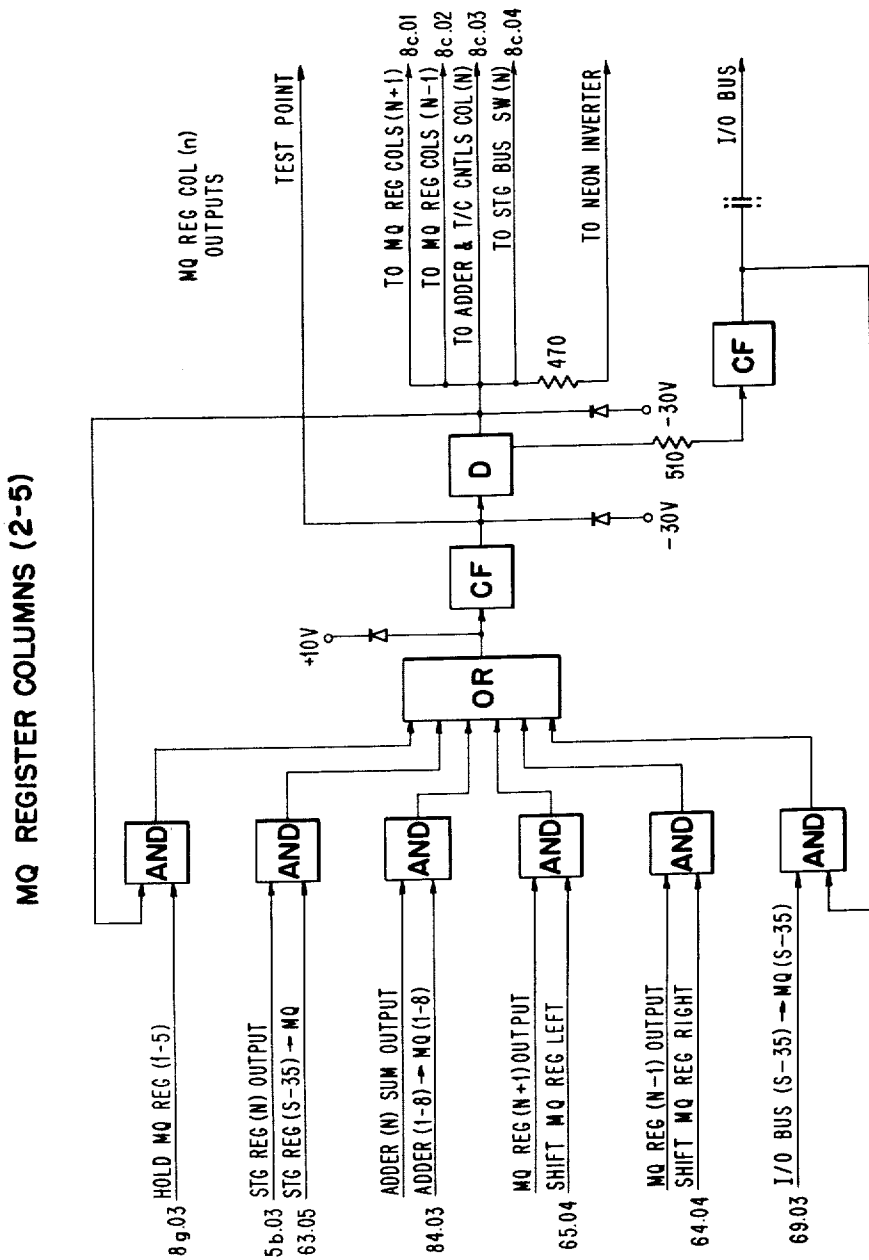
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FIG. 8b



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**FIG. 8c**

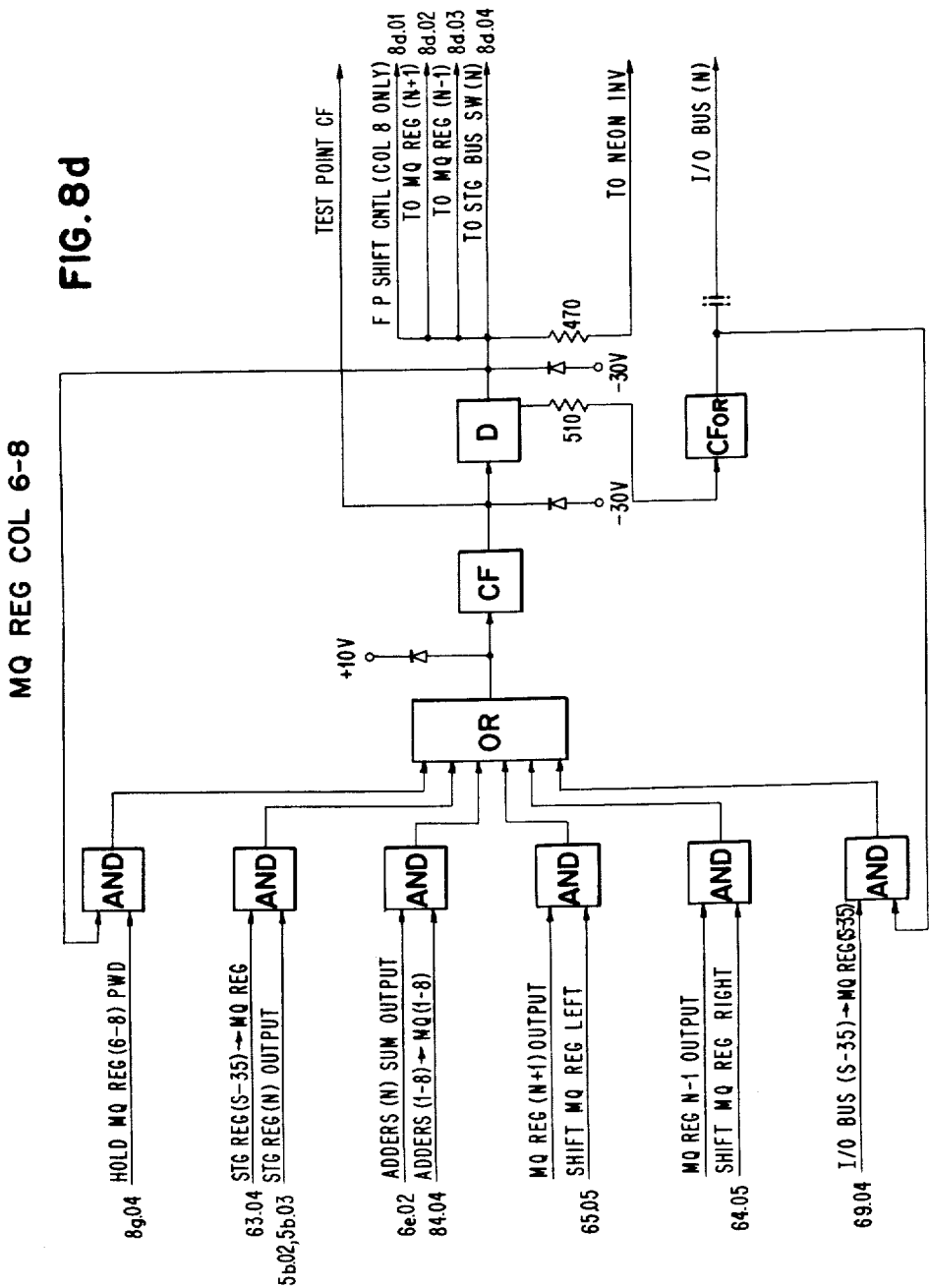
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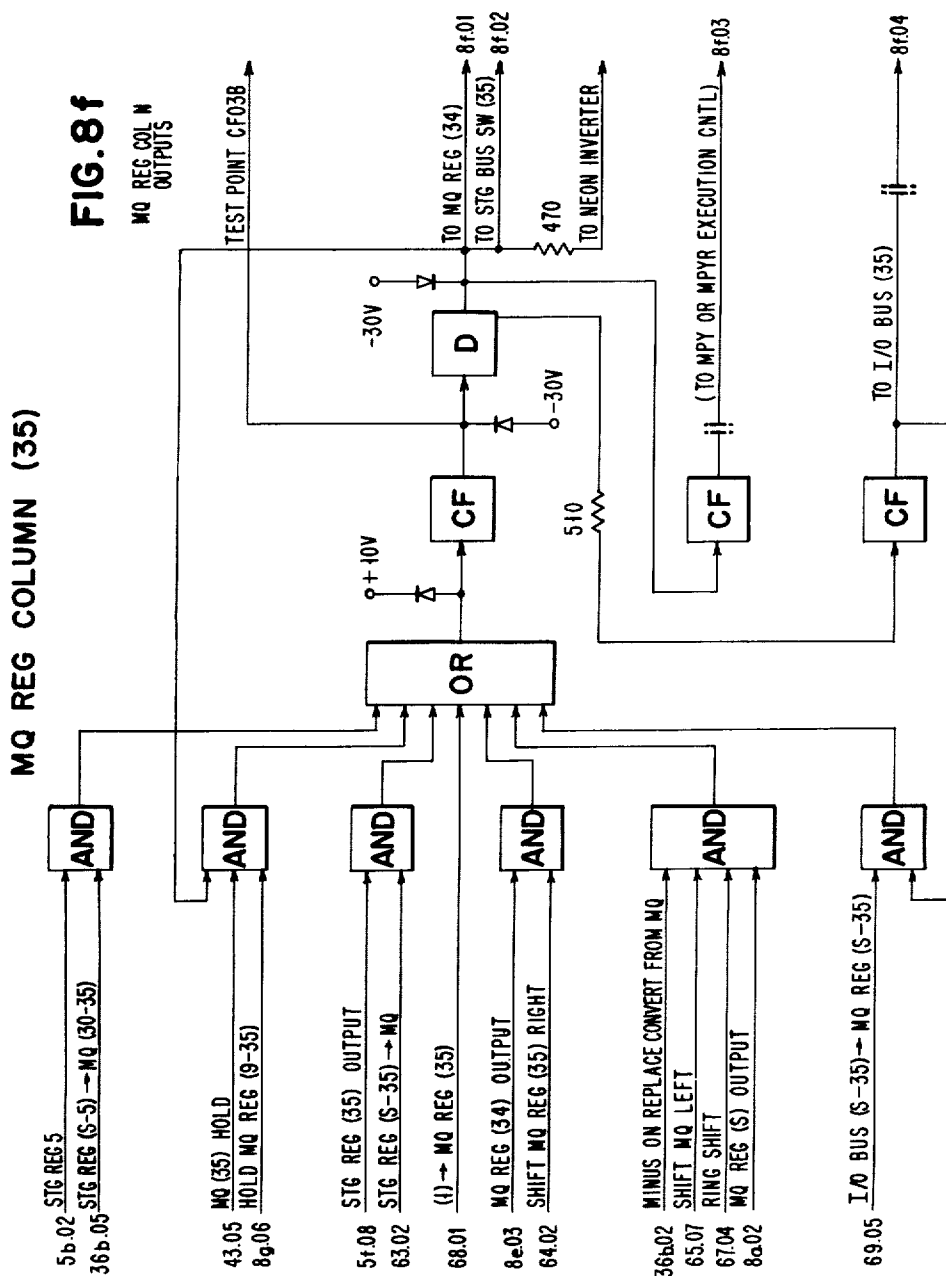
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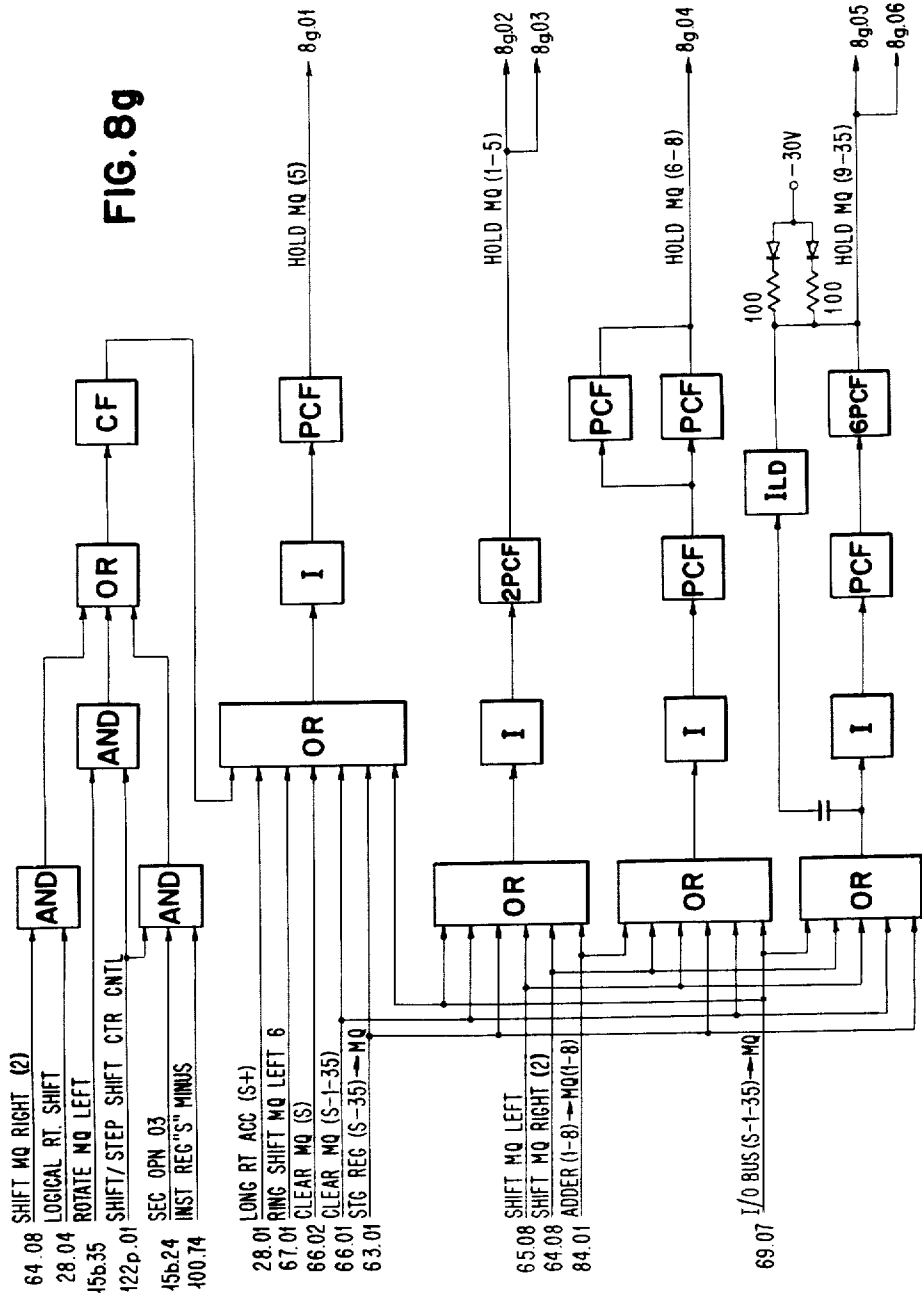
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MQ REGISTER COLS(S,1-35)HOLD CIRCUITS

FIG. 8g



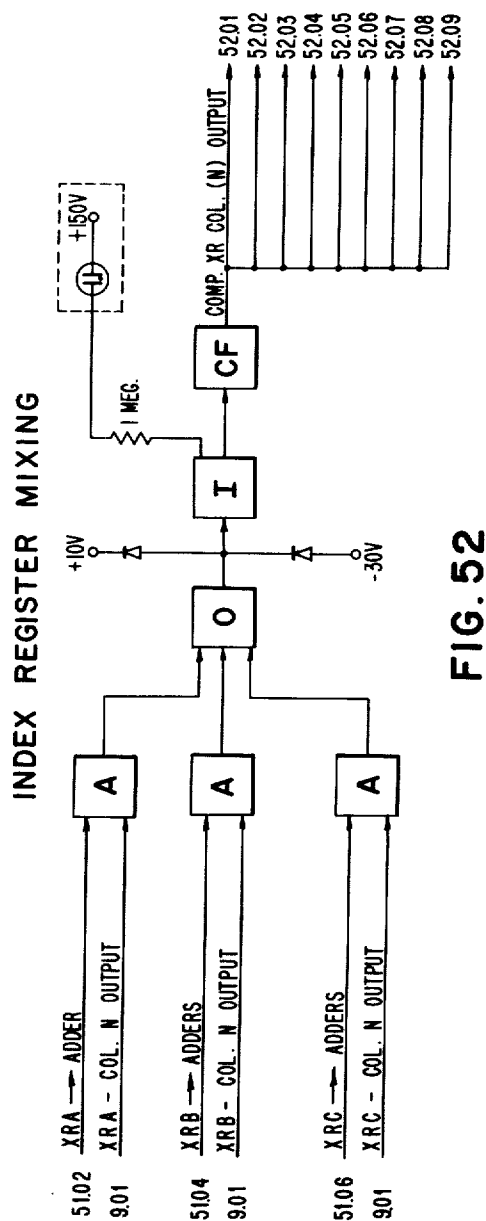
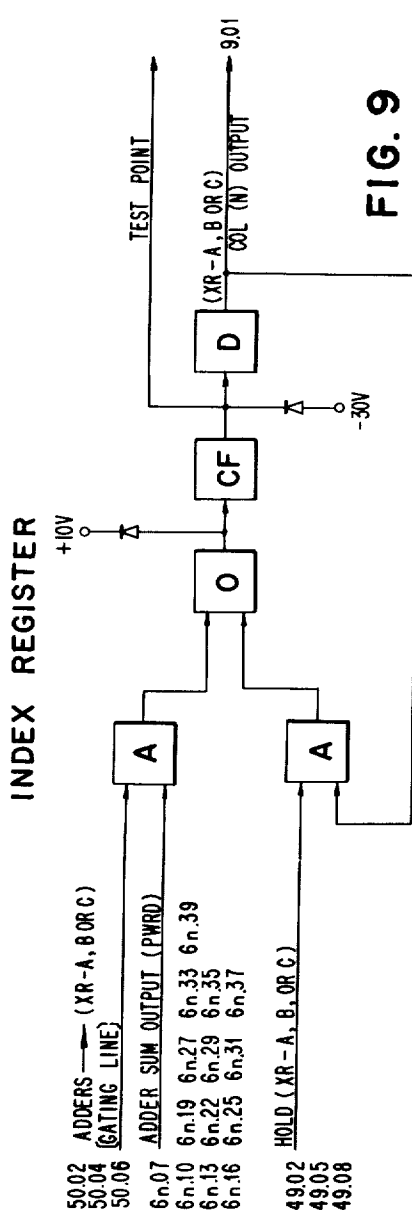
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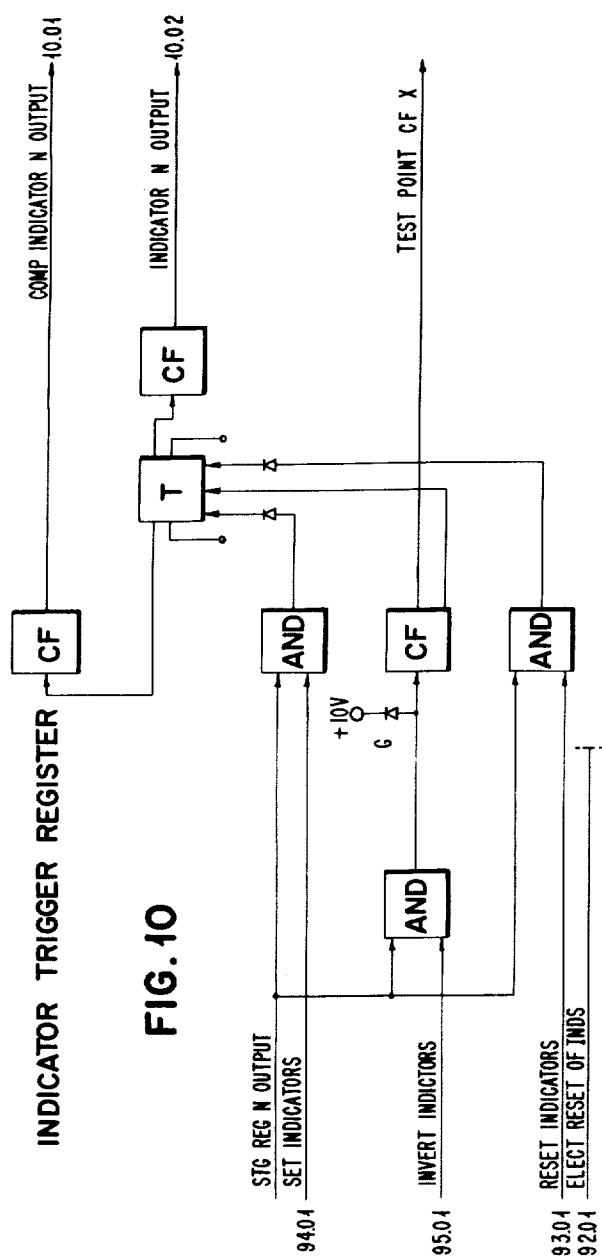
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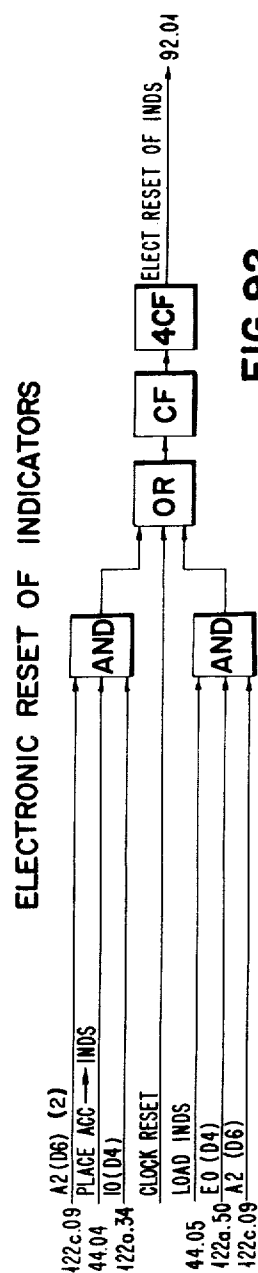
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**FIG. 10**



**FIG. 92**

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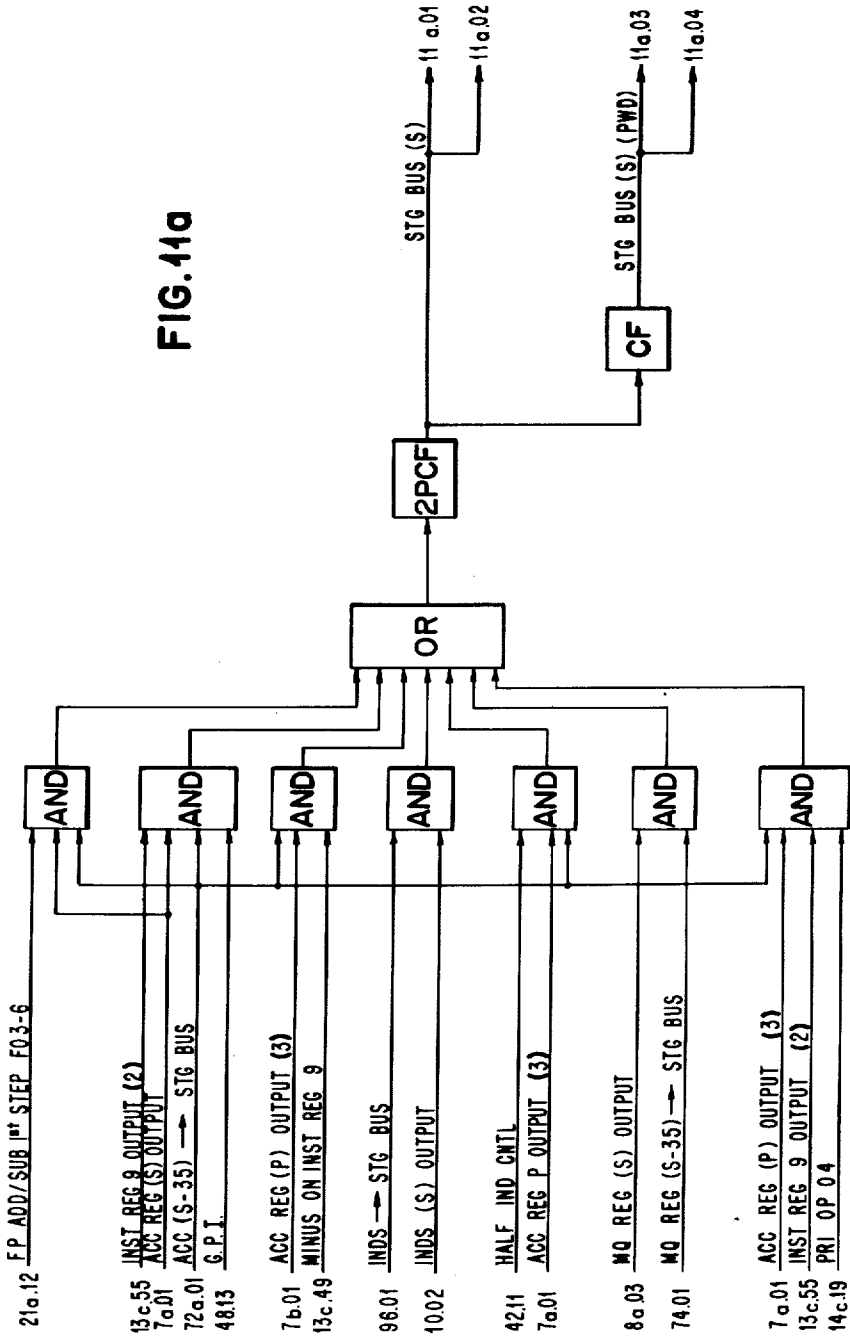
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STORAGE BUS SWITCHING COLUMN S

FIG. 41a



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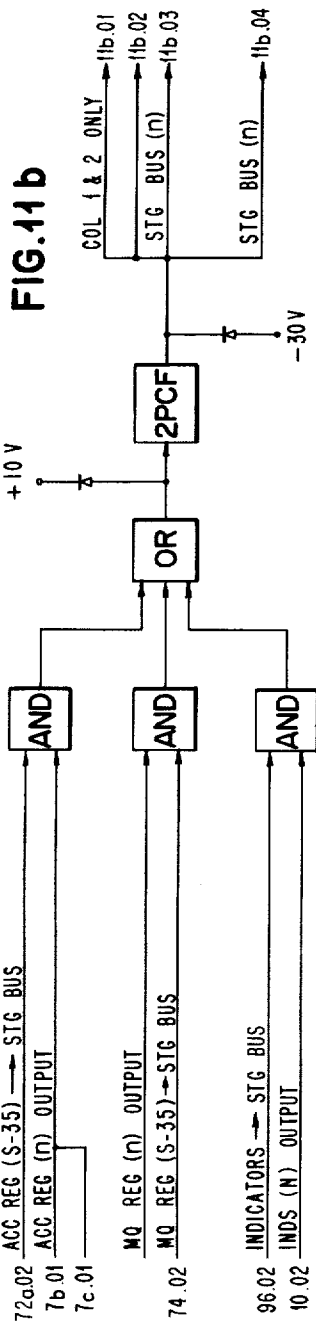
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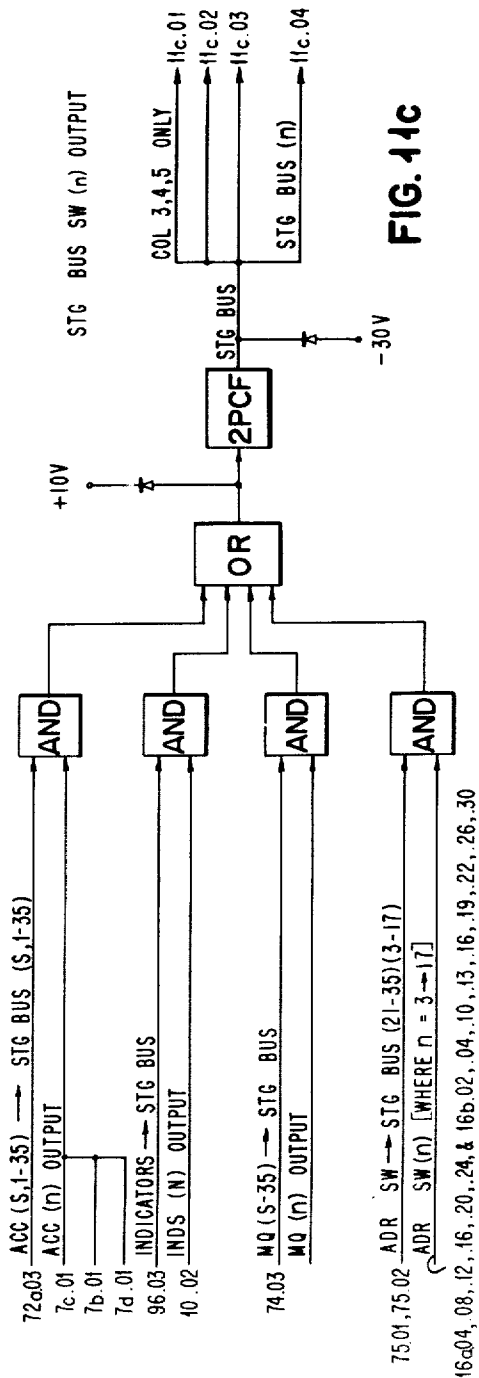
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STORAGE BUS SWITCHING COLUMNS (1,2,18,19,20)



STORAGE BUS SWITCHING COLUMNS (21-35), (3-17)



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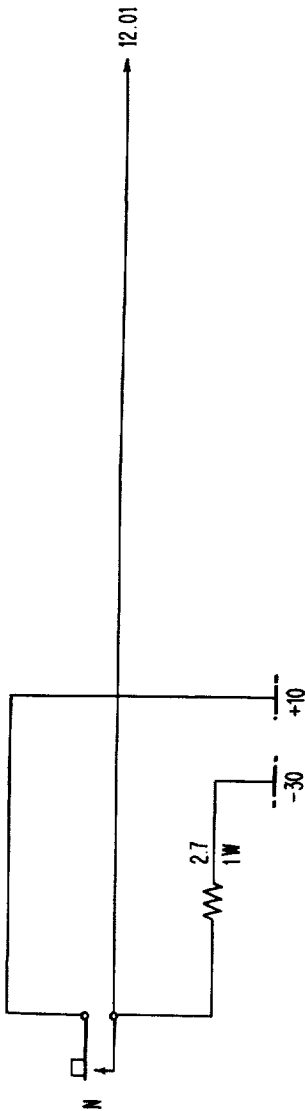
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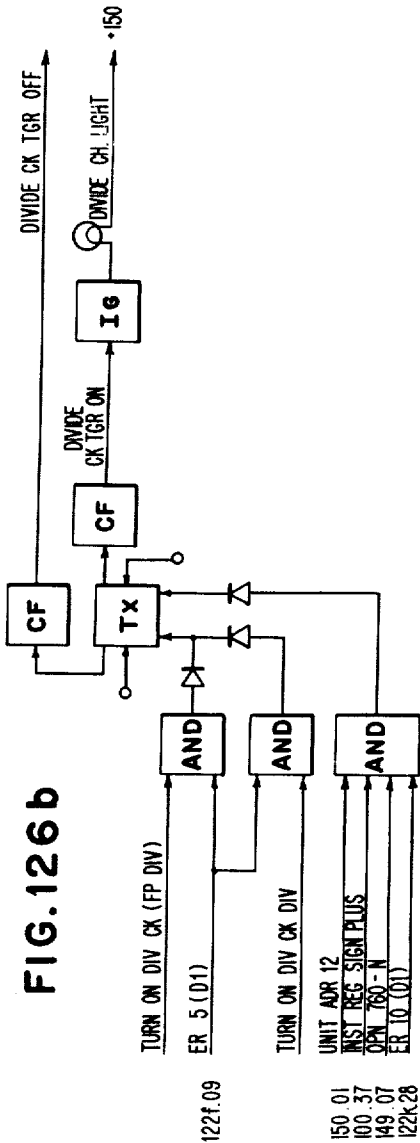
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FIG.12 OPERATORS PANEL ENTRY KEYS (S THRU 35)



DIVIDE CHECK TRIGGER



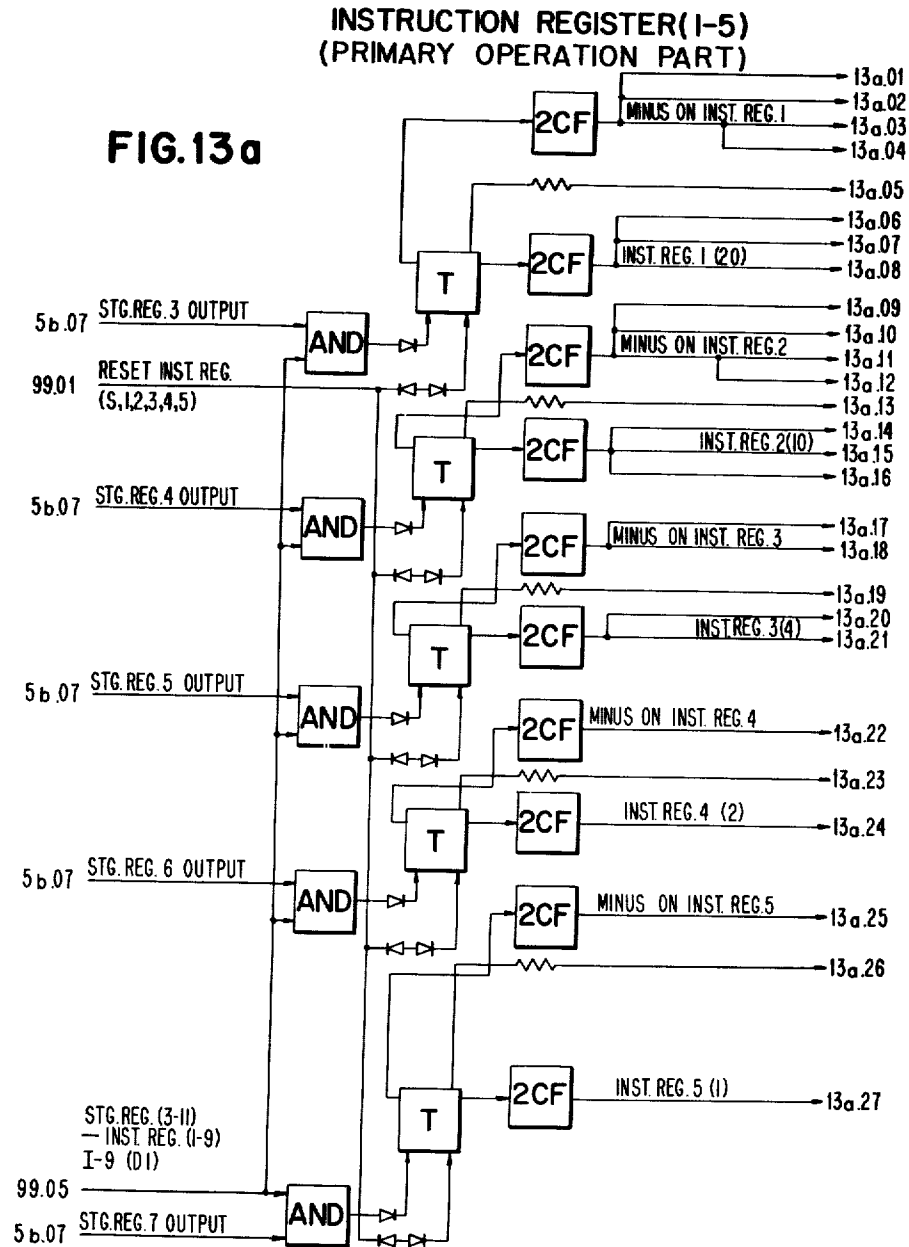
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INSTRUCTION REGISTER (6-7)

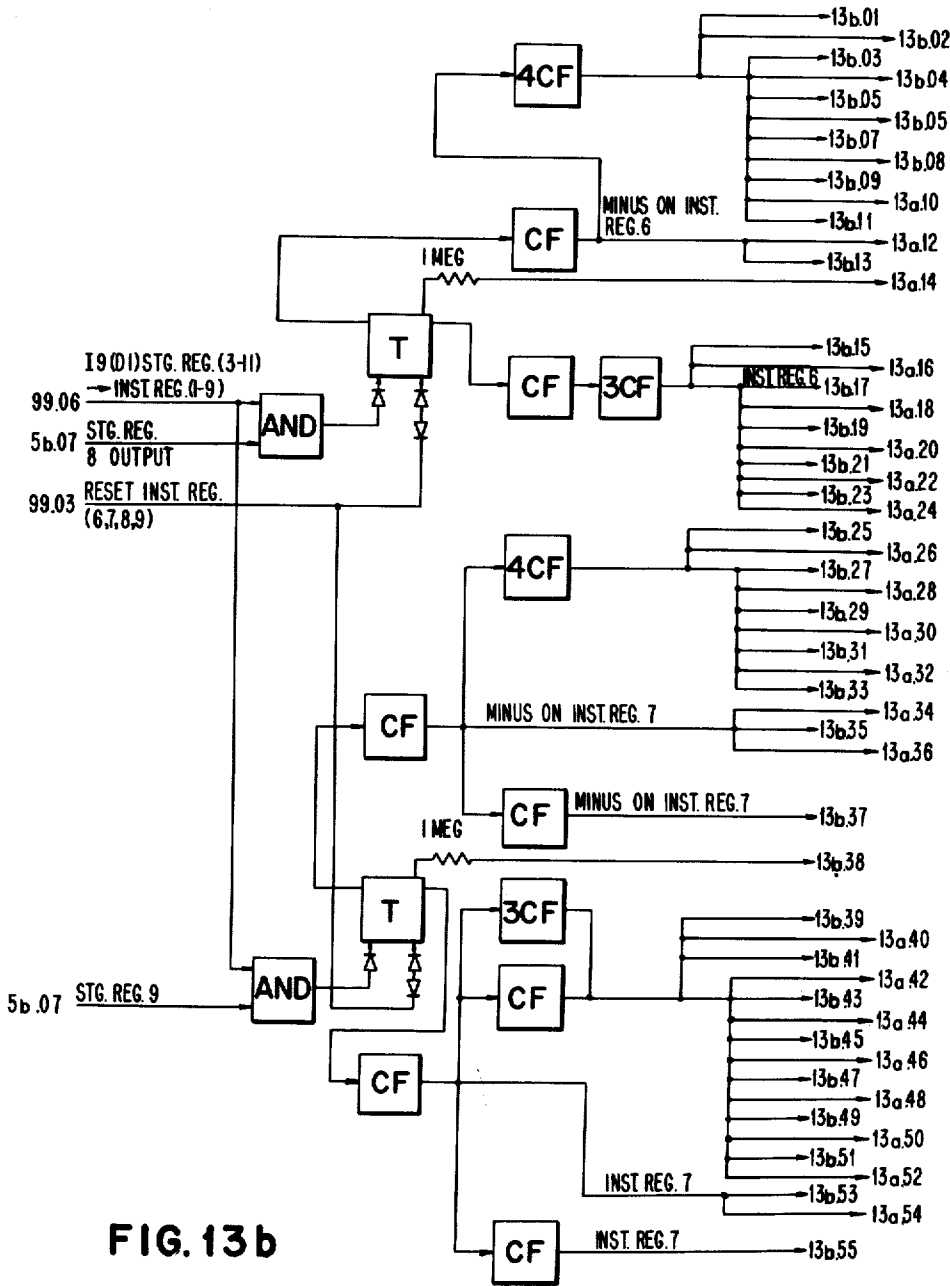


FIG. 13b

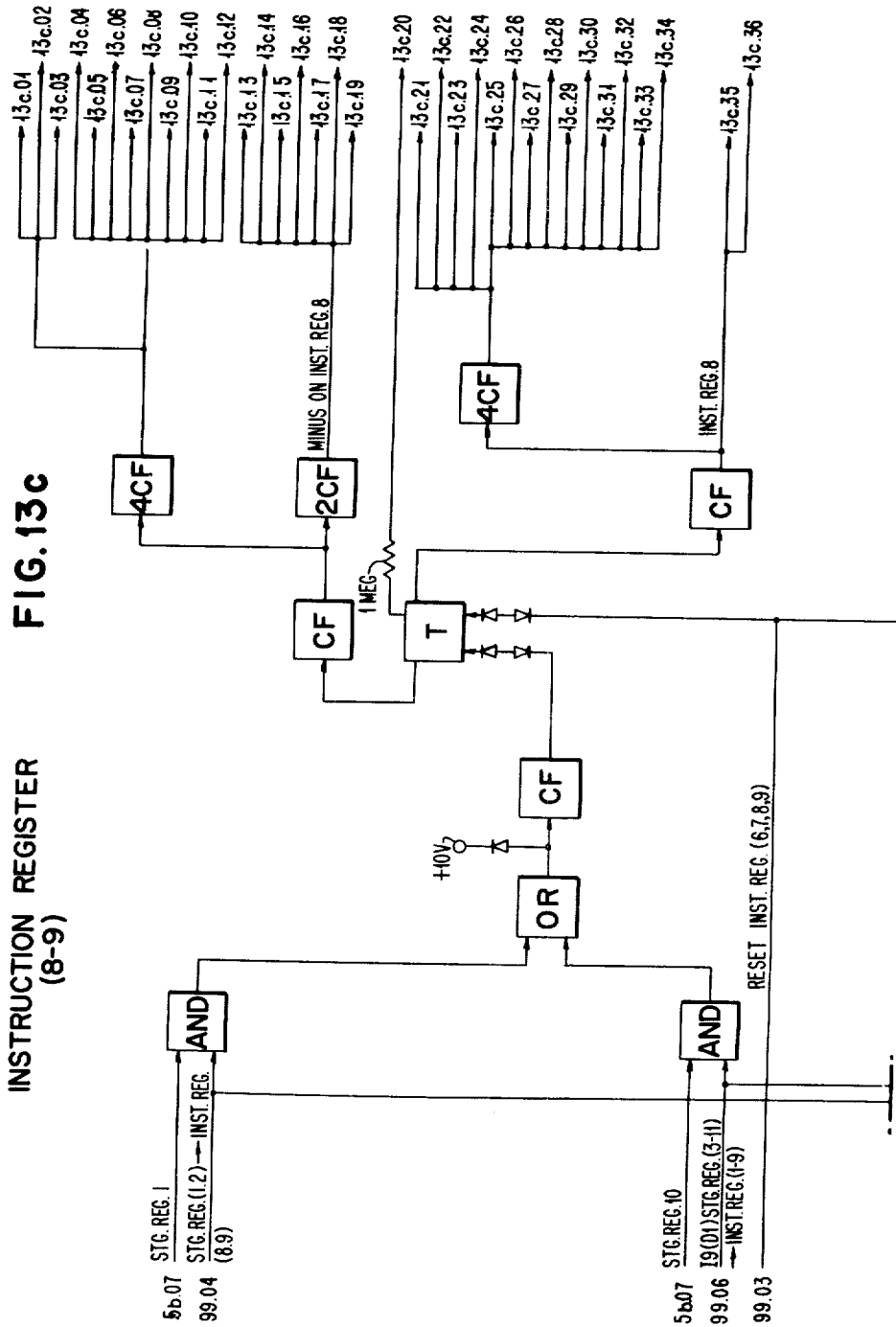
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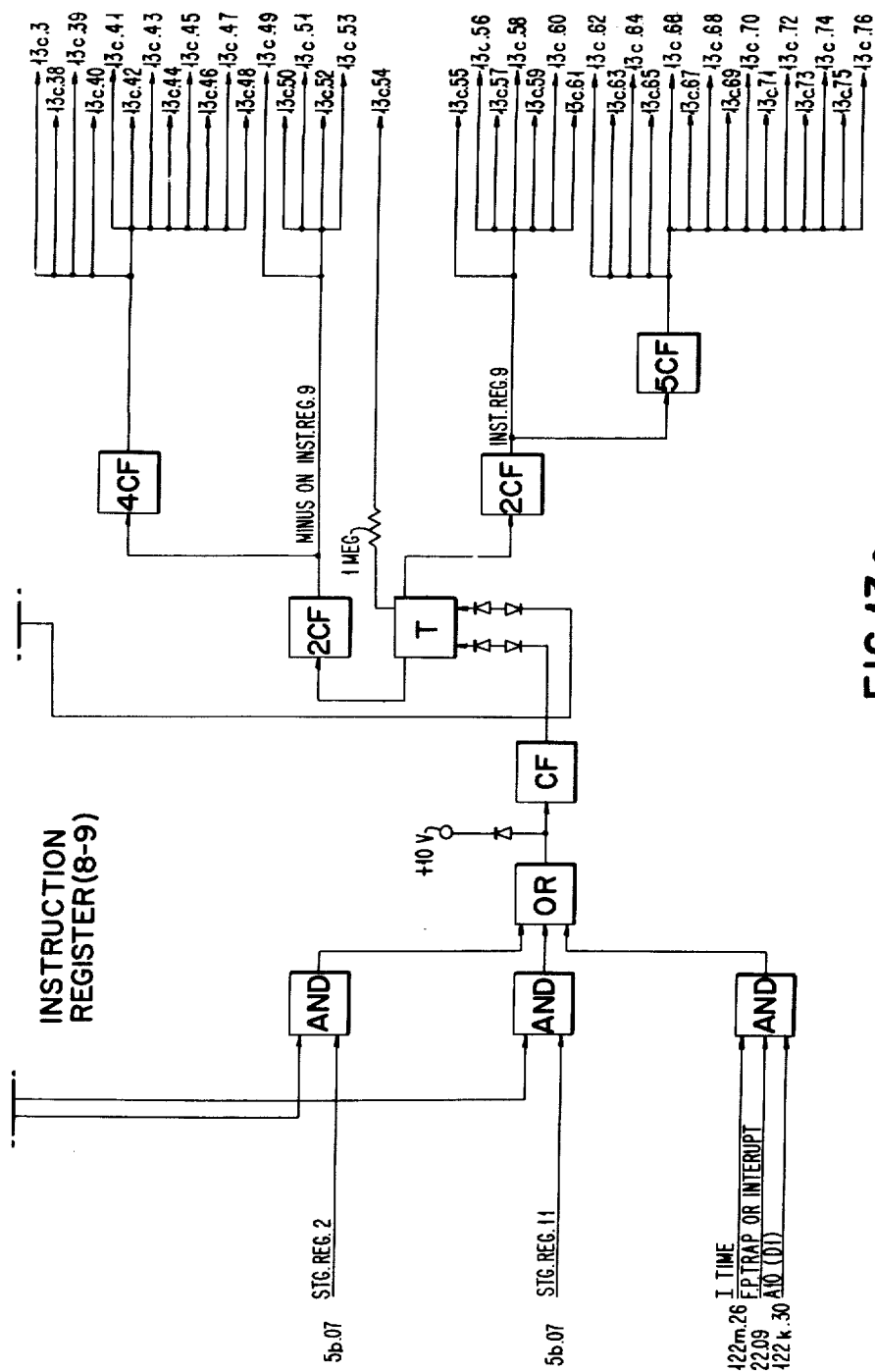
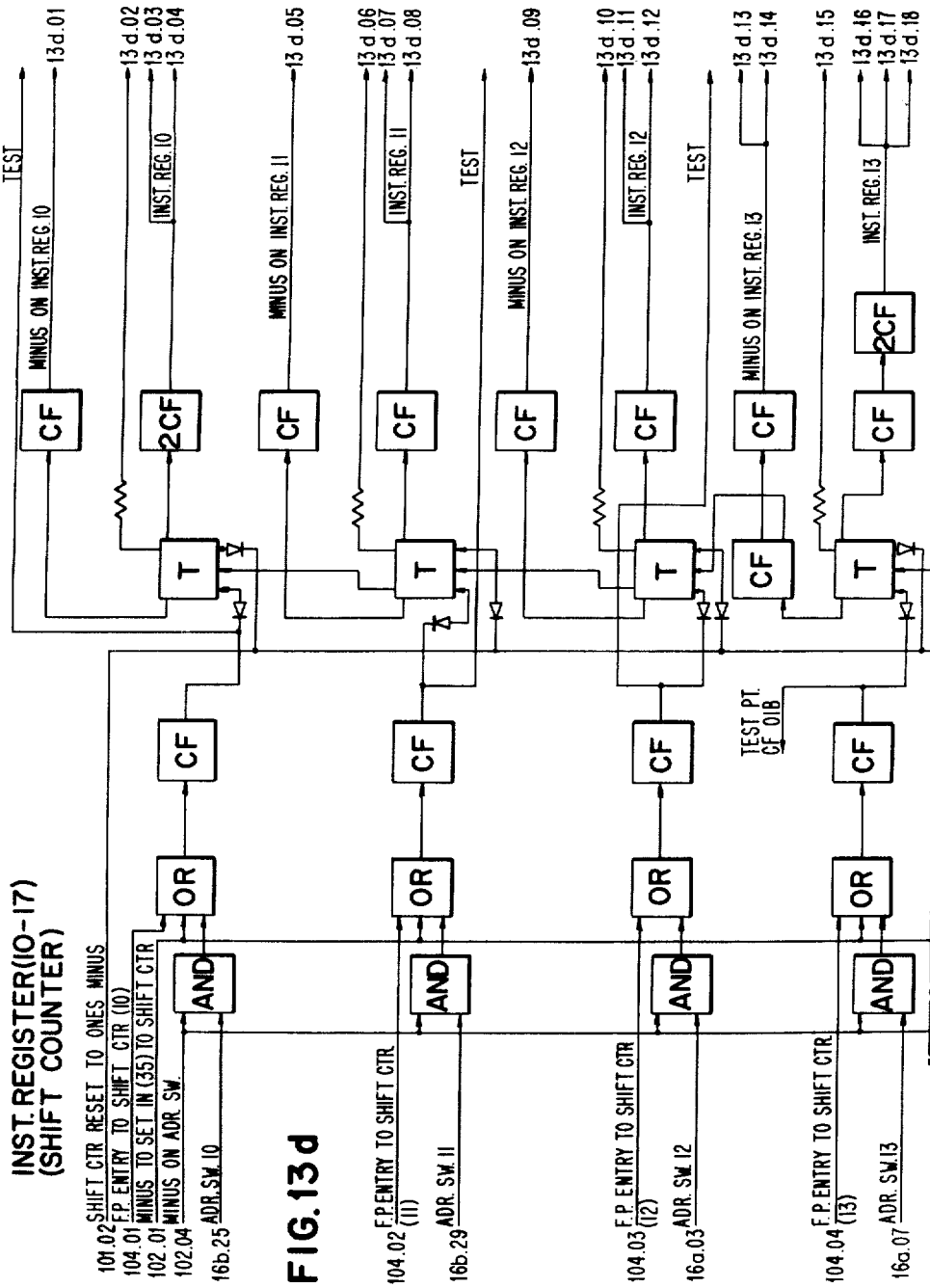


FIG. 13c



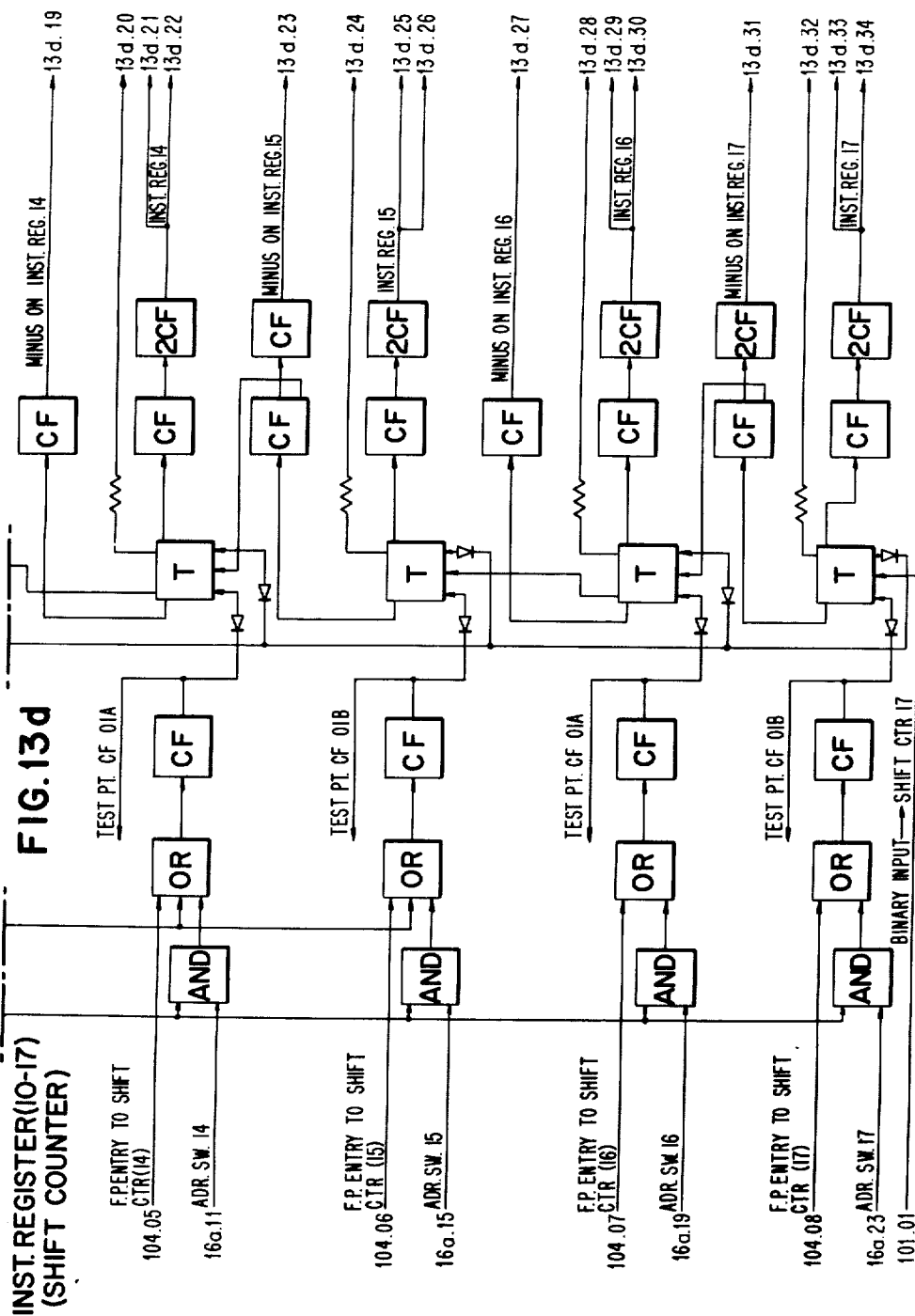
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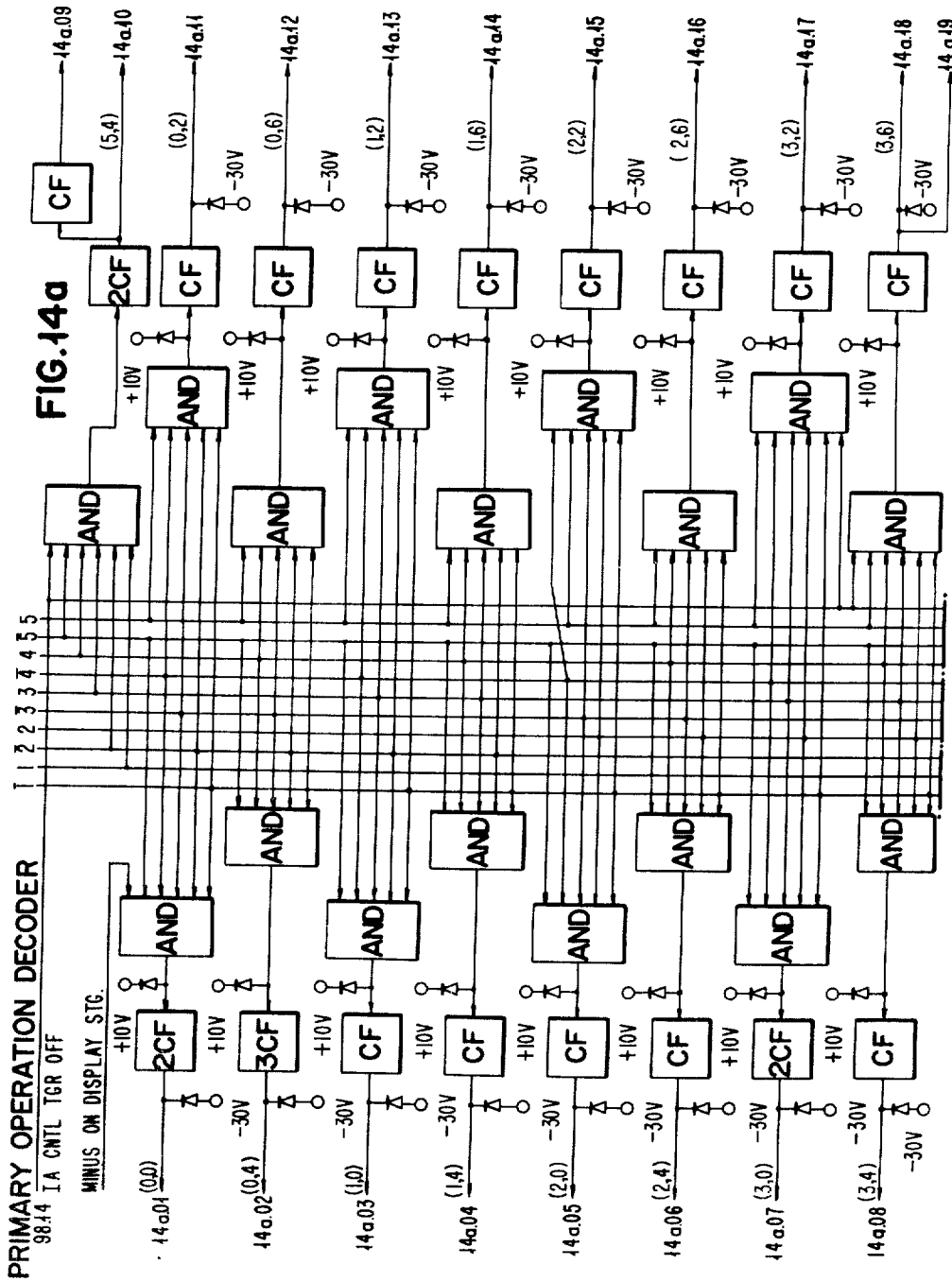
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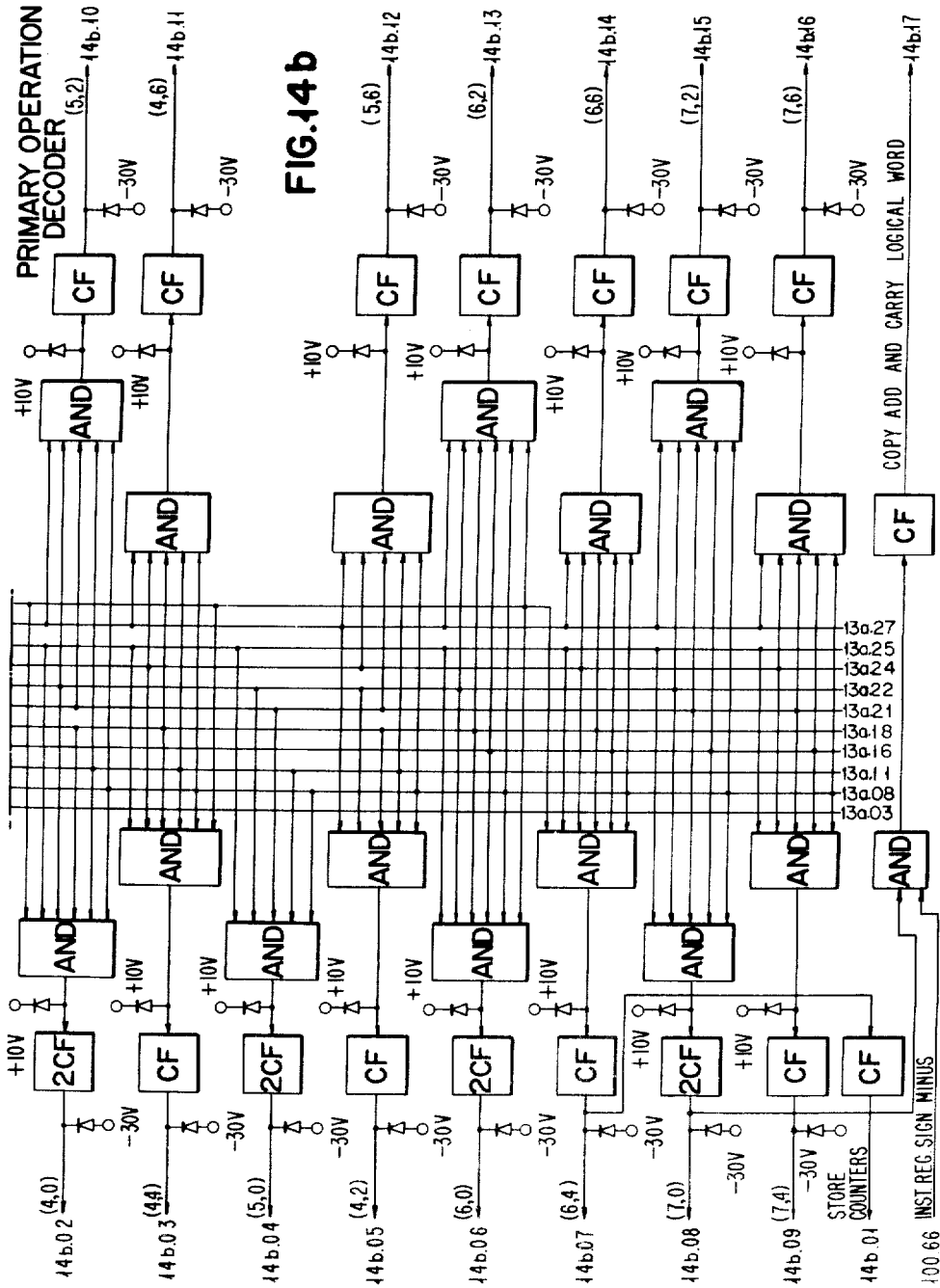
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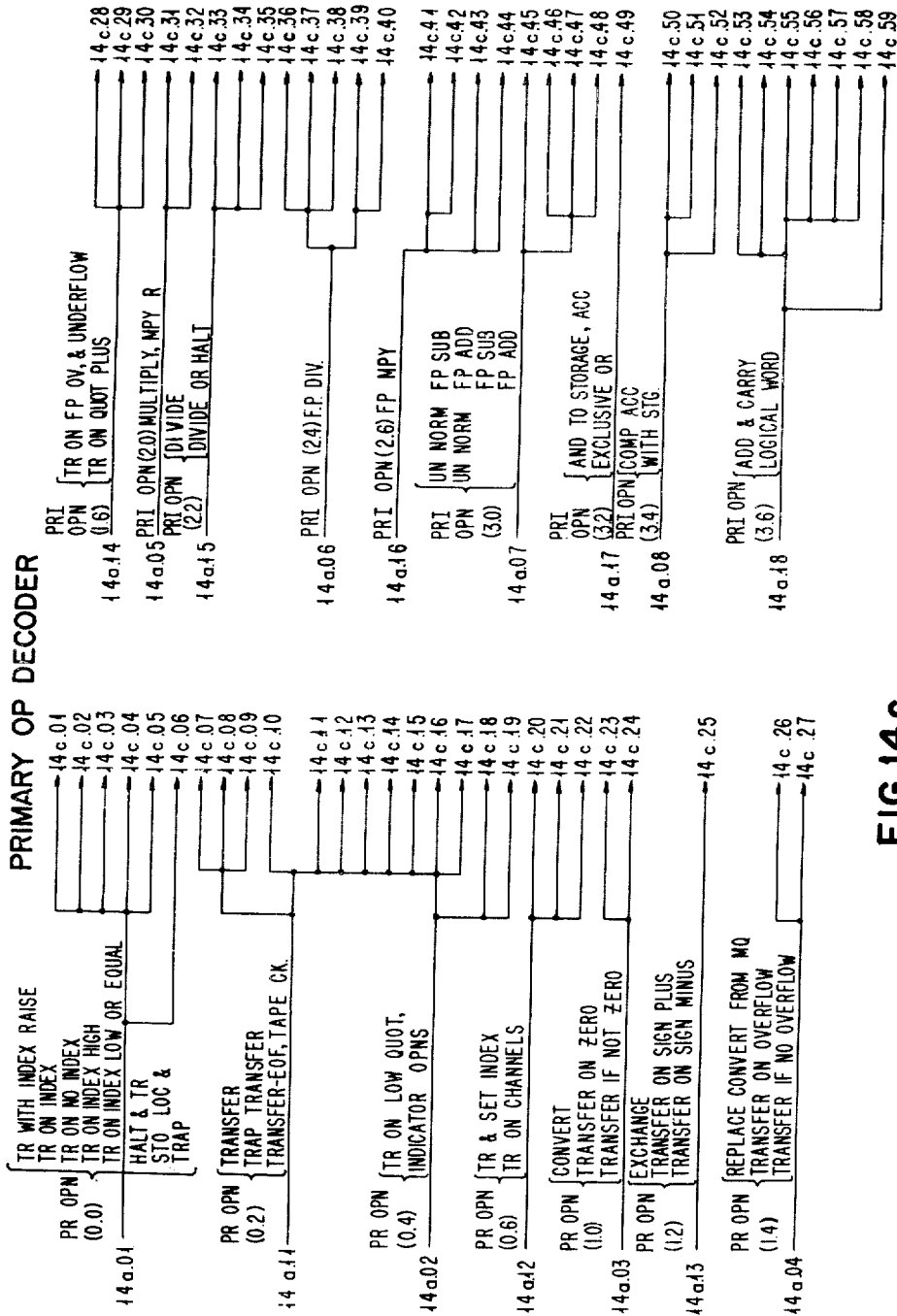


FIG.14c

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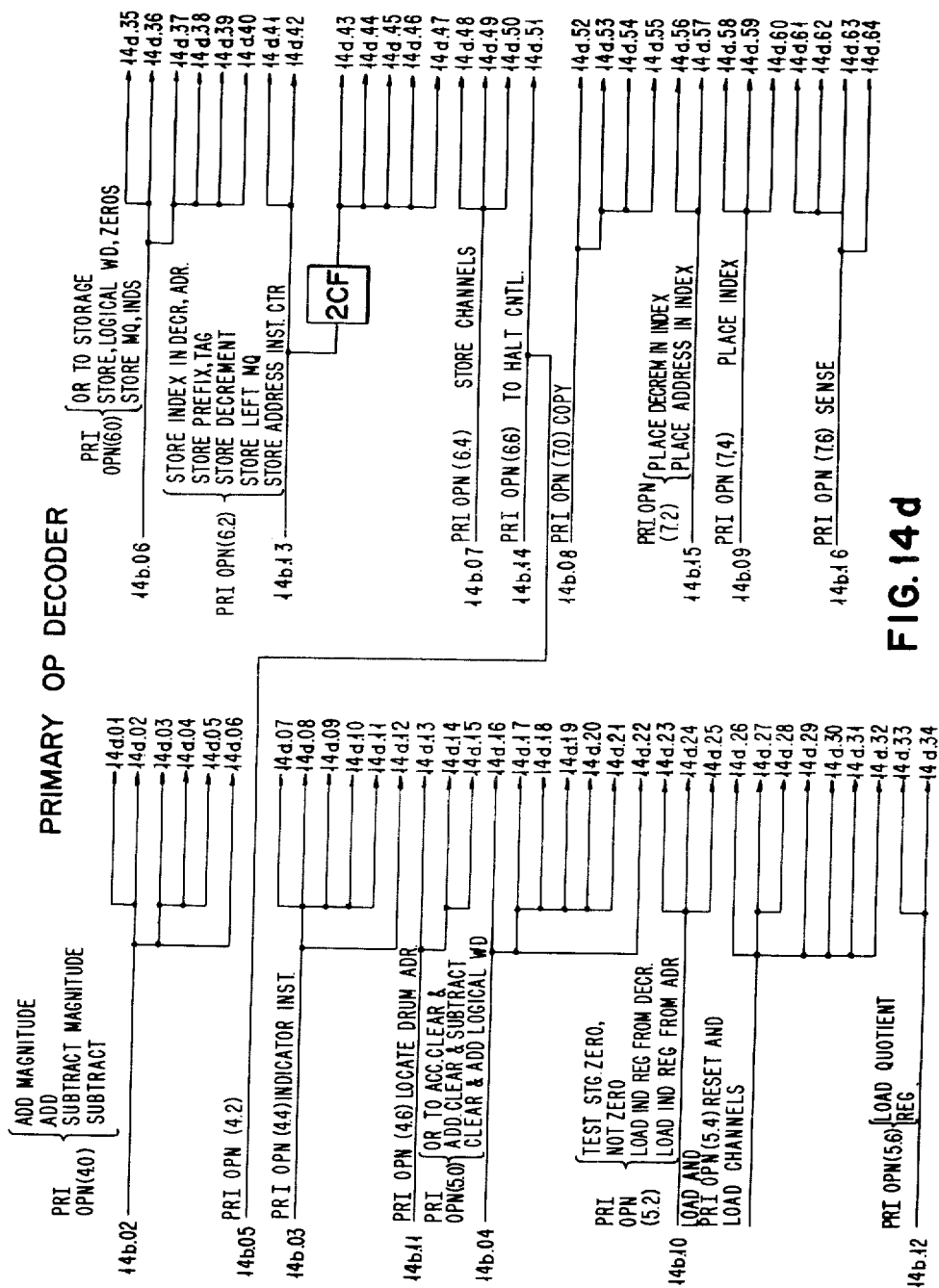


FIG. 14d

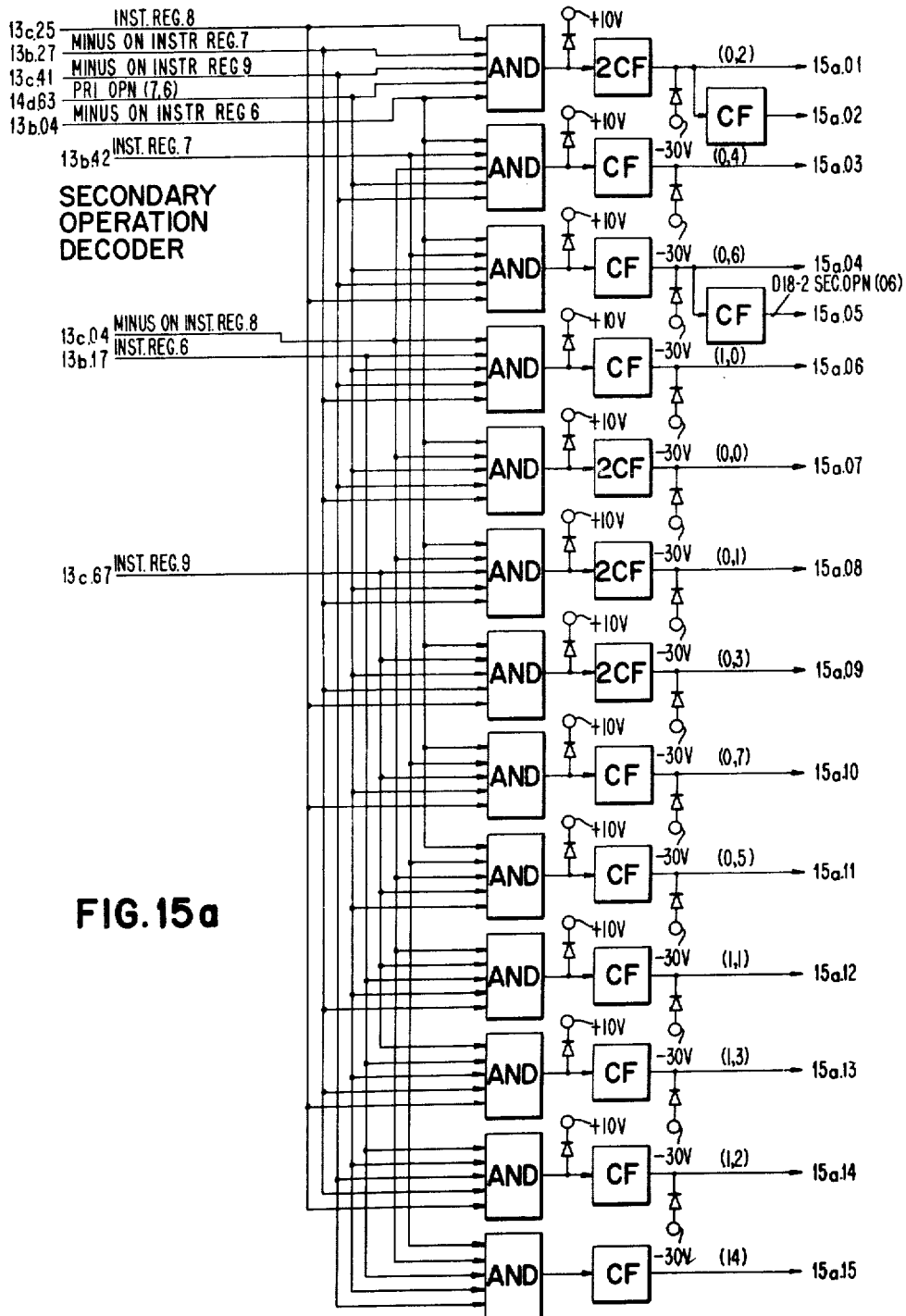
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## SECONDARY OPERATION DECODER

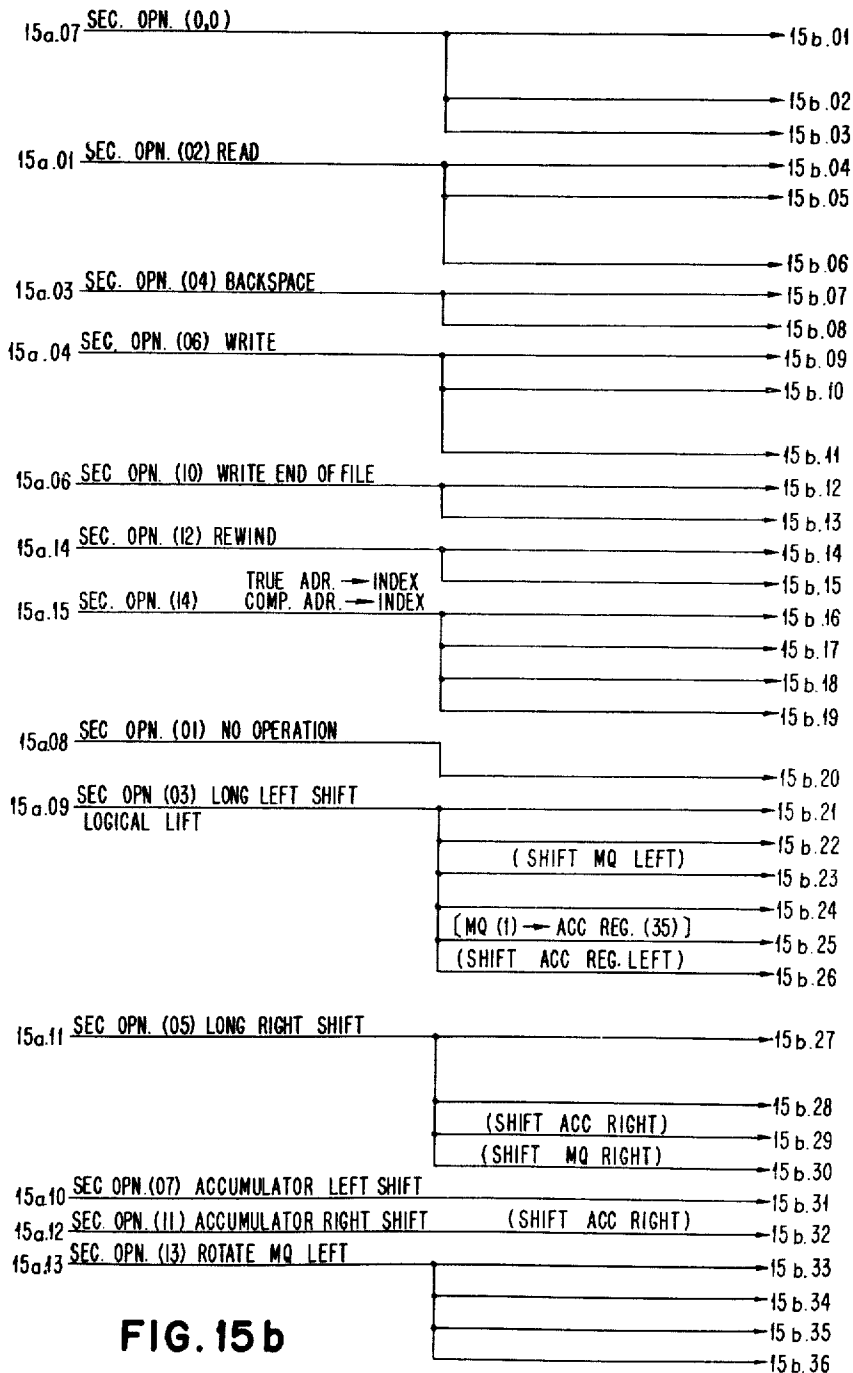
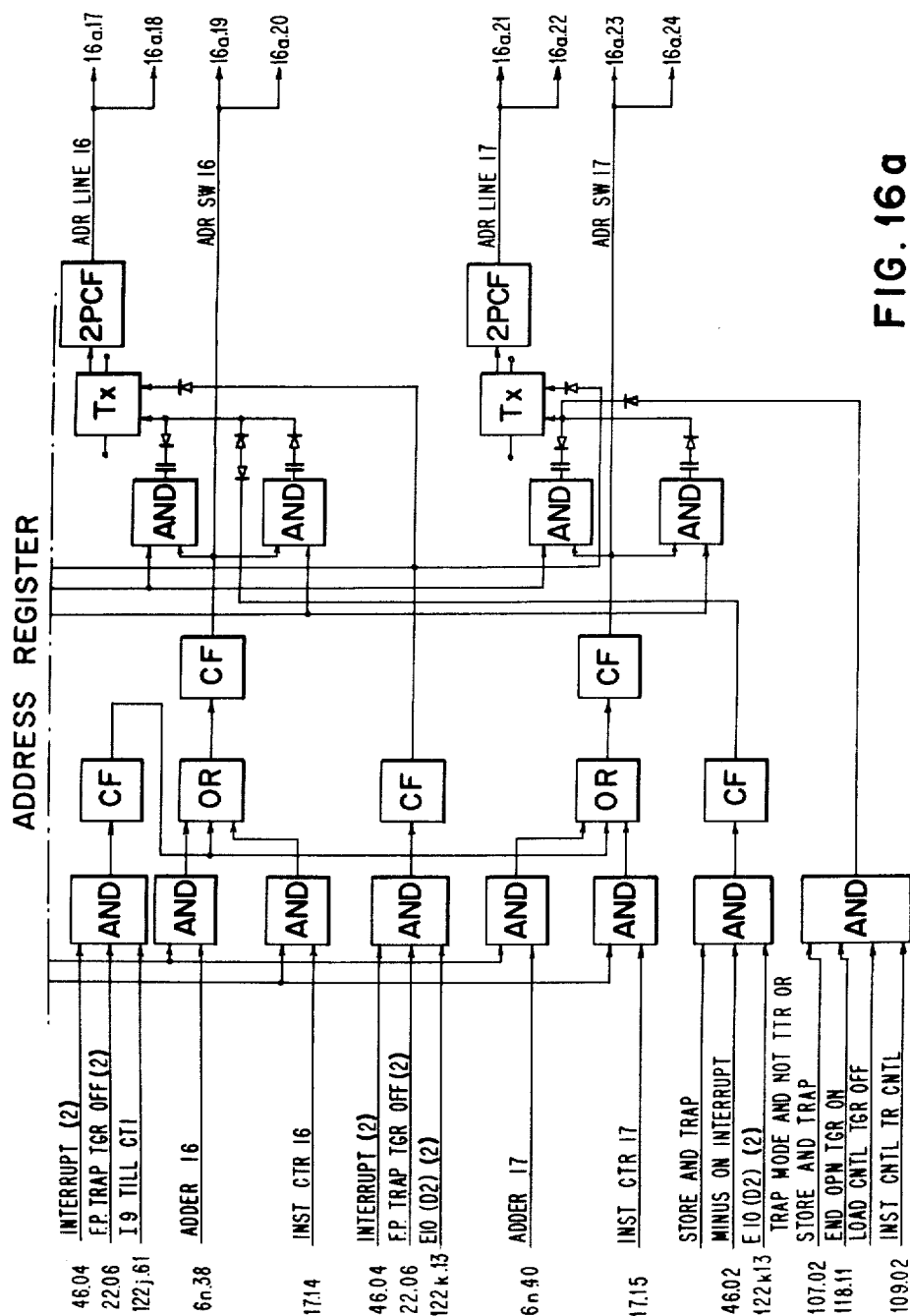


FIG. 15b

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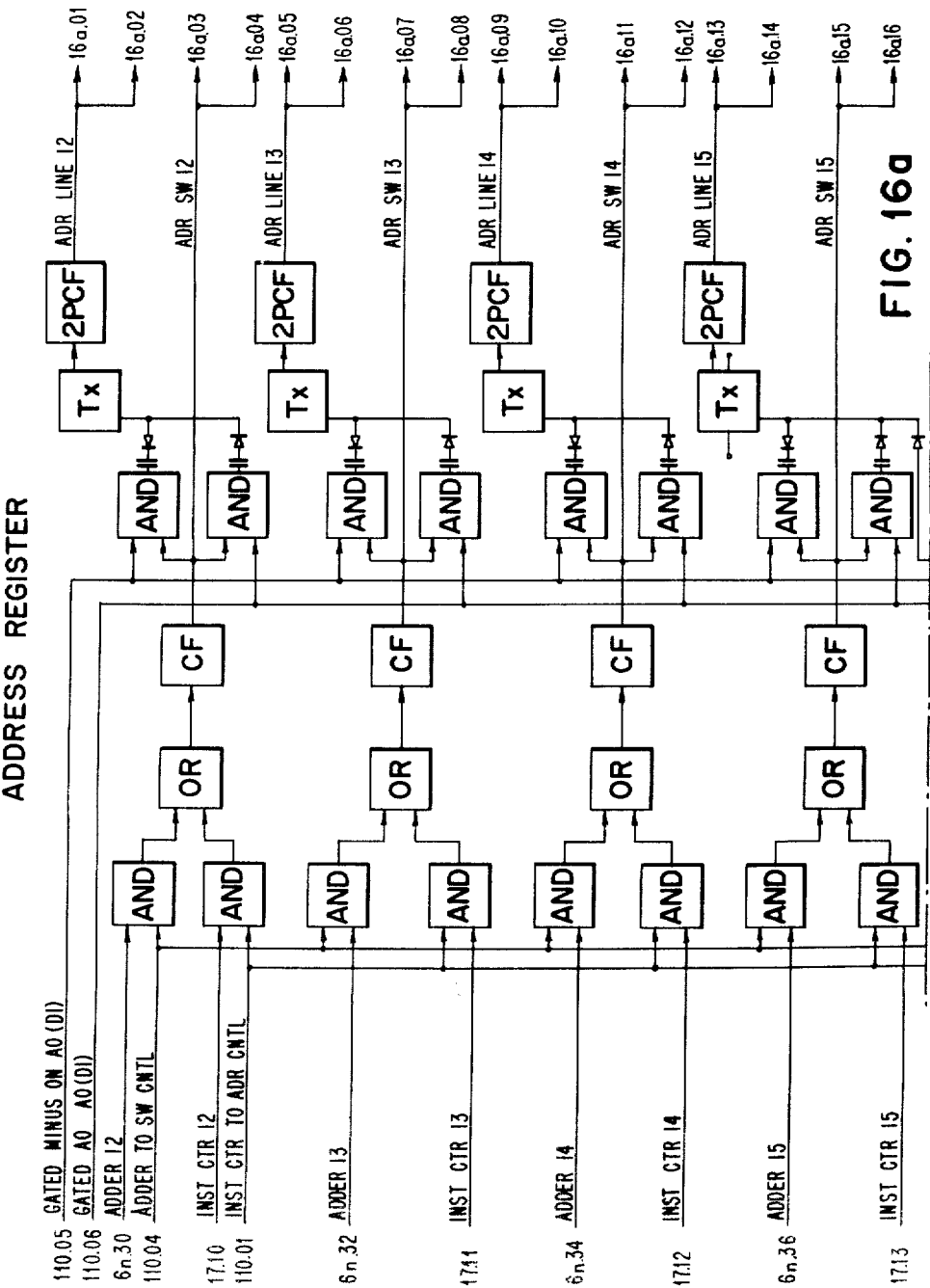
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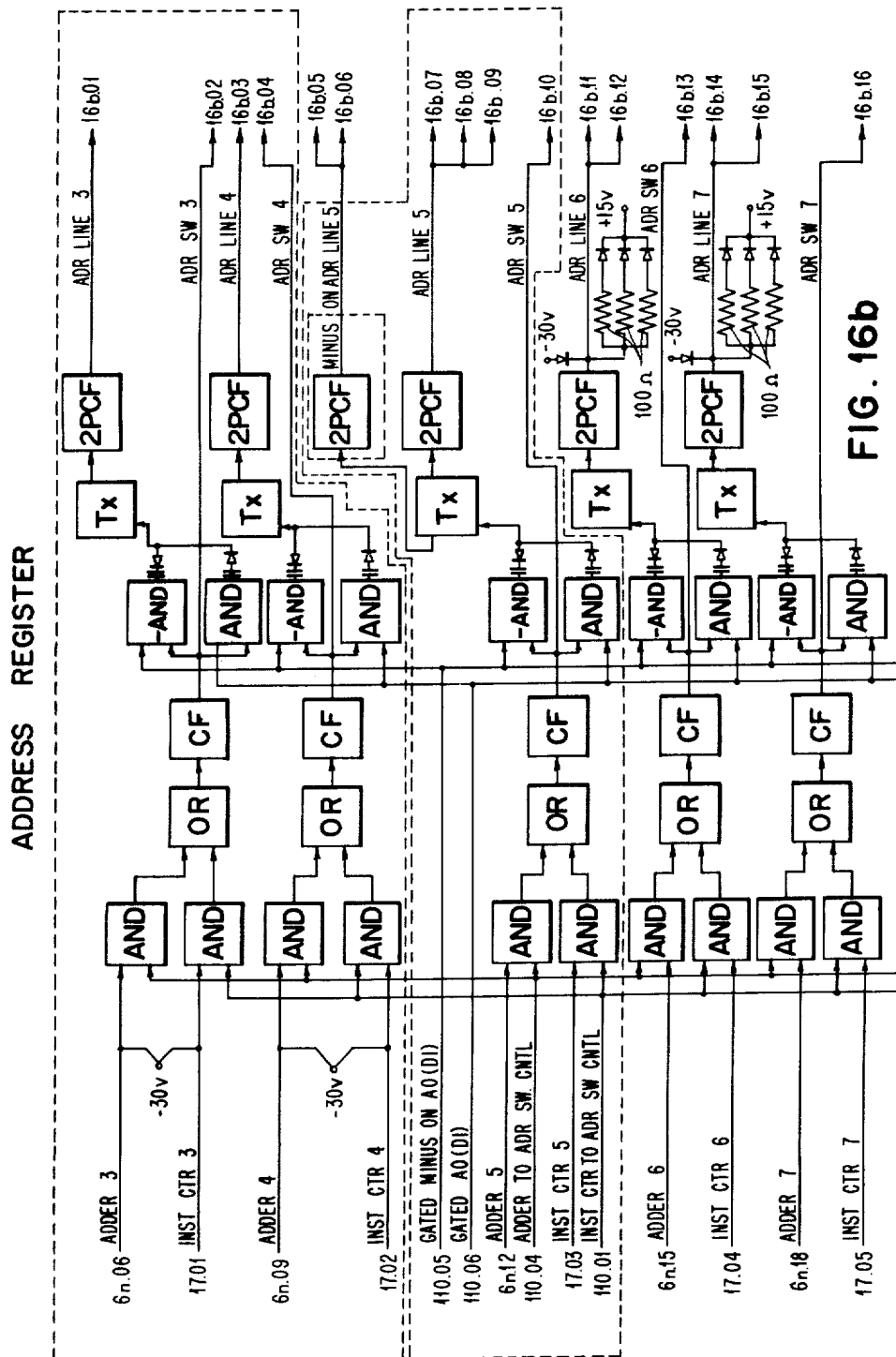
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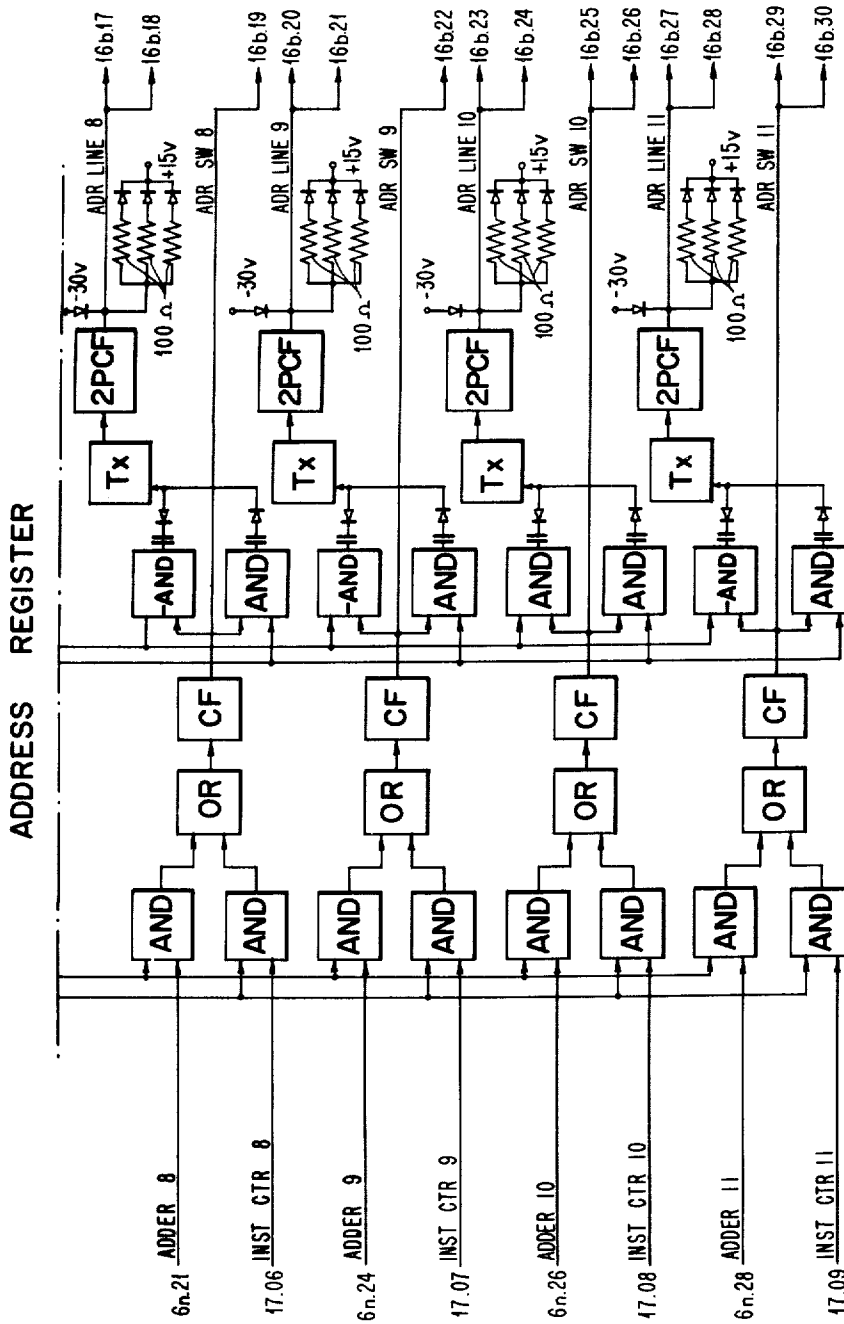


FIG. 16b

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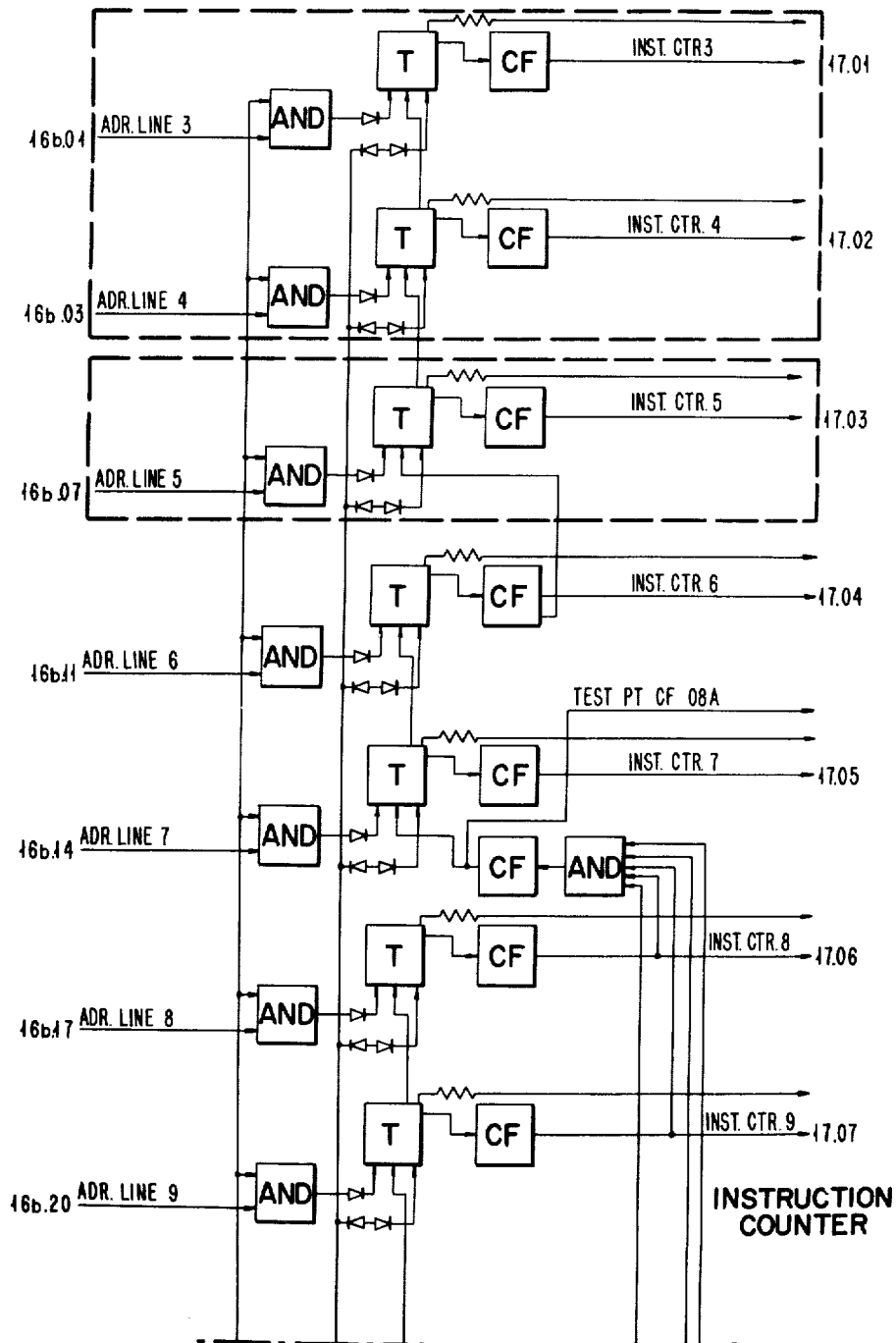


FIG. 17



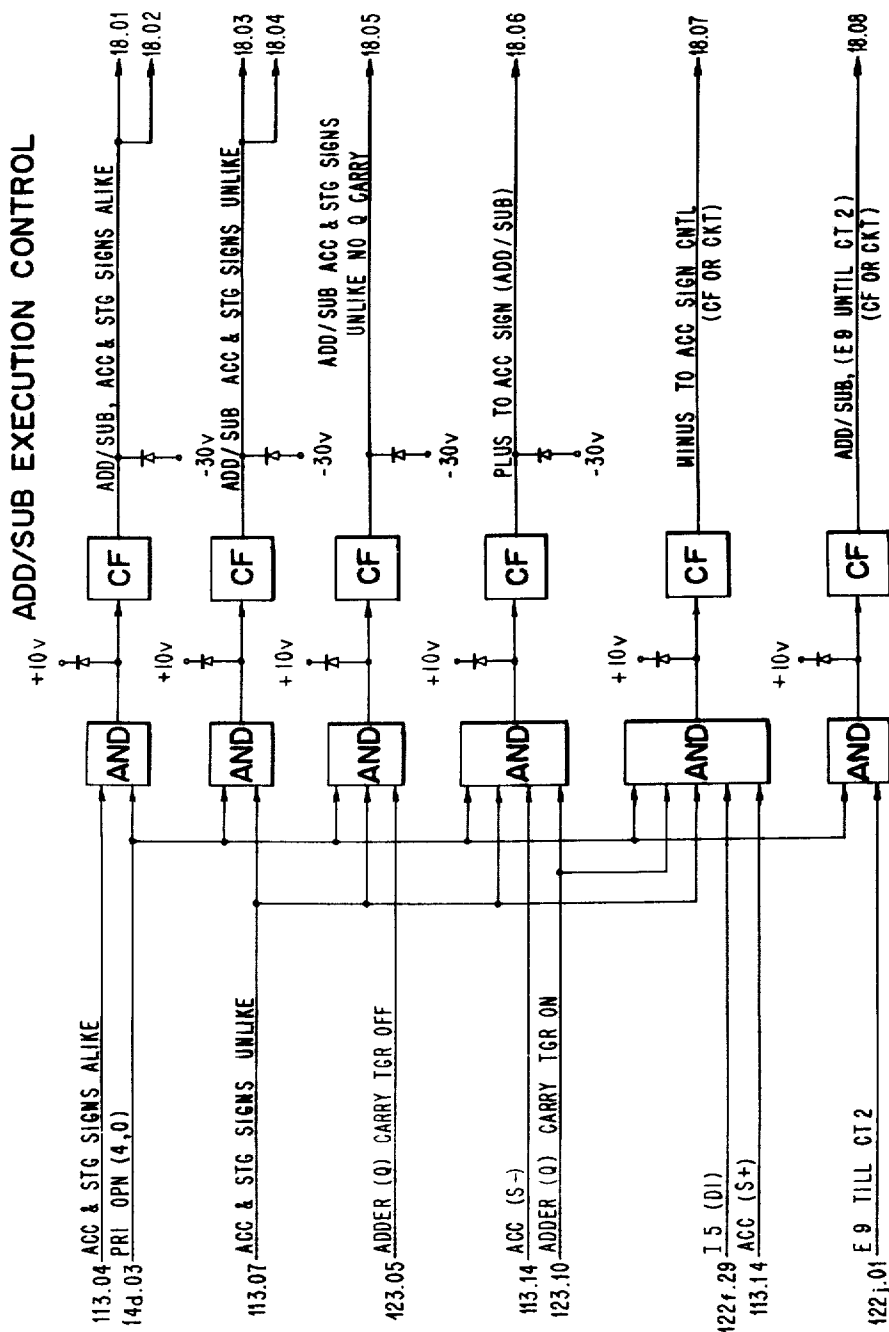
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**FIG.48**

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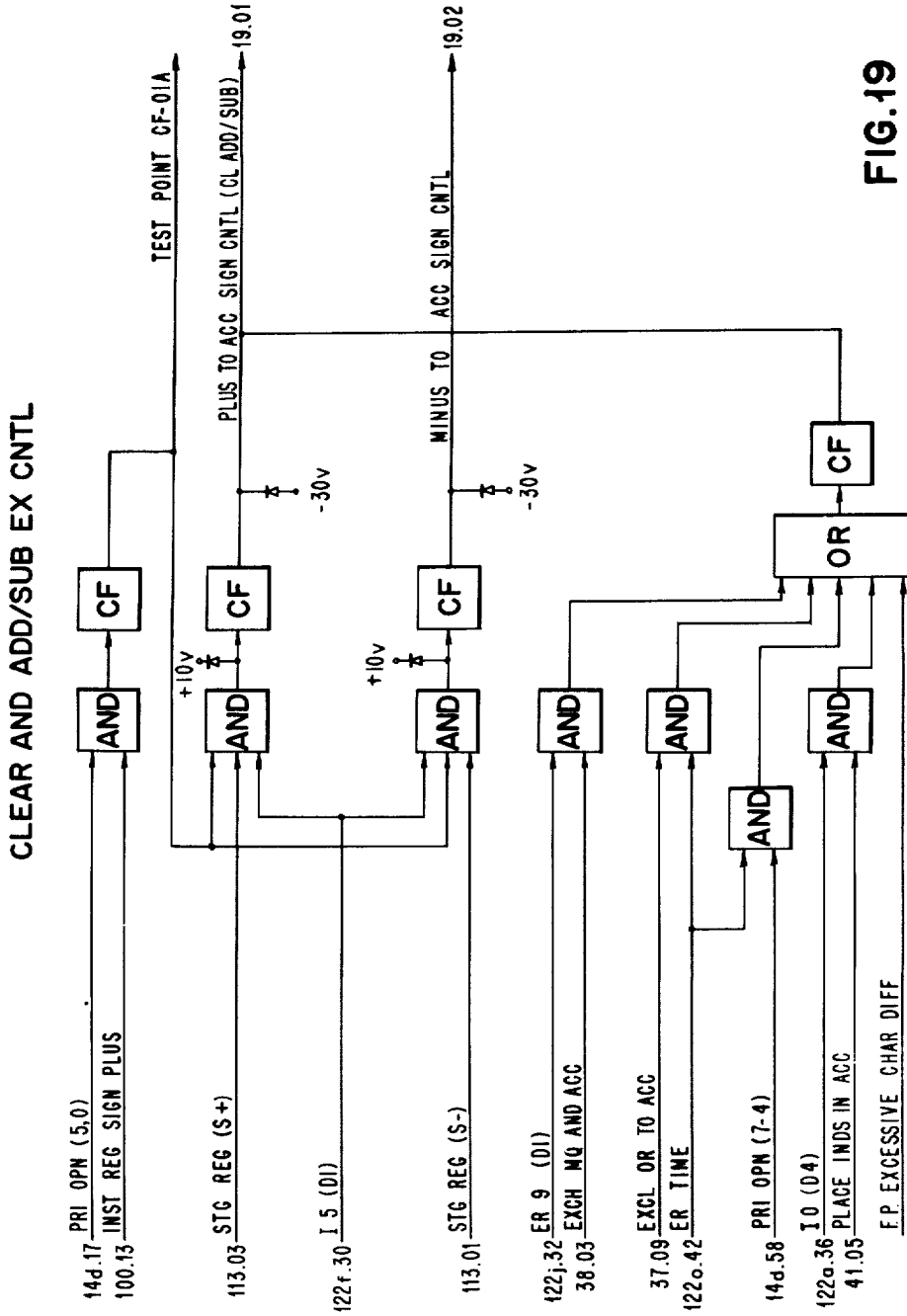


FIG.19

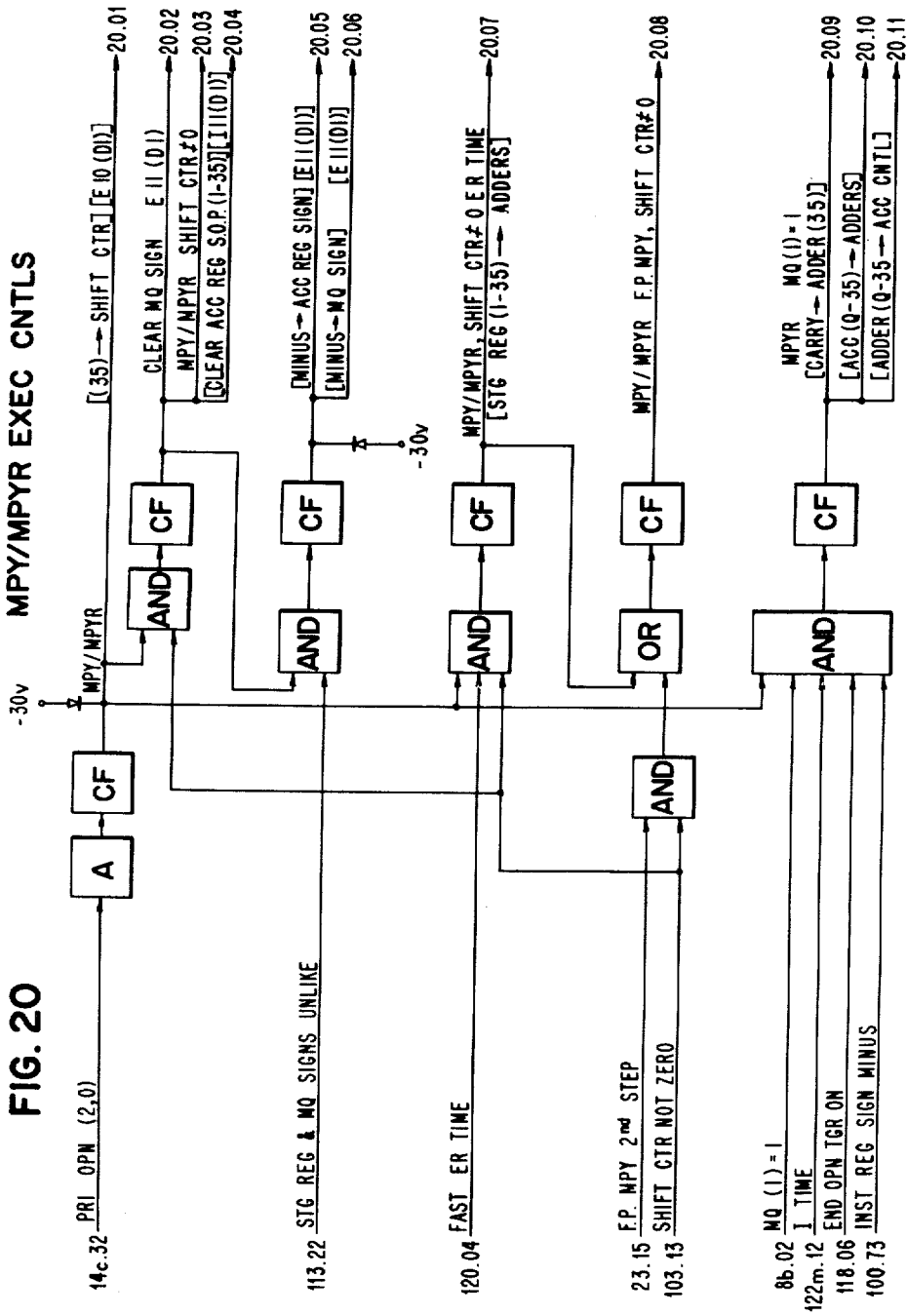
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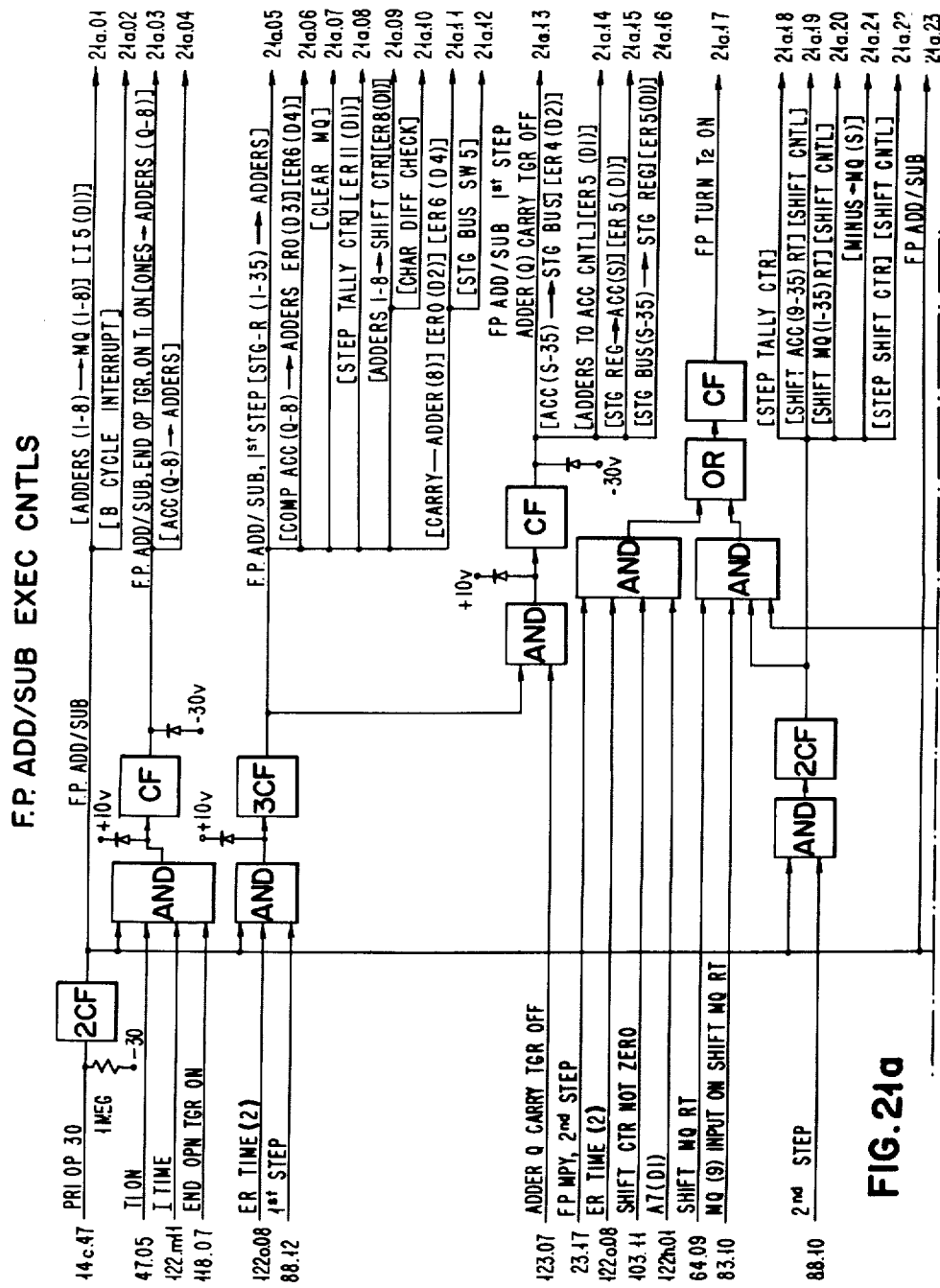
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**FIG. 21a**

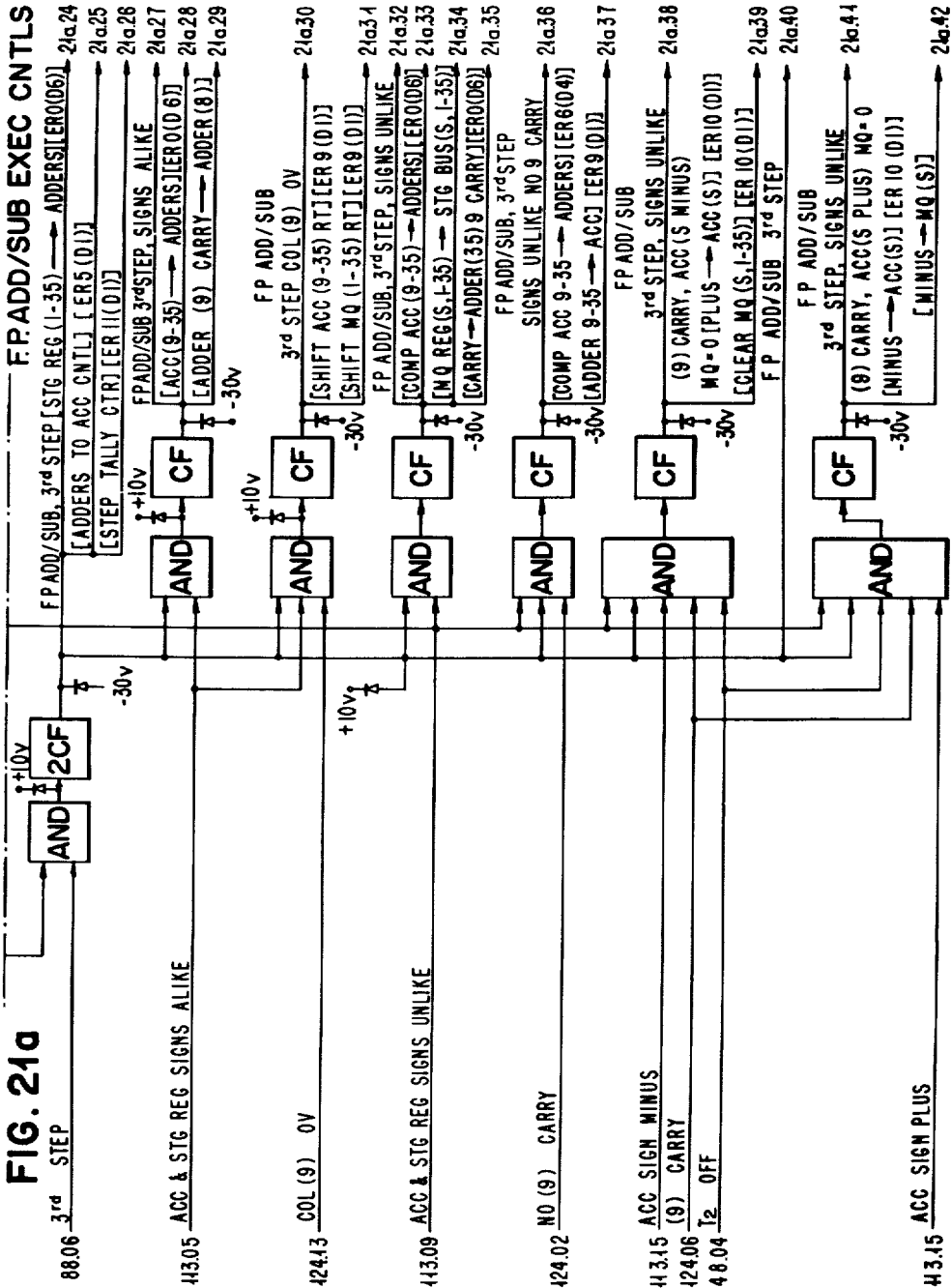
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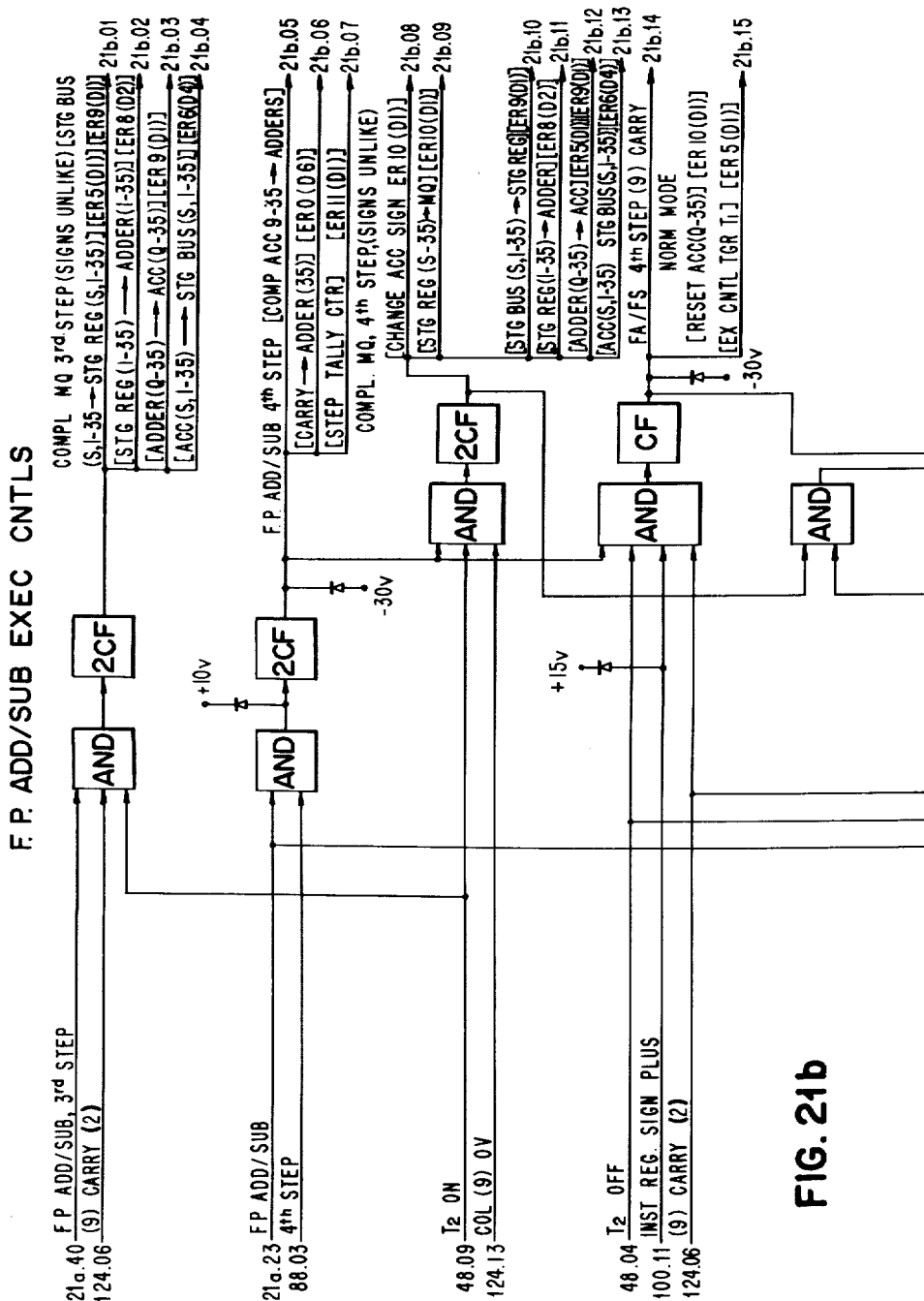
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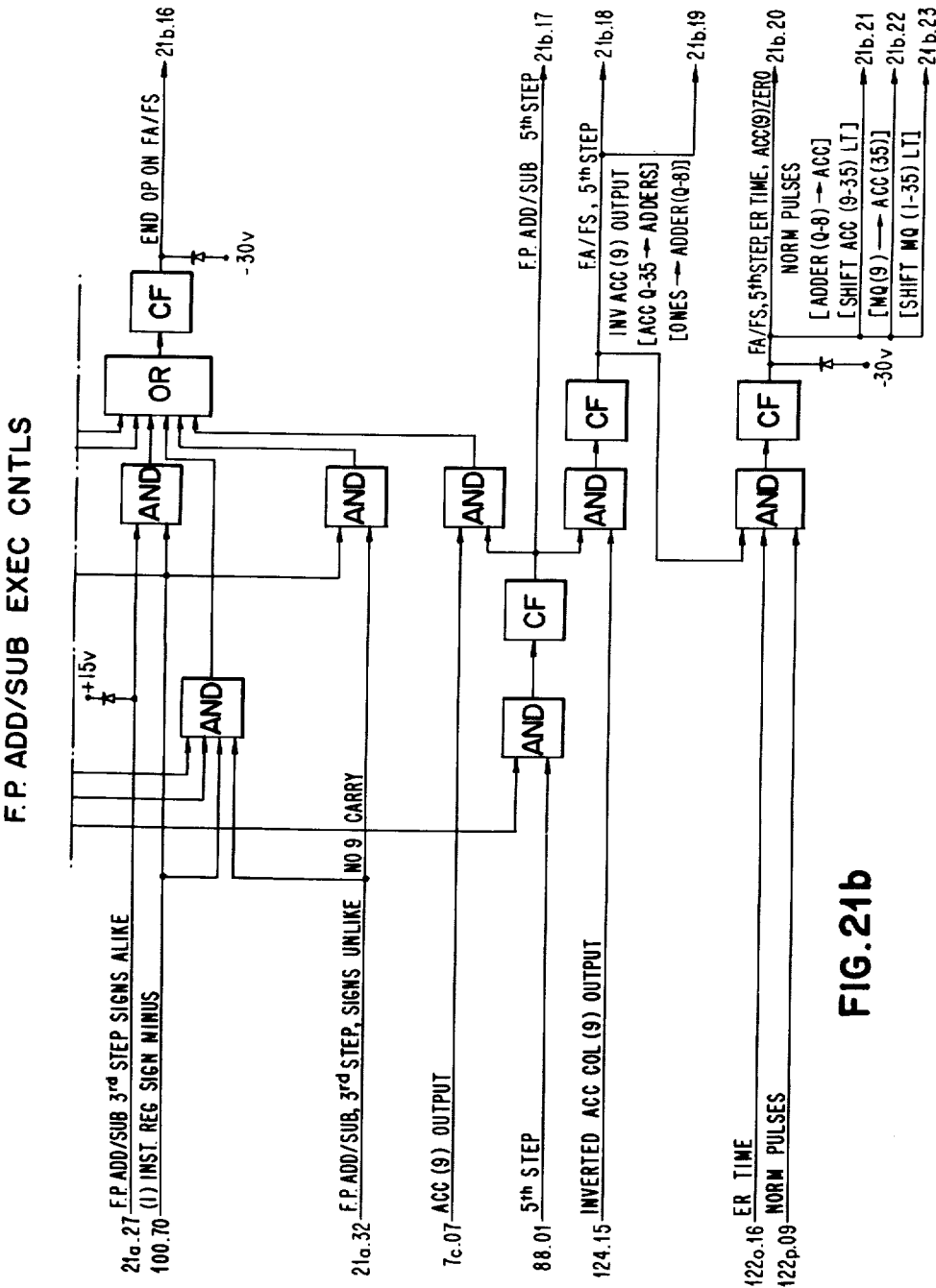


FIG. 21b

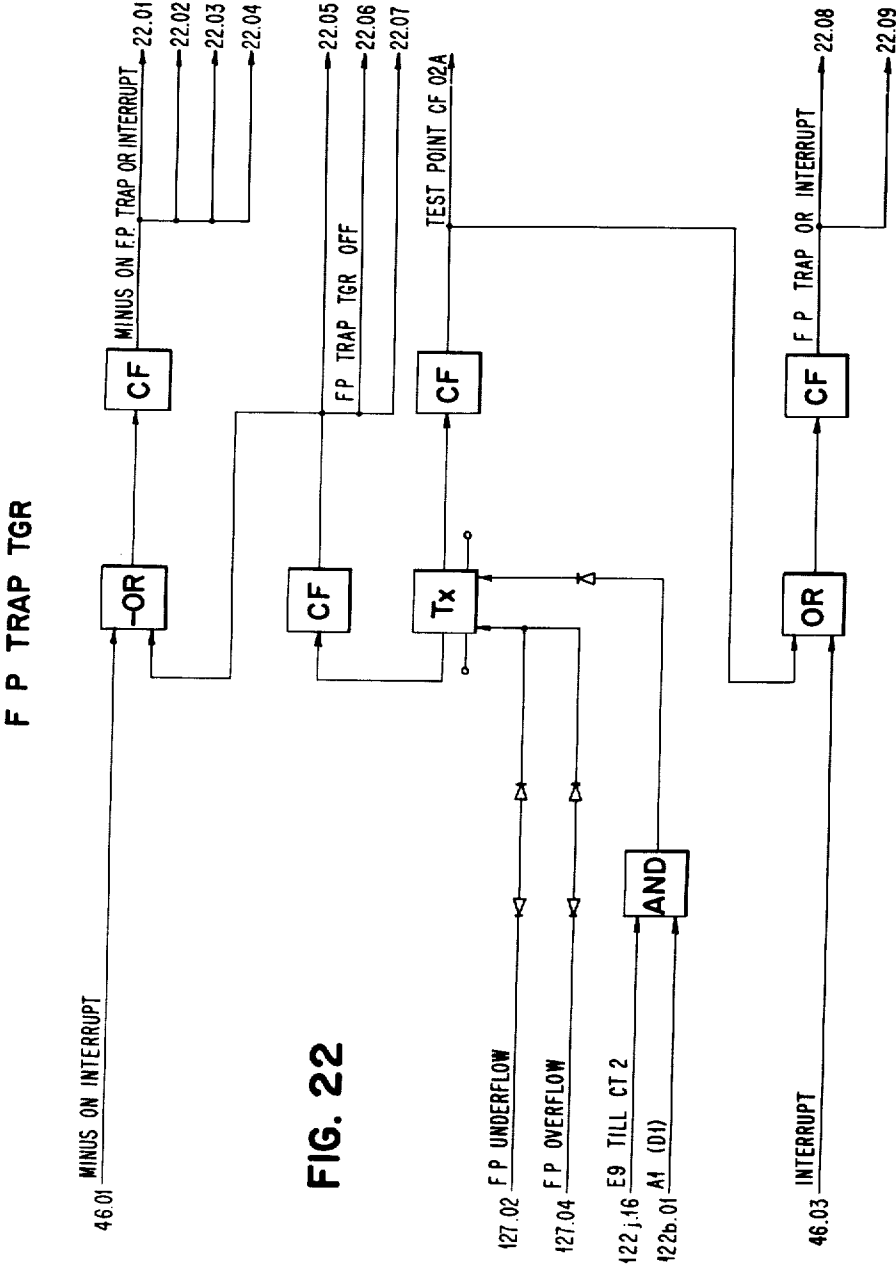
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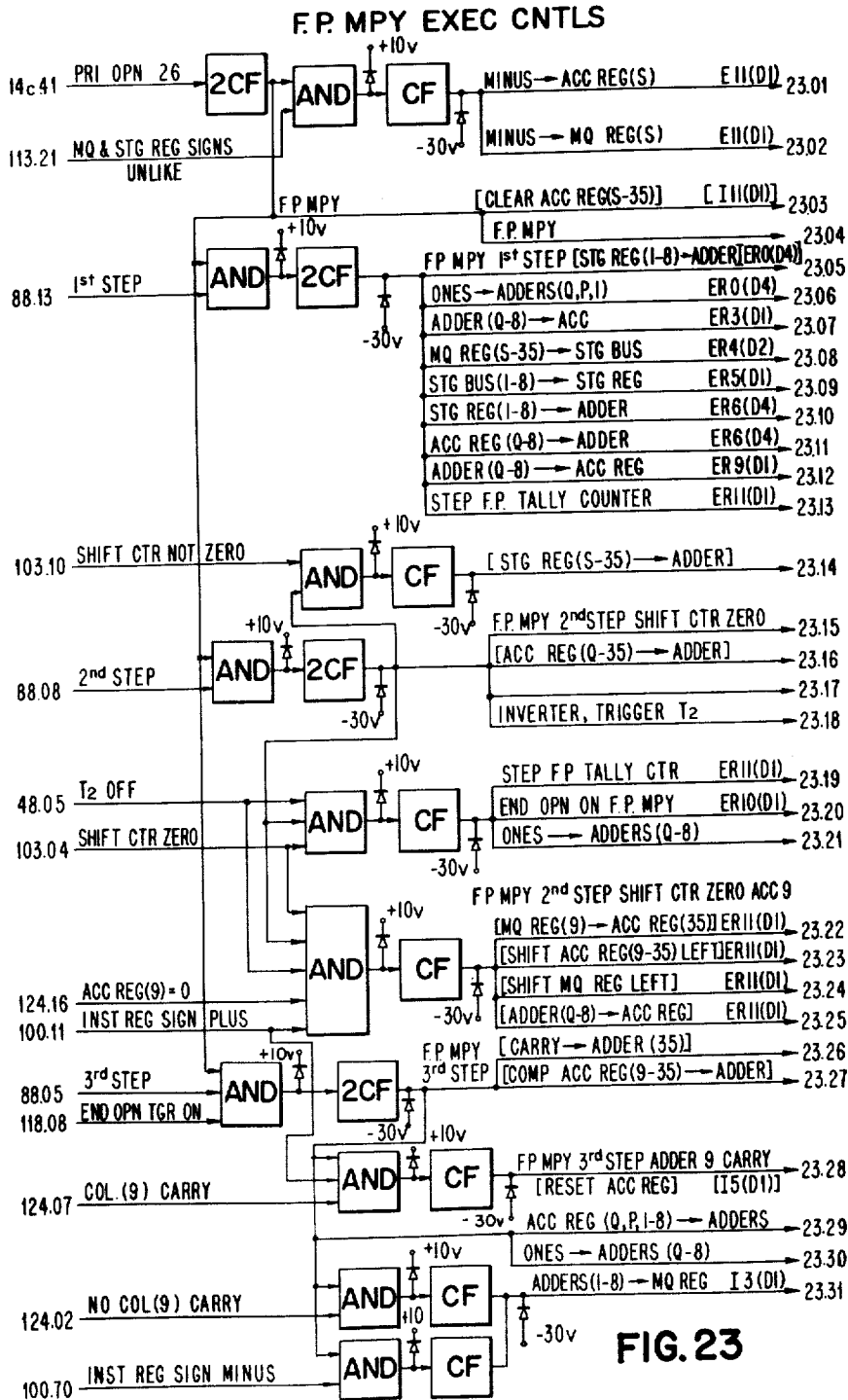


FIG. 23

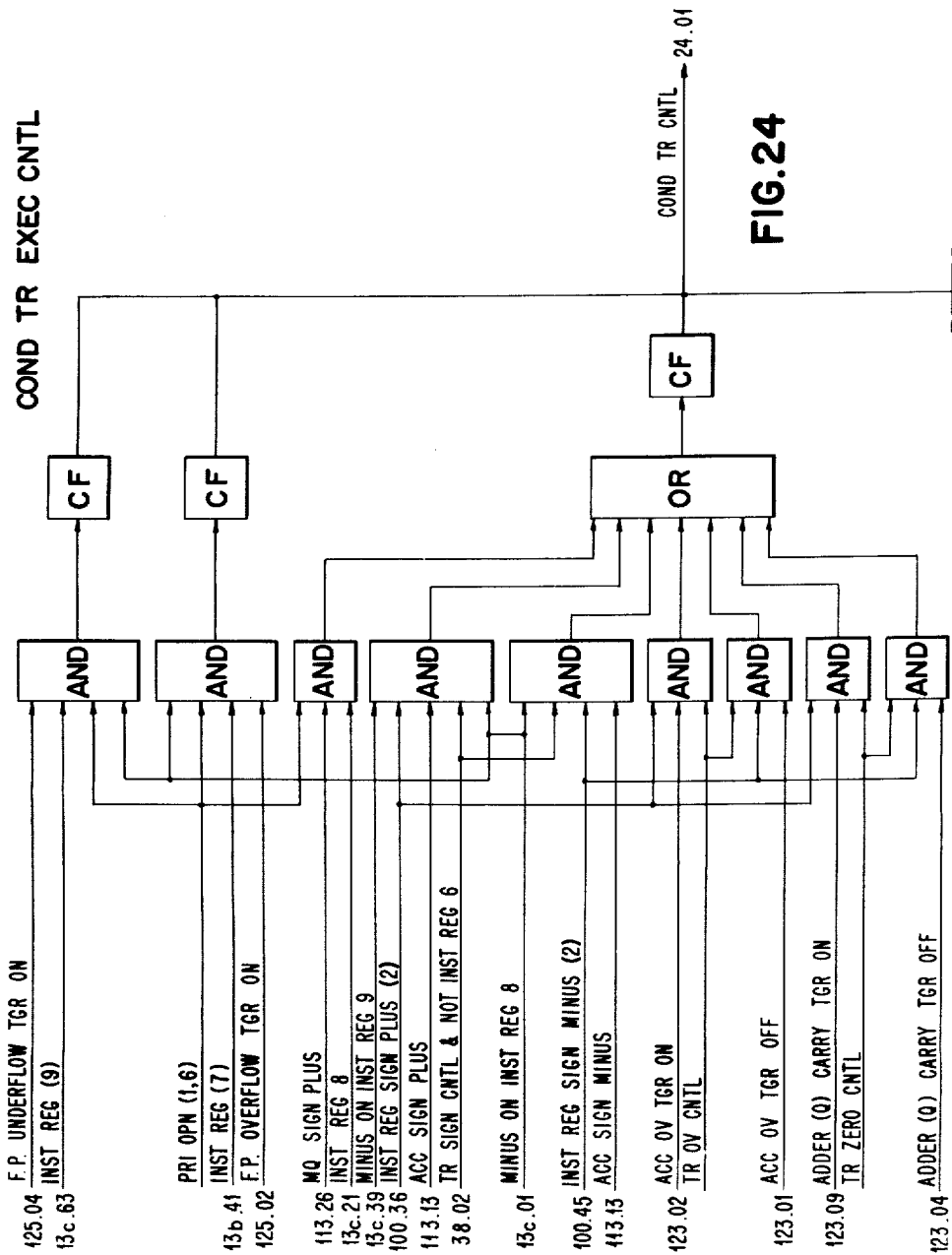
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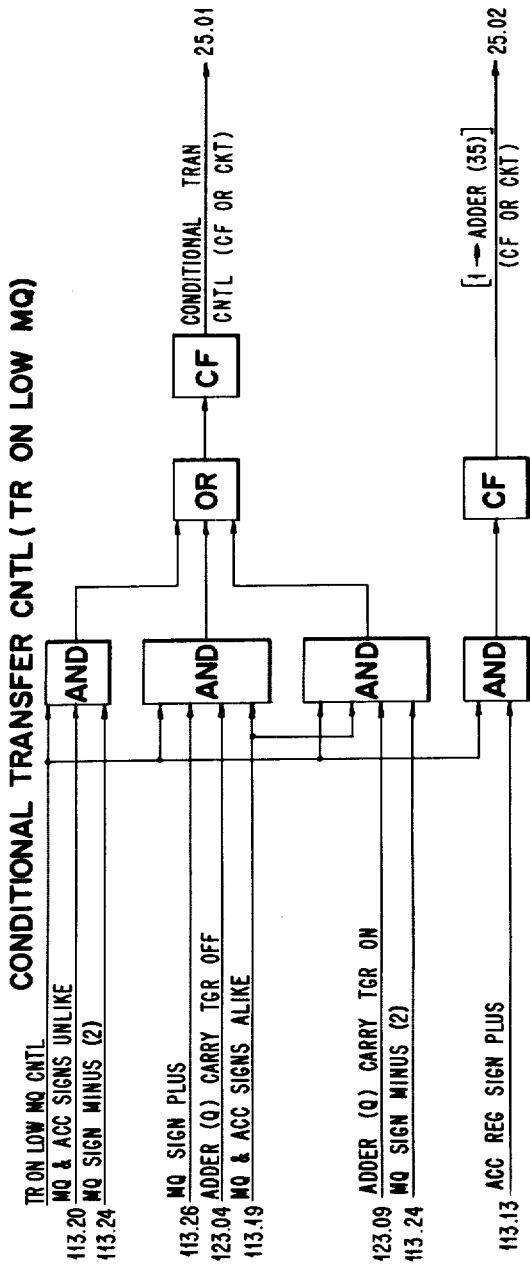
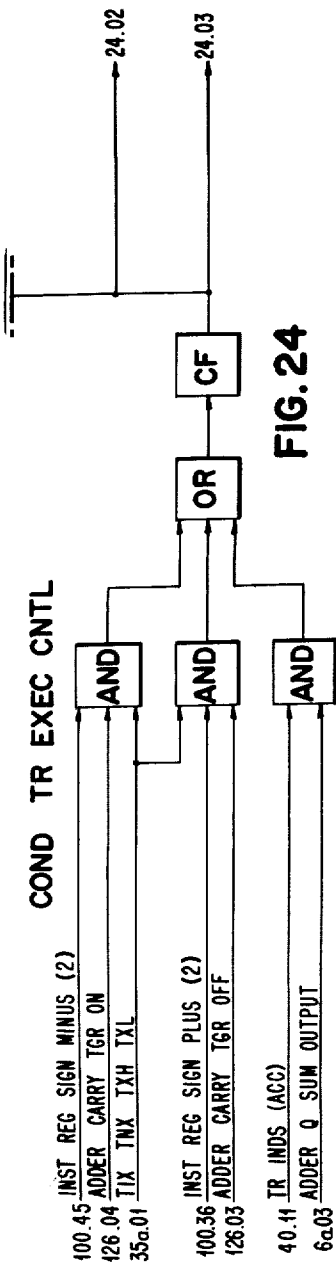
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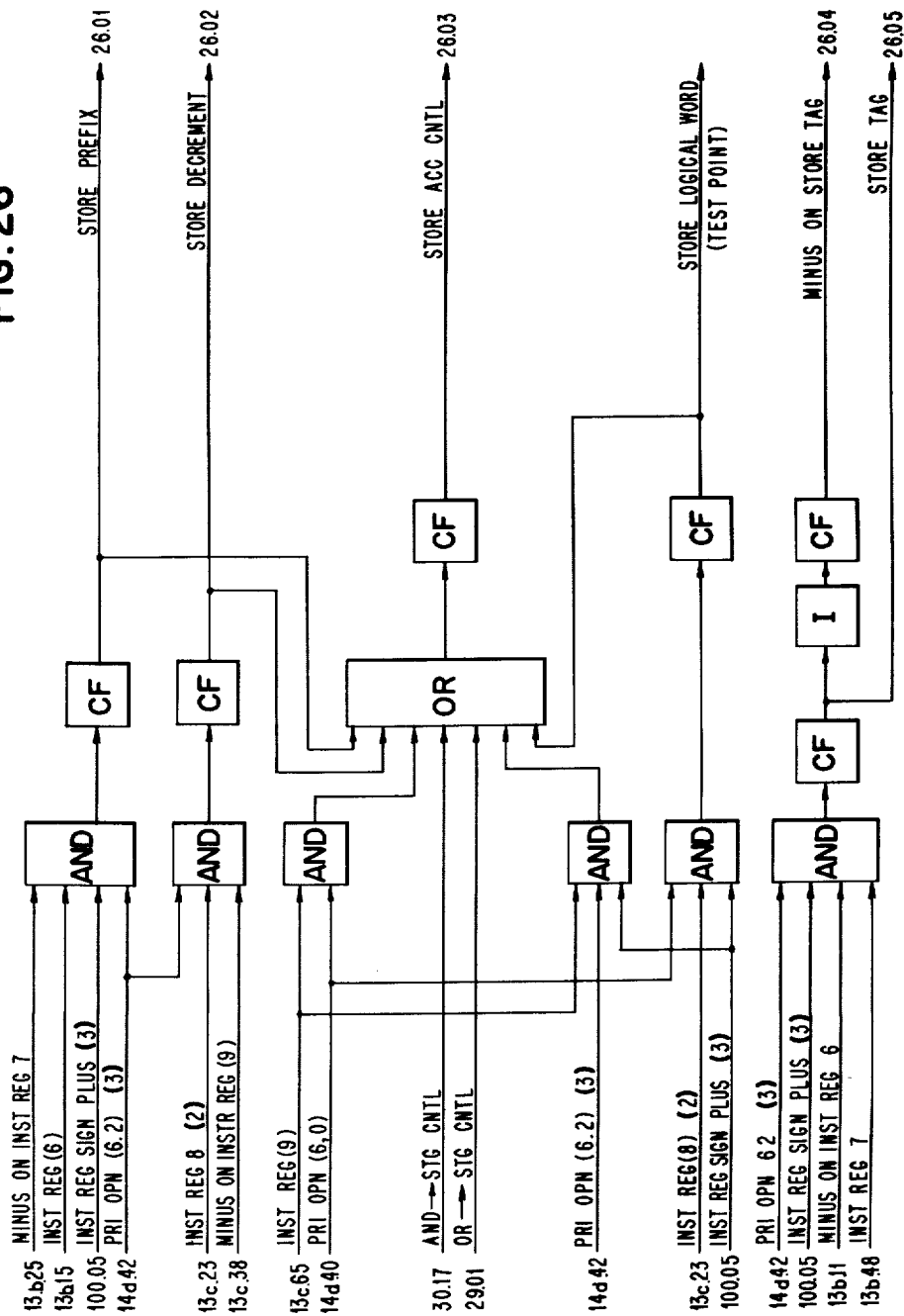
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STORE EXECUTION CNTL  
FIG. 26



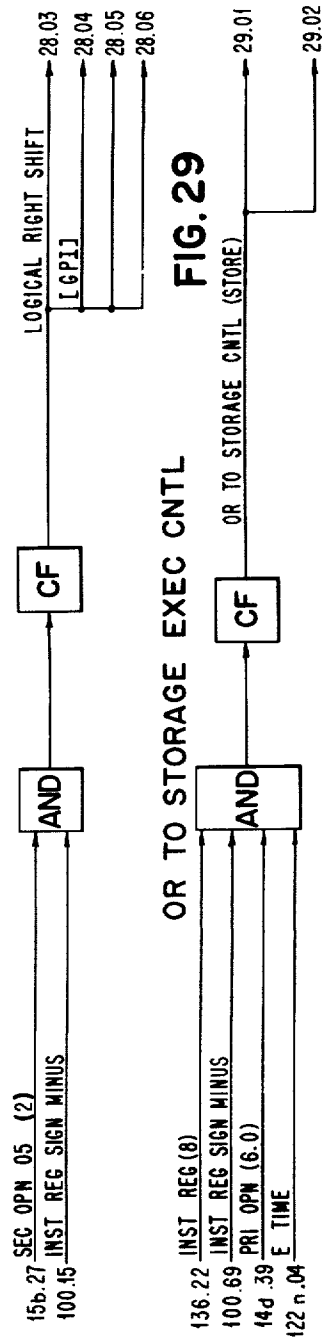
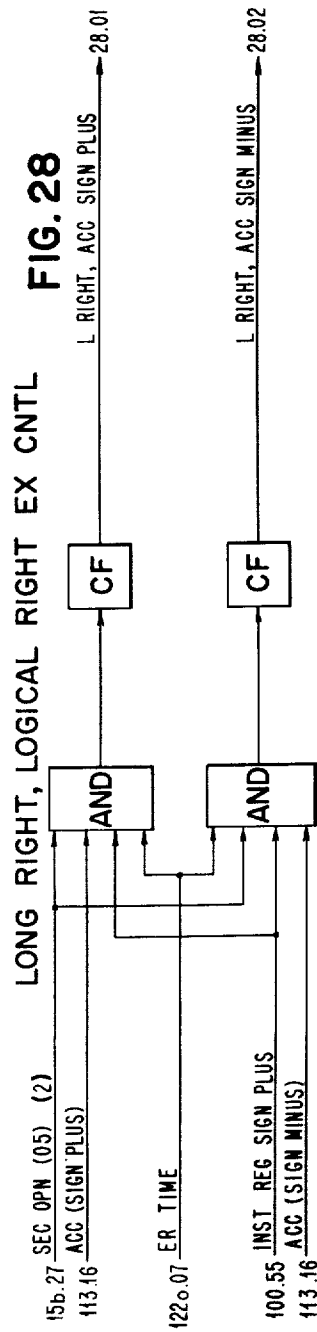
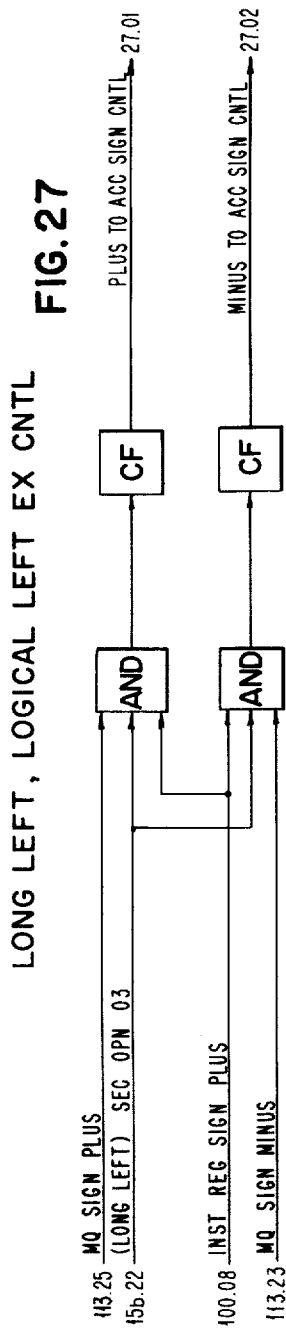
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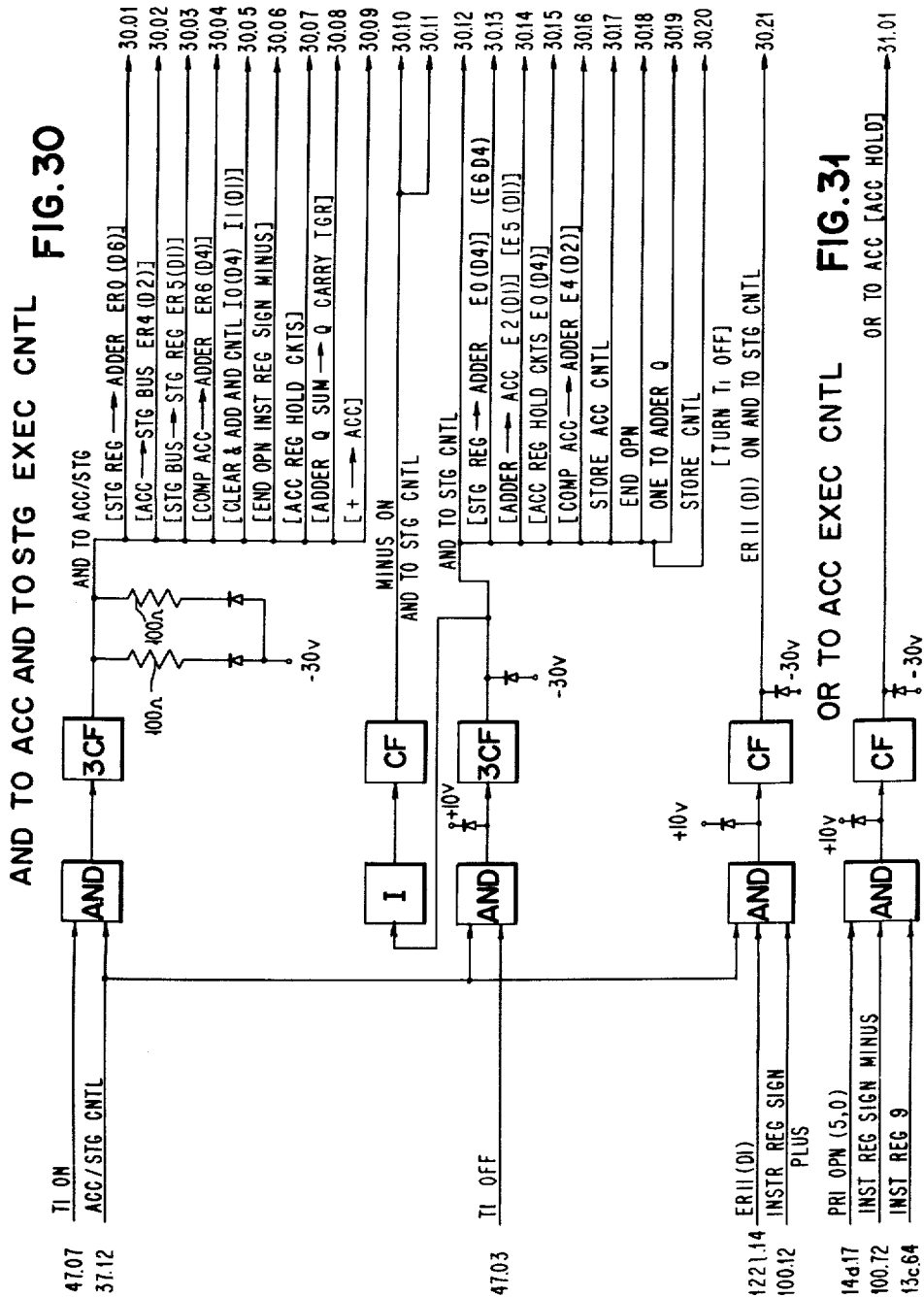
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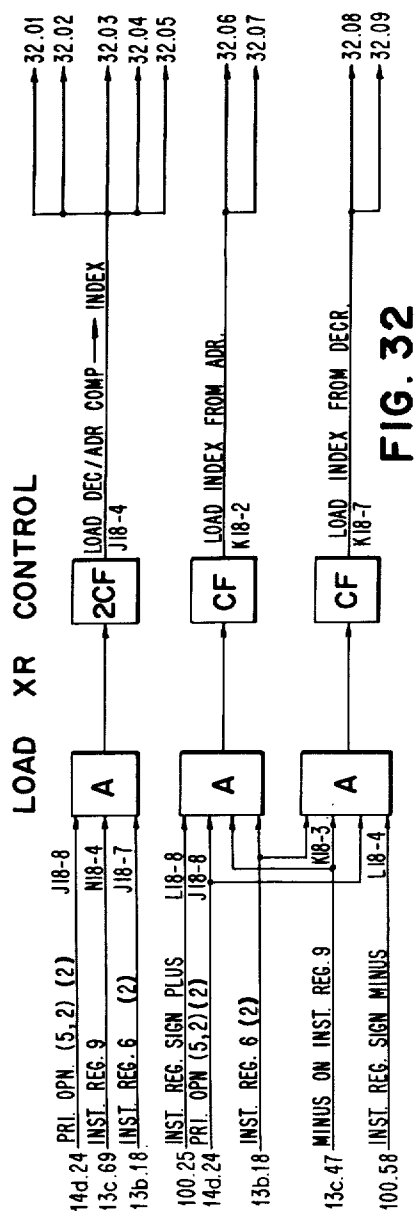


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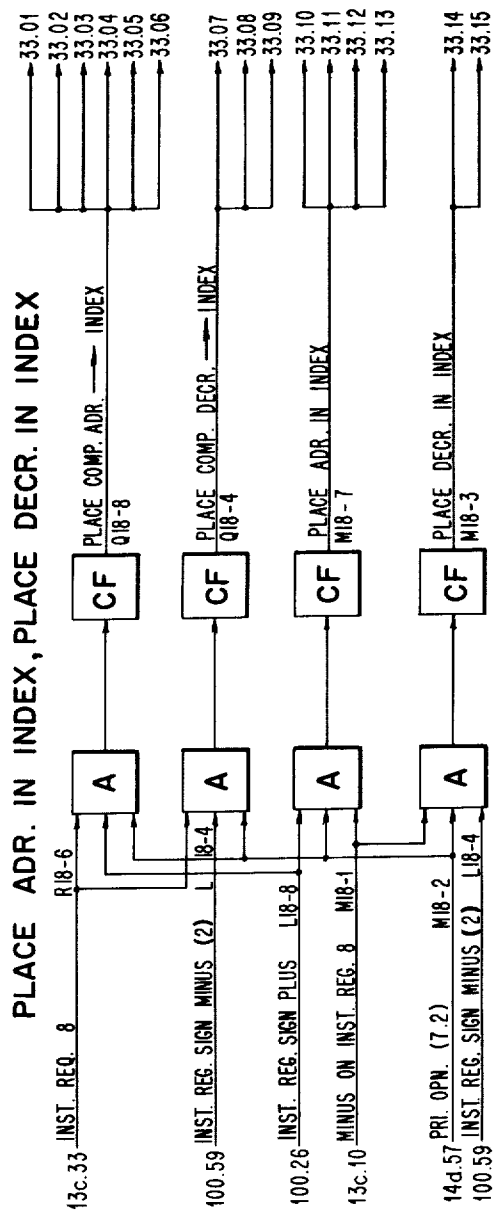


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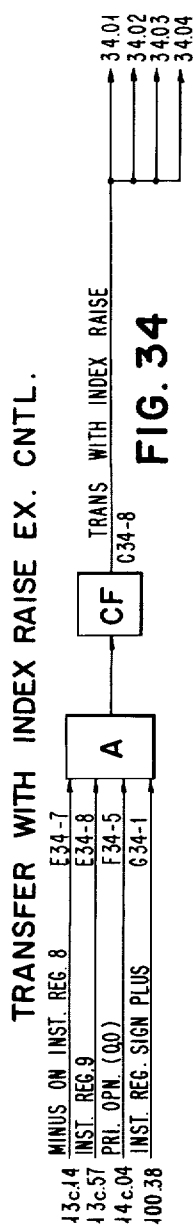
**FIG. 32**



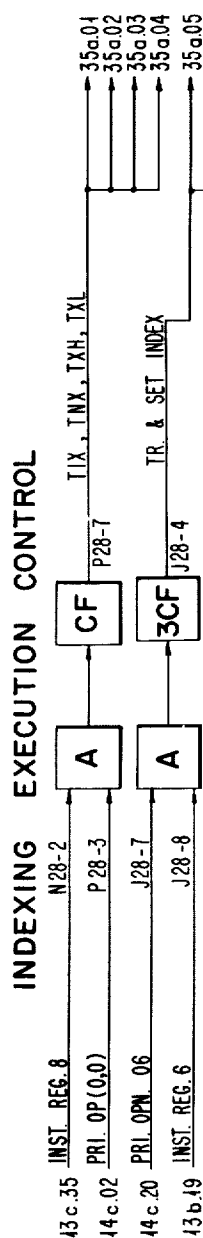
**FIG. 33**

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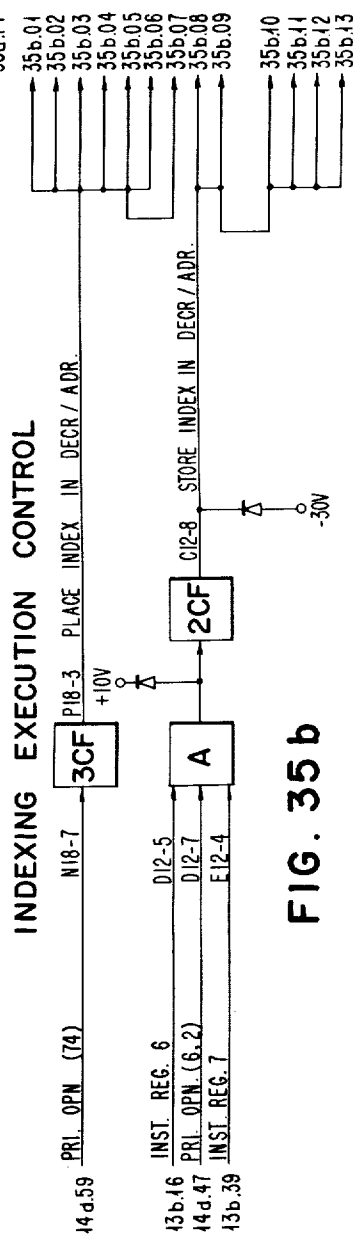
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**FIG. 34**



**FIG. 35d**



**FIG. 35b**

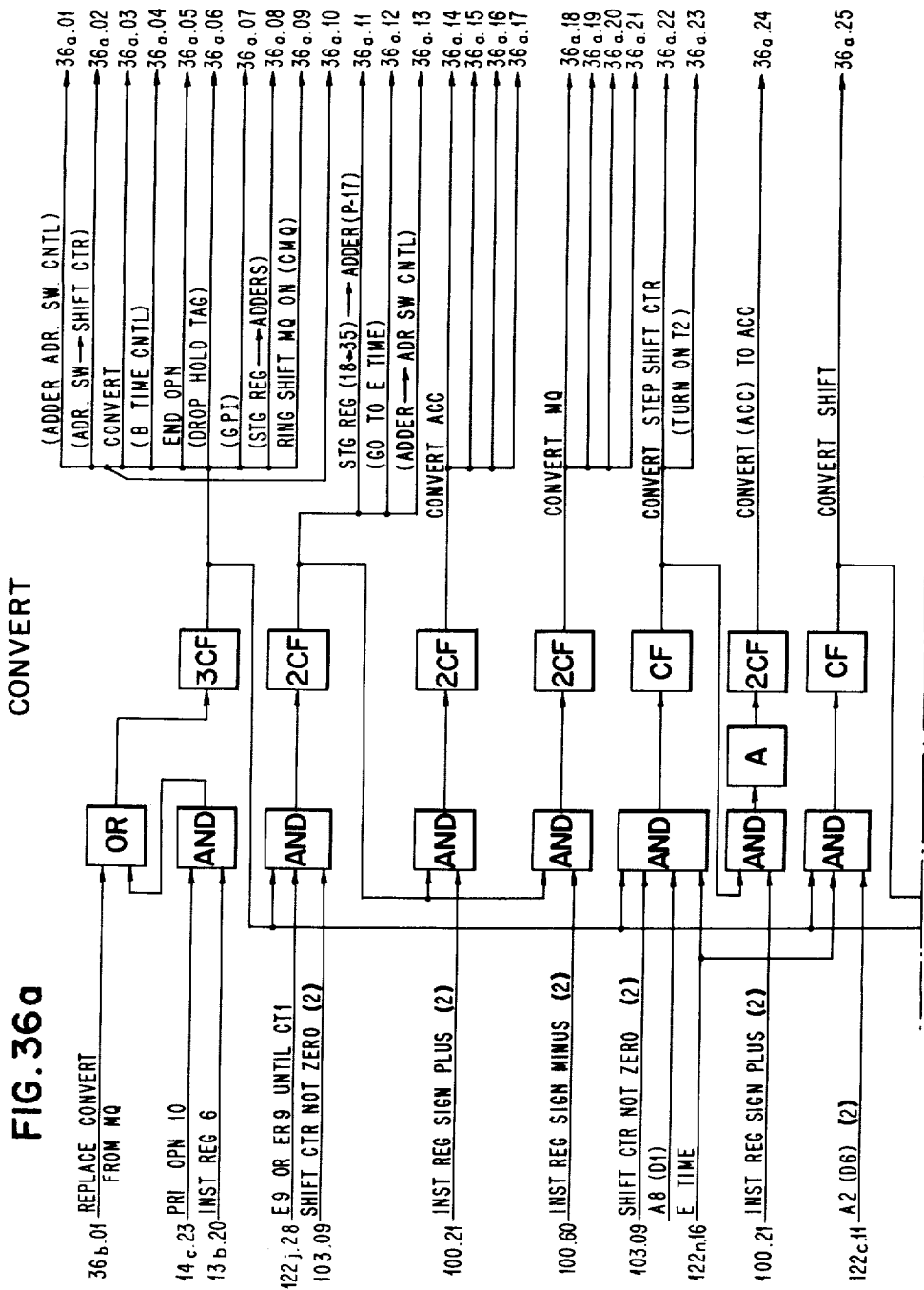
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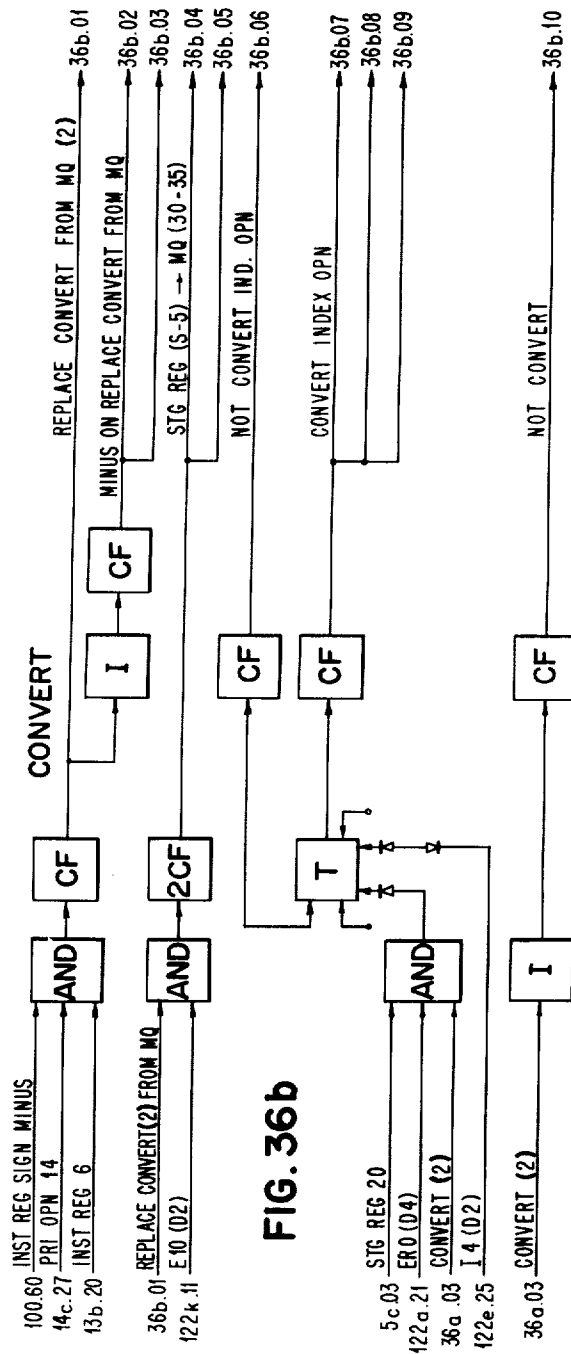
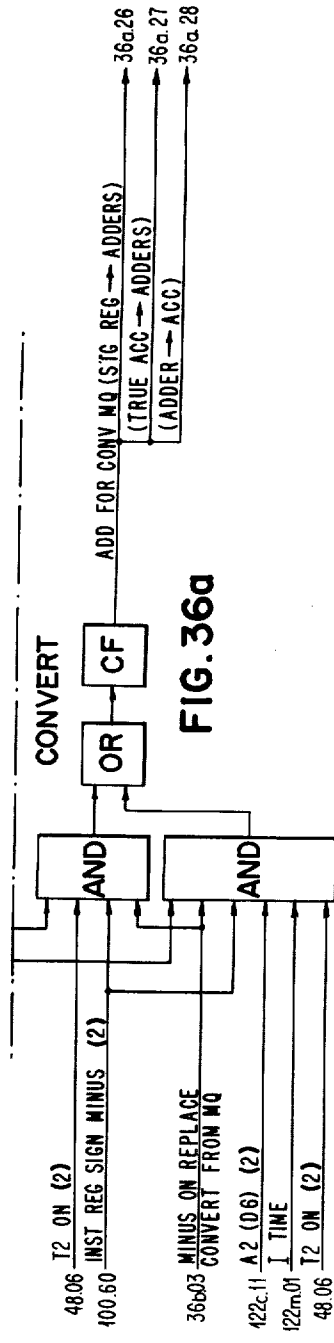
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AN INDICATING REGISTER

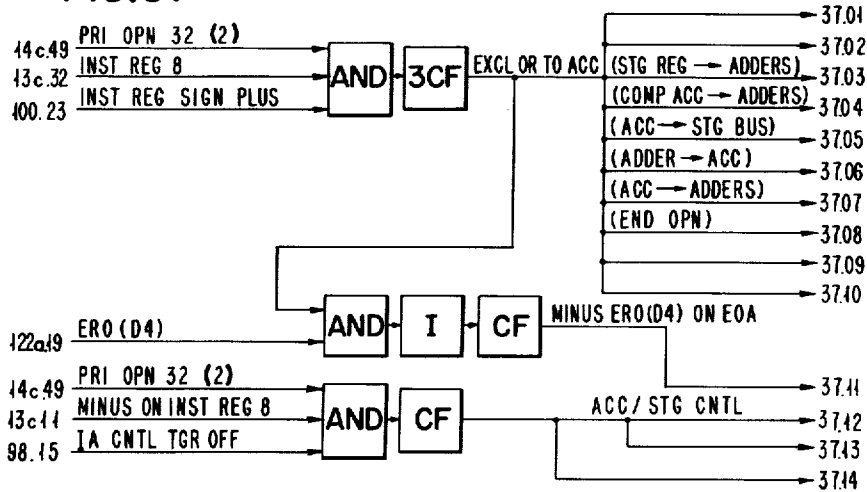
3,019,976

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FIG. 37

EXCLUSIVE OR TO ACC



EXCHANGE, TRANSFER SIGN CONTROL

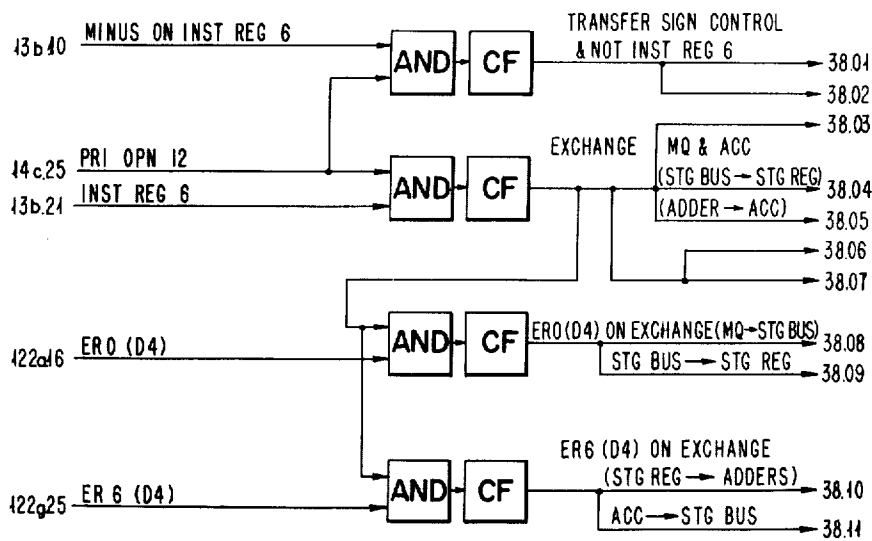


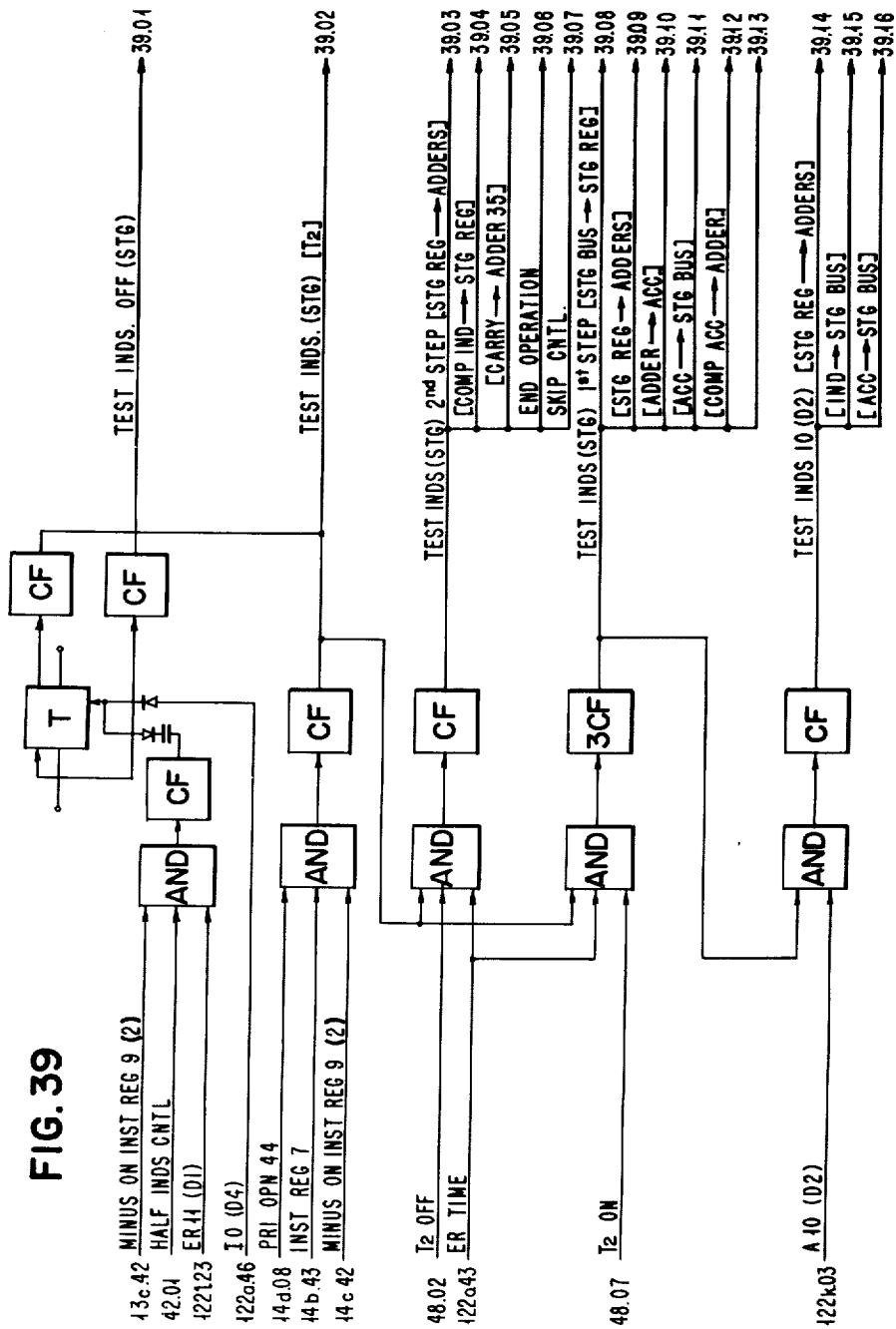
FIG. 38

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## TEST INDICATORS (STORAGE) HALF TEST INDICATORS

**FIG. 39**



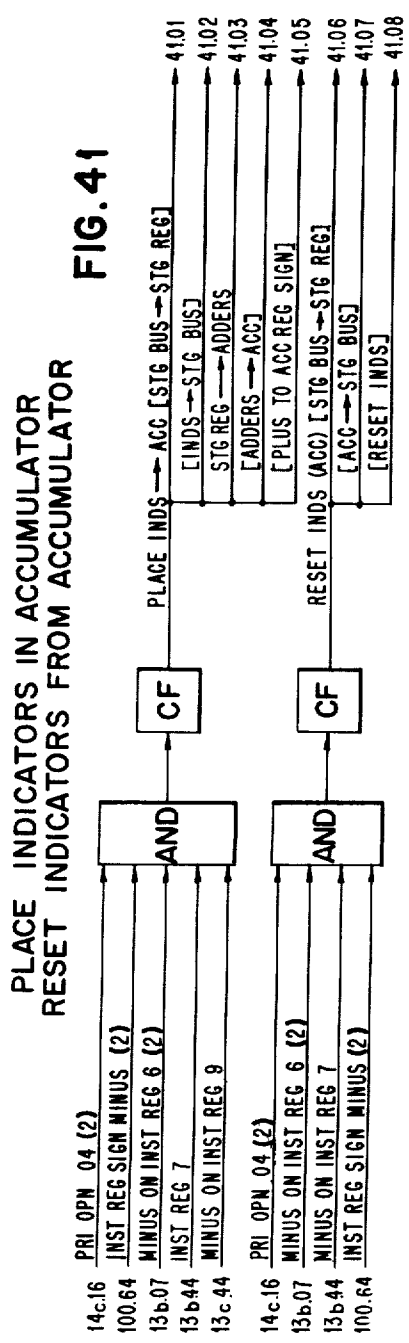
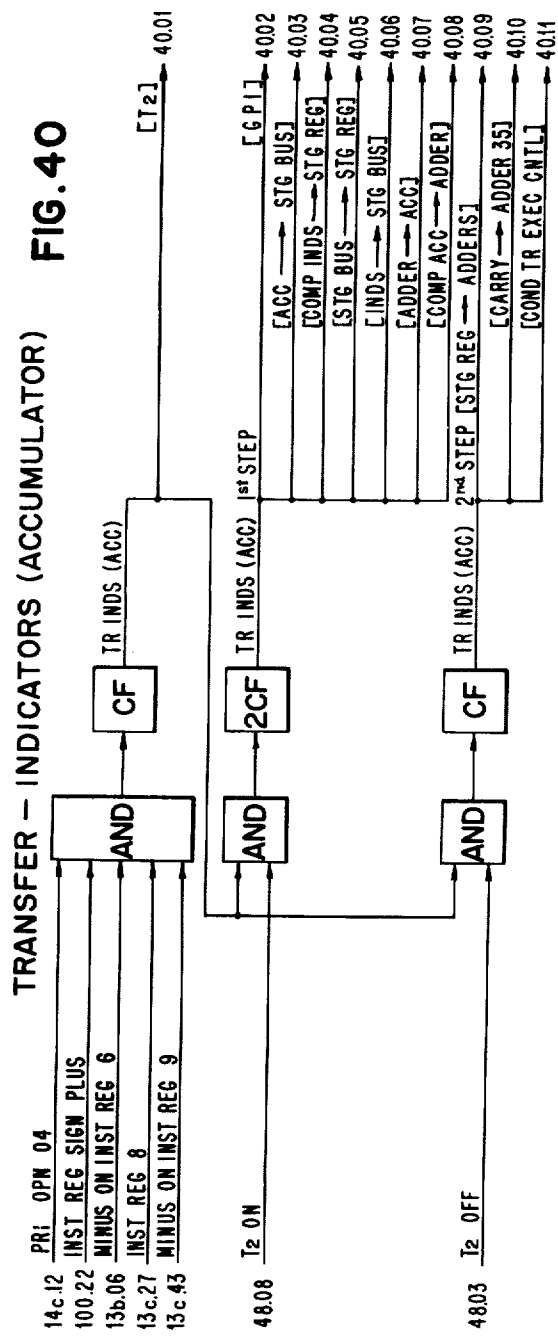
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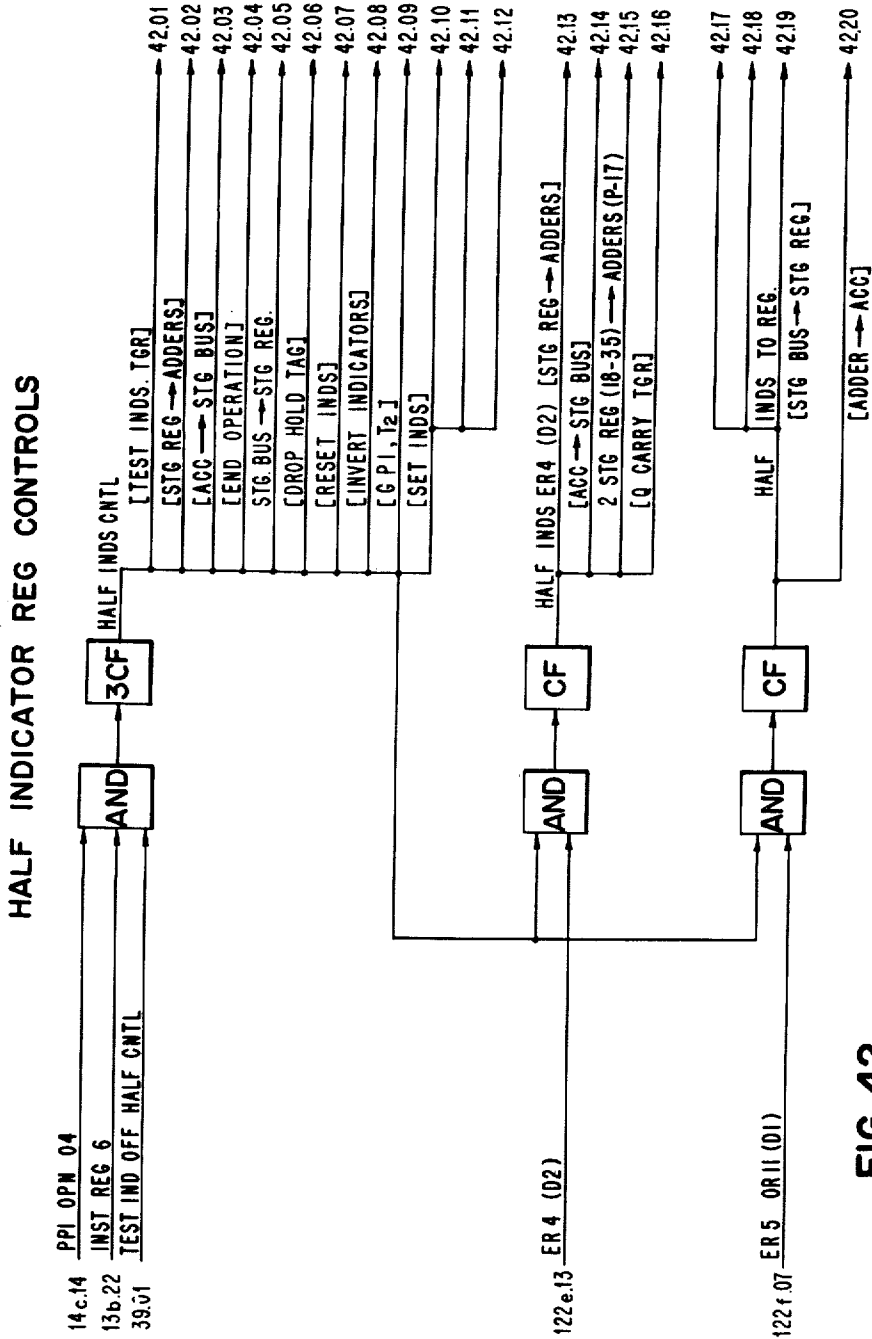
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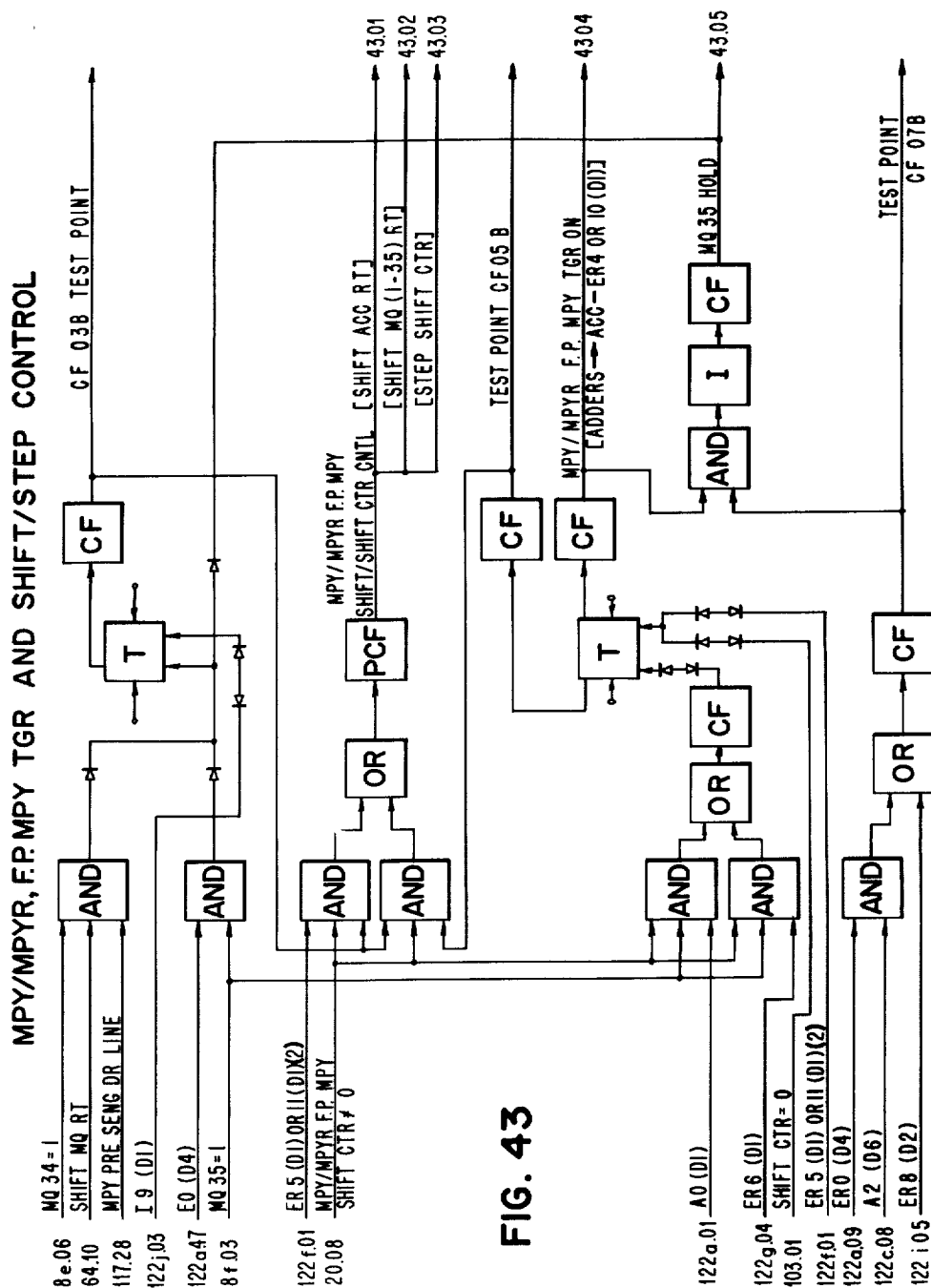
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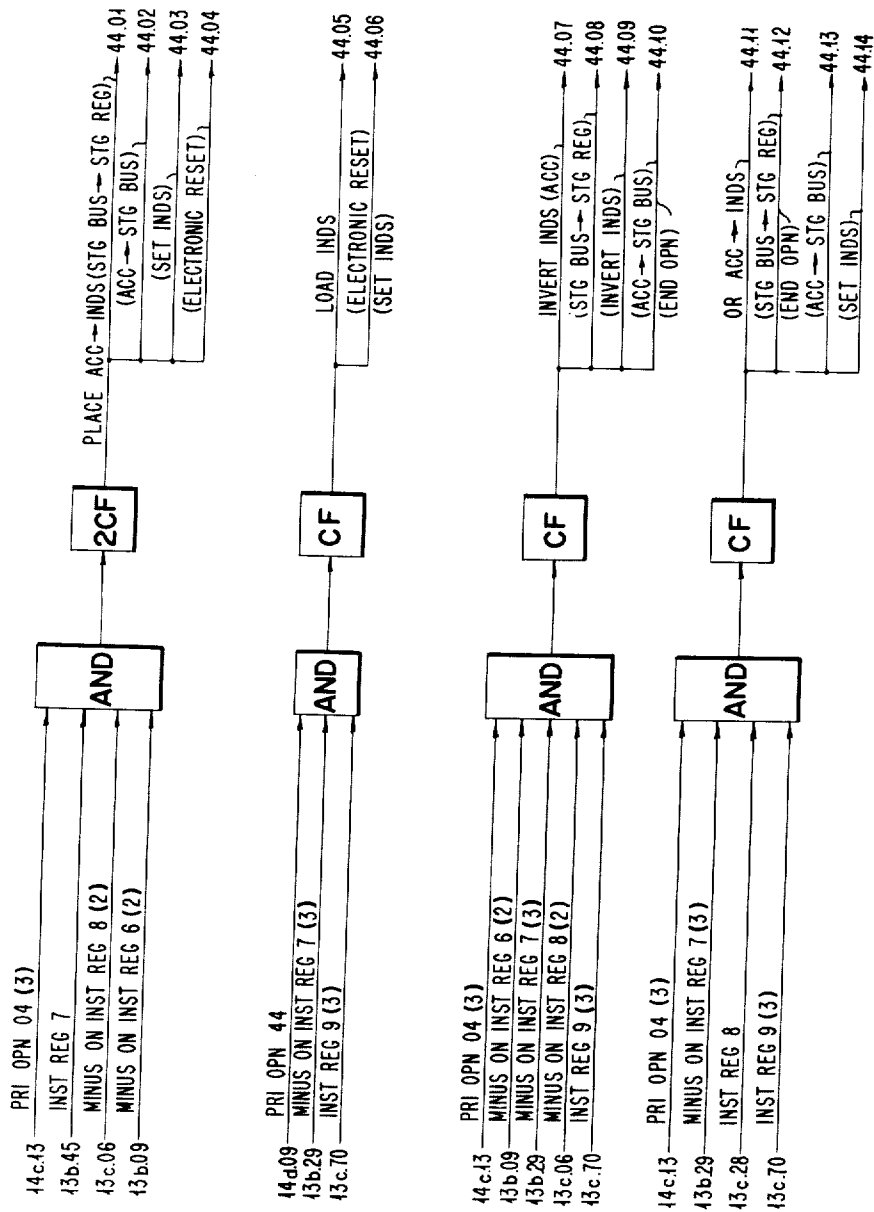
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AN INDICATING REGISTER

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FIG. 44  
PLACE ACCUMULATOR IN INDICATORS  
LOAD INDICATORS, INVERT INDICATORS,  
OR ACCUMULATOR TO INDICATORS



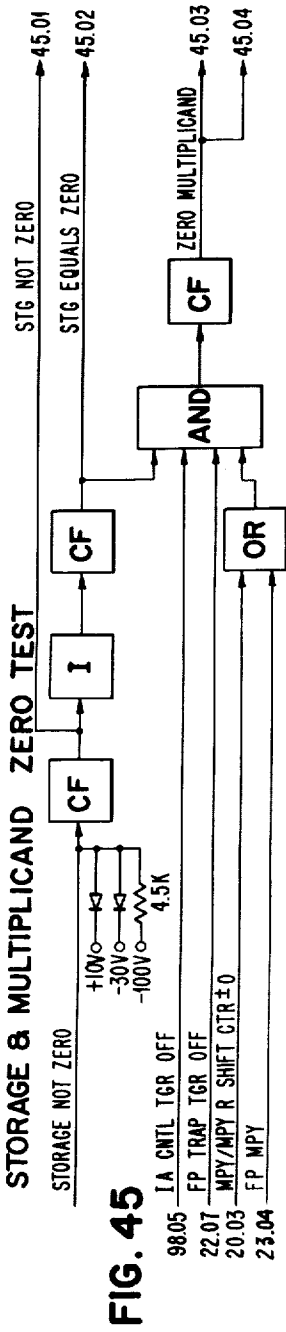
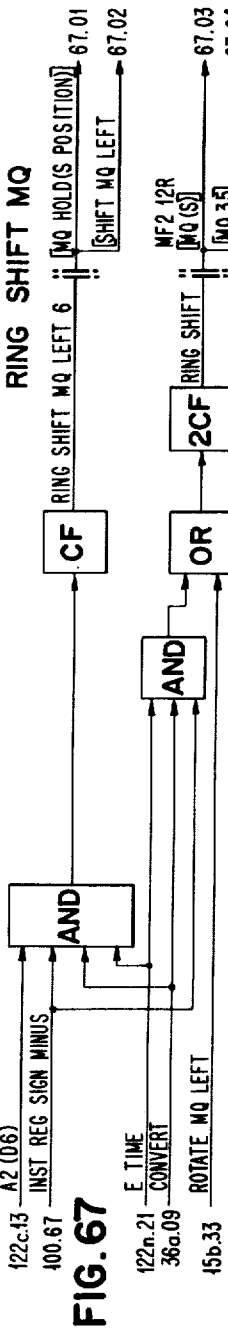
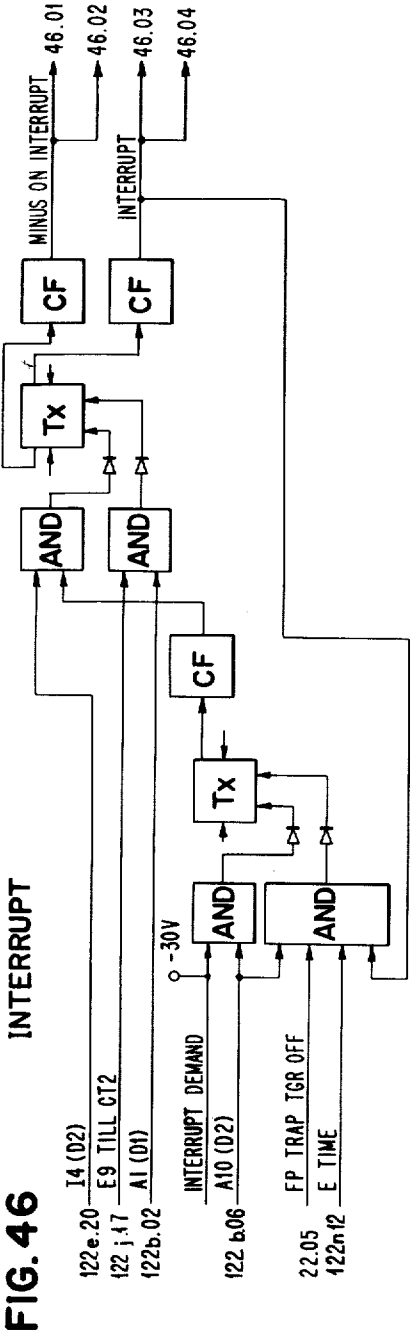
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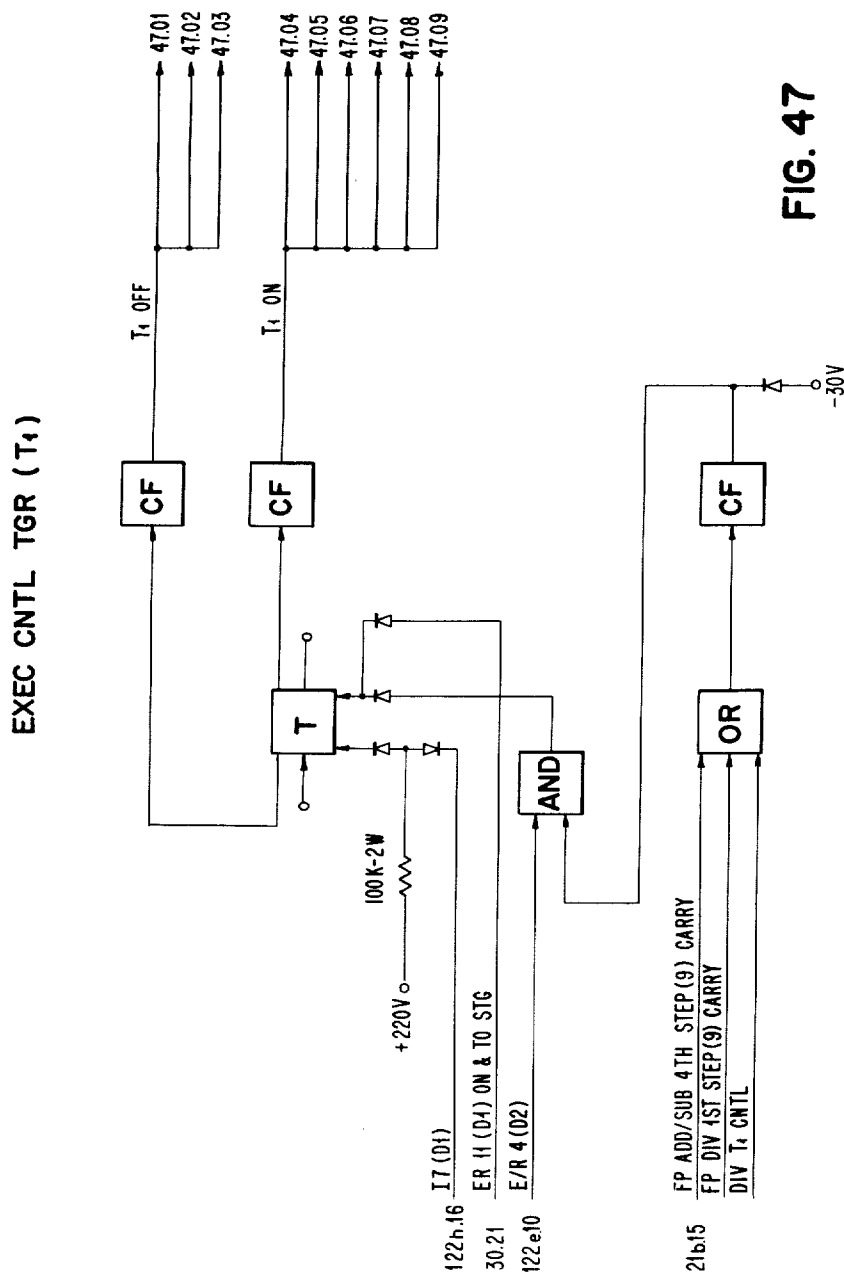


FIG. 47

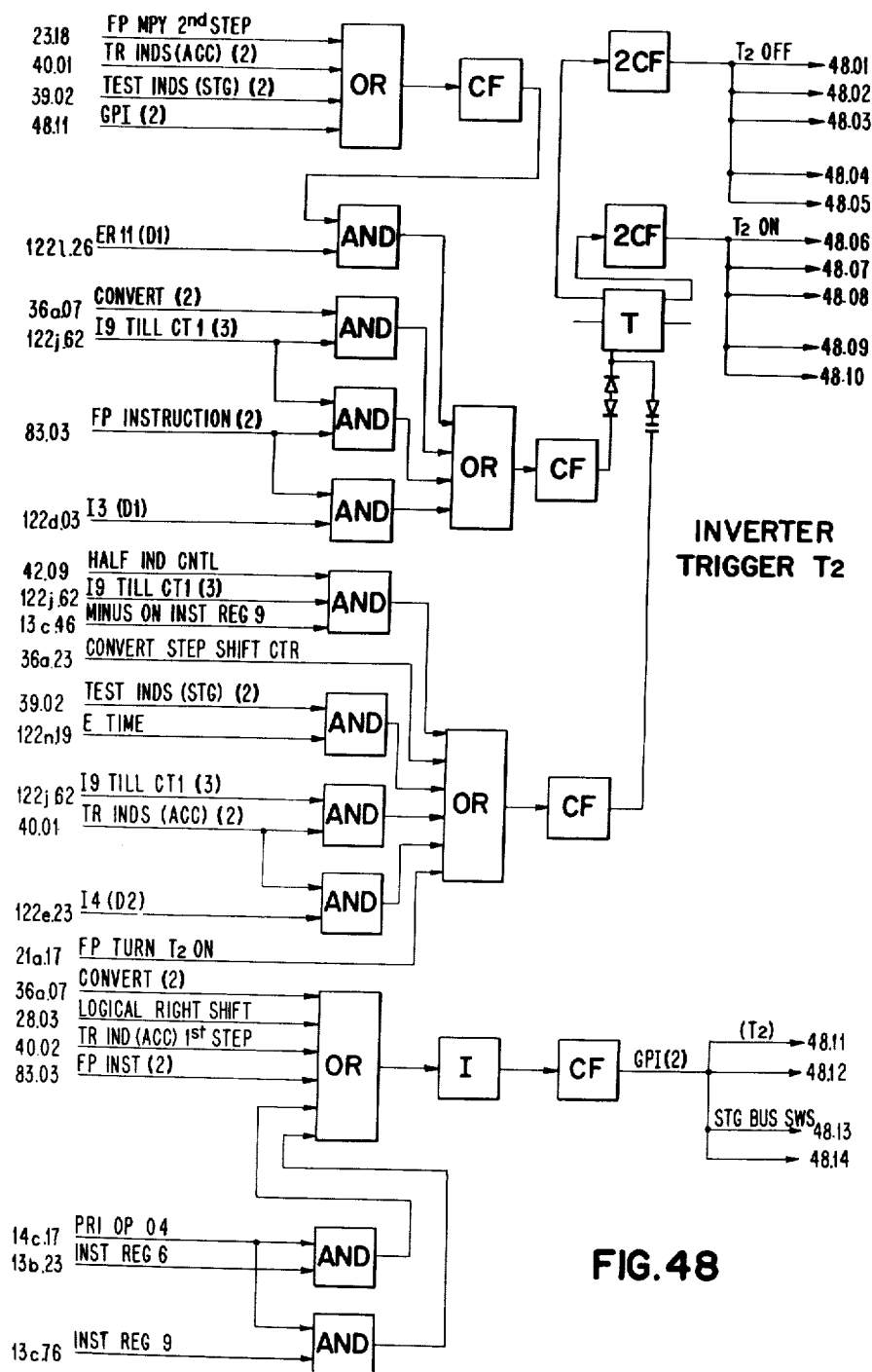
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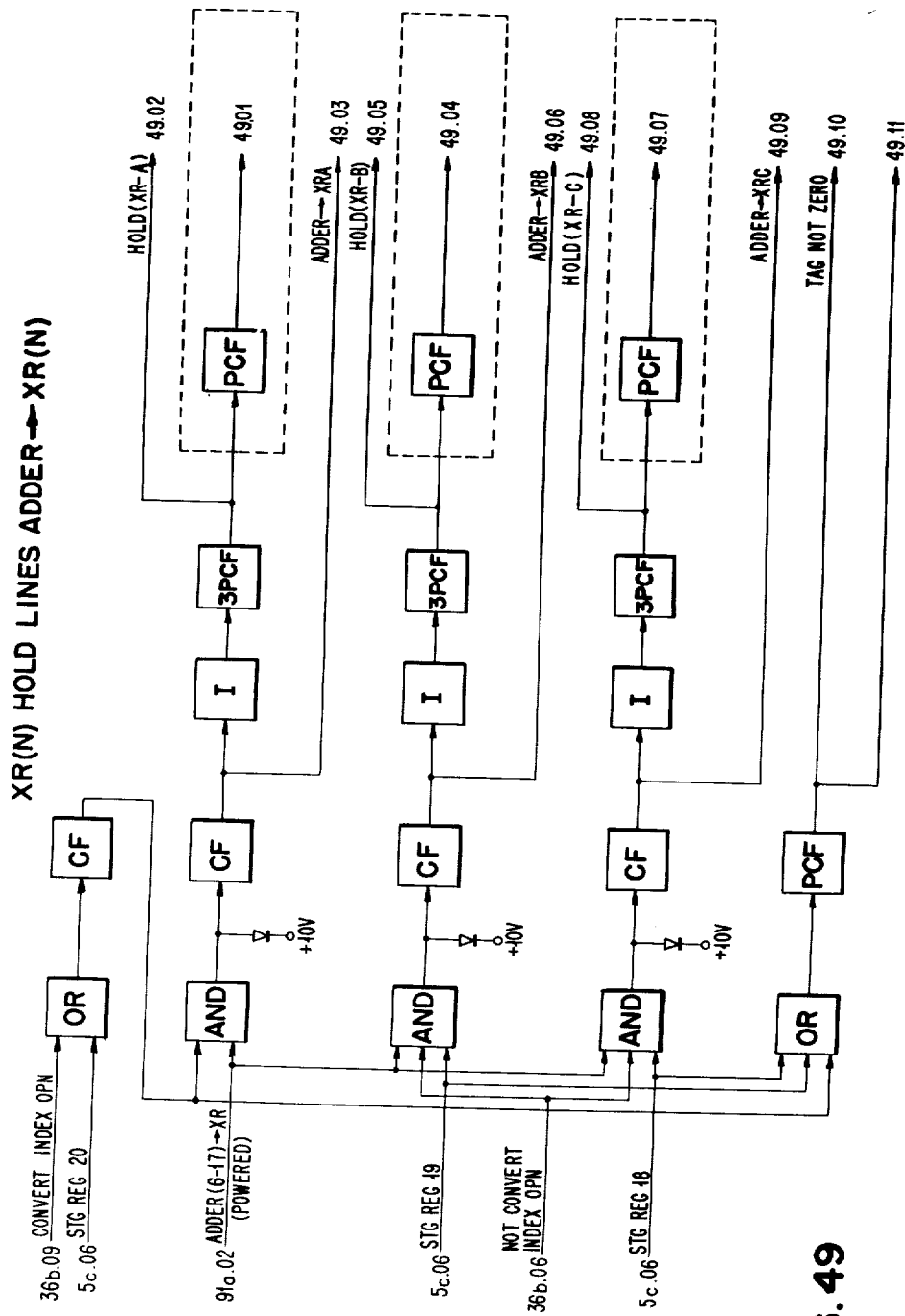


FIG. 49



**J. M. TAYLOR**  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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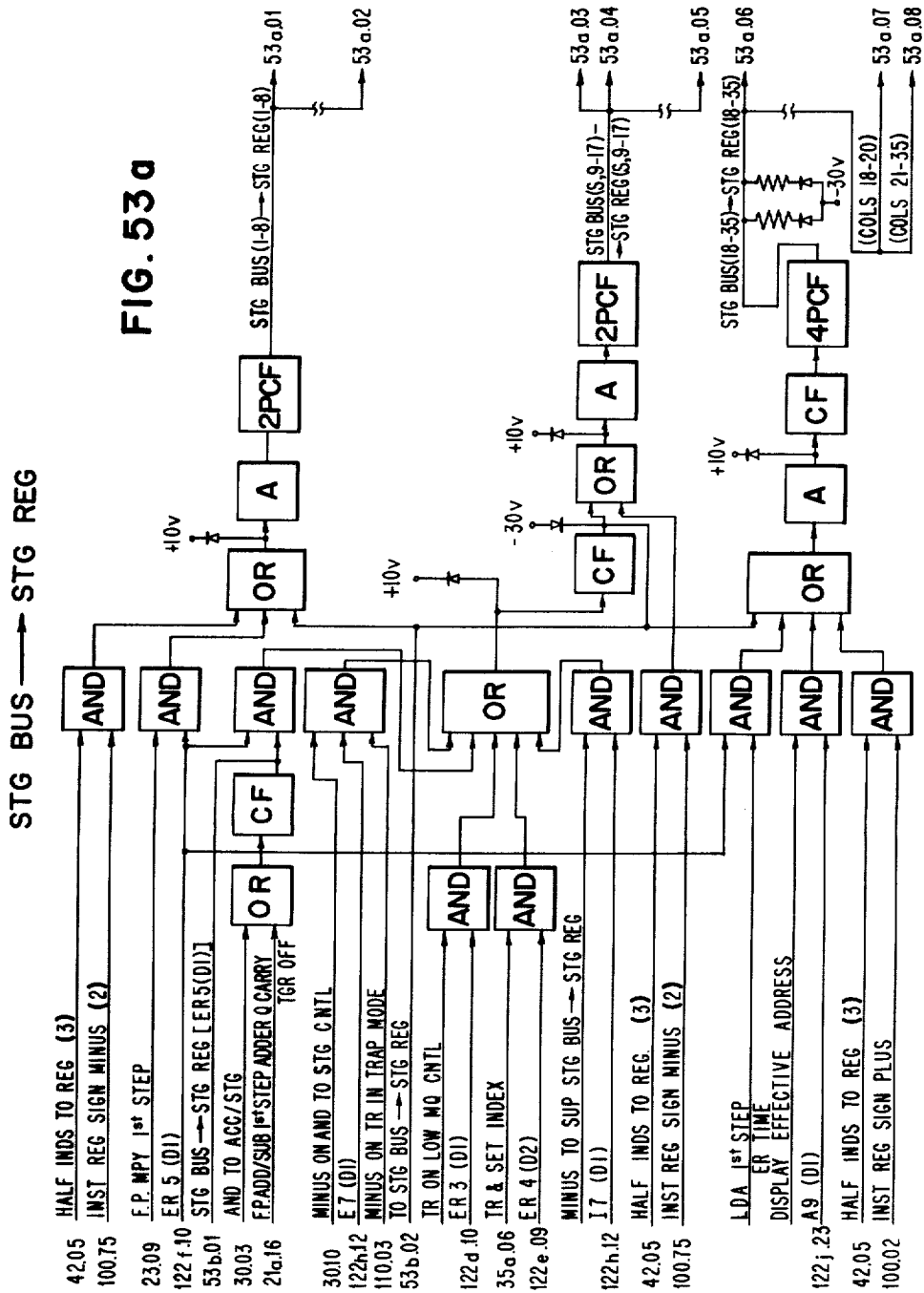
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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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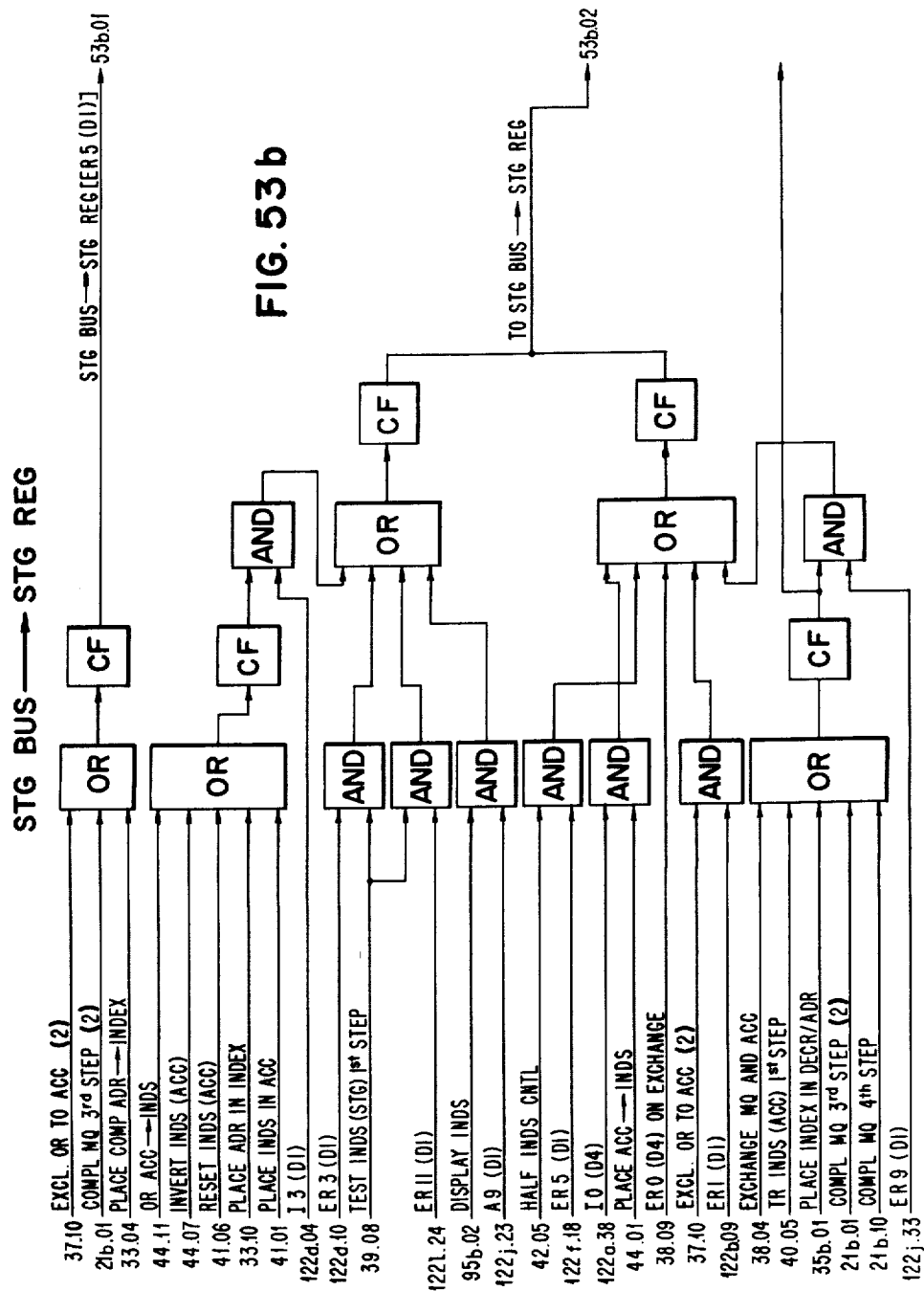
Feb. 6, 1962

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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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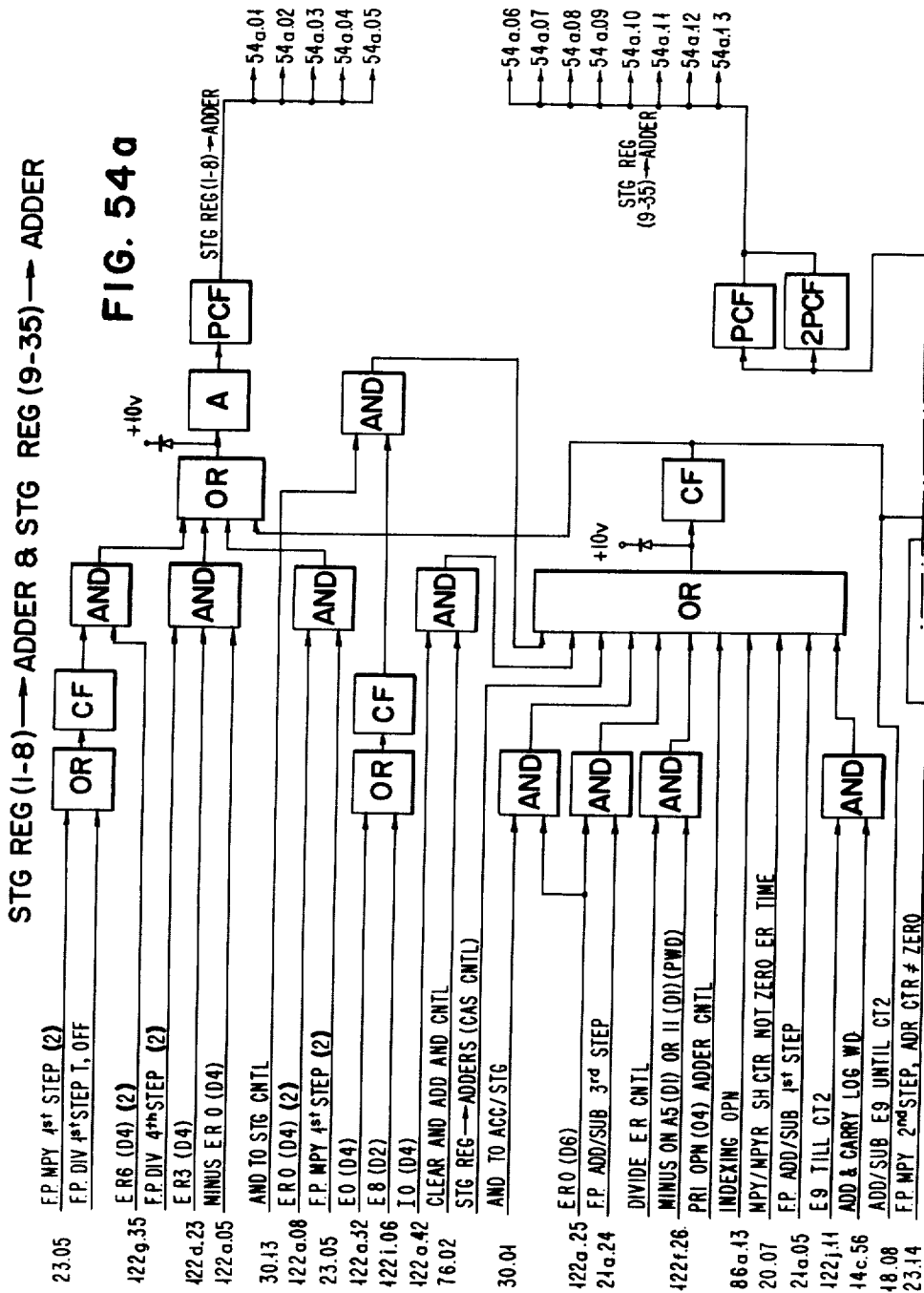
Filed Dec. 26, 1957

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Filed Dec. 26, 1957

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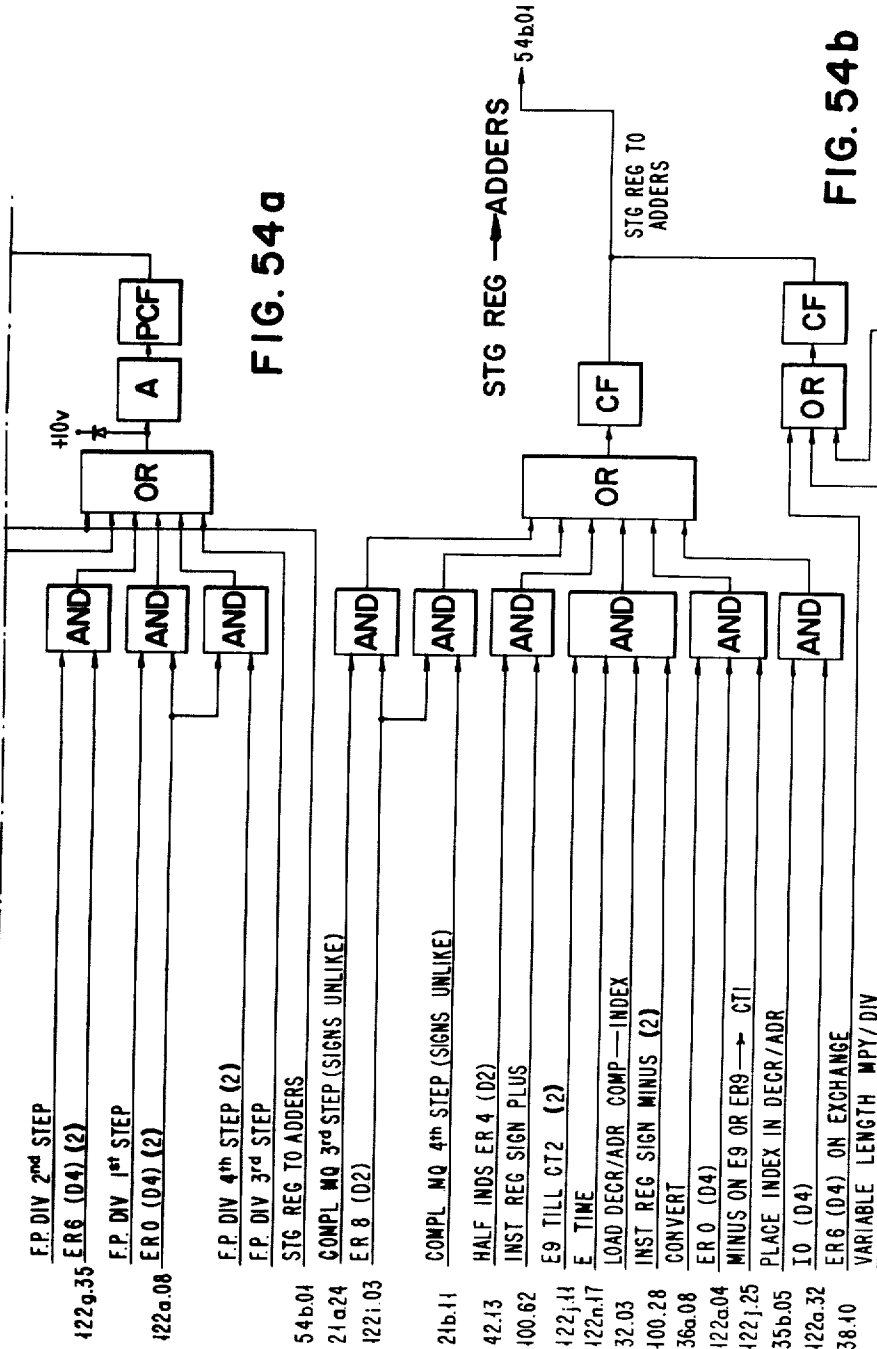
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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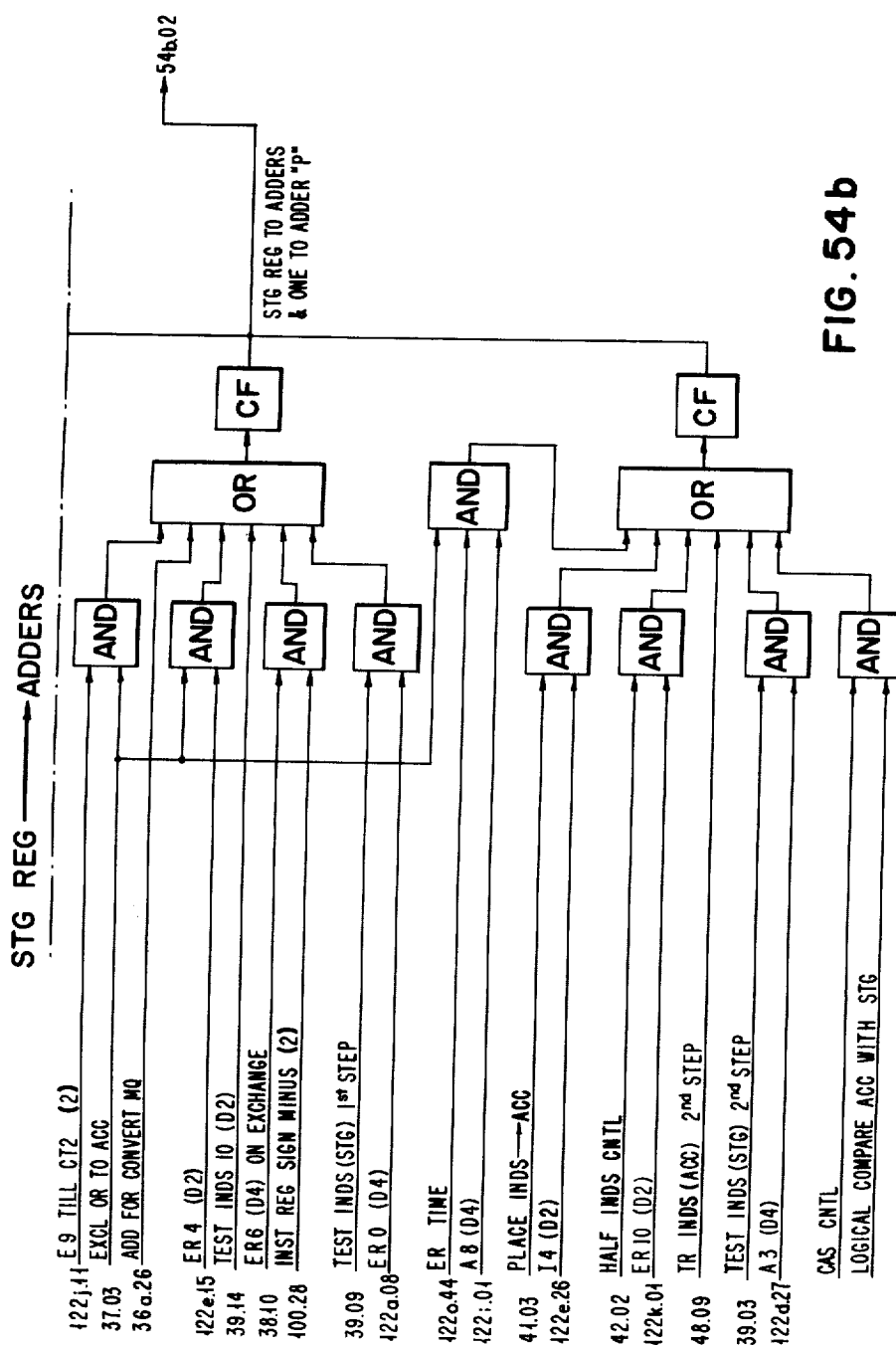
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STG REG (1-8) → ADDER & STG REG (9-35) → ADDER



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**FIG. 54b**

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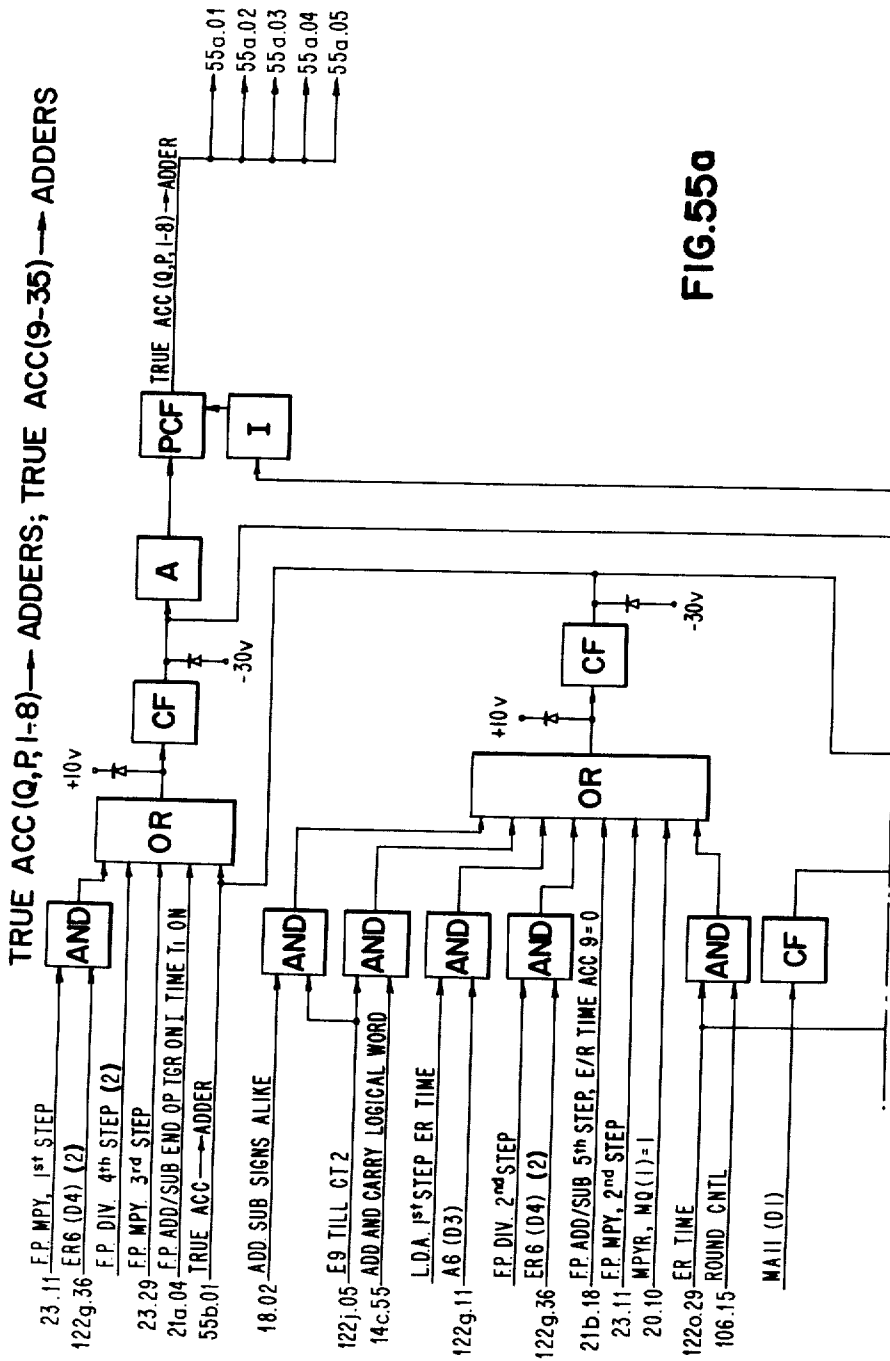


FIG. 55a

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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

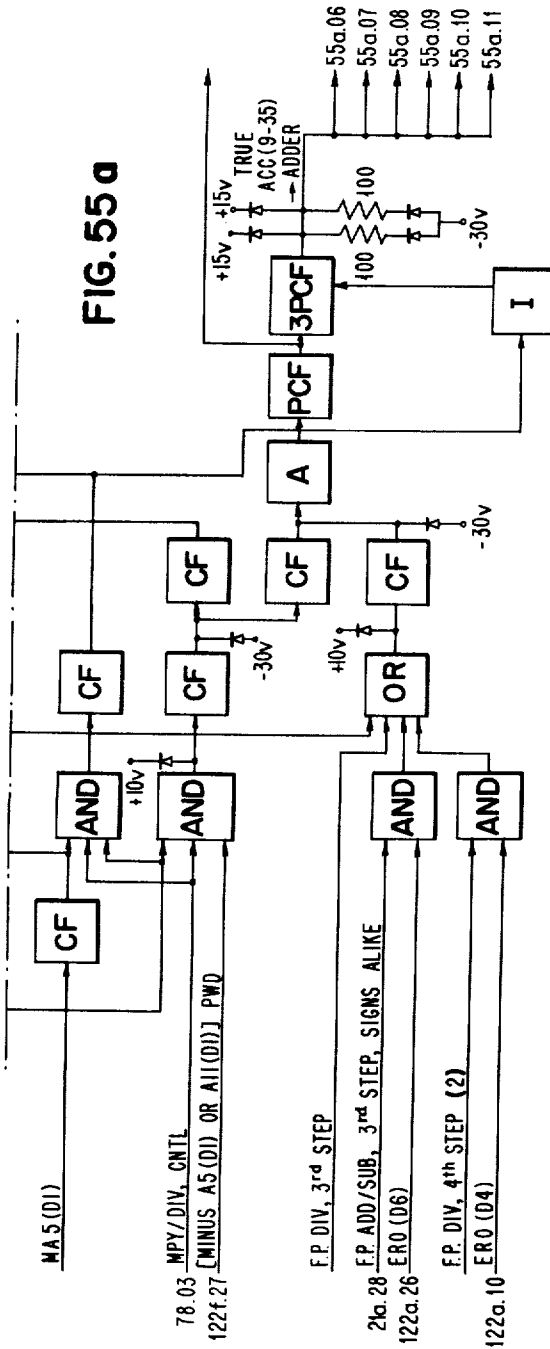
3,019,976

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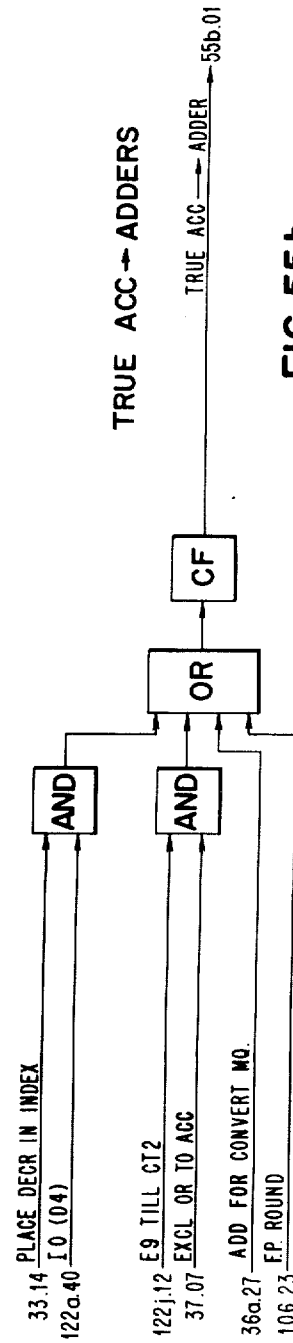
TRUE ACC(Q,P,I-8) → ADDERS; TRUE ACC(9-35) → ADDERS

FIG. 55a



TRUE ACC → ADDERS

FIG. 55b



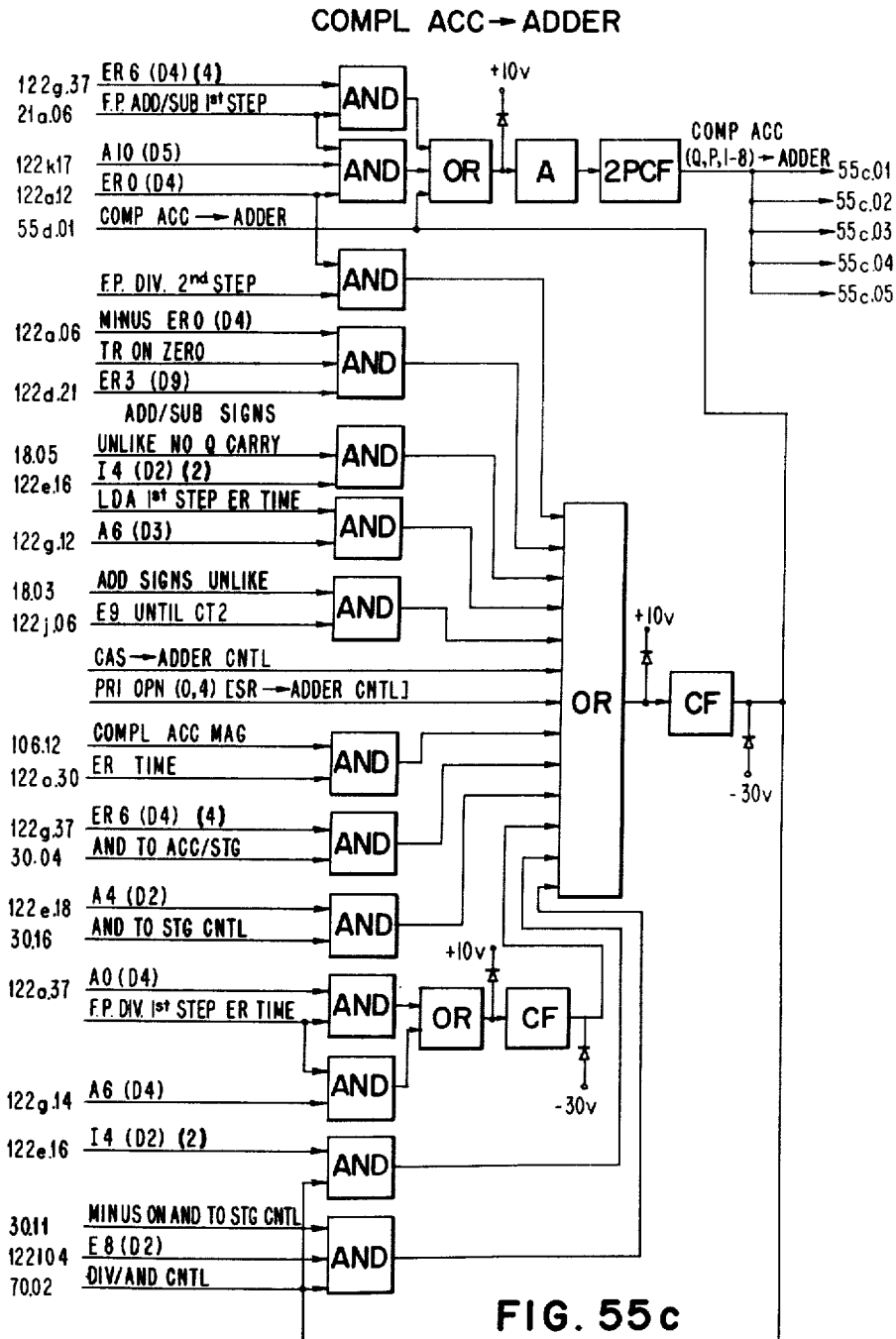
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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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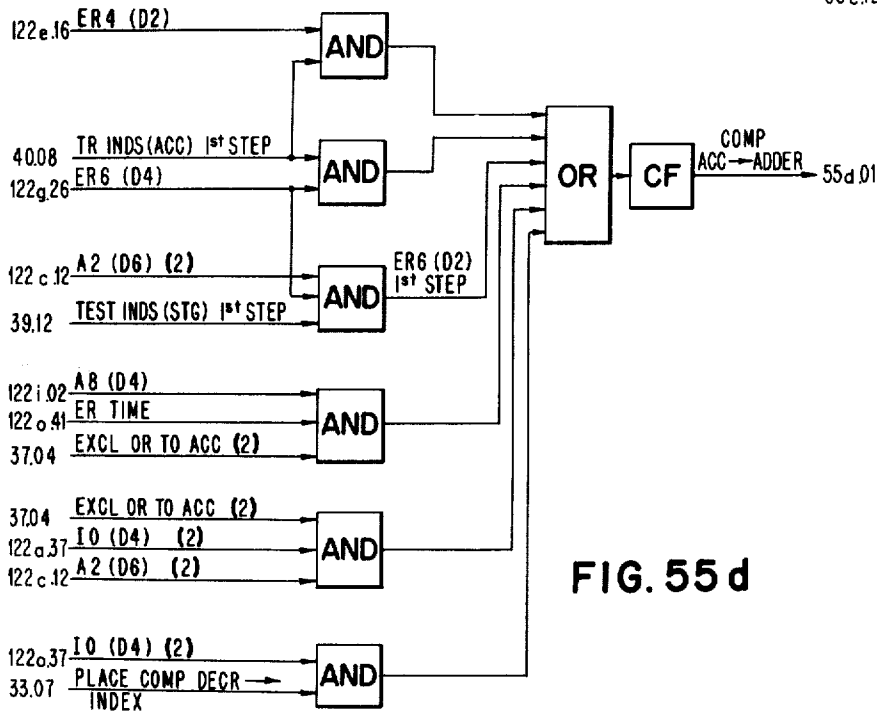
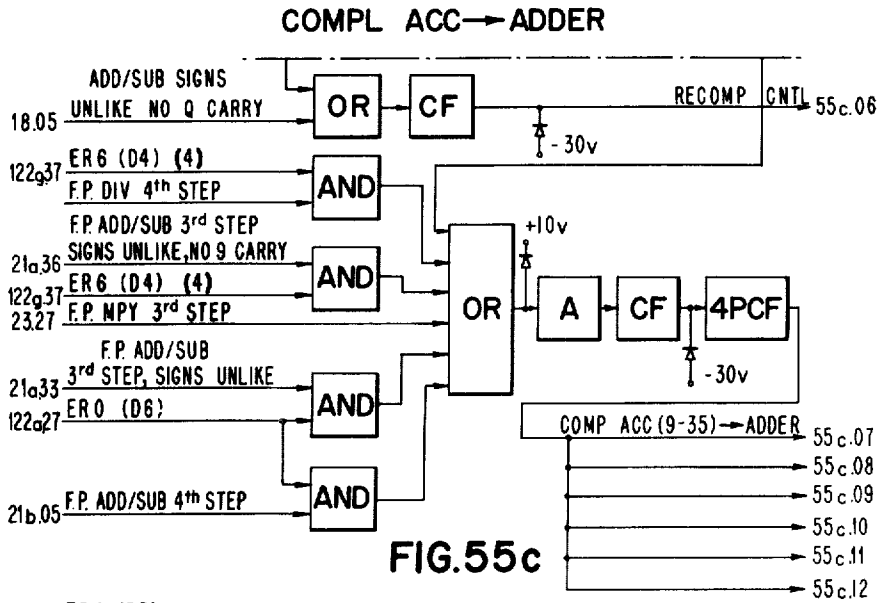
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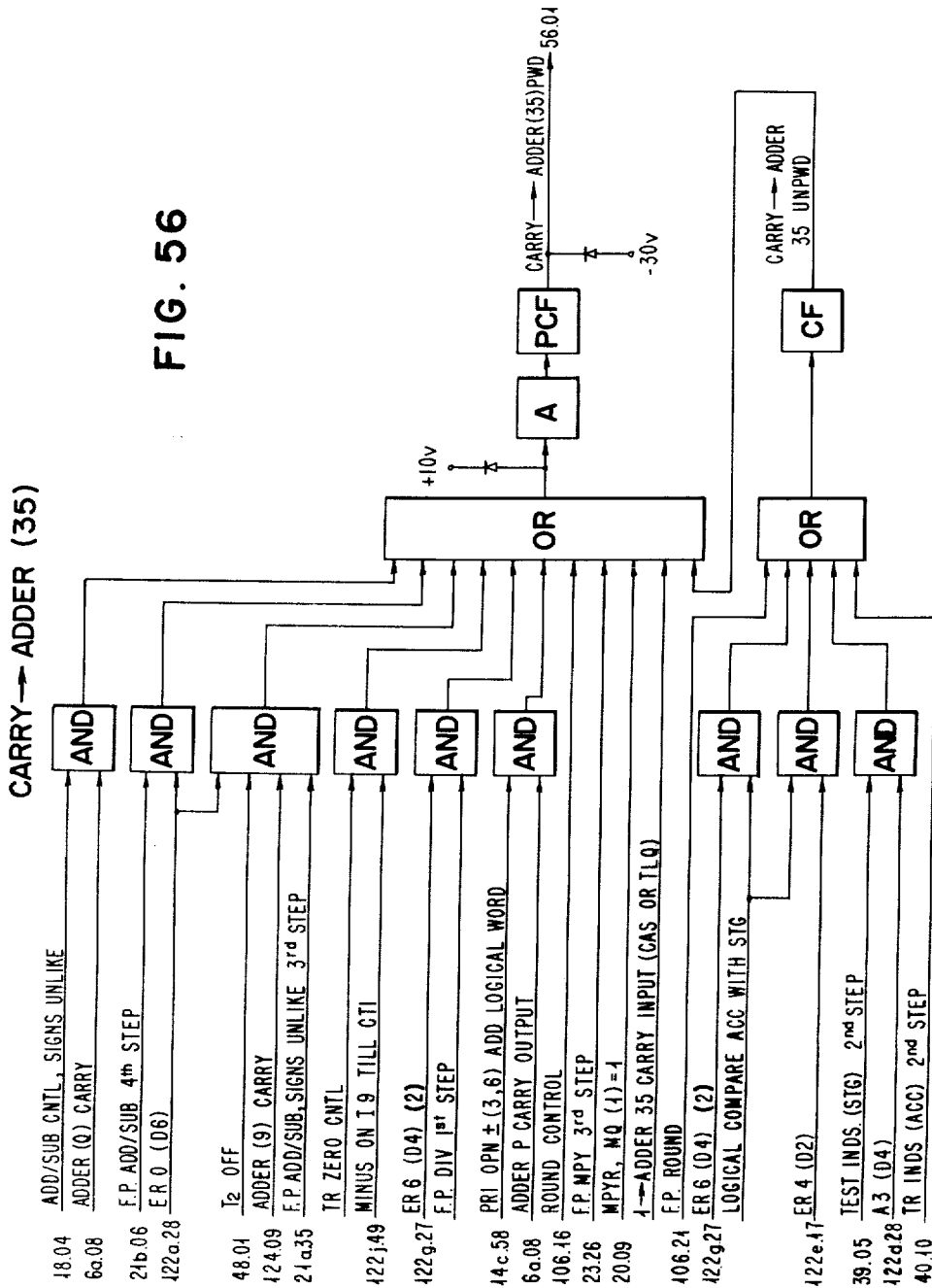
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FIG. 56



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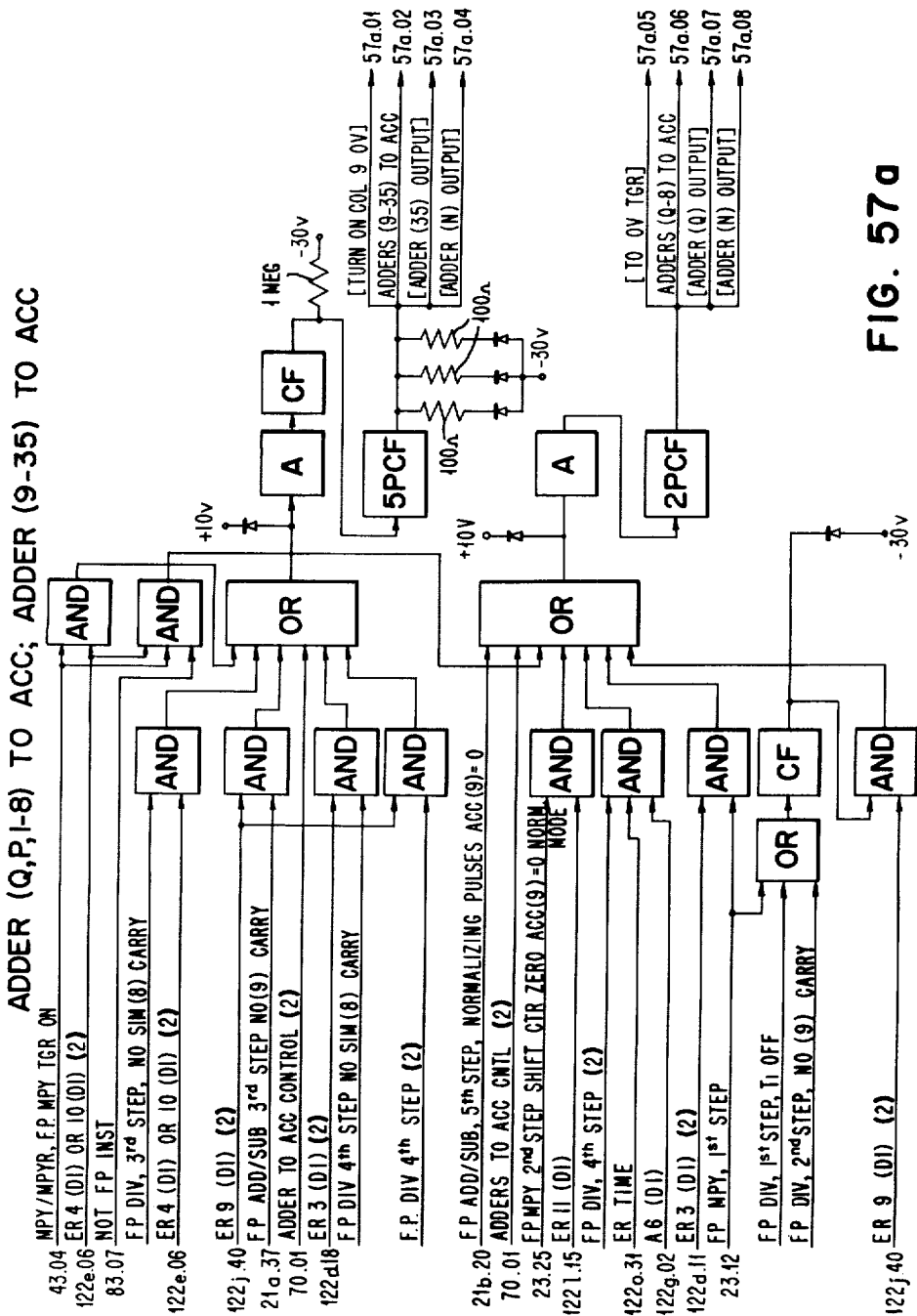


FIG. 57a

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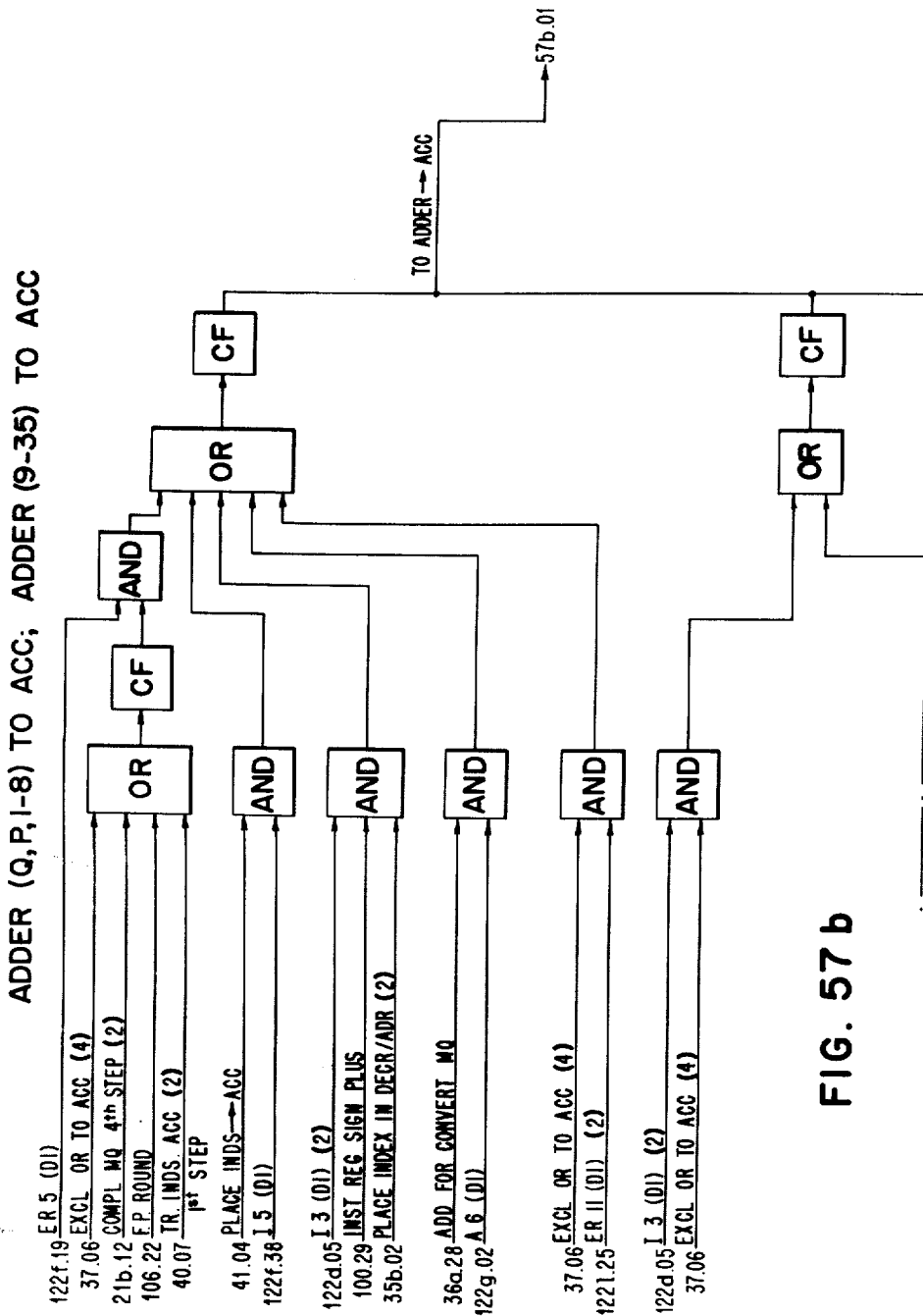


FIG. 57b

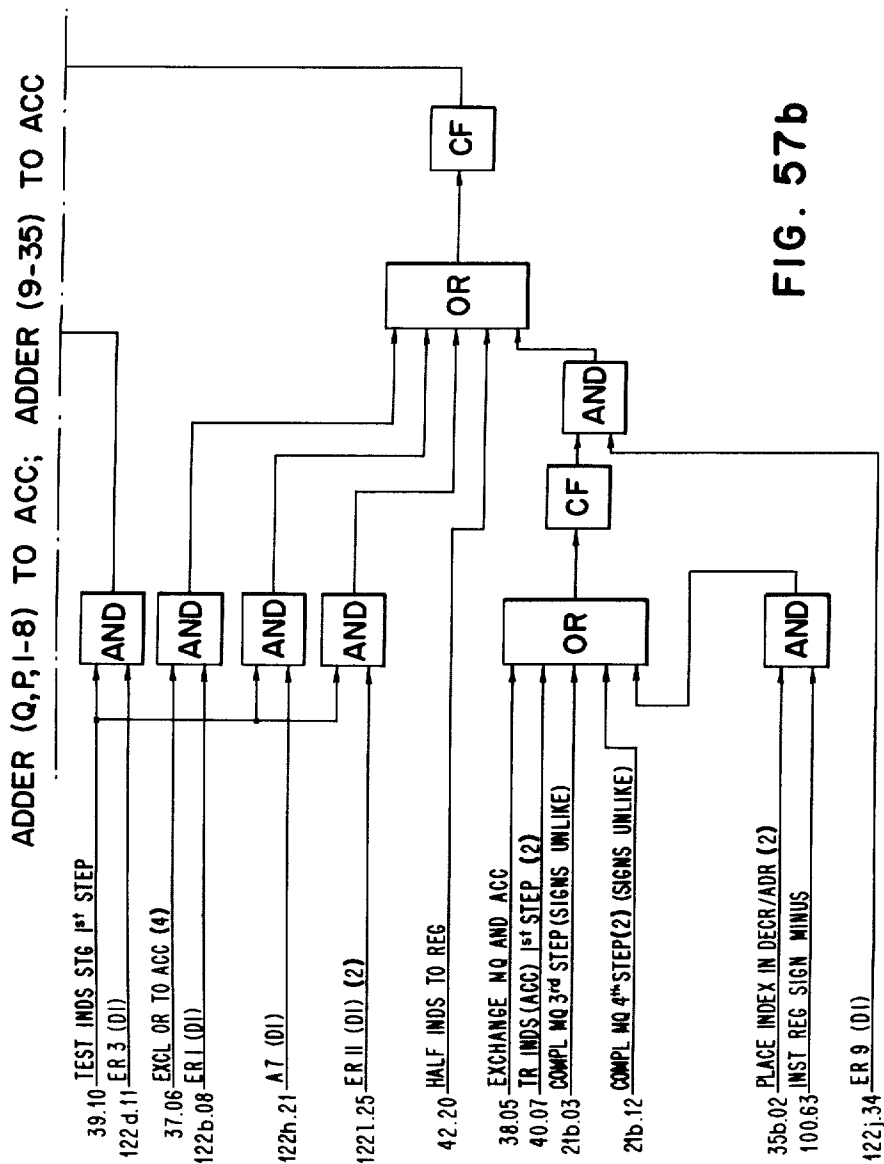
Feb. 6, 1962

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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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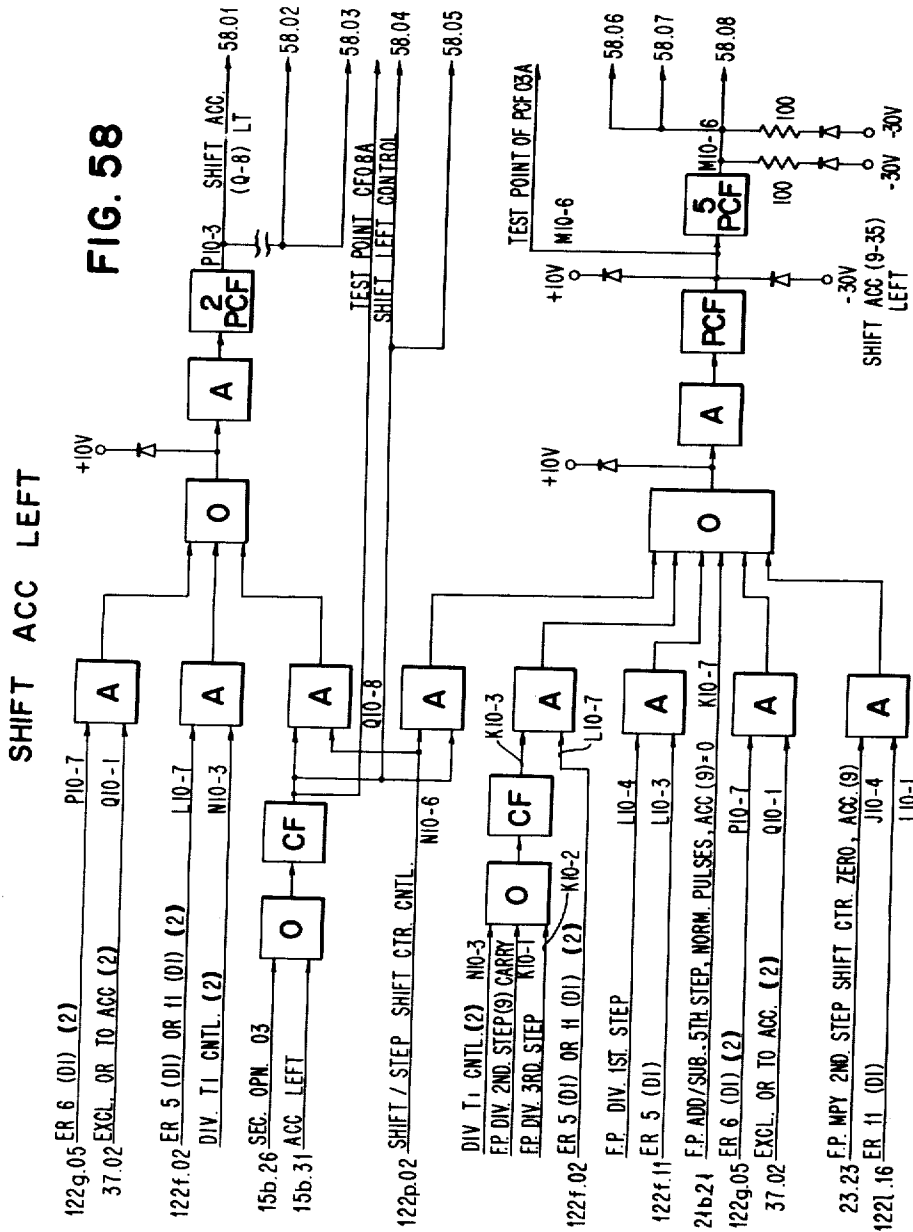
Feb. 6, 1962

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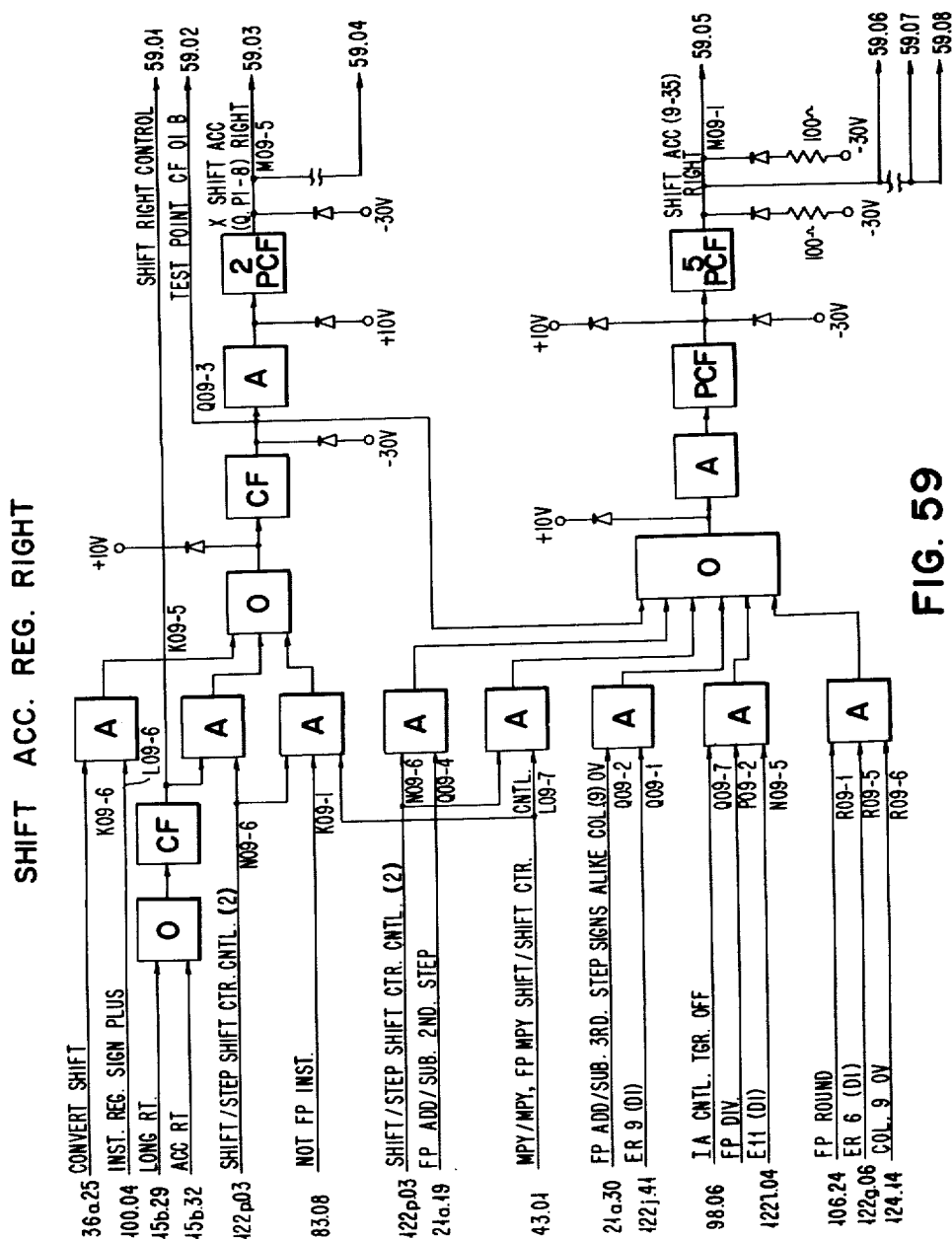
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**FIG. 59**

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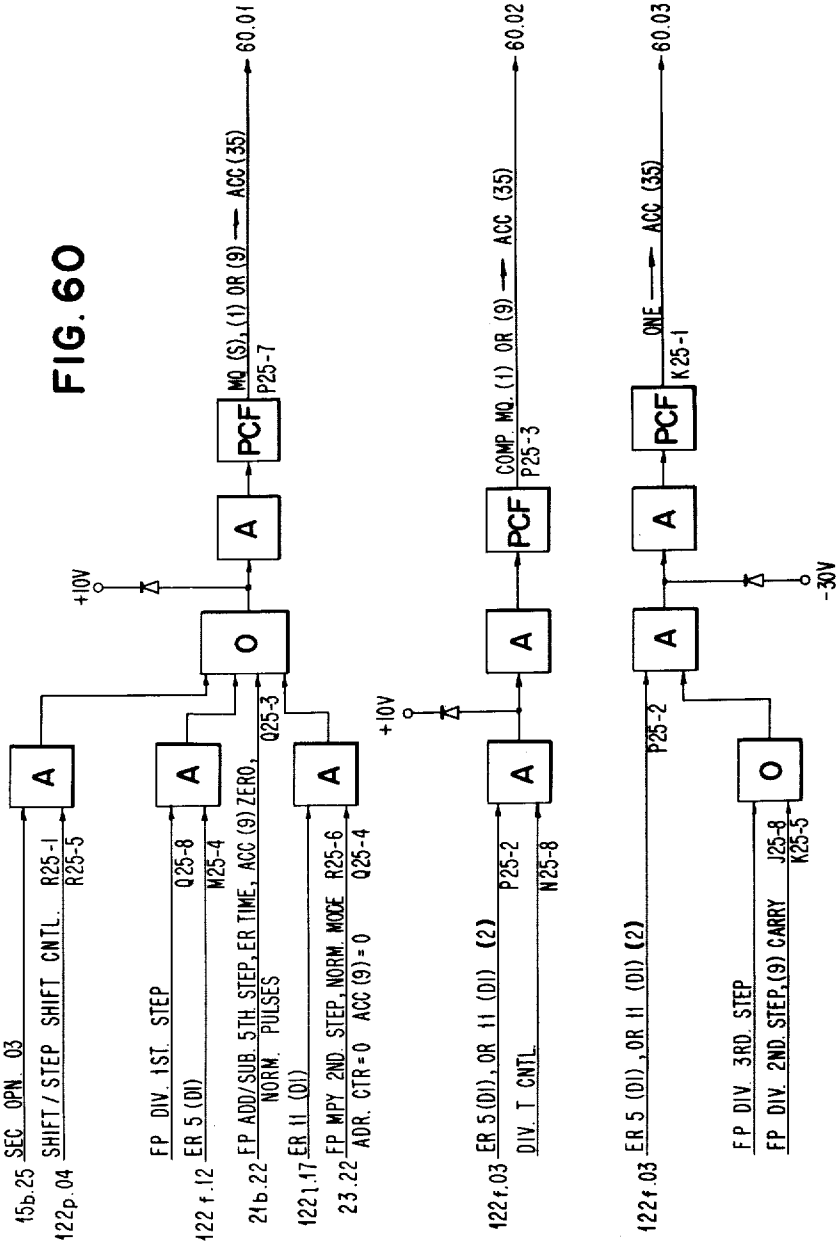
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MQ (S), (1) OR(9) TO ACC. (35), 1 TO ACC. (35)

FIG. 60



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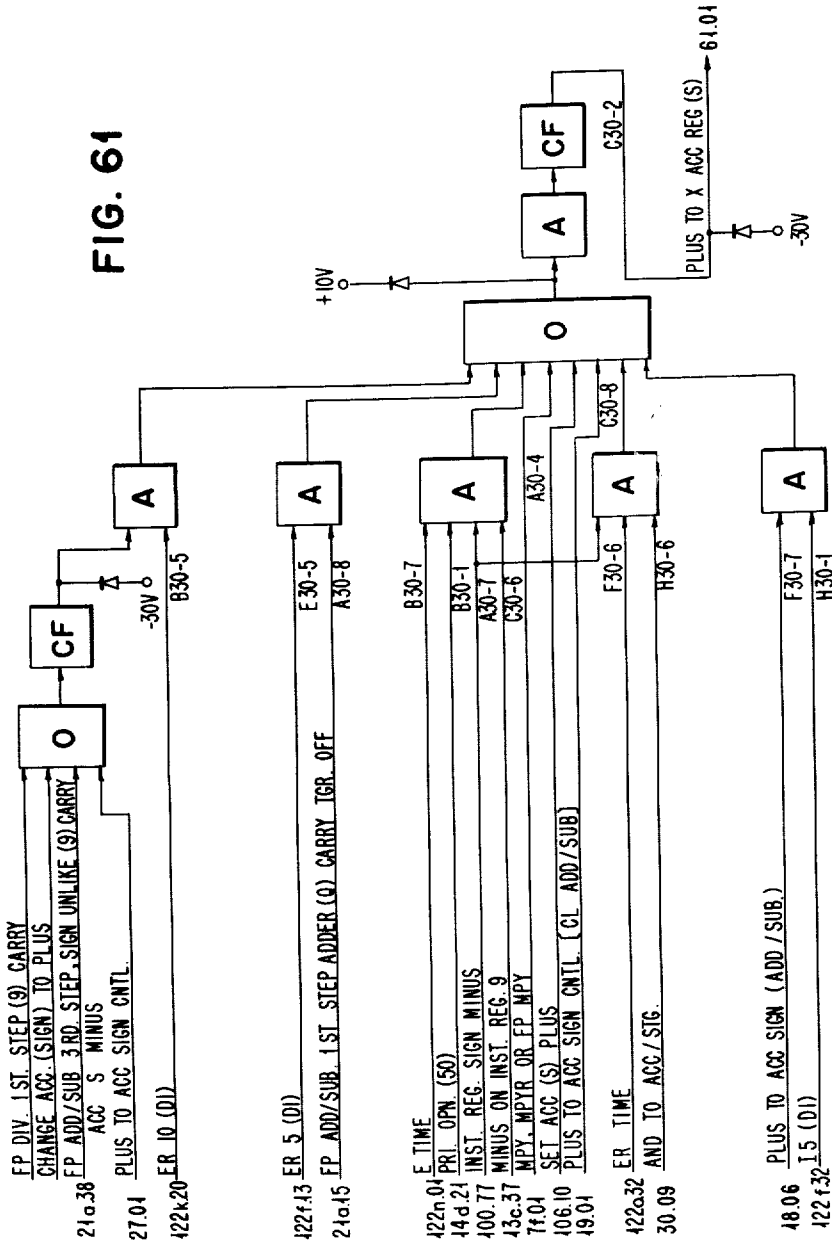
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PLUS TO ACC. REG. (S)



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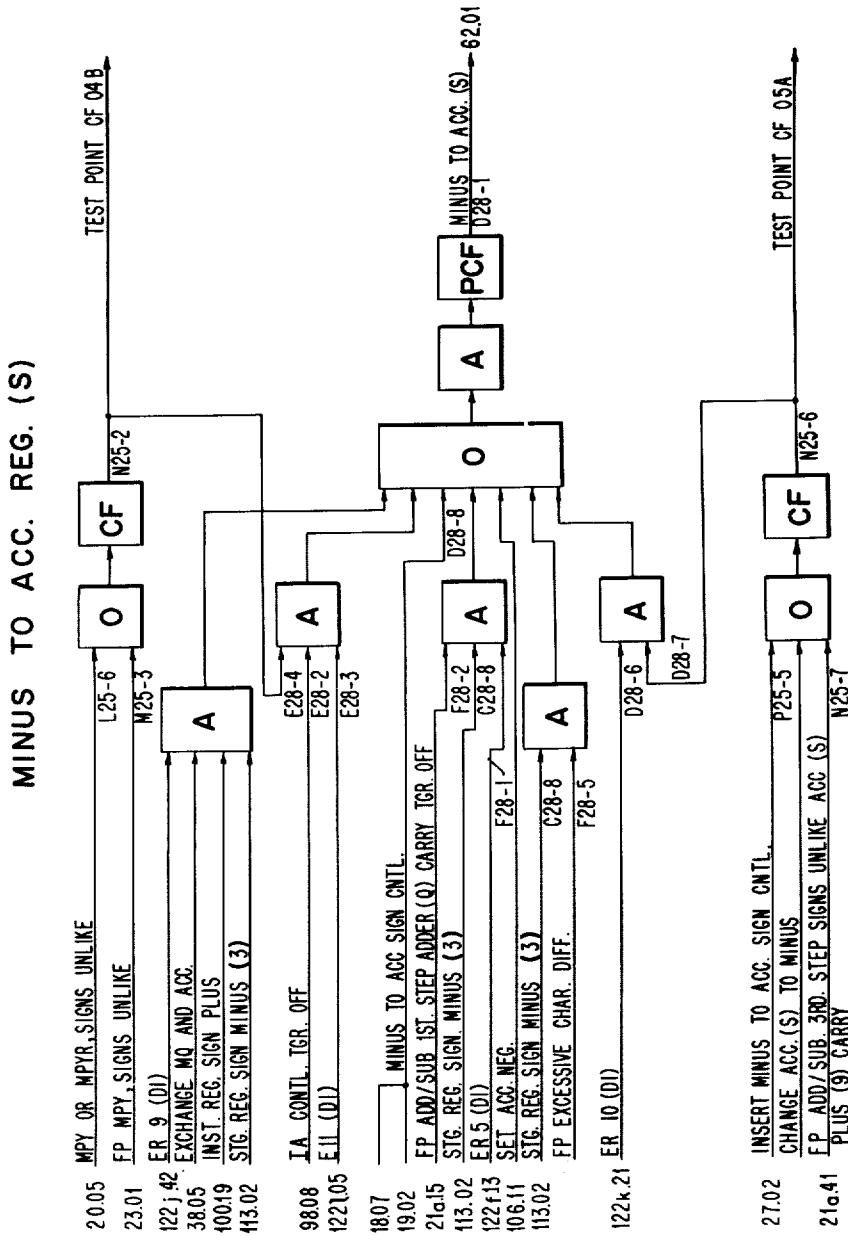


FIG. 62

Feb. 6, 1962

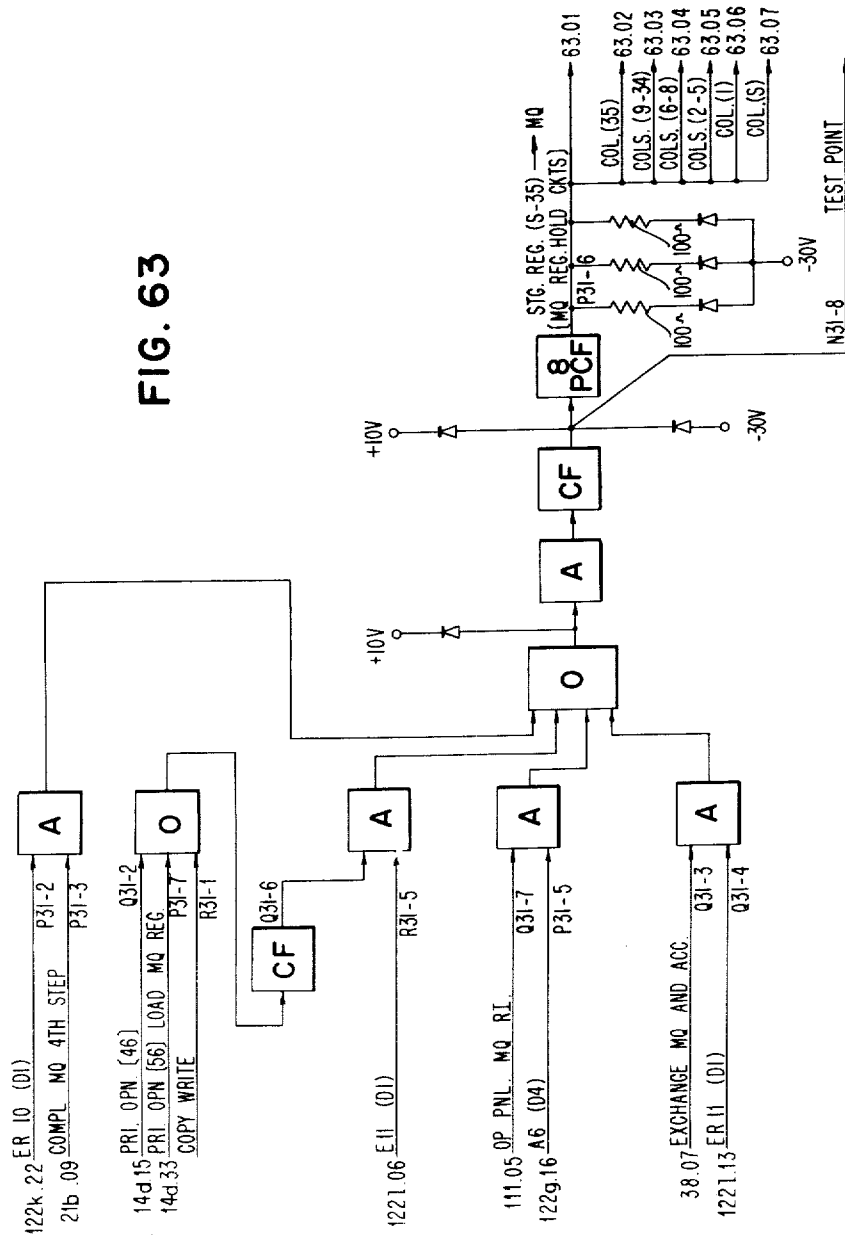
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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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STG. REG. (S-35) → MQ REG.



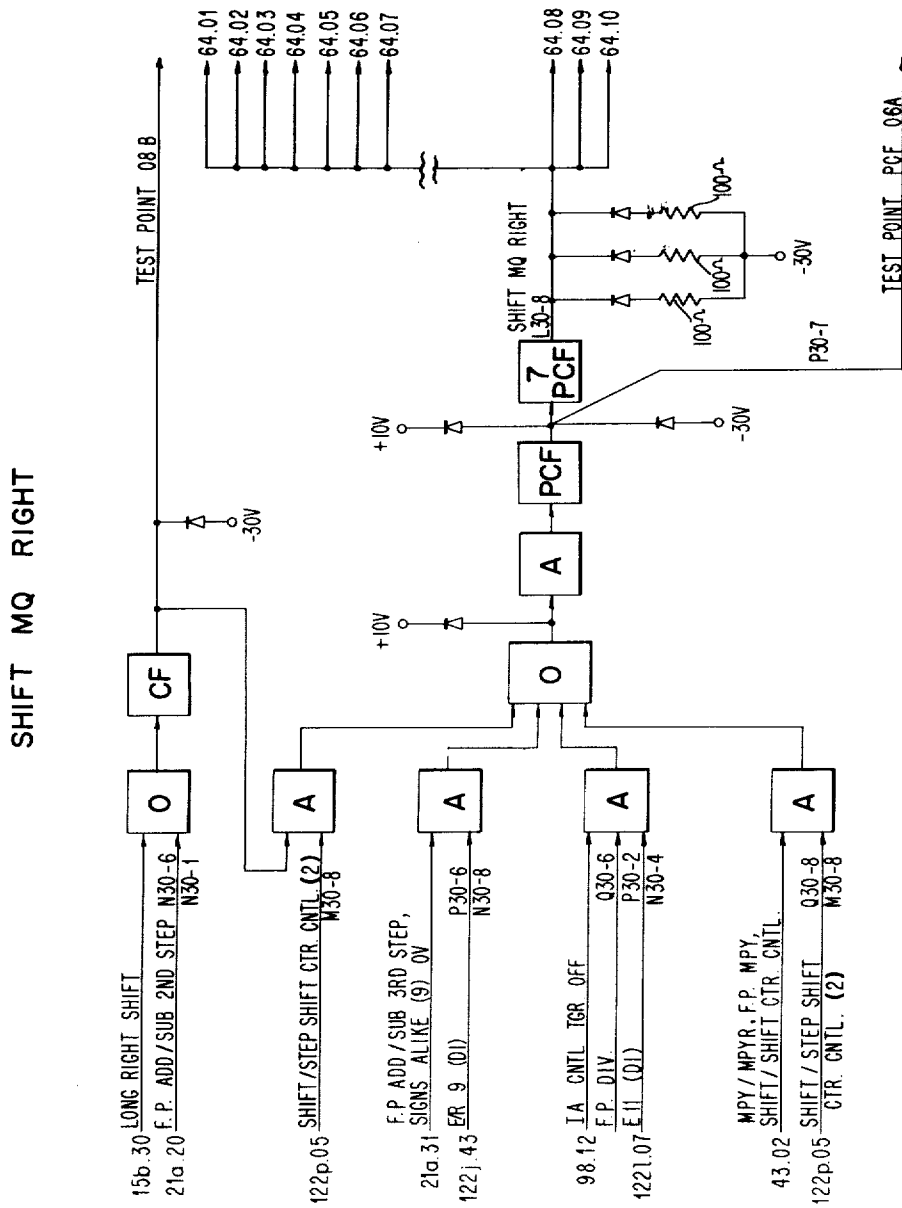
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AN INDICATING REGISTER

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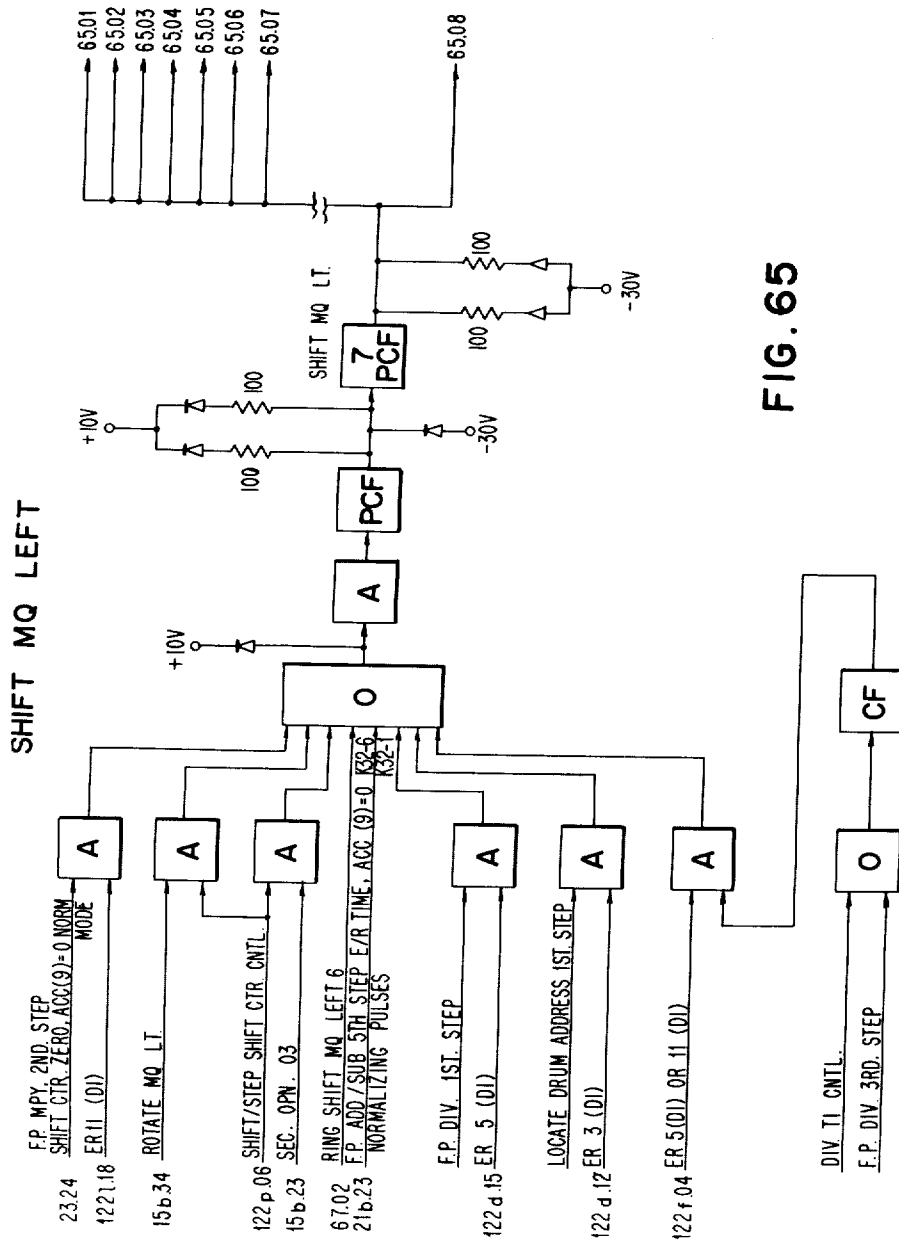
Filed Dec. 26, 1957

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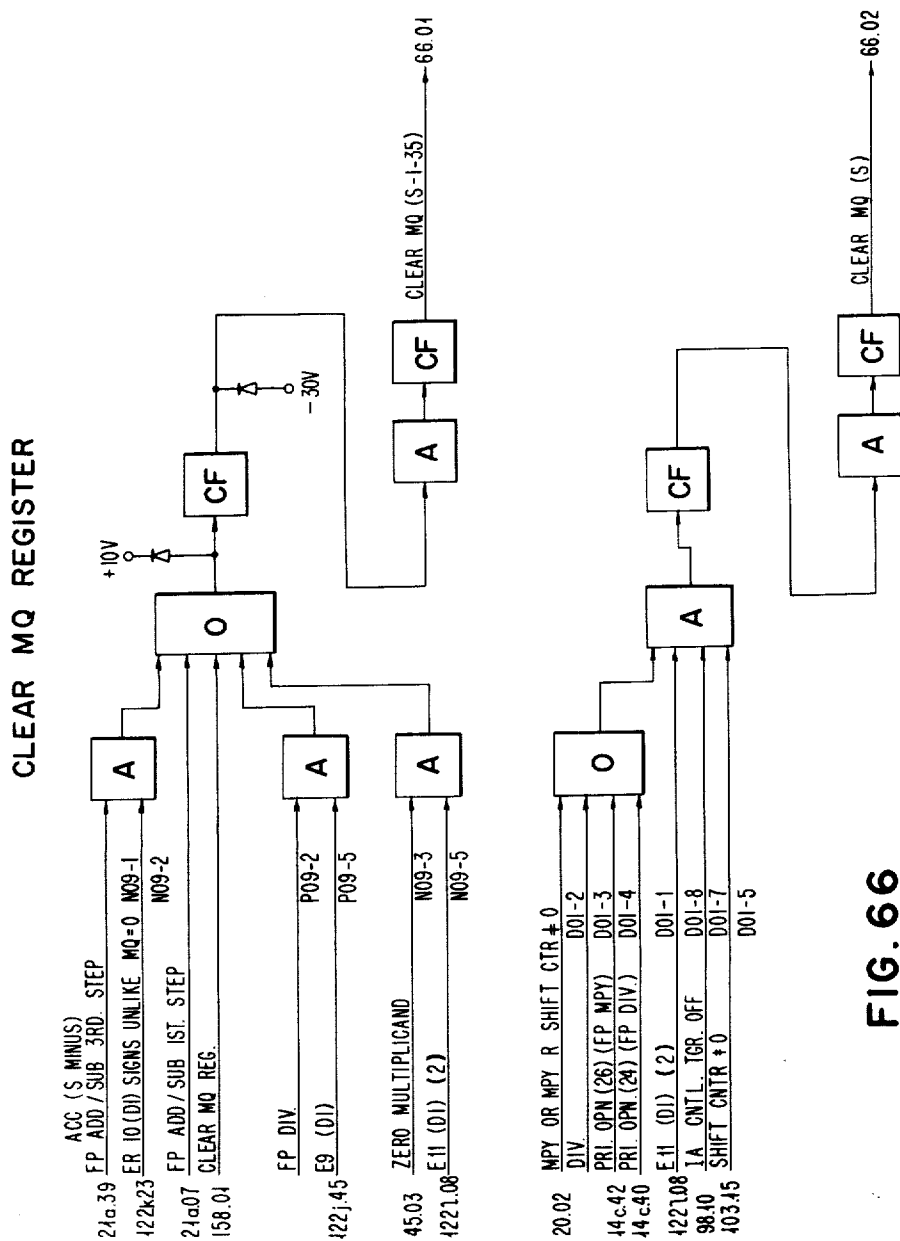


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**FIG. 65**



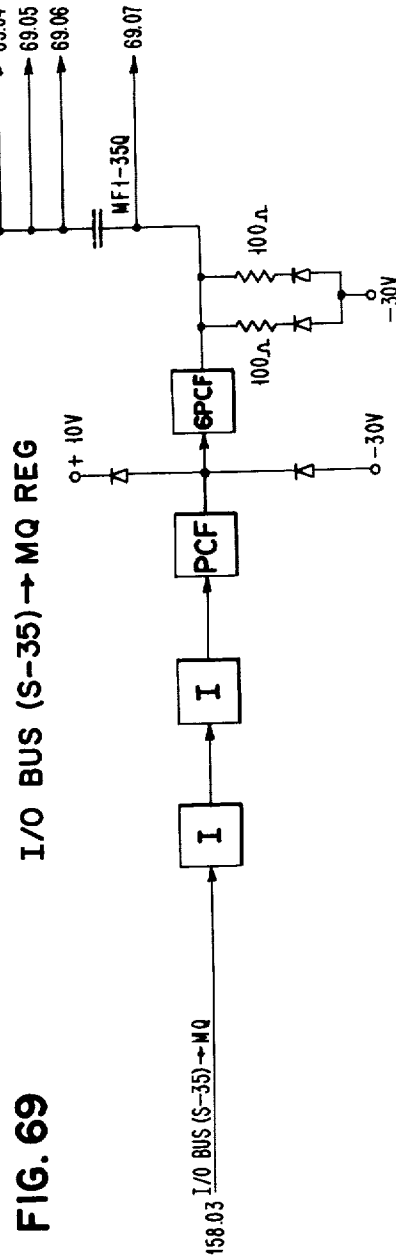
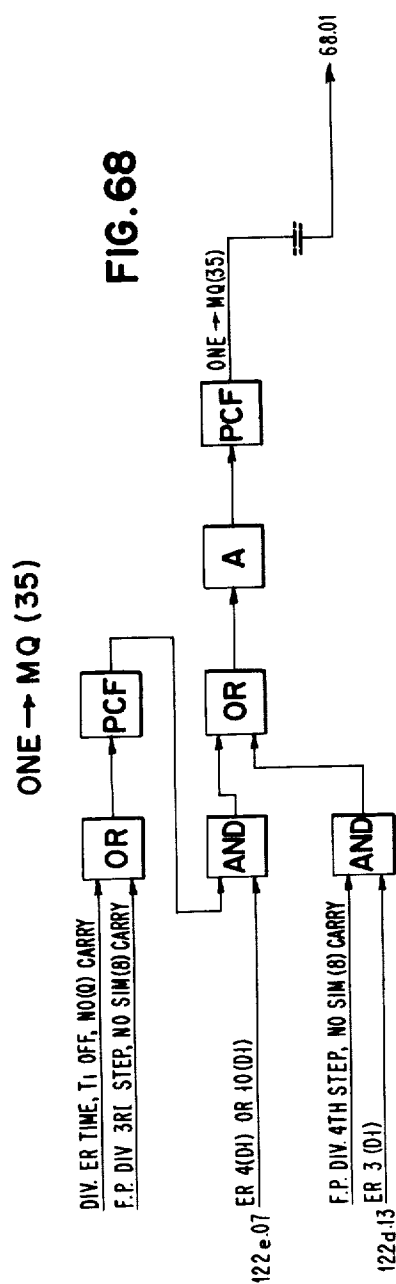
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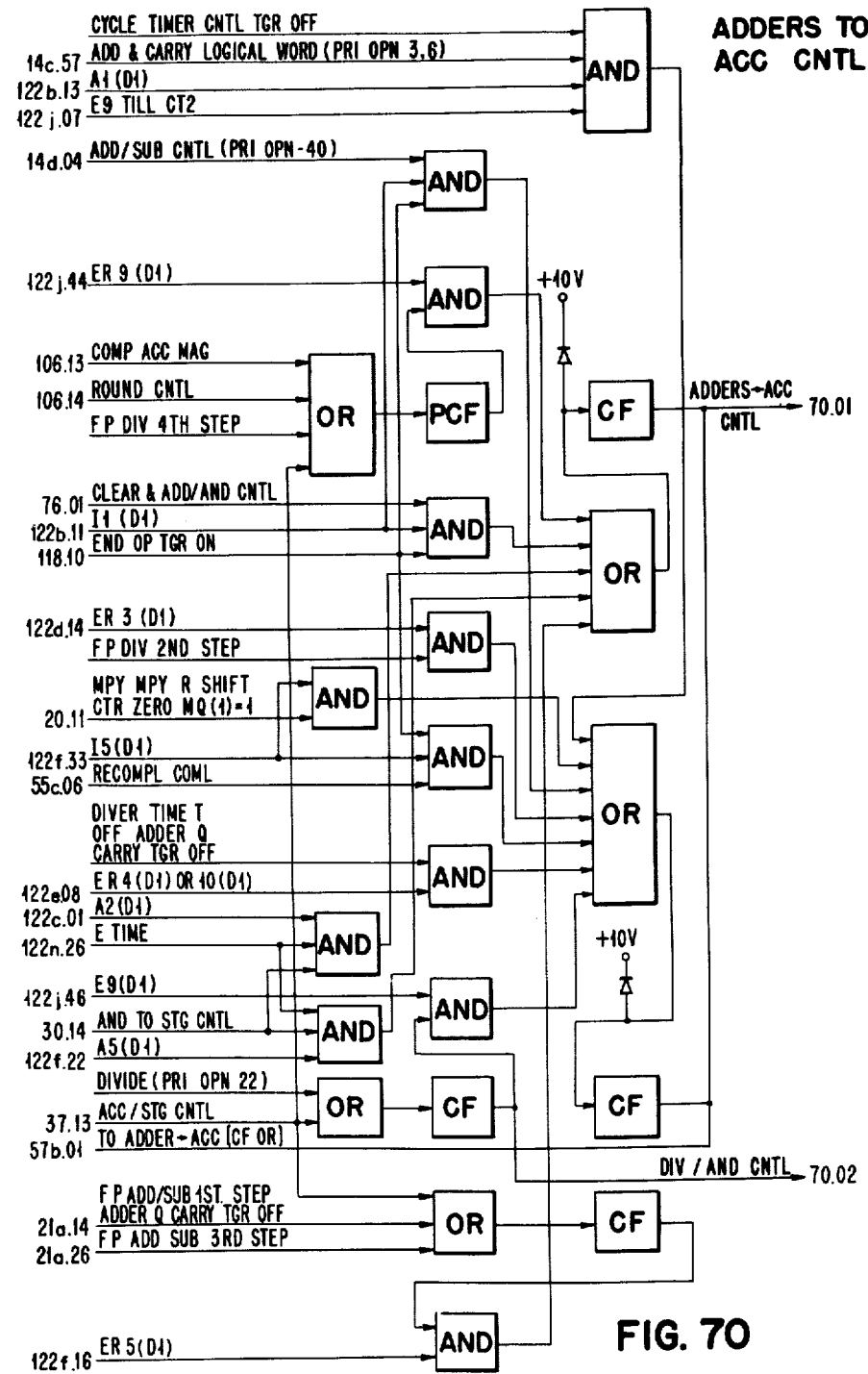


FIG. 70

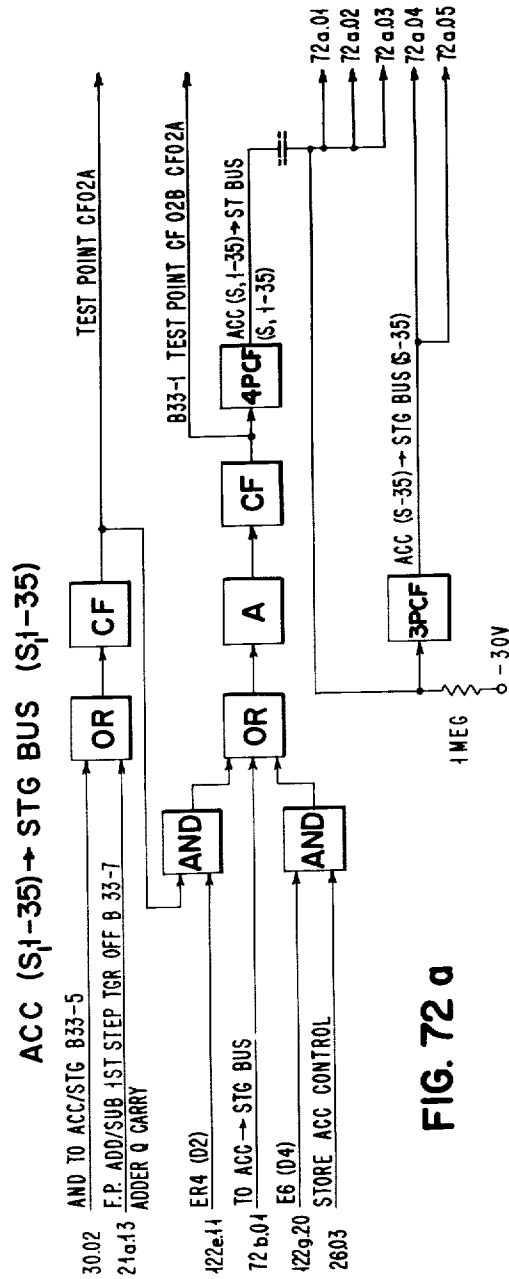
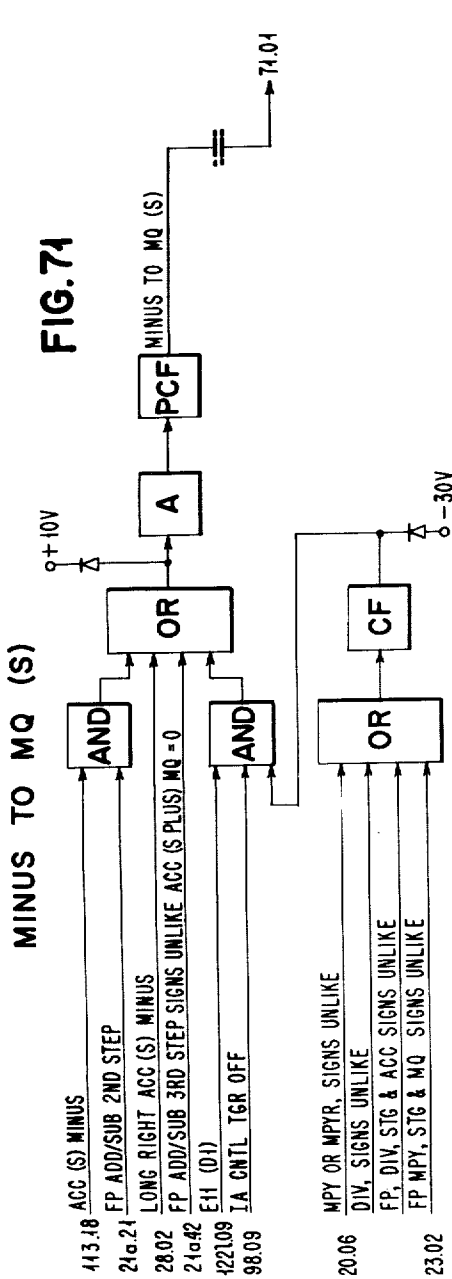
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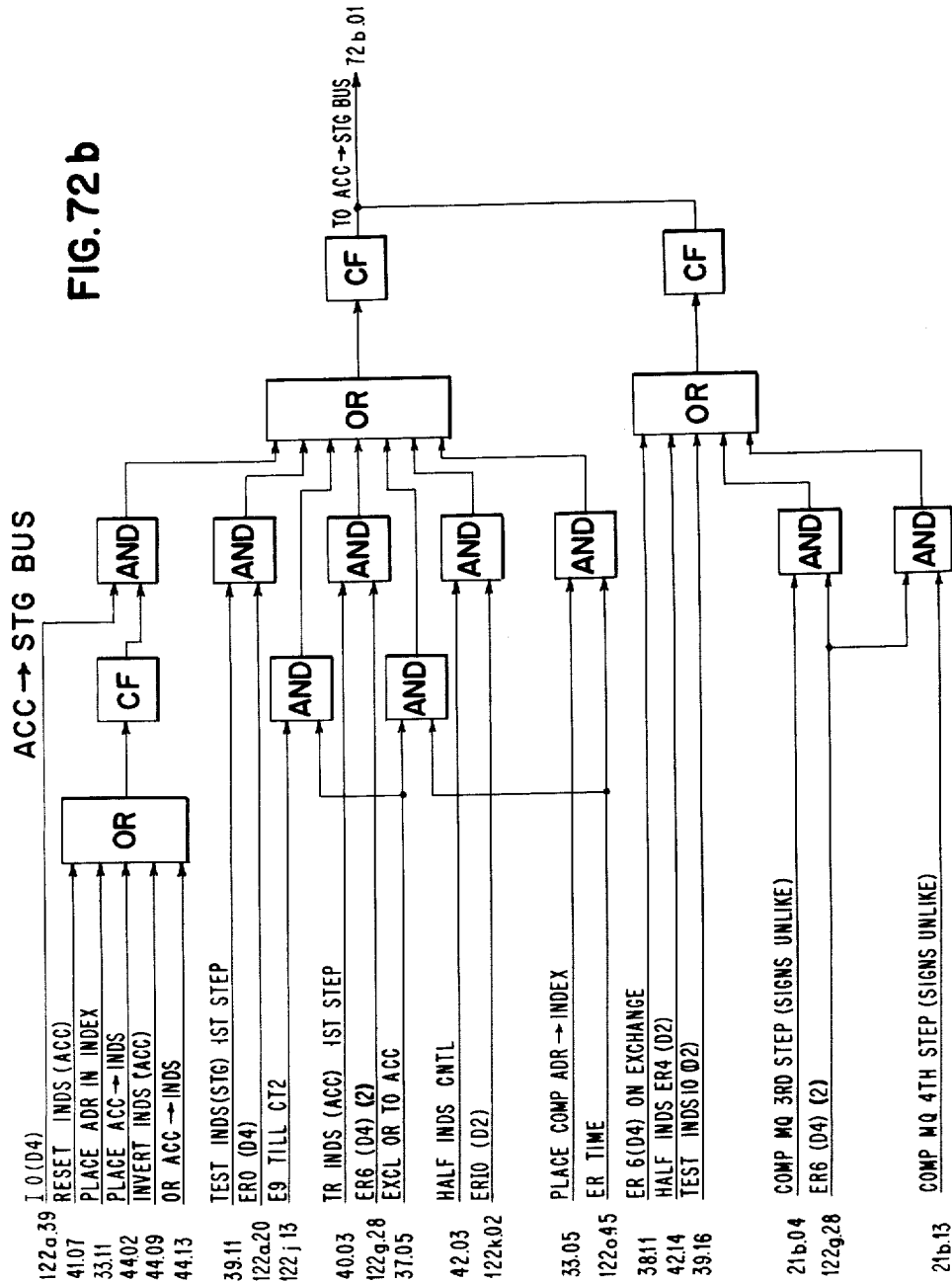
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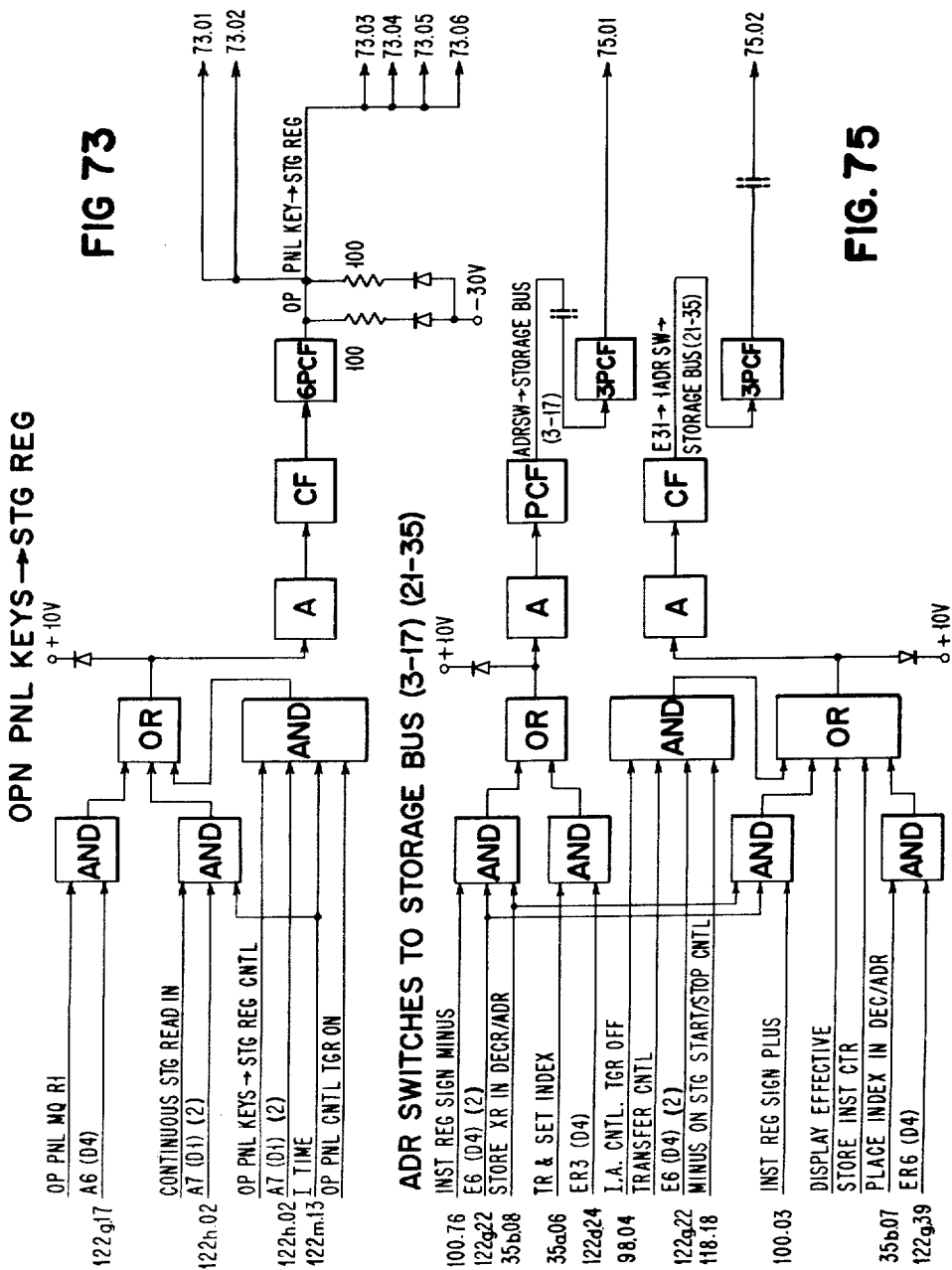
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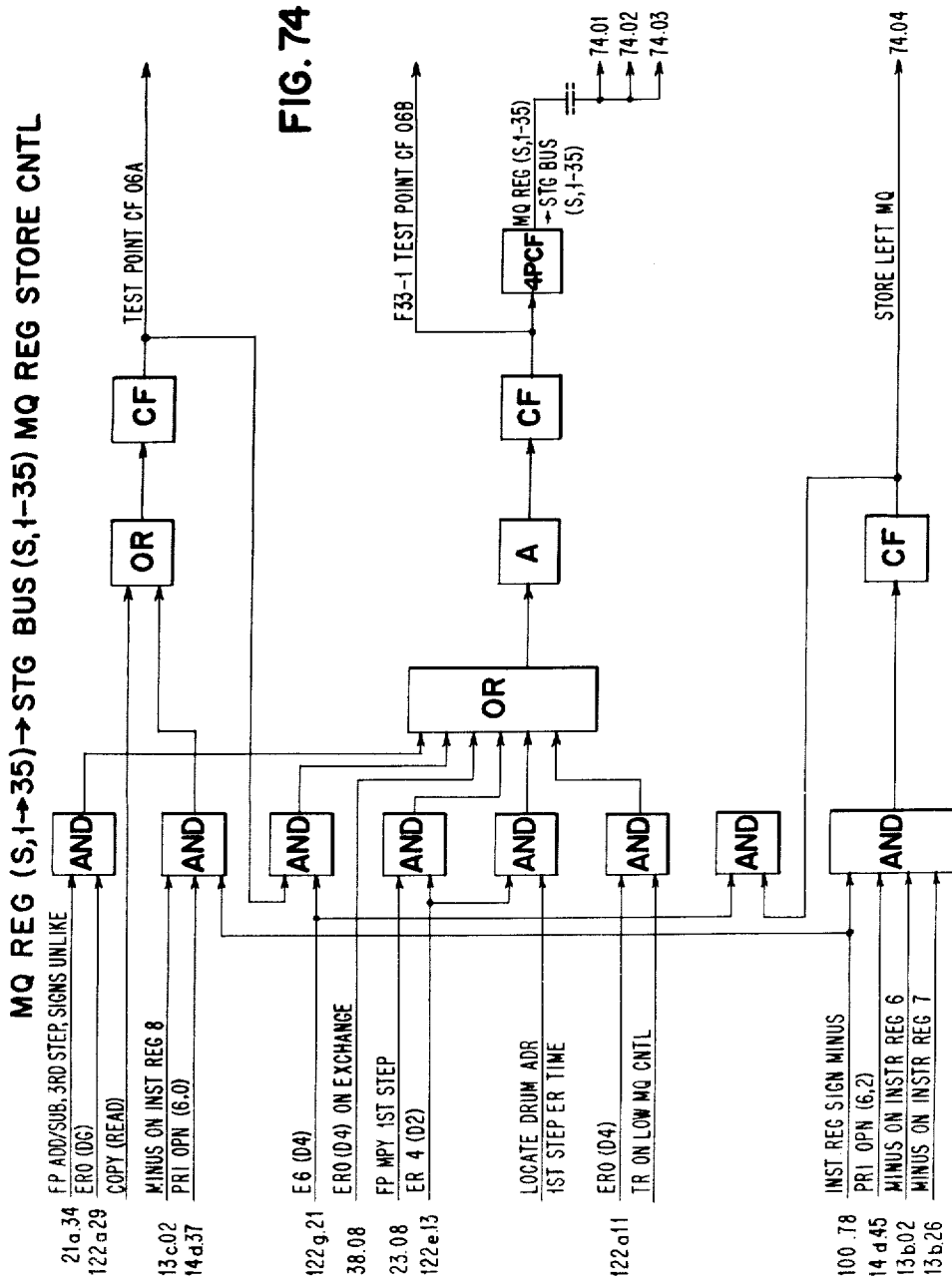
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FIG. 76  
CLEAR AND ADD/AND CNTL

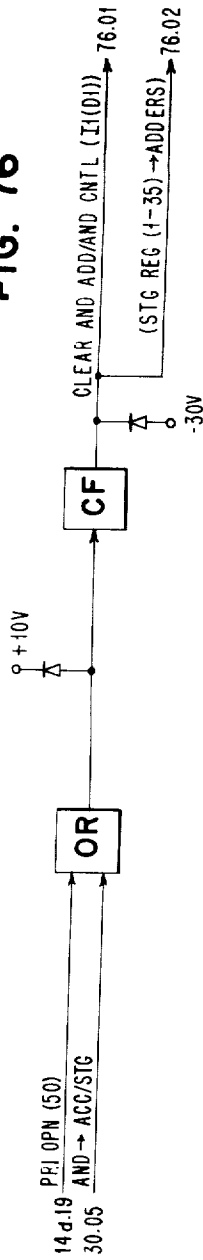
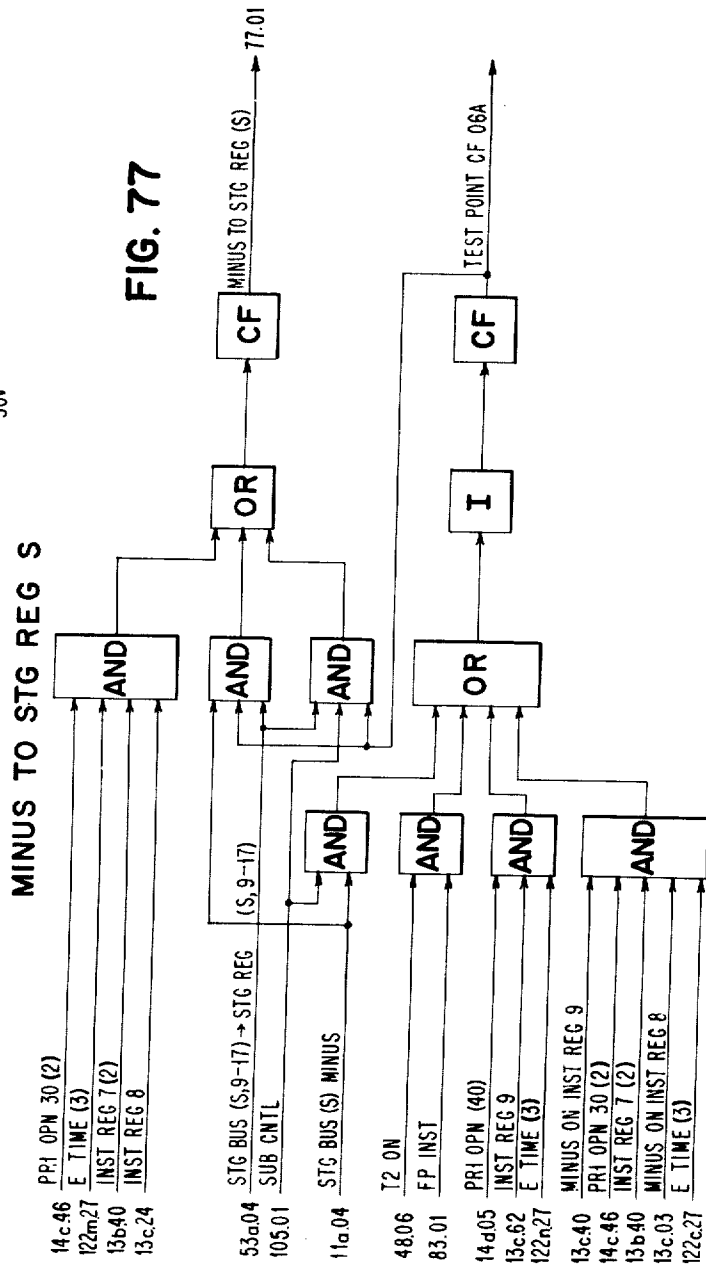


FIG. 77



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FIG. 78

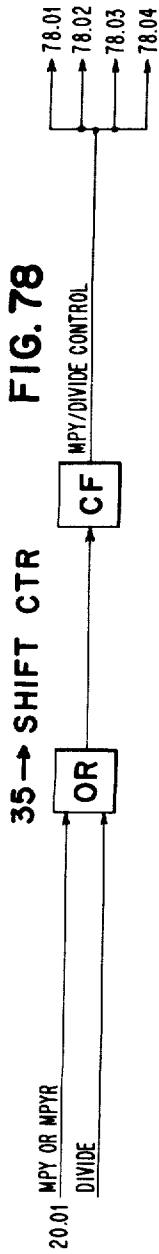
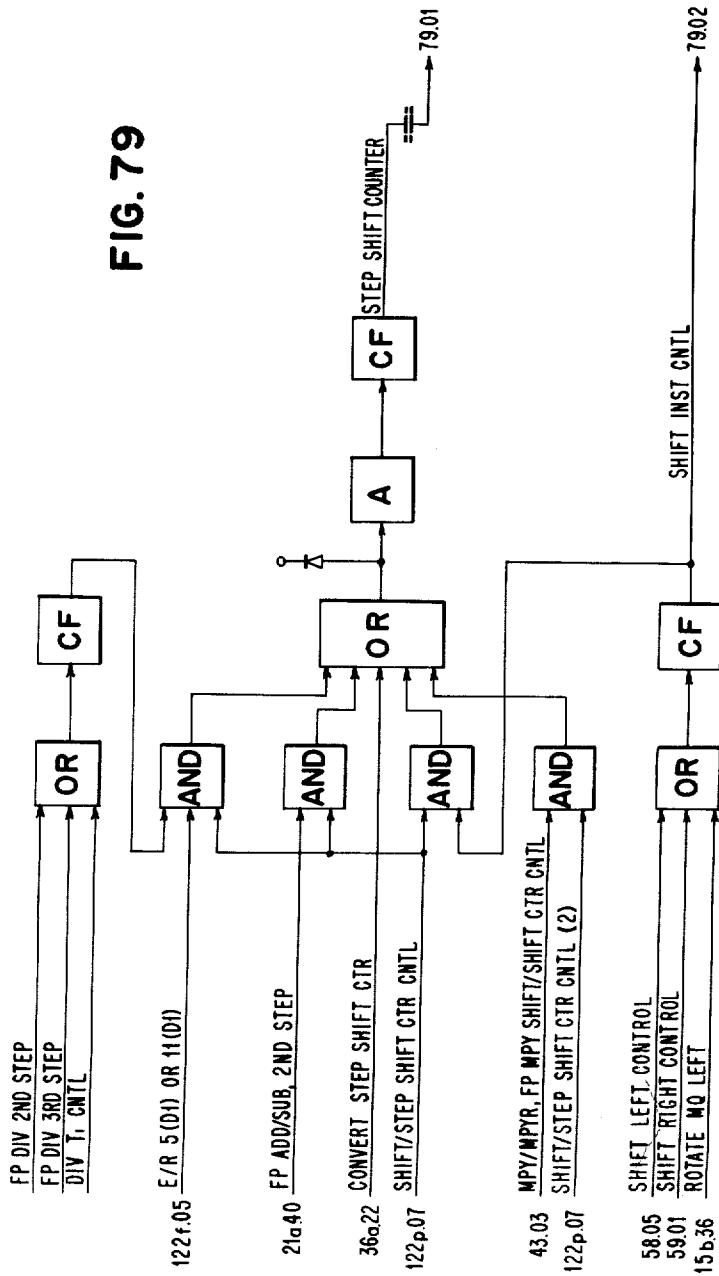


FIG. 79

STEP SHIFT COUNTER



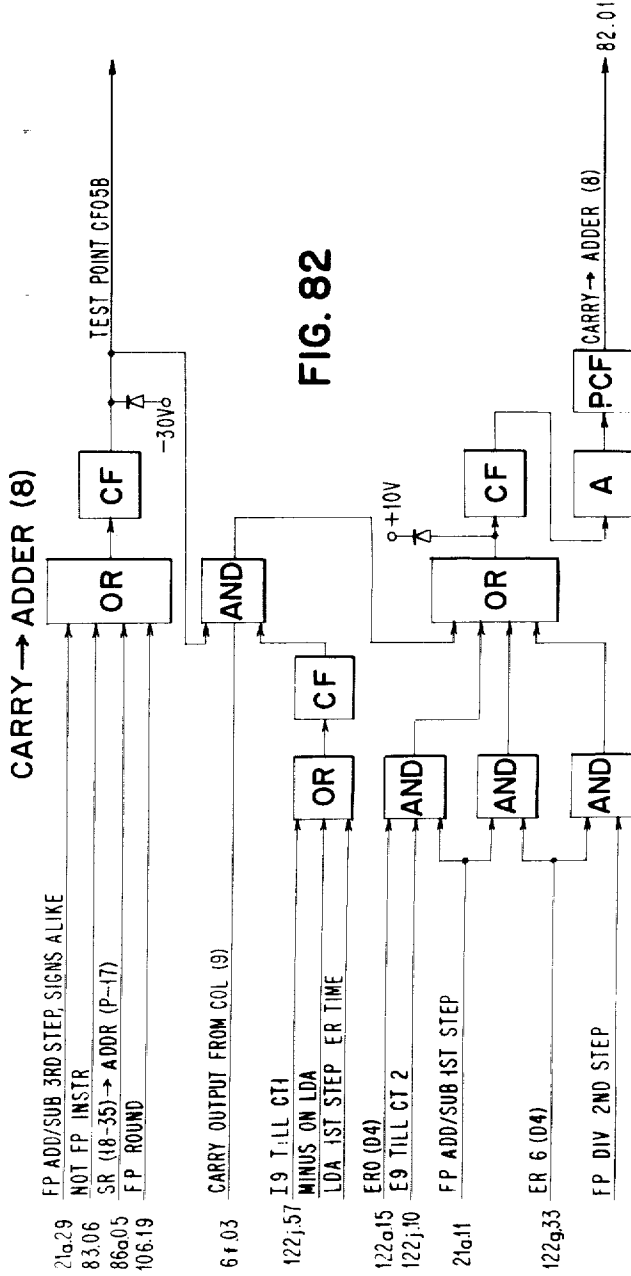
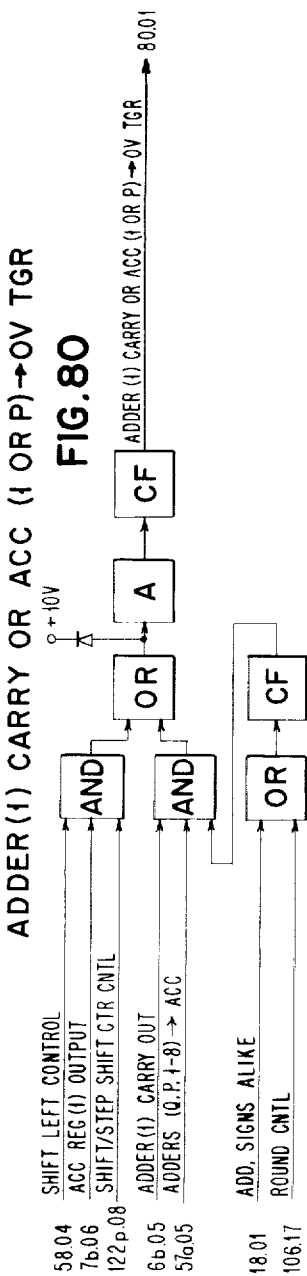
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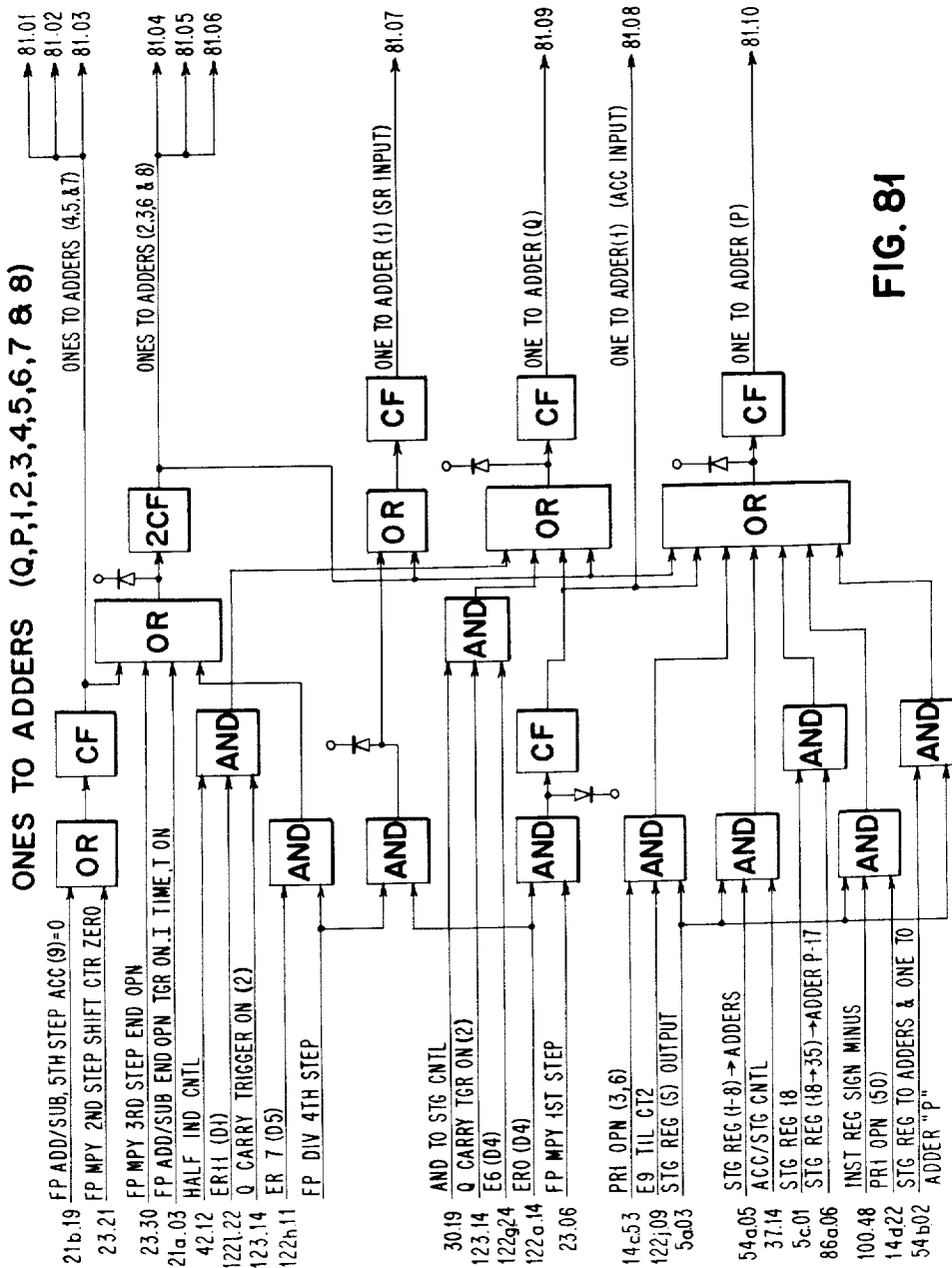
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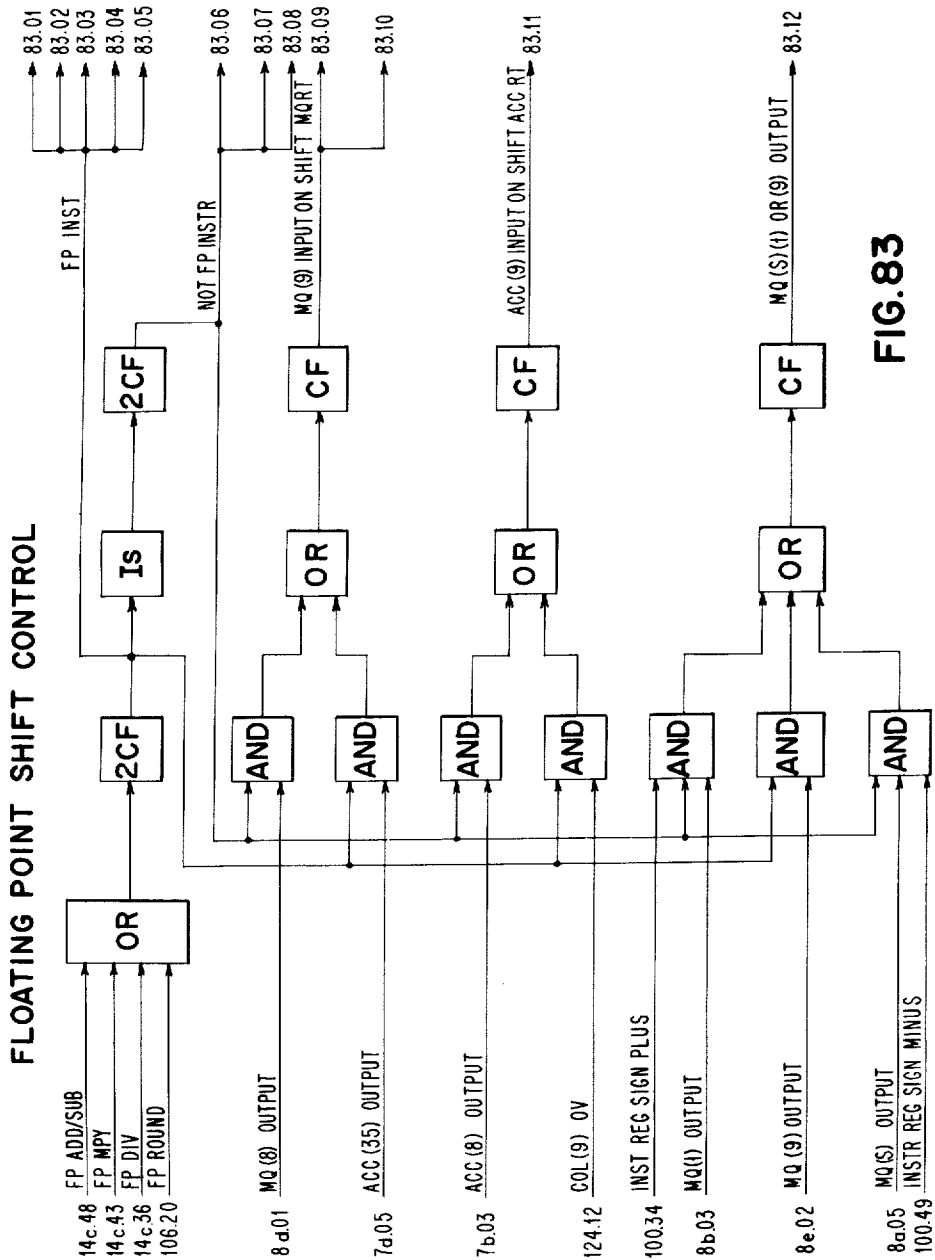


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**FIG. 81**



**FIG. 83**

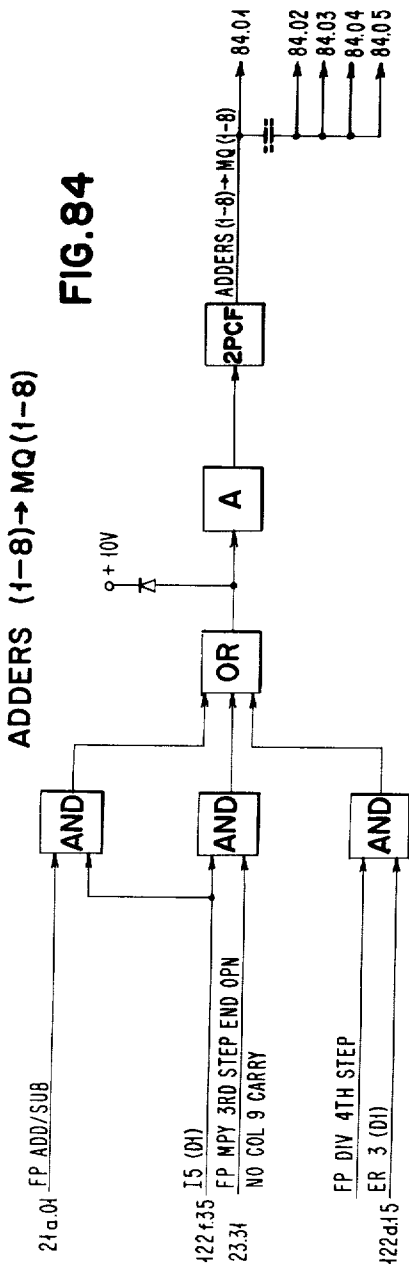
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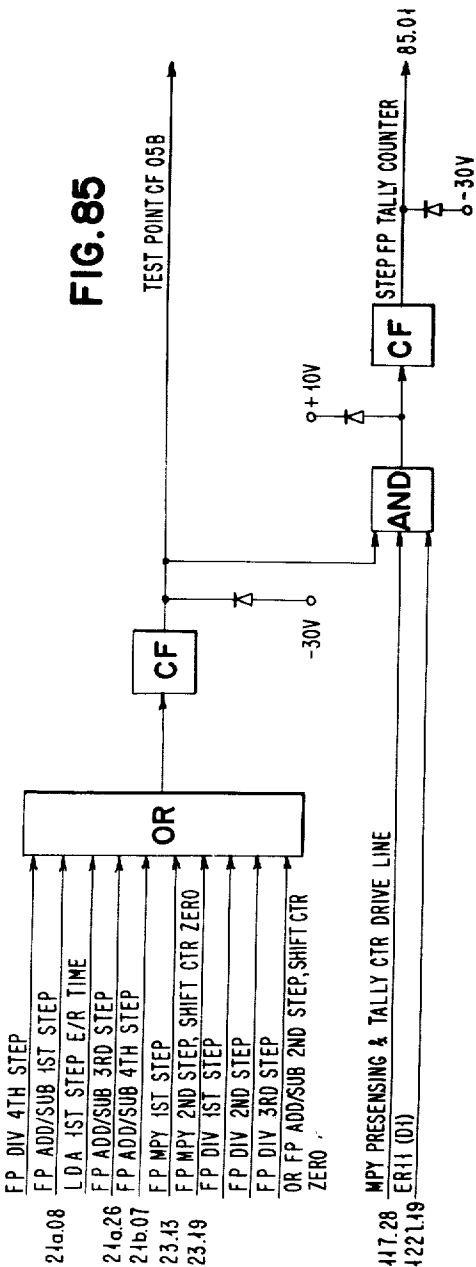
3,019,976

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STEP FLOATING POINT TALLY COUNTER



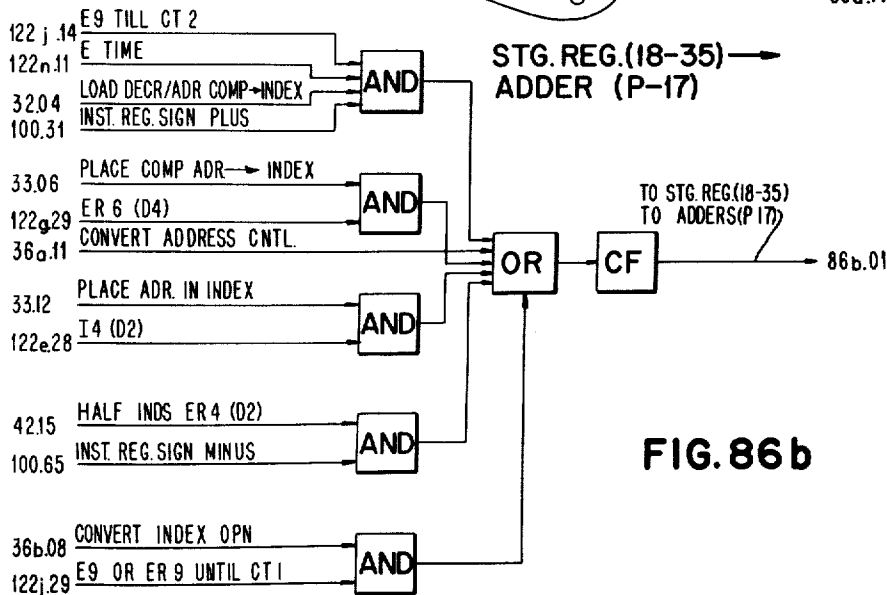
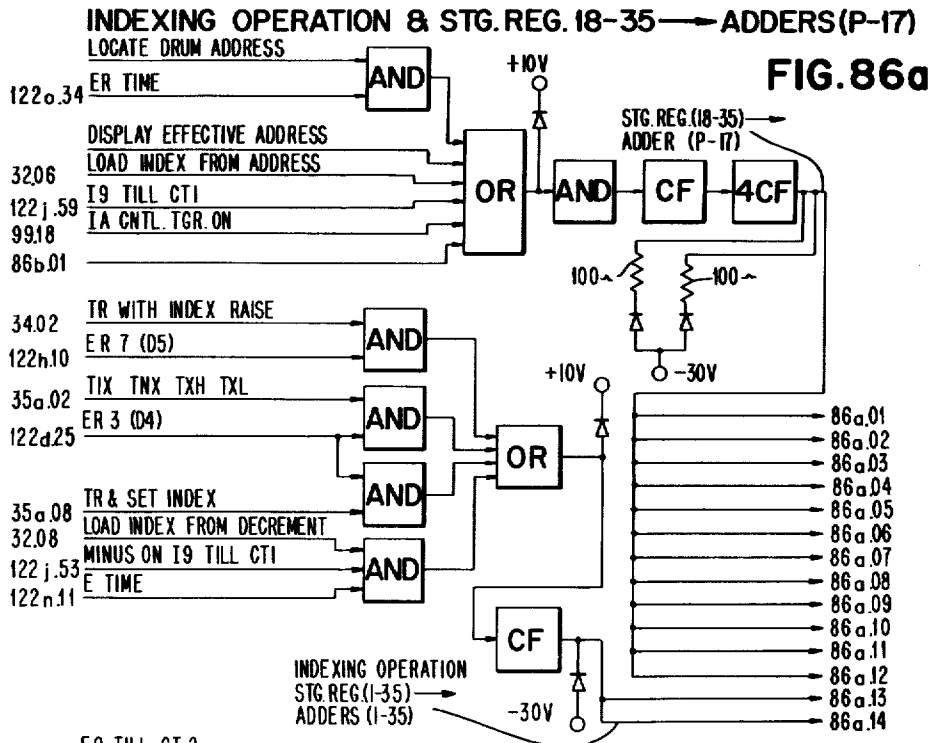
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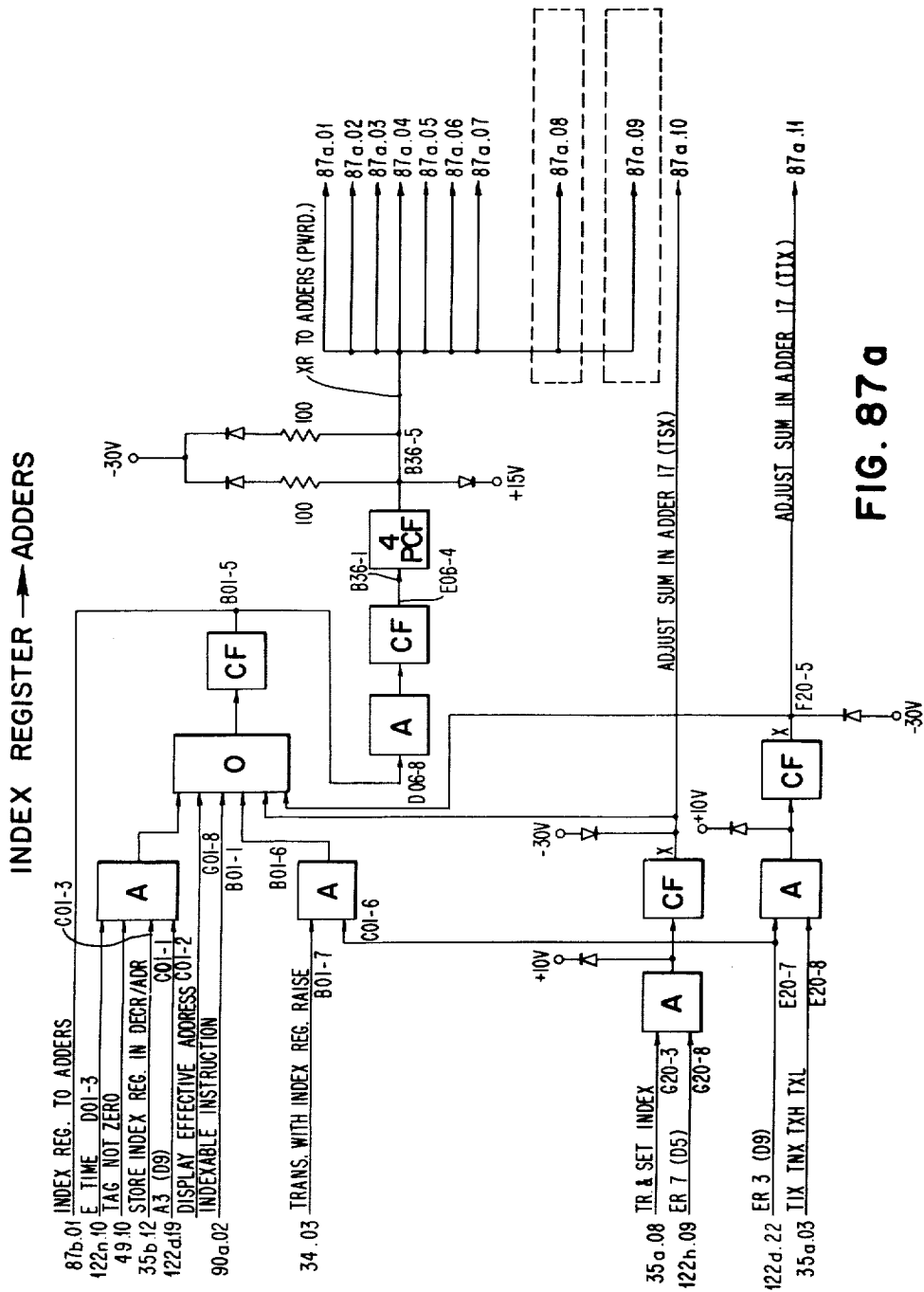
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**FIG. 87d**

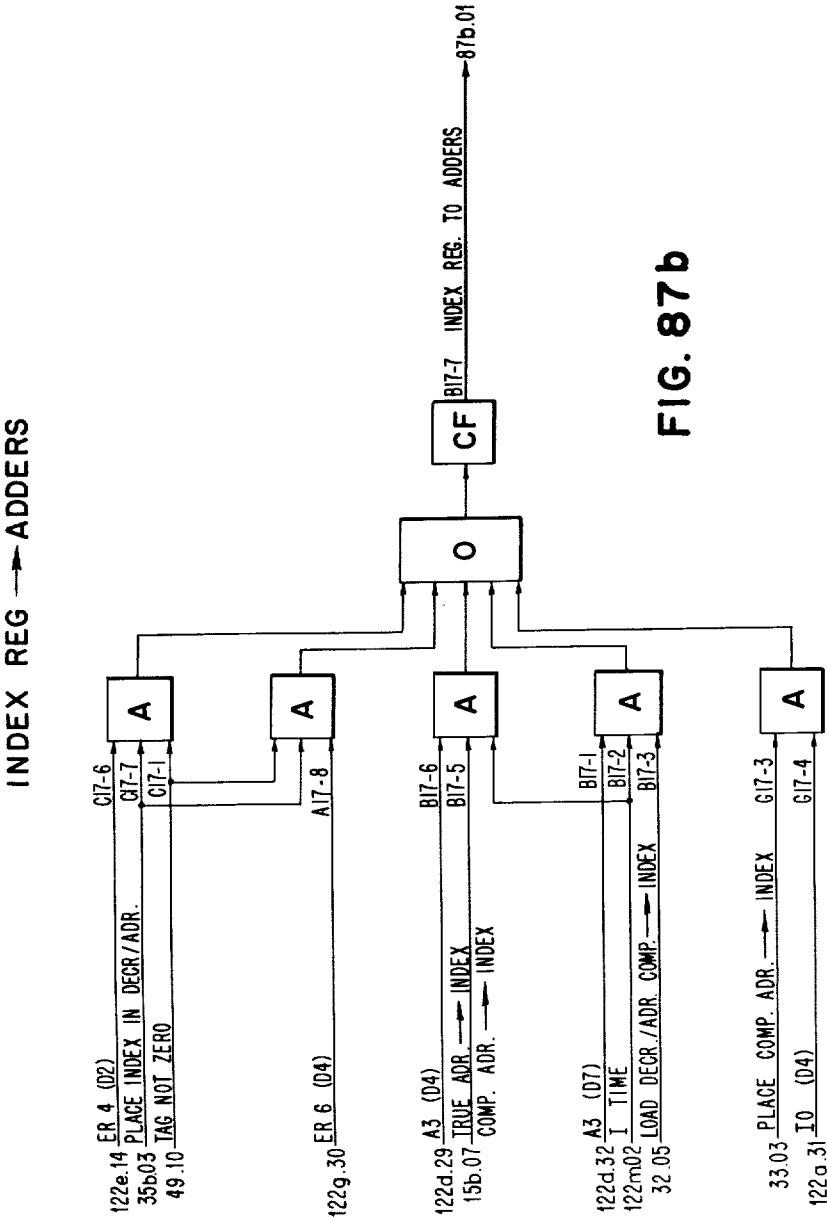
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## FLOATING POINT TALLY COUNTER



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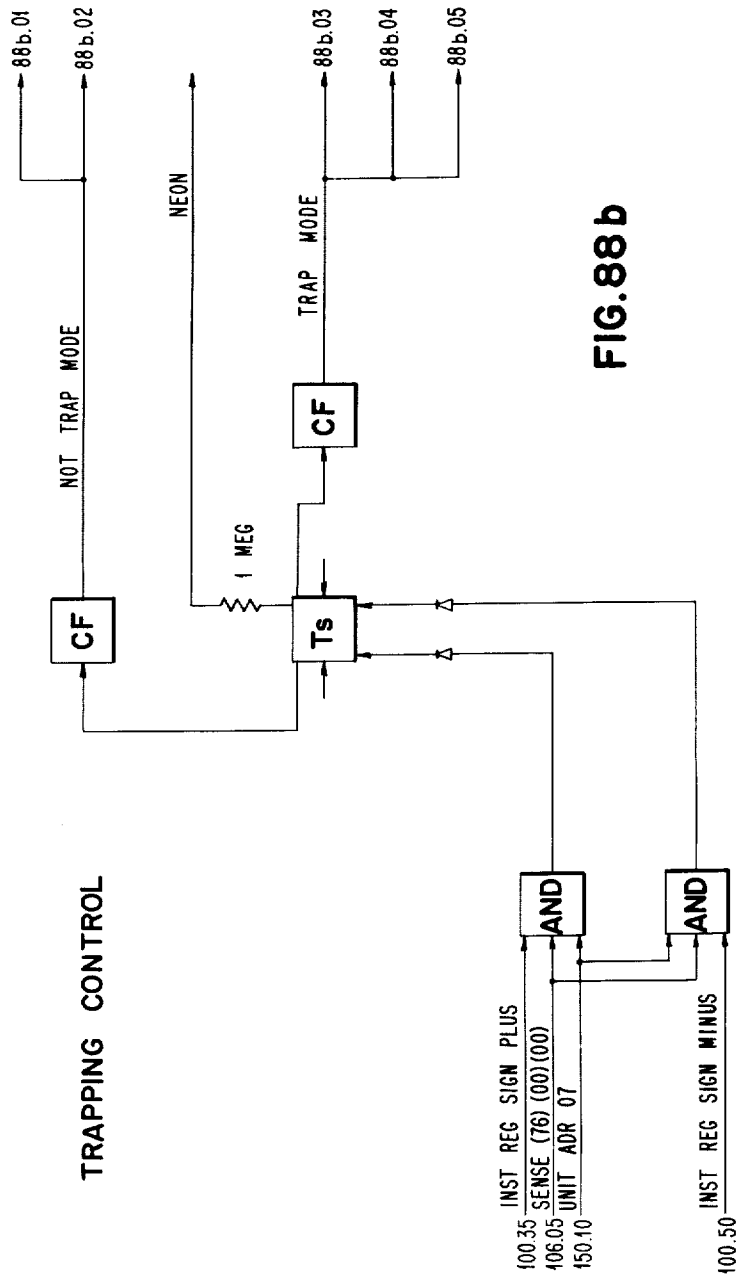


FIG. 88b

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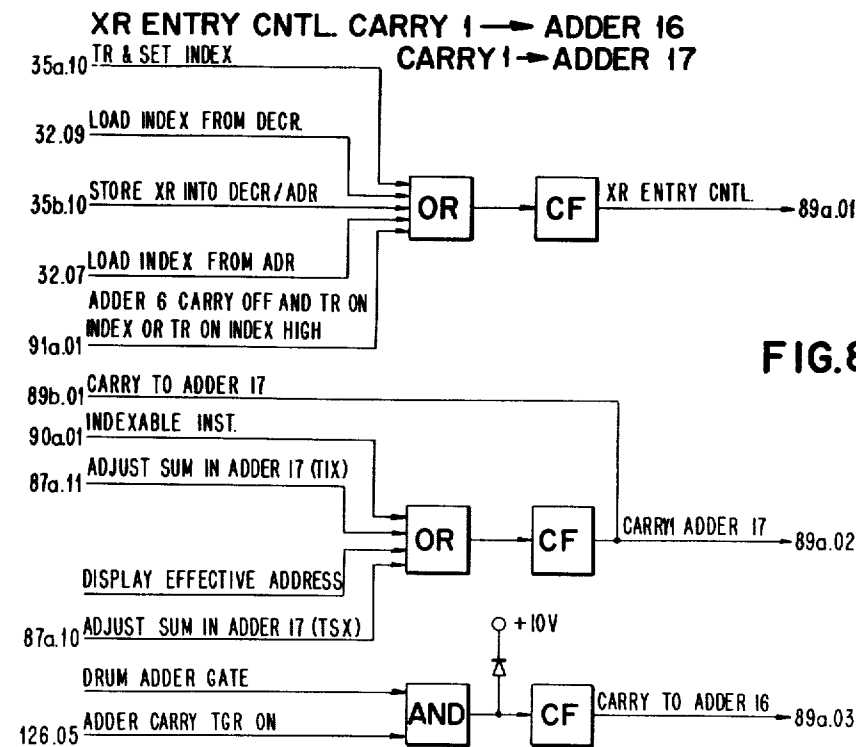


FIG. 89a

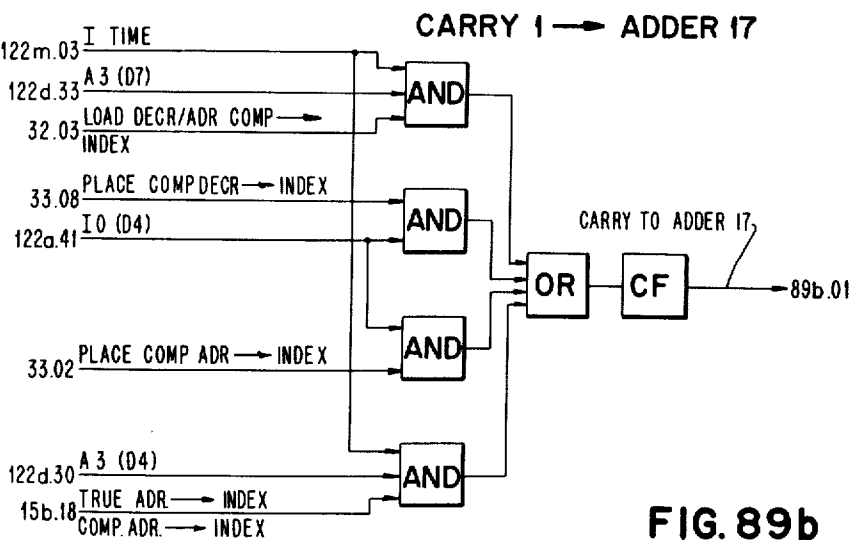
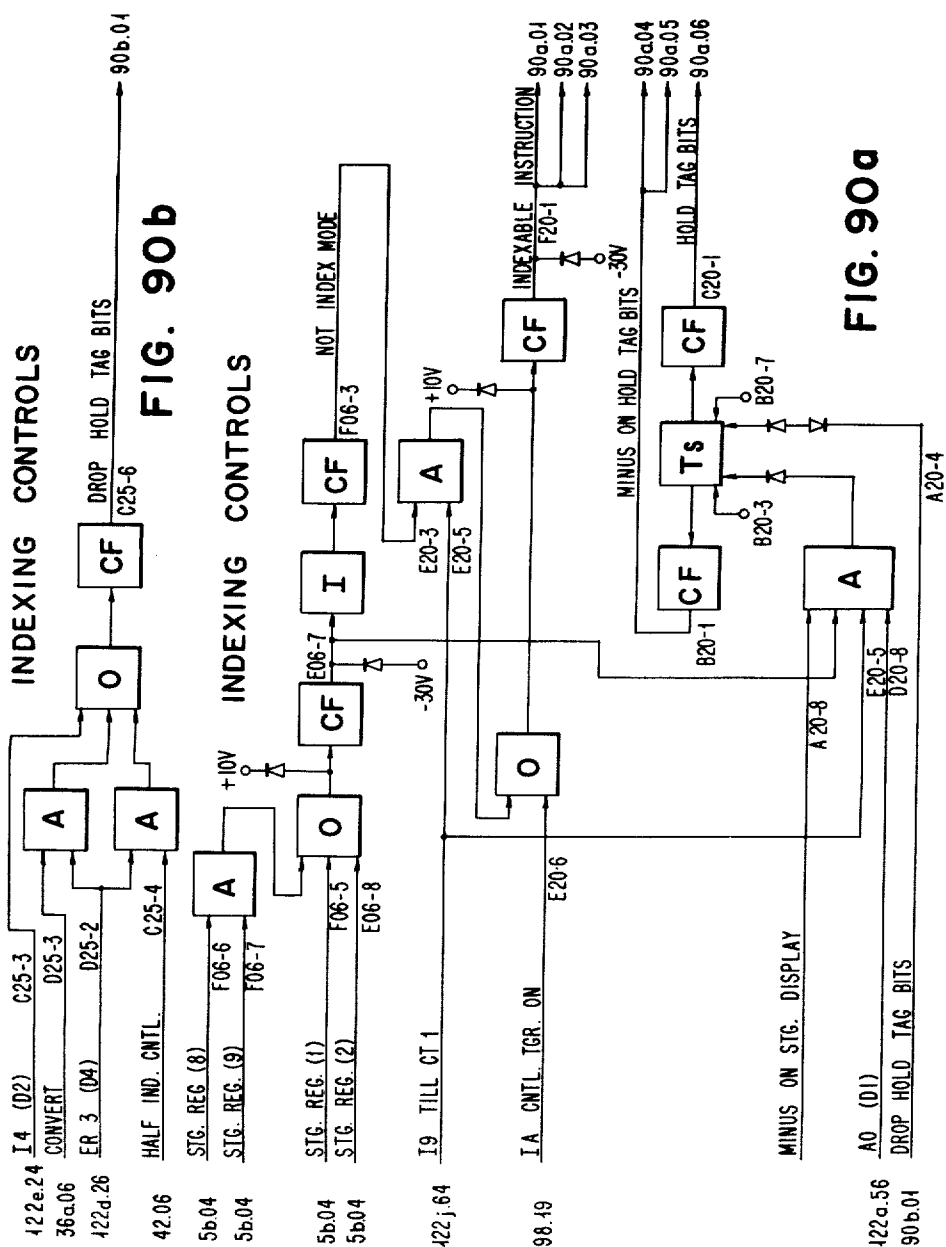


FIG. 89b

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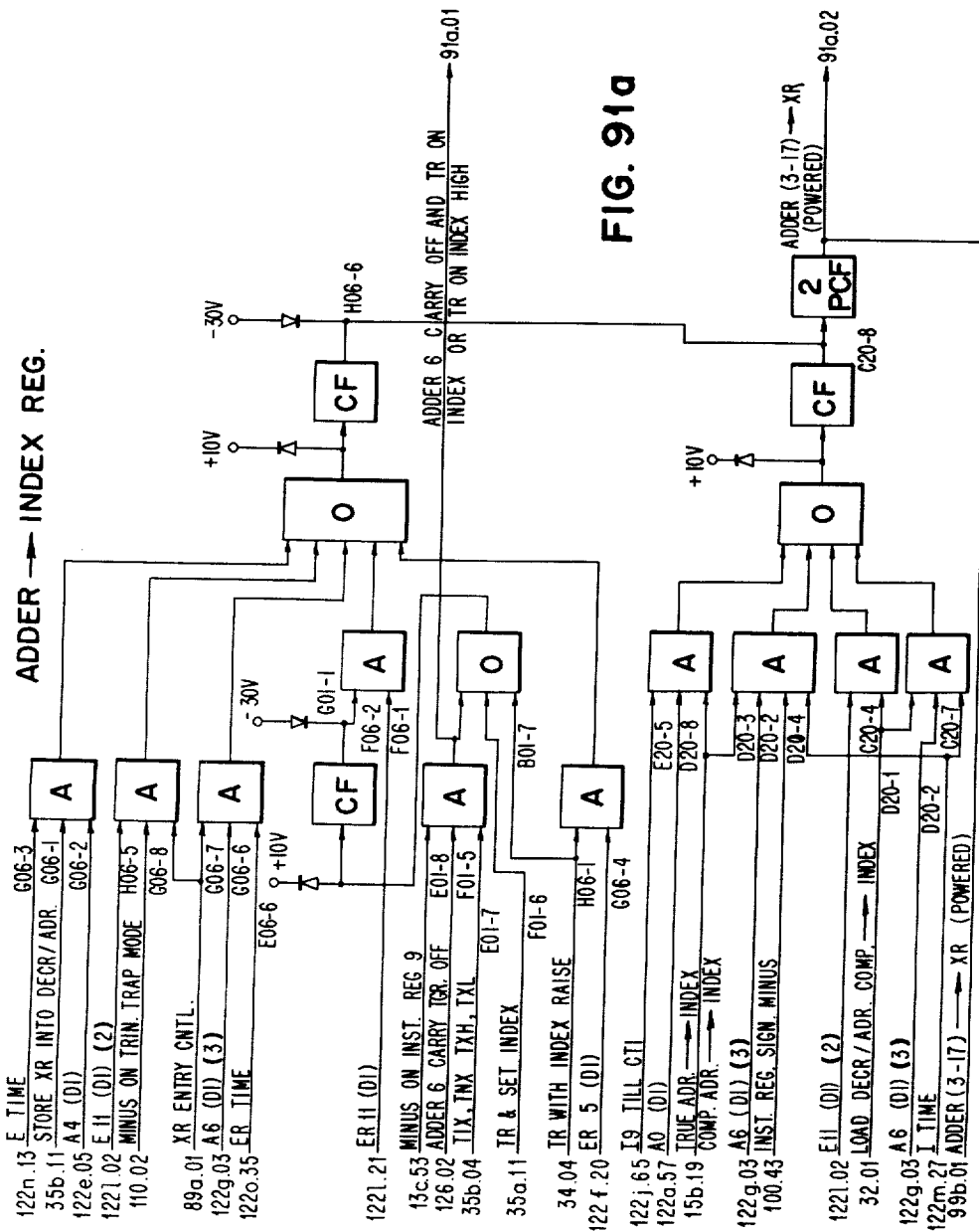
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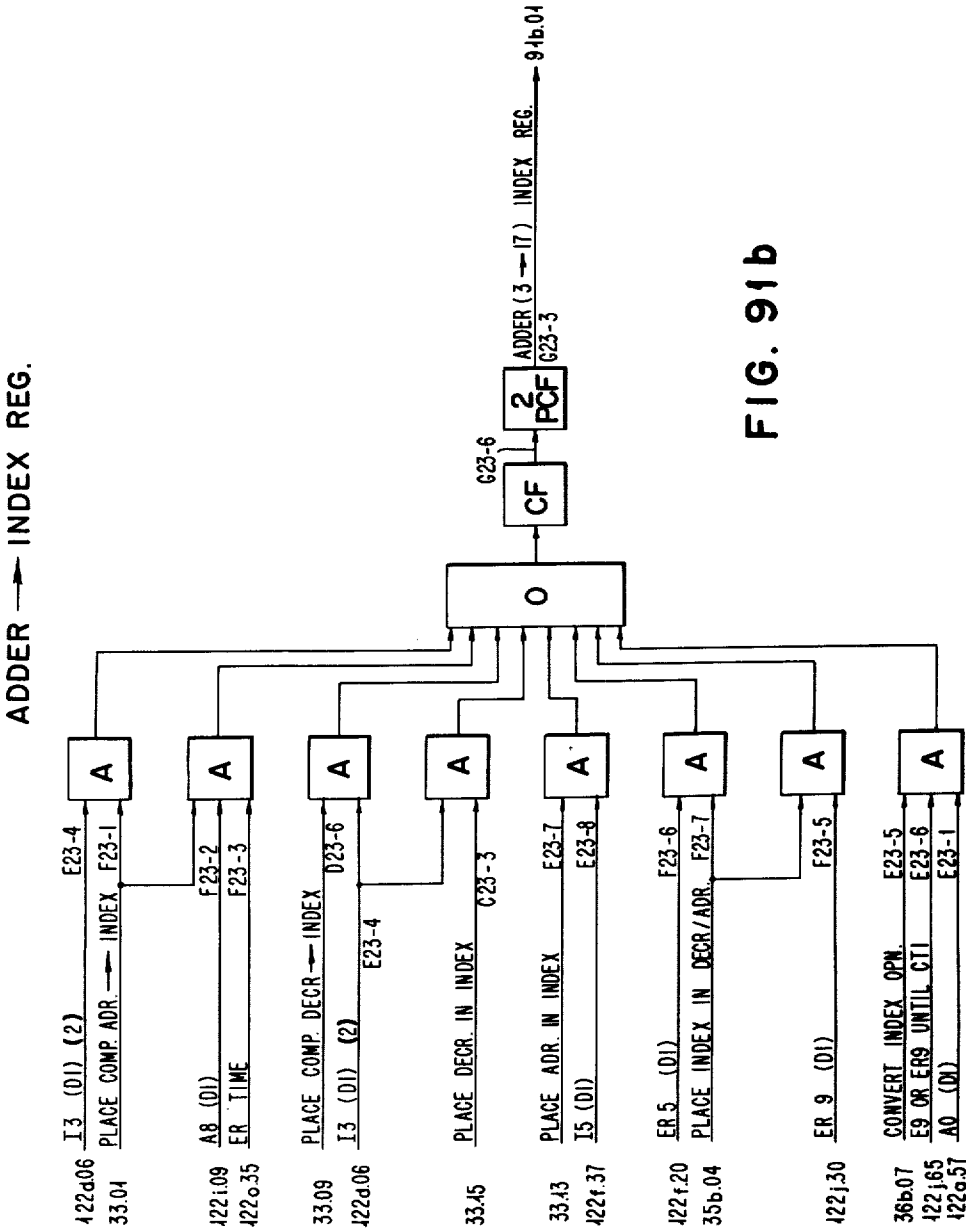
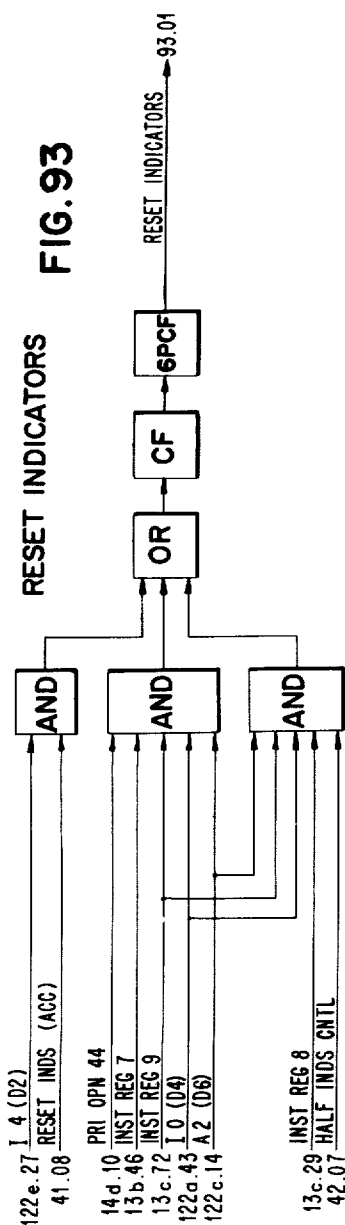
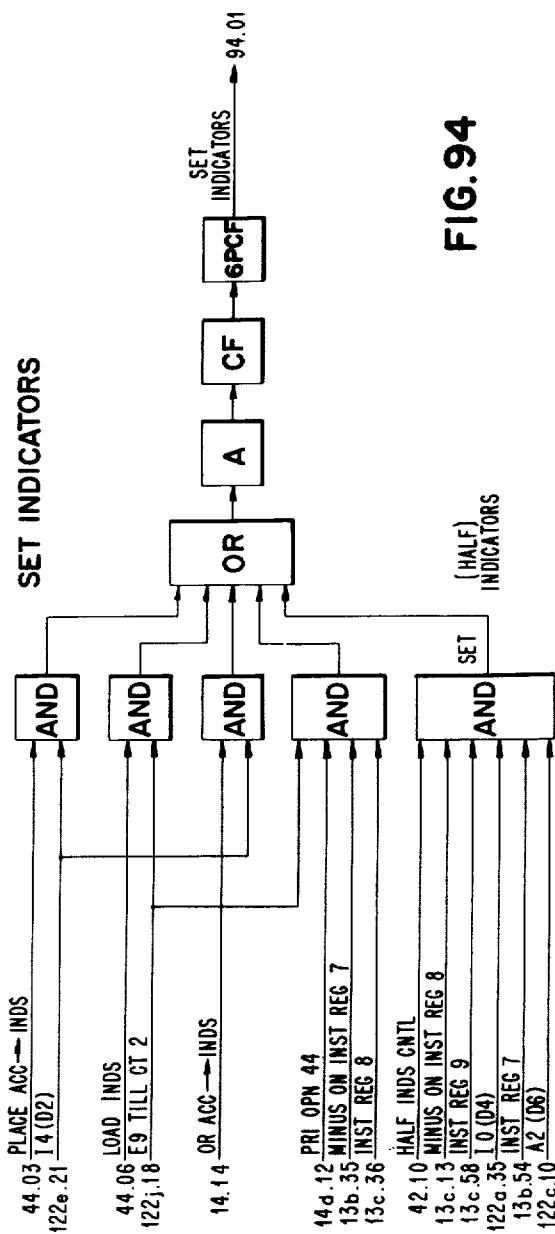


FIG. 91b



**FIG. 93**



**FIG. 94**

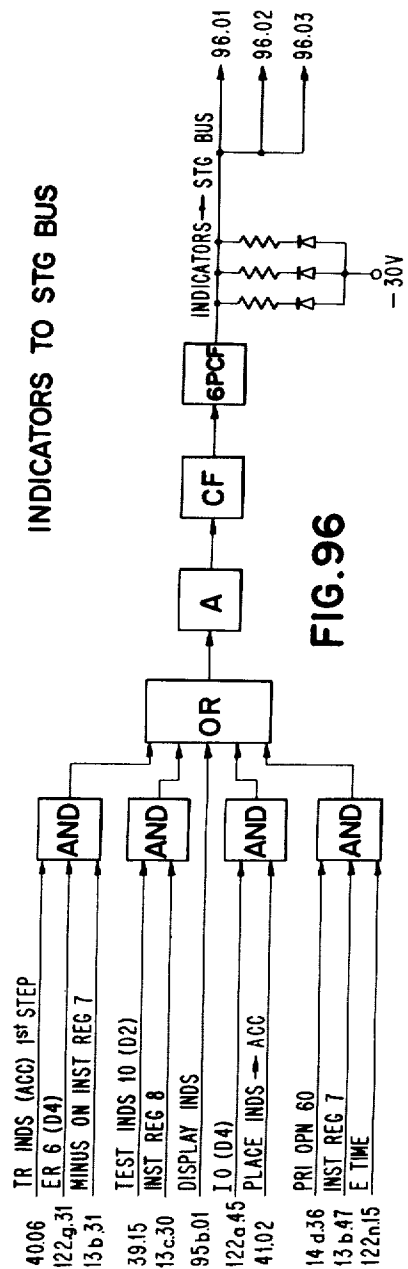
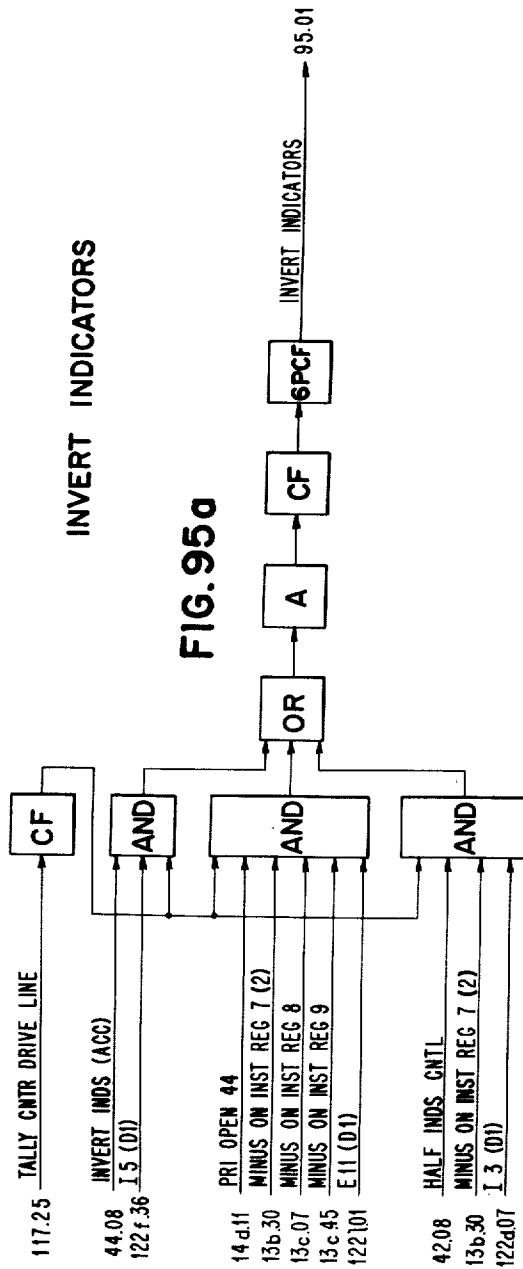
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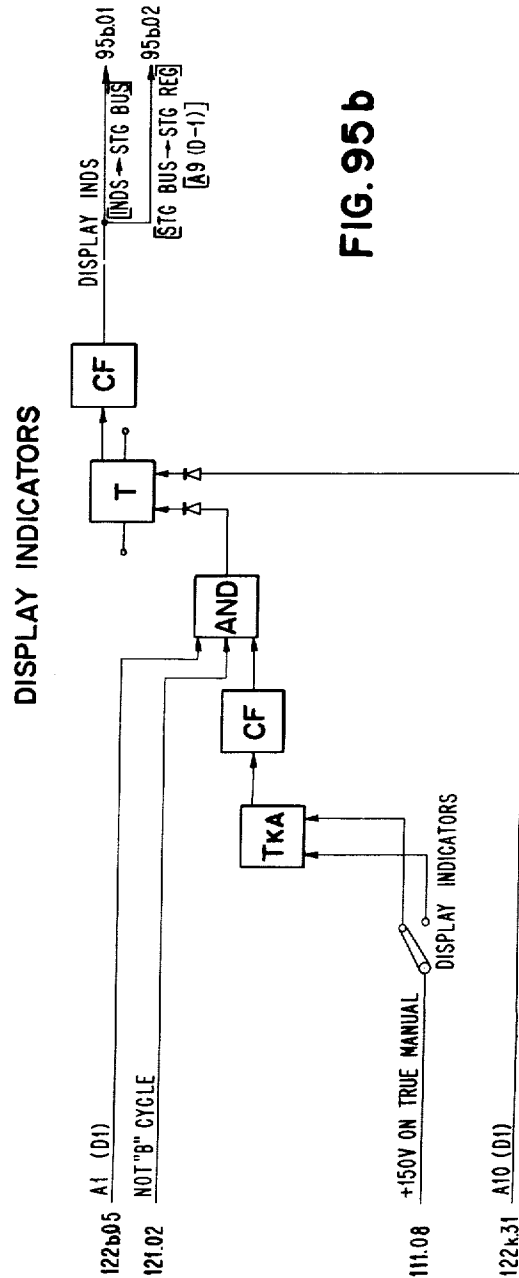
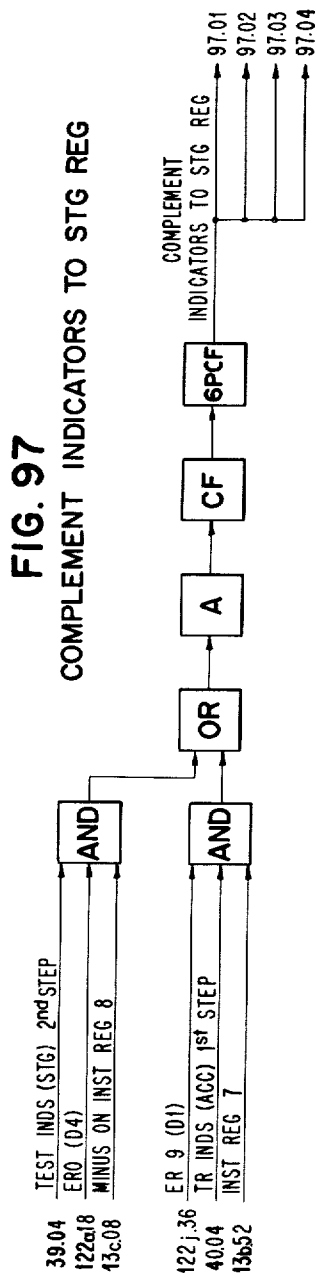
Feb. 6, 1962

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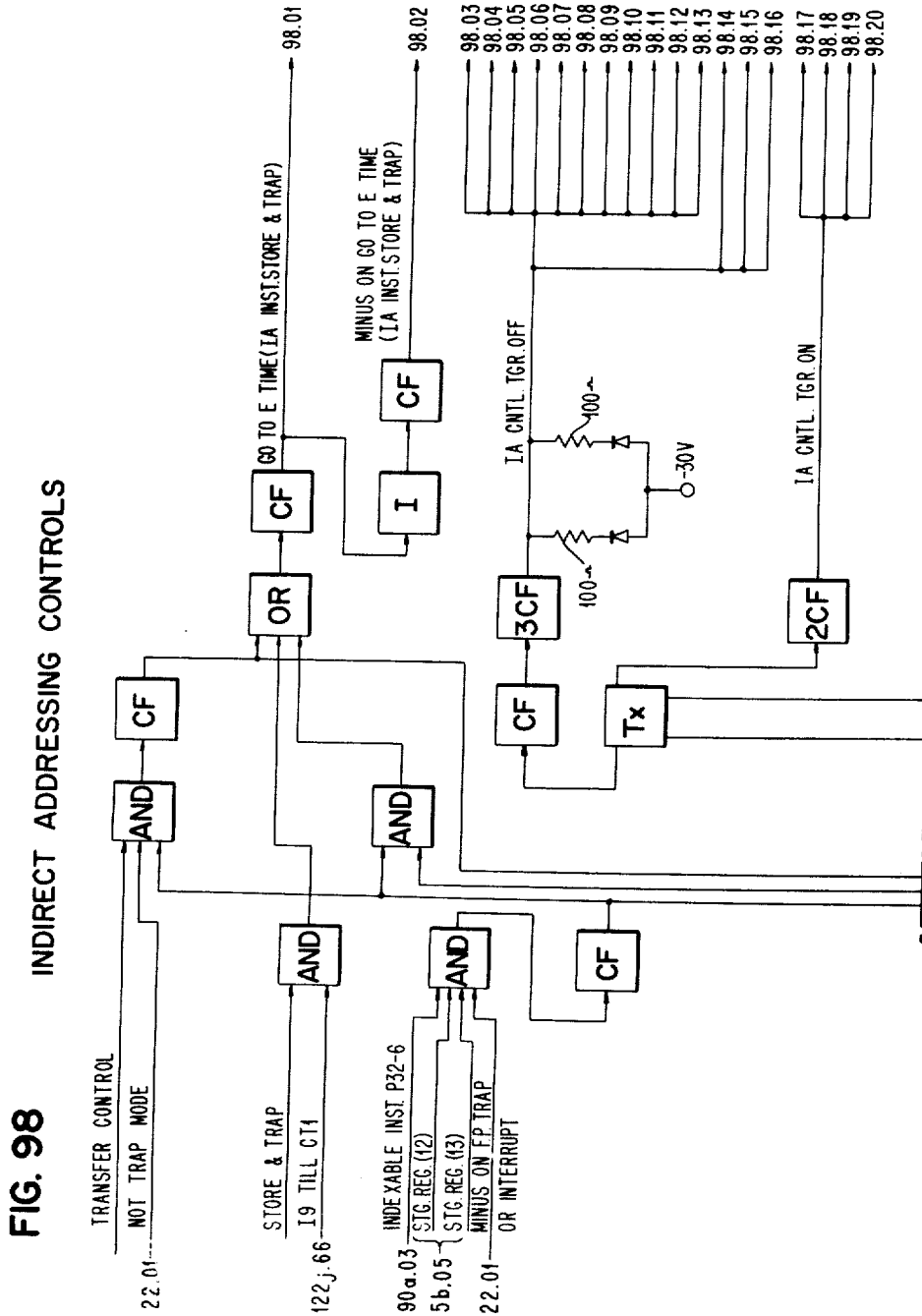
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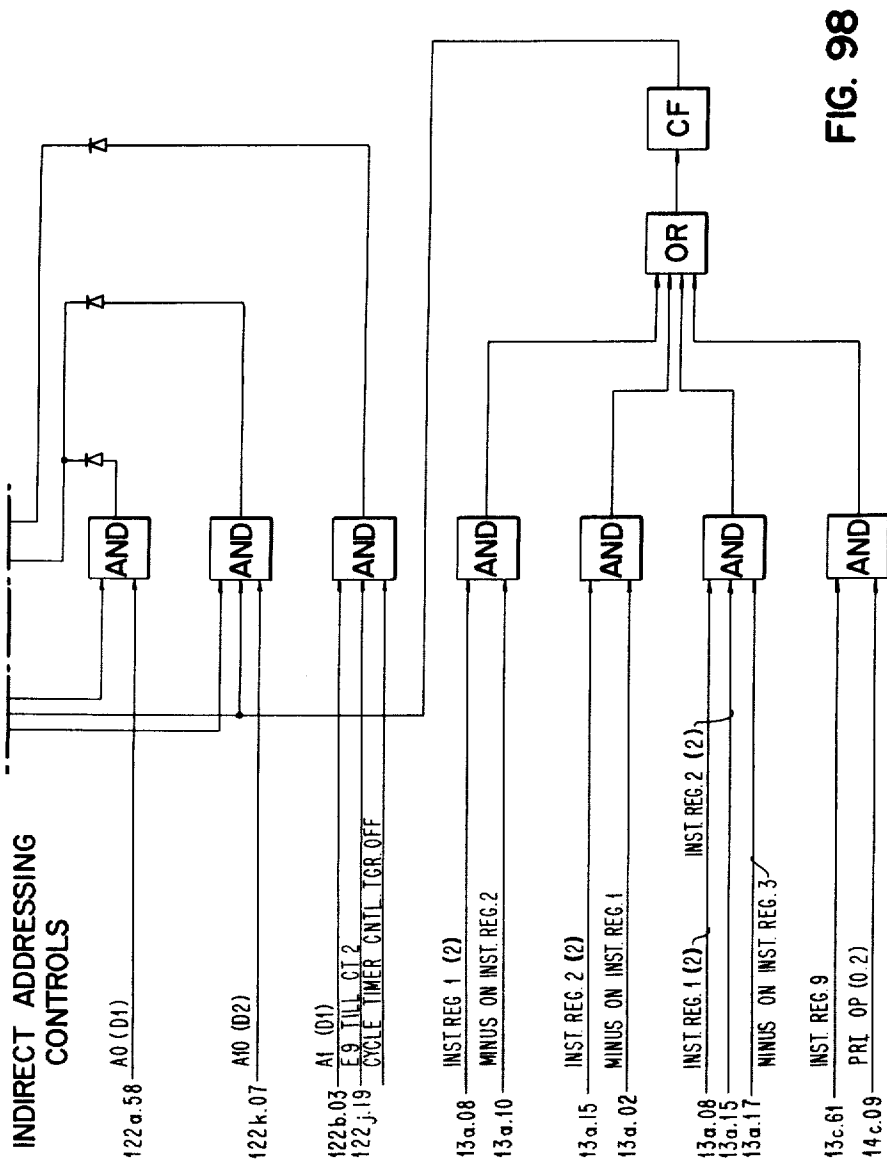


FIG. 98

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# INSTRUCTION REGISTER PULSE GENERATOR

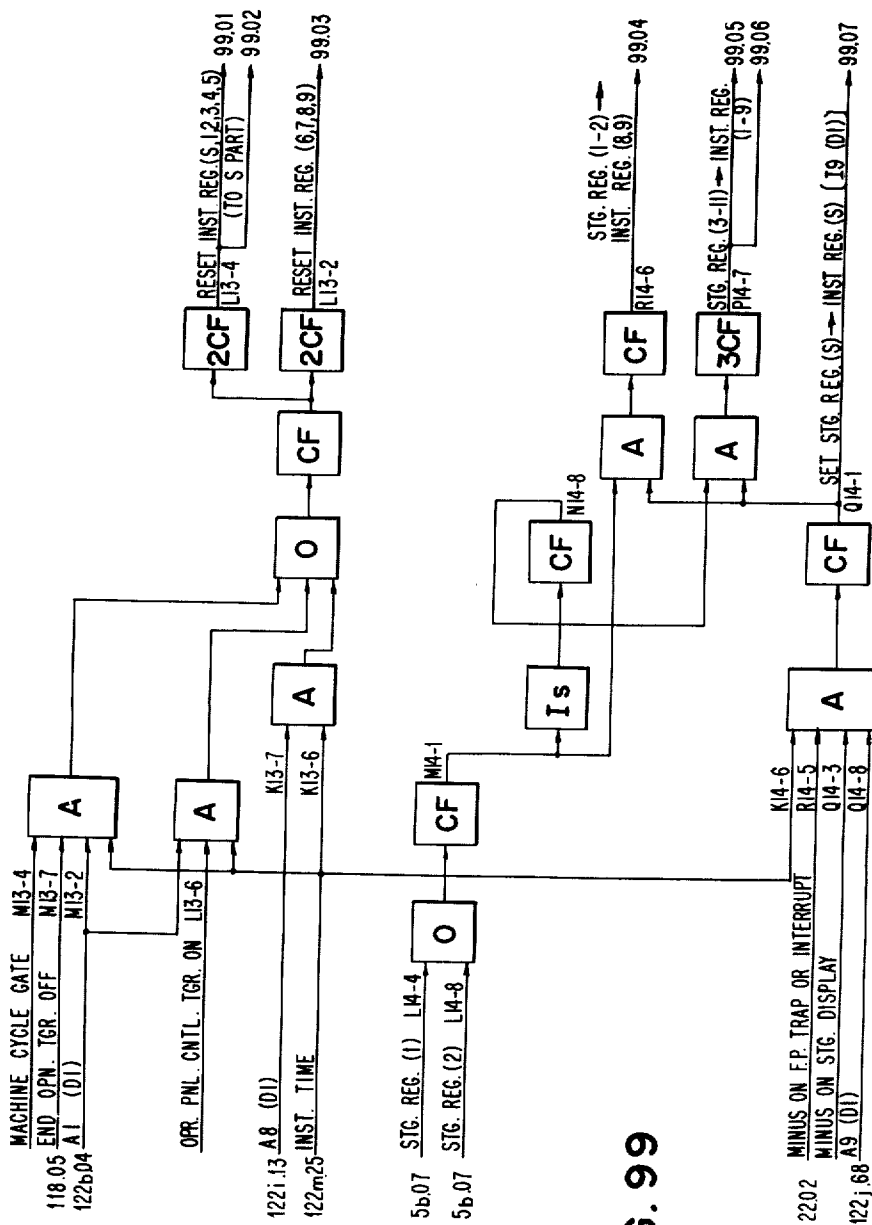


FIG. 99

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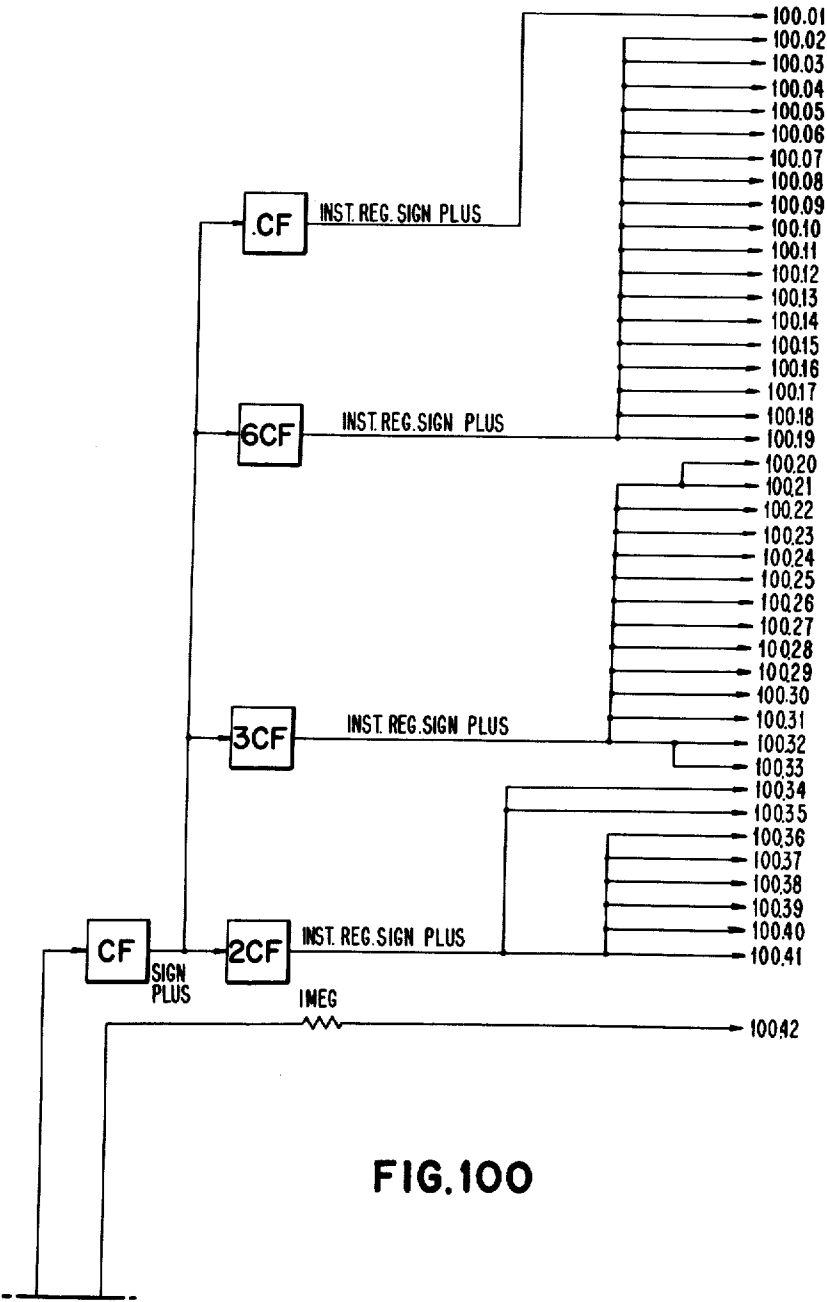
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INSTRUCTION REGISTER SIGN PLUS & MINUS



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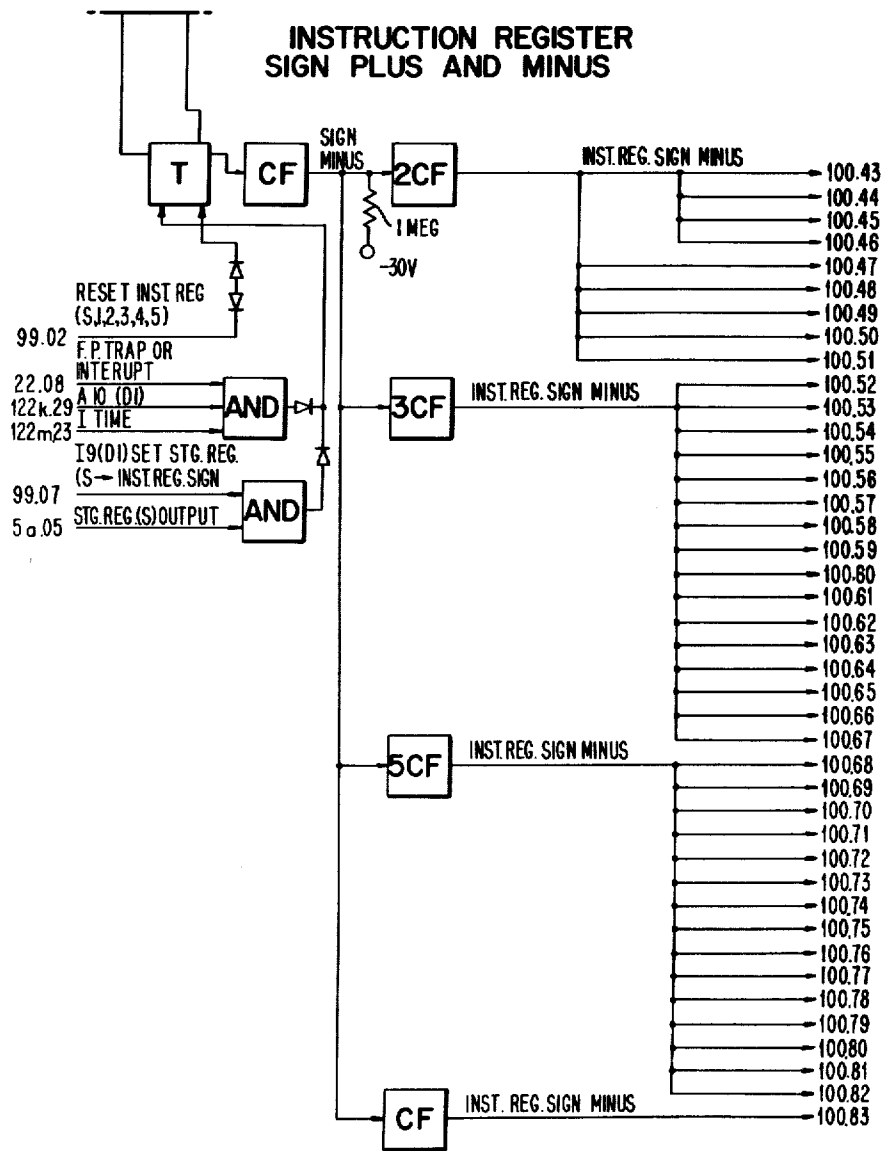


FIG.100

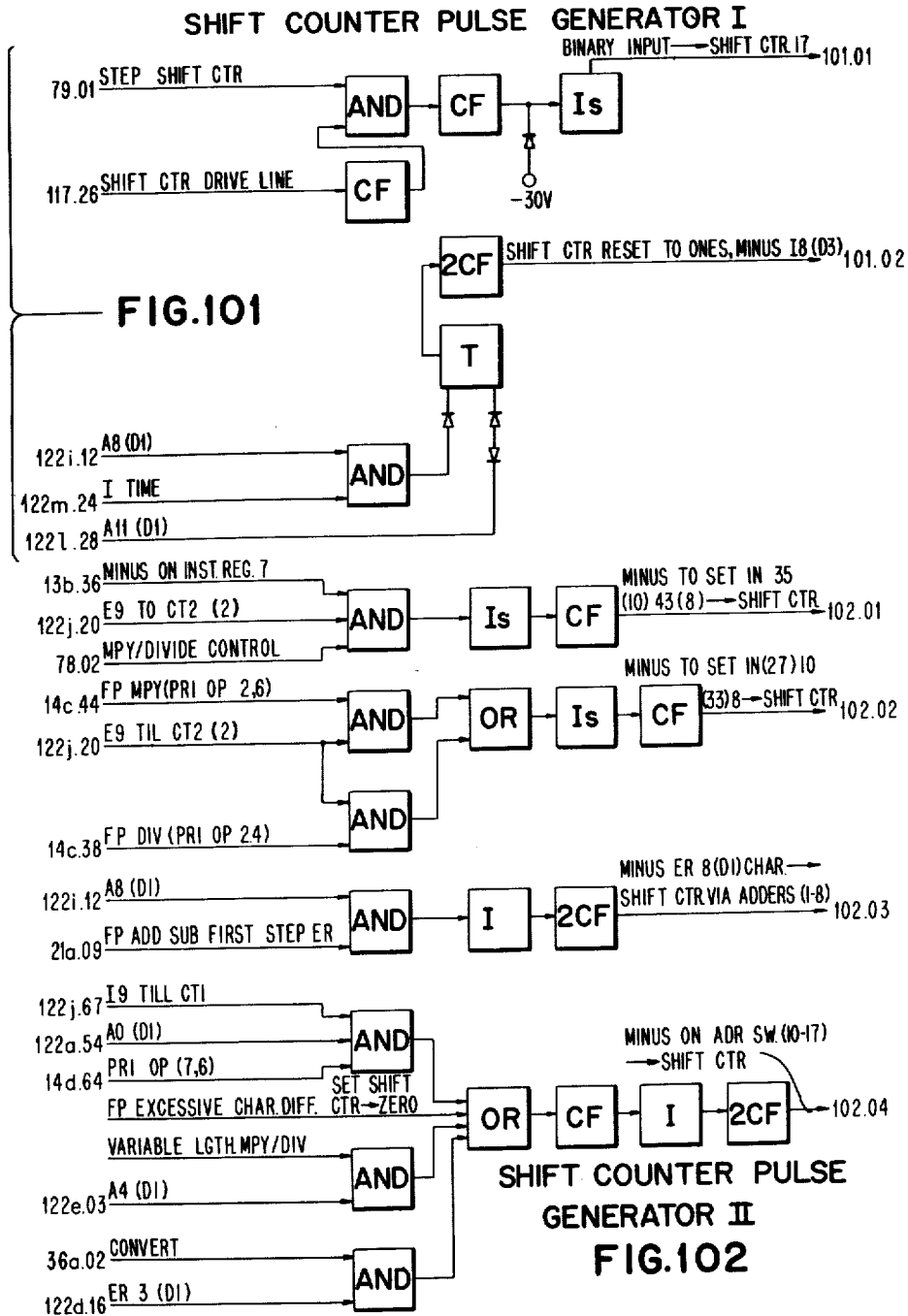
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ZERO ADDRESS CONTROLS

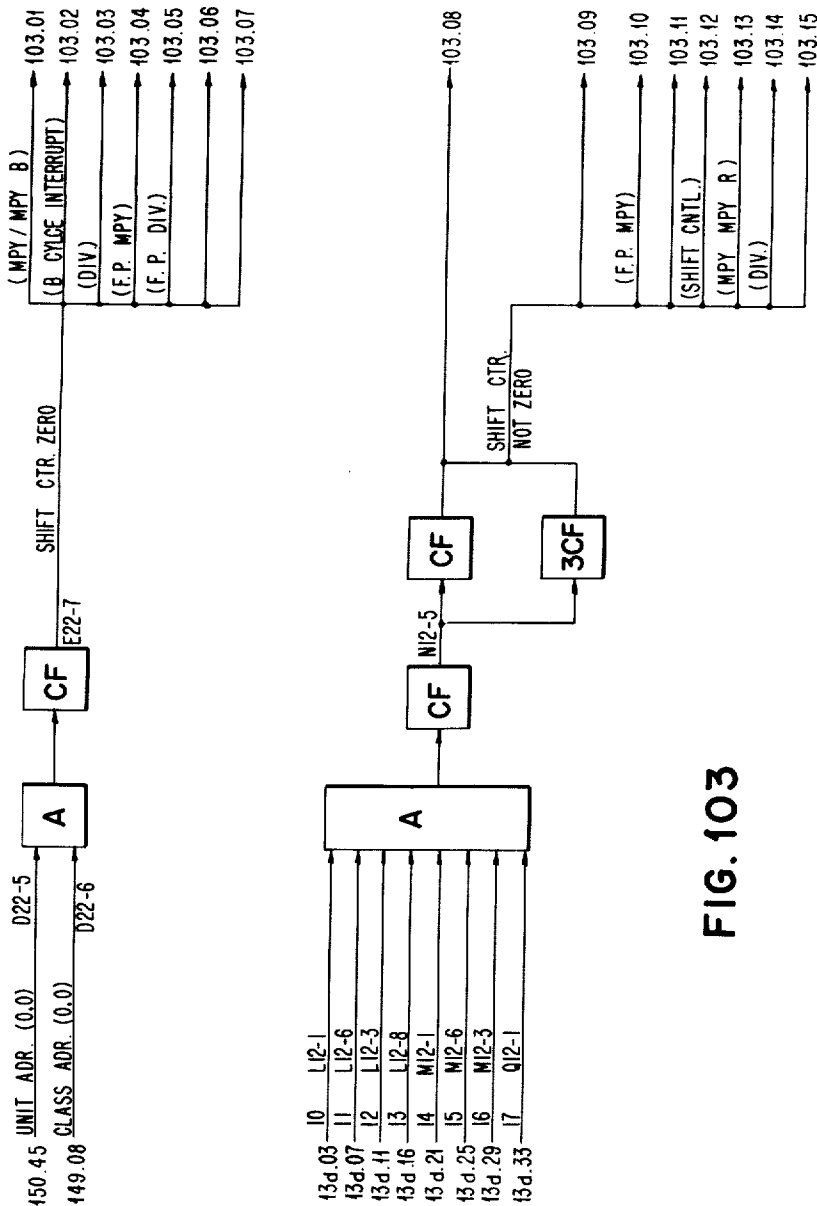


FIG. 103

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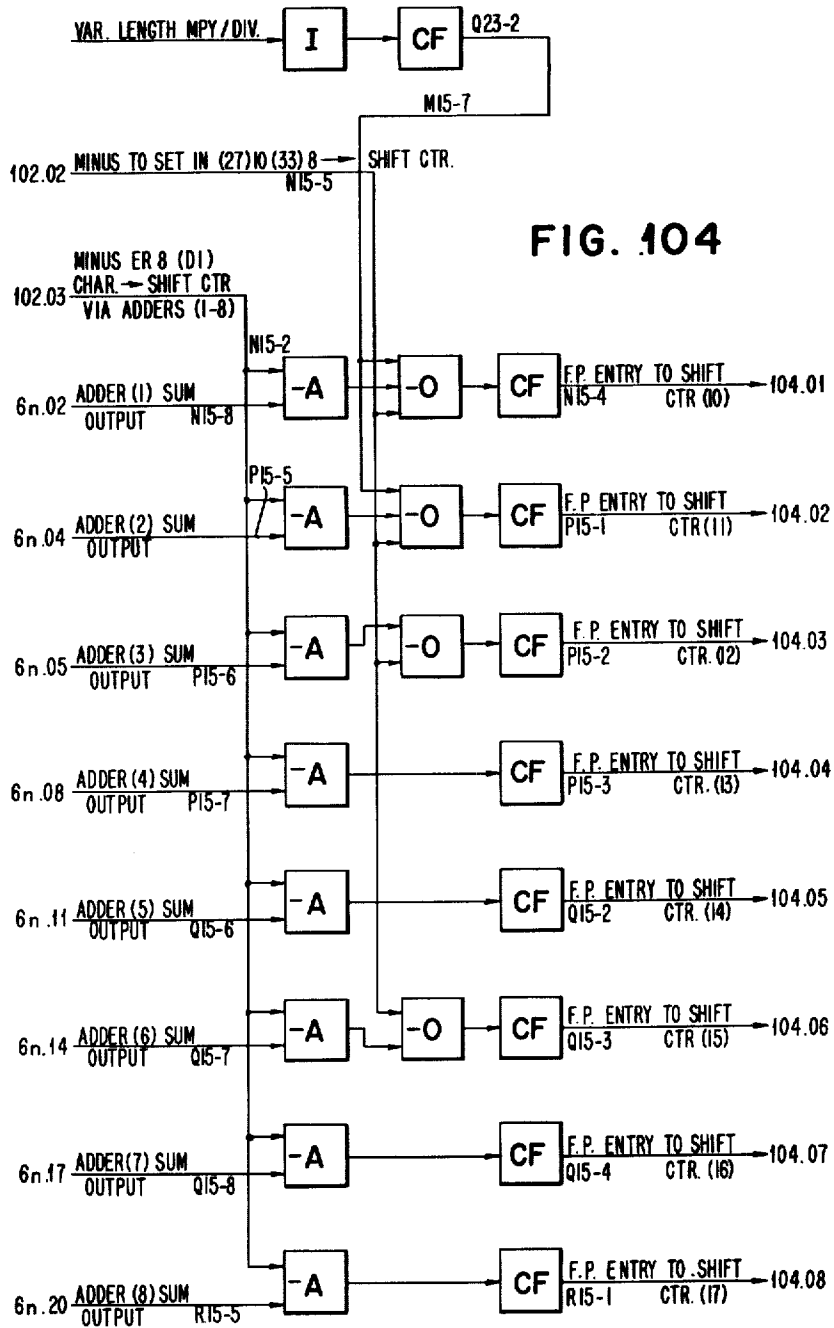
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# F.P. ENTRY TO SHIFT CTR. (10-17)



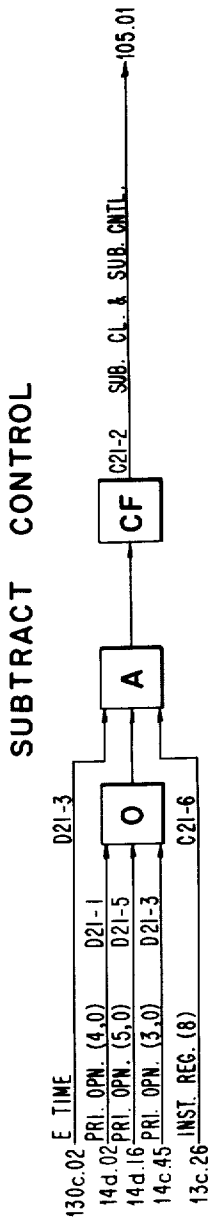
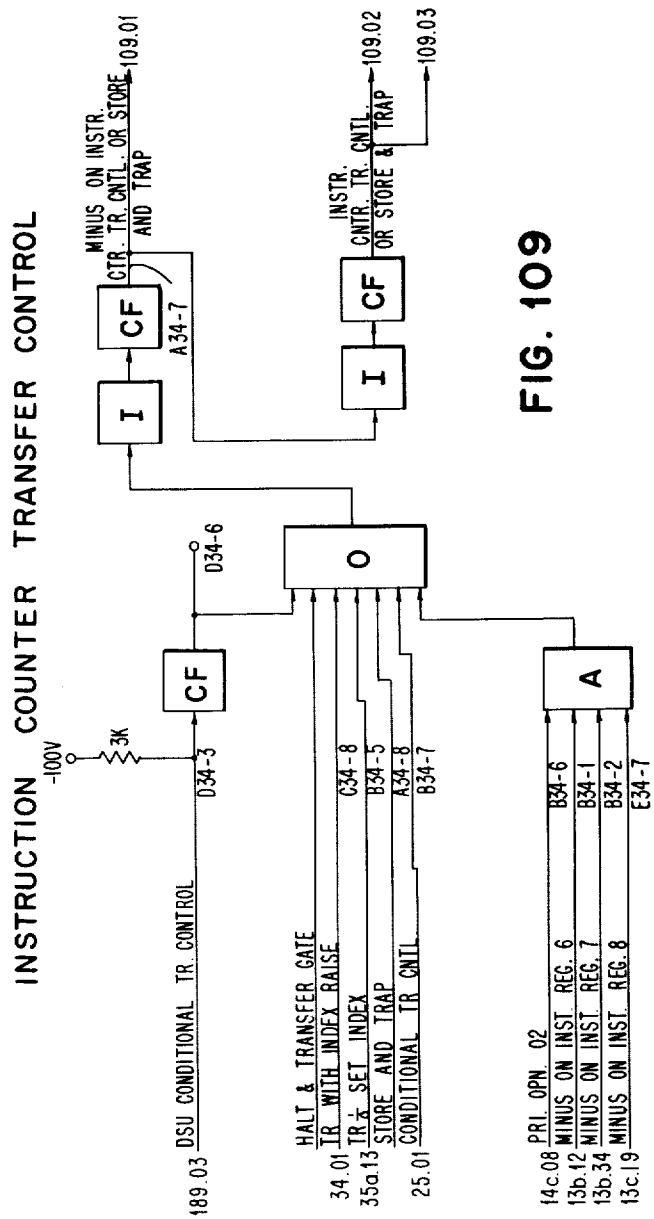
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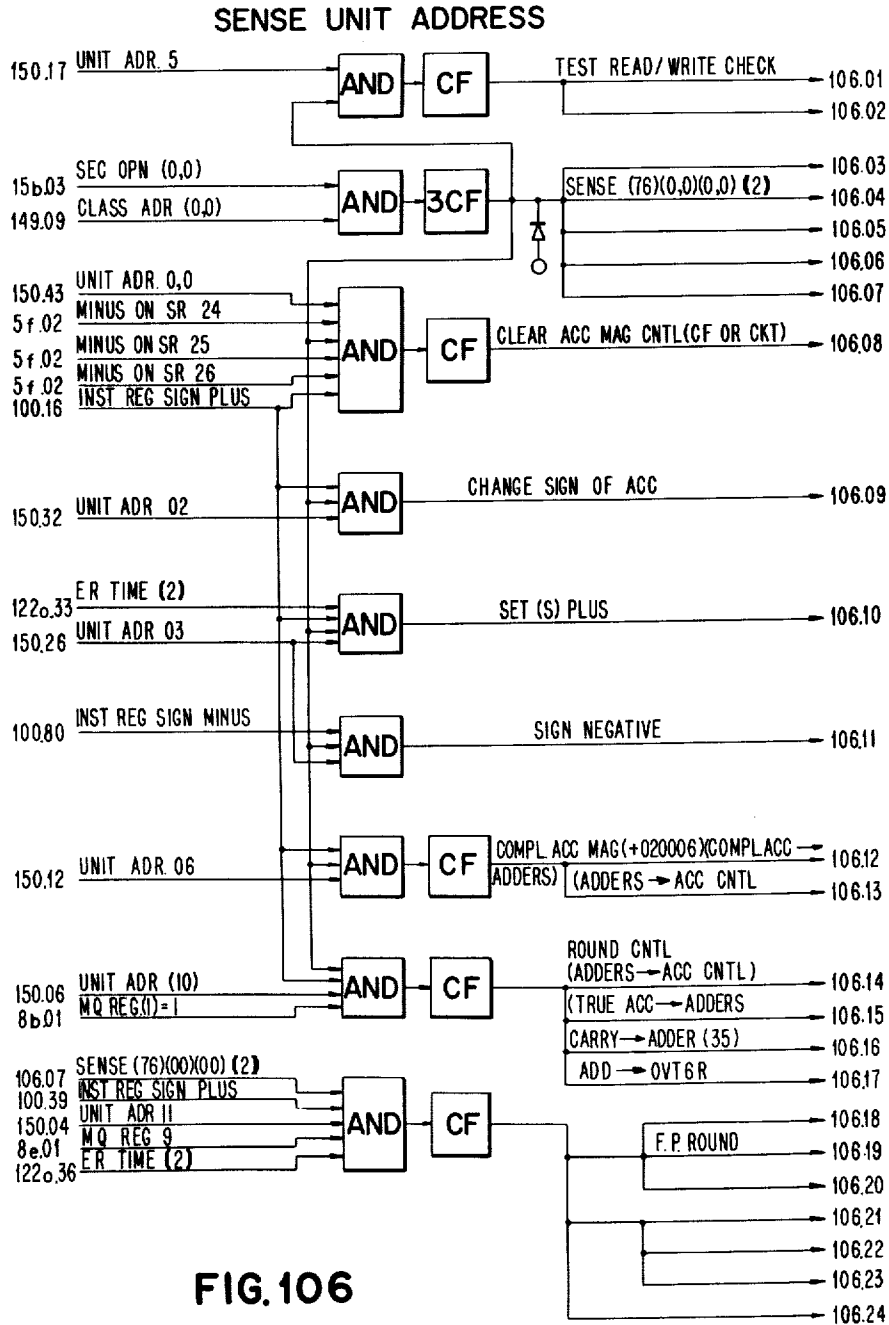
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**FIG. 106**

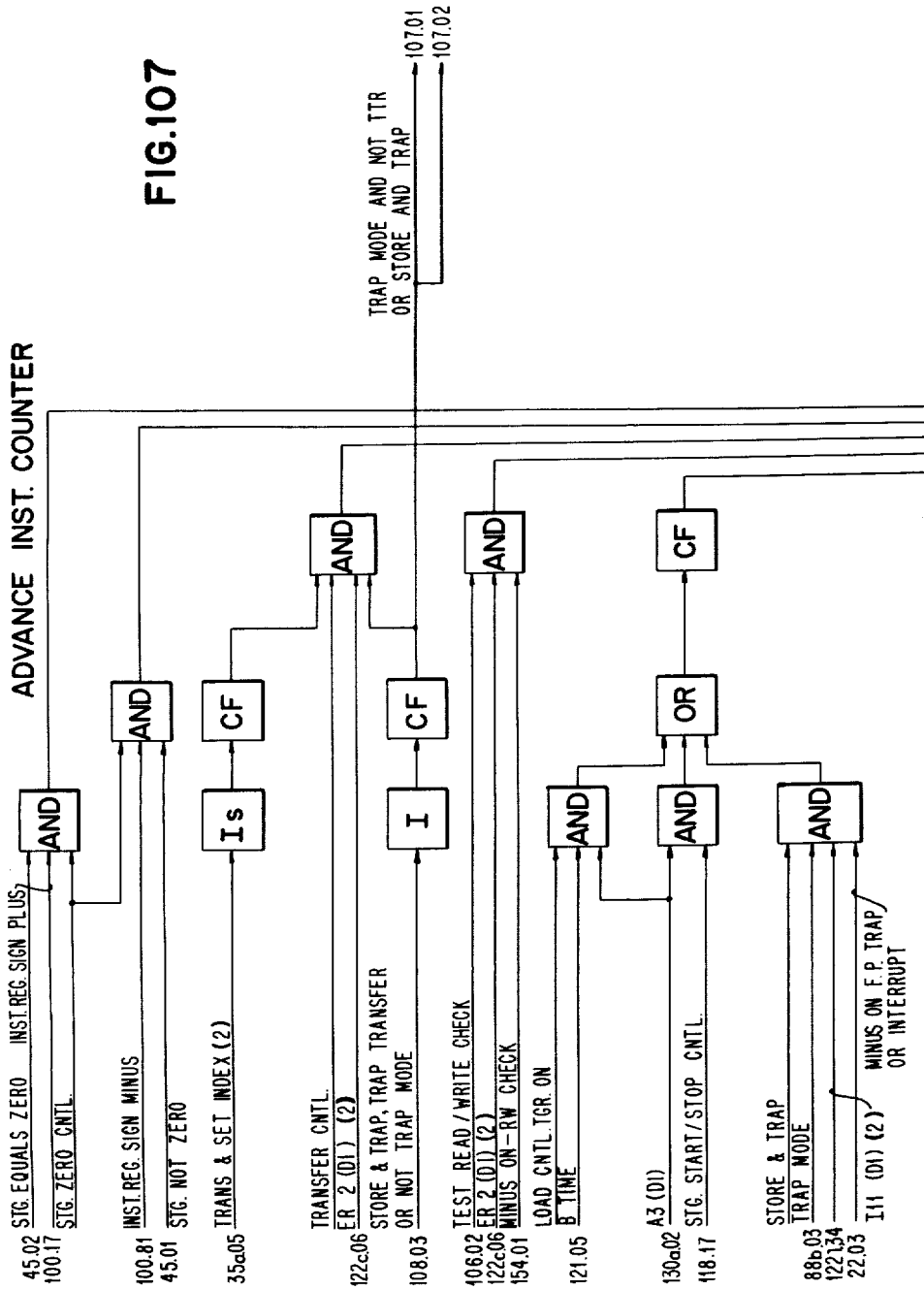
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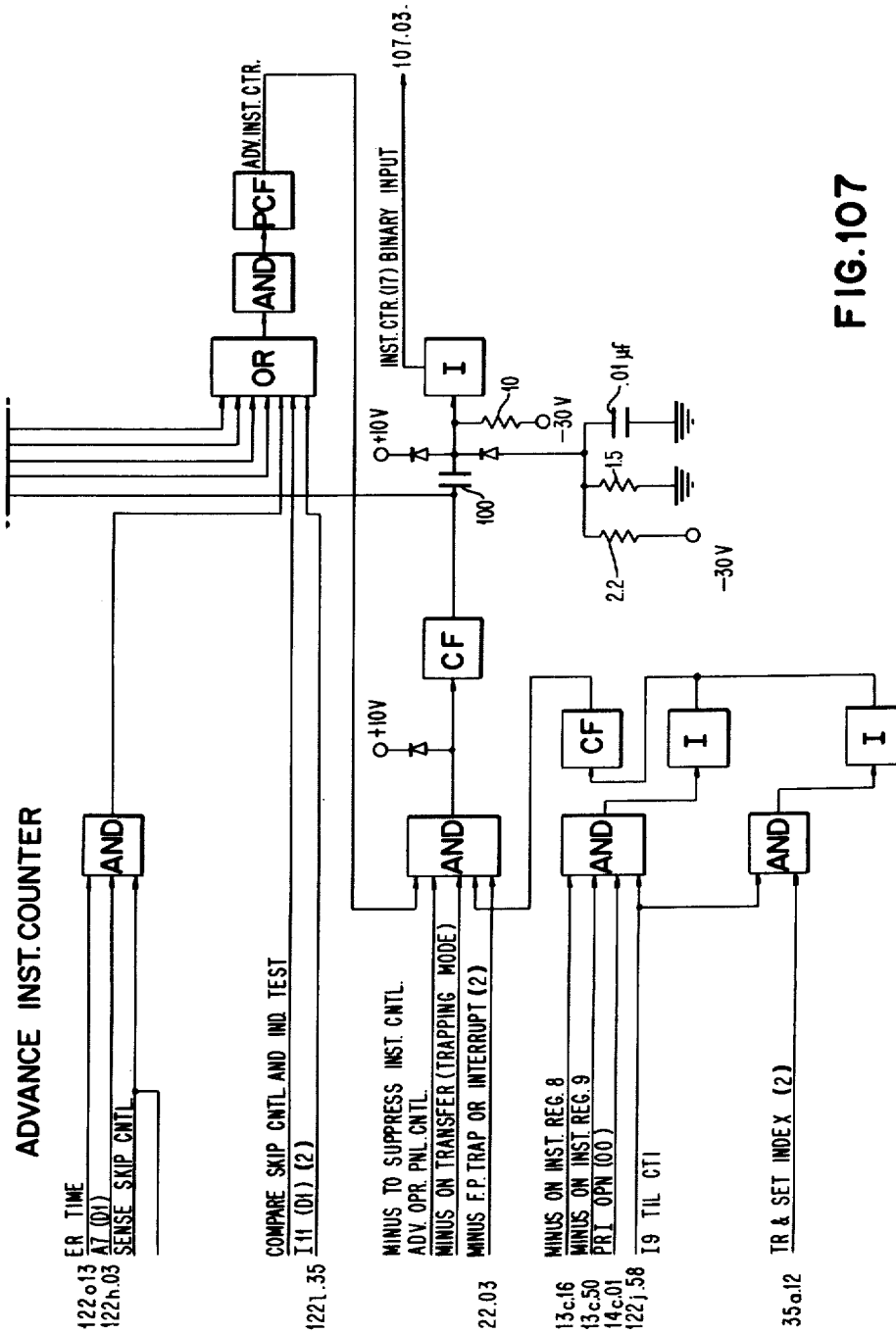
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**FIG.107**

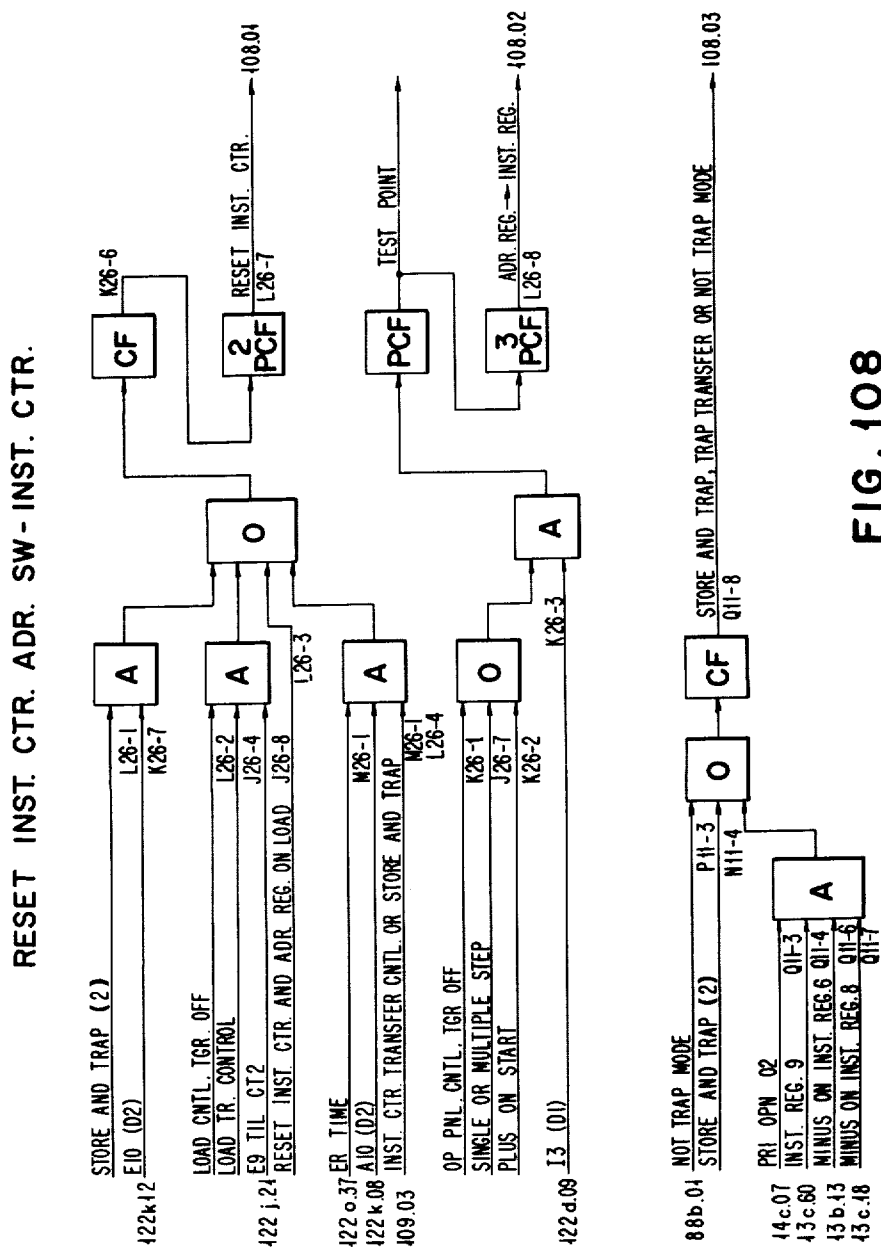
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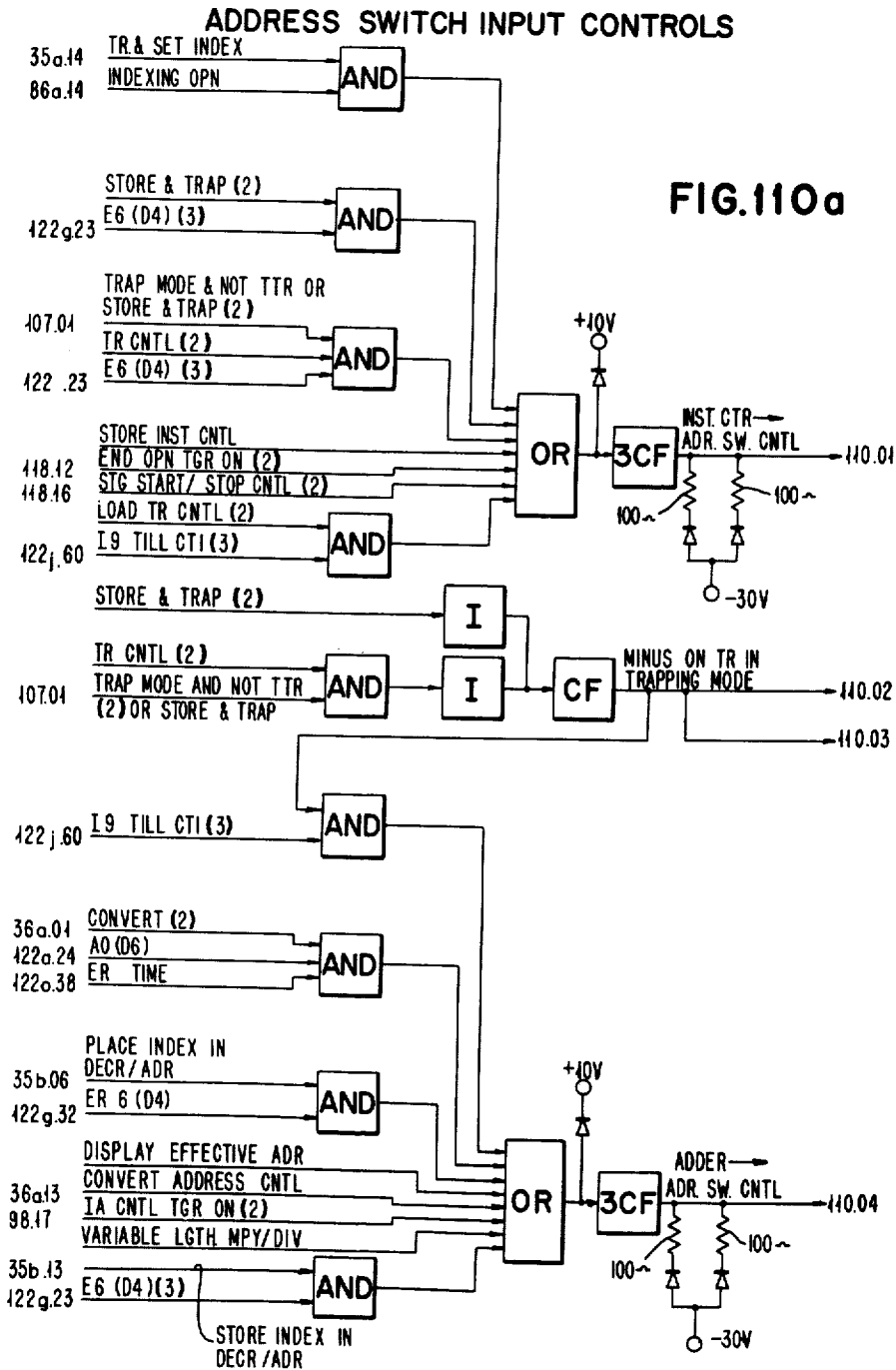
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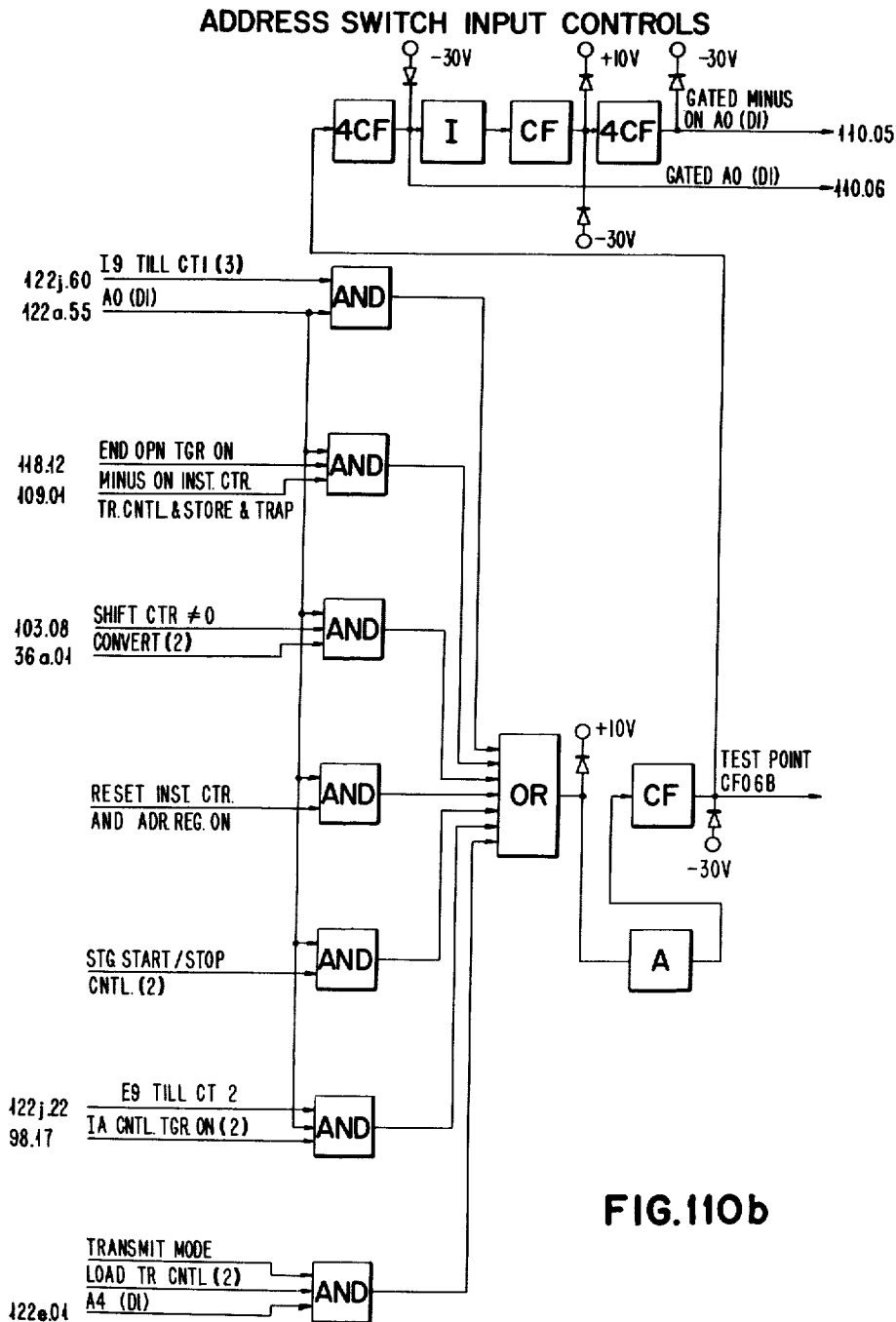
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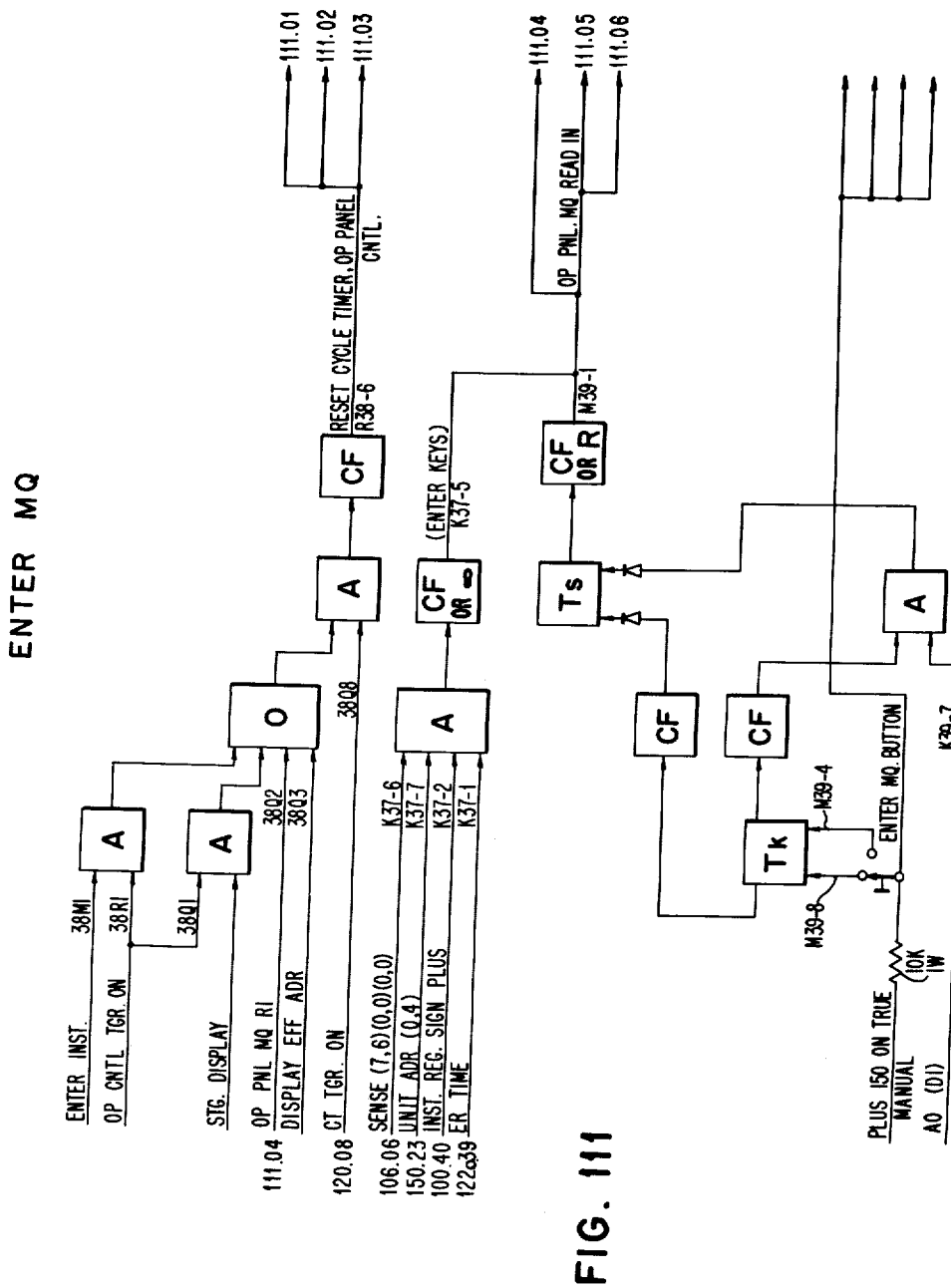


FIG. 111

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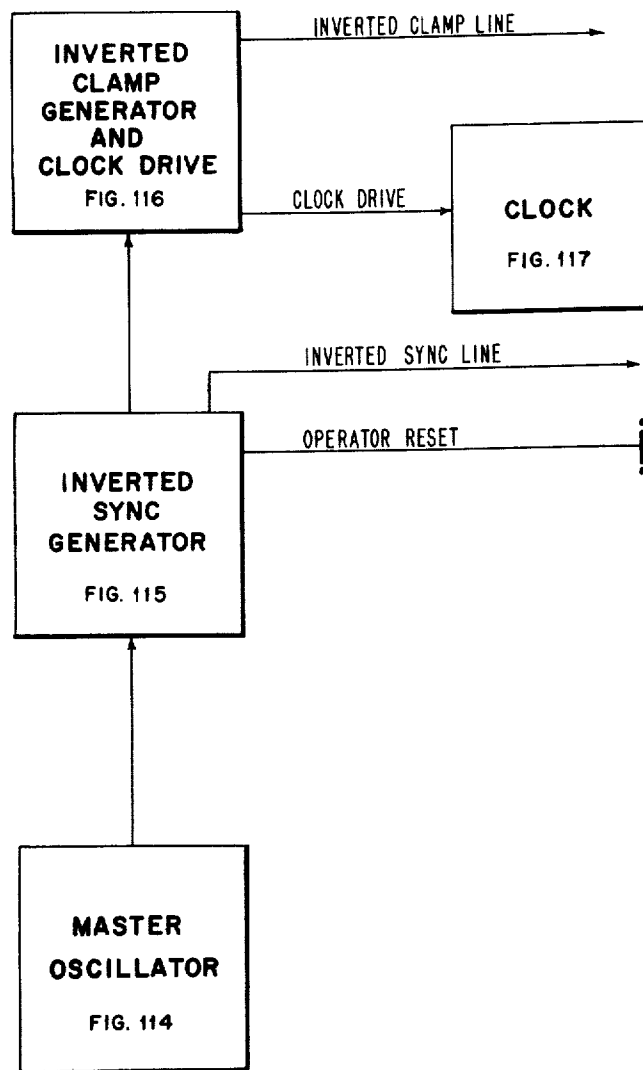
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FIG. 112

PRIMARY DRIVE CIRCUITS



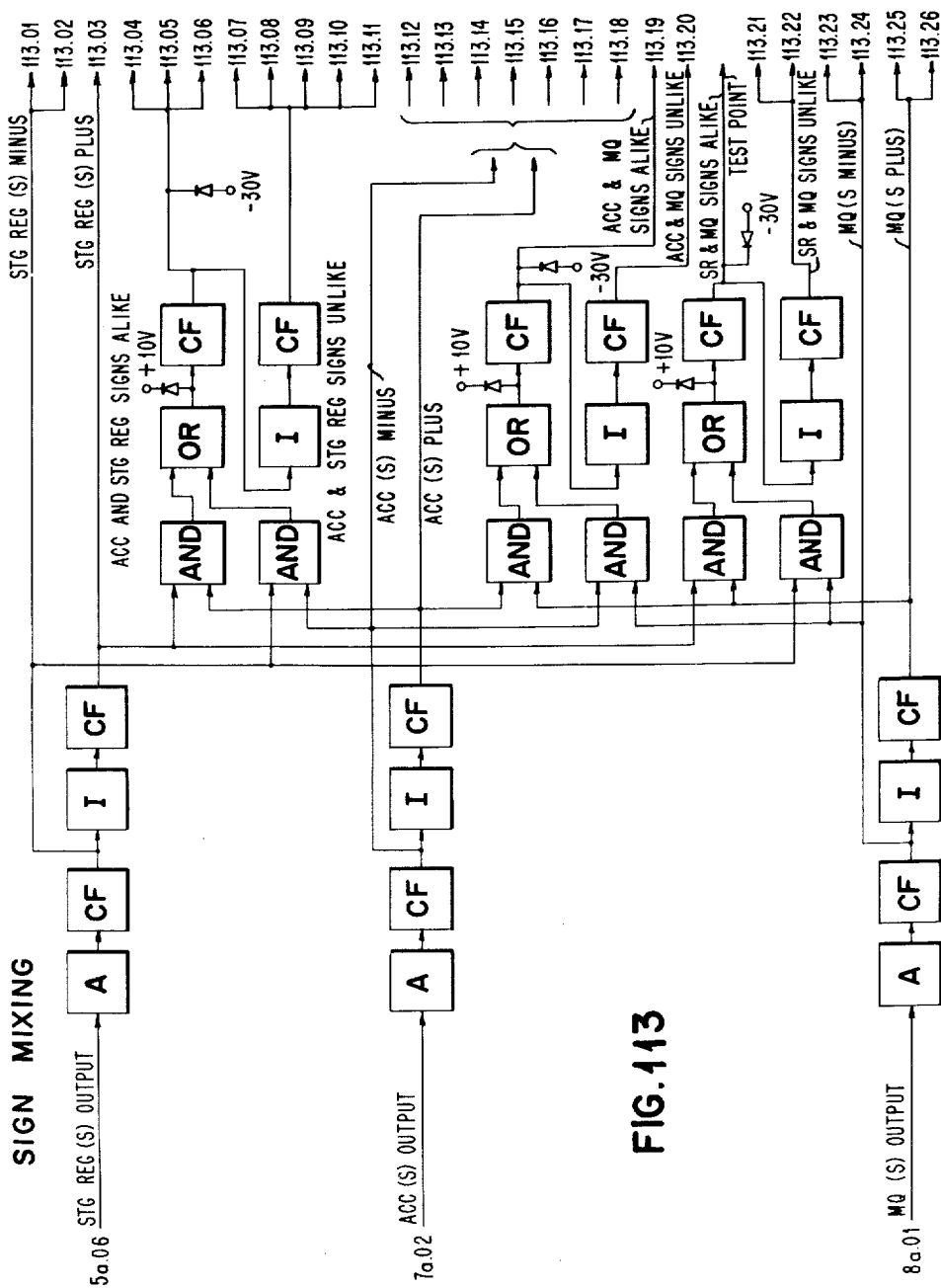
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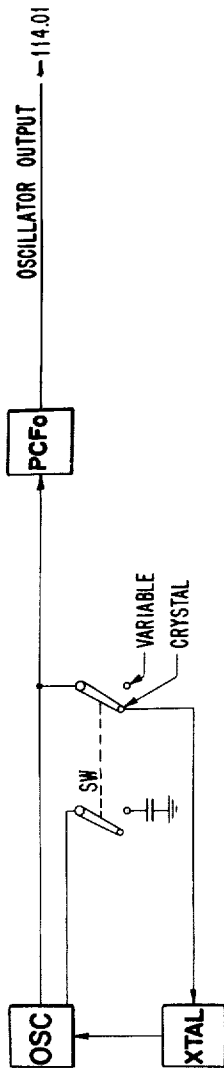
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FIG. 114

MASTER OSCILLATOR



INVERTED CLAMP GENERATOR AND CLOCK DRIVE

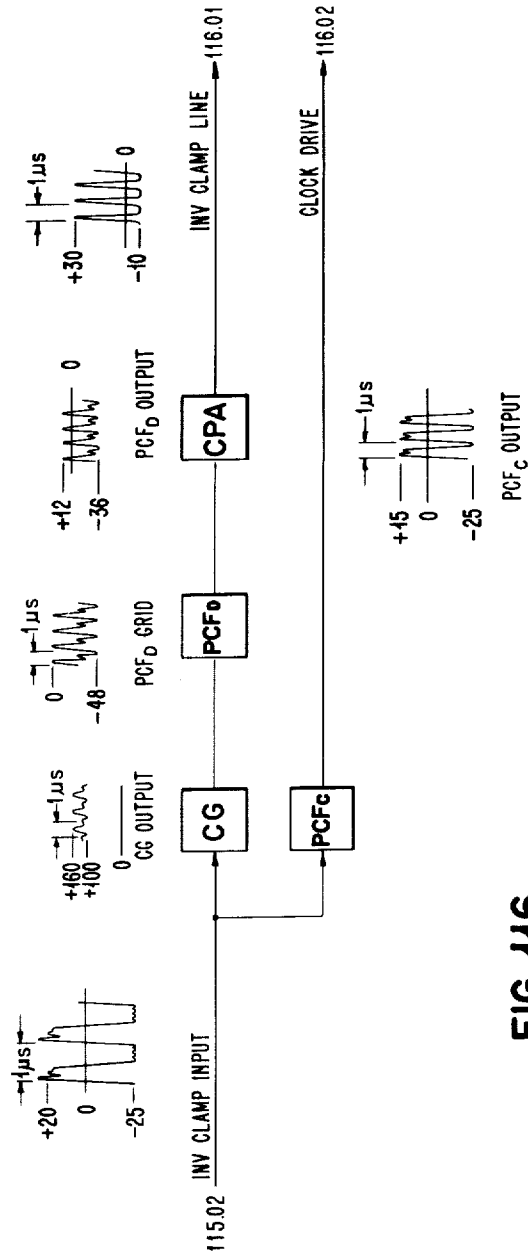


FIG. 116

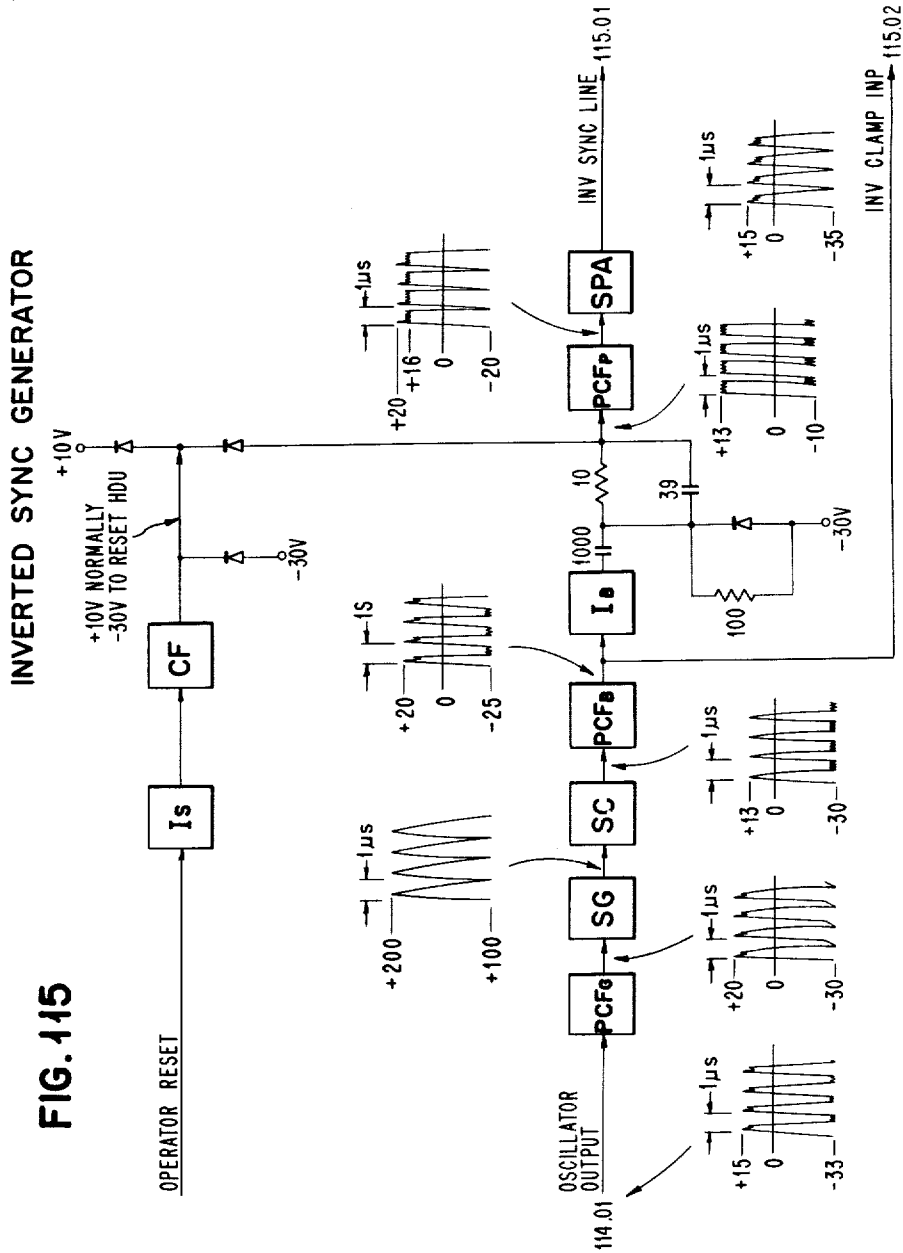
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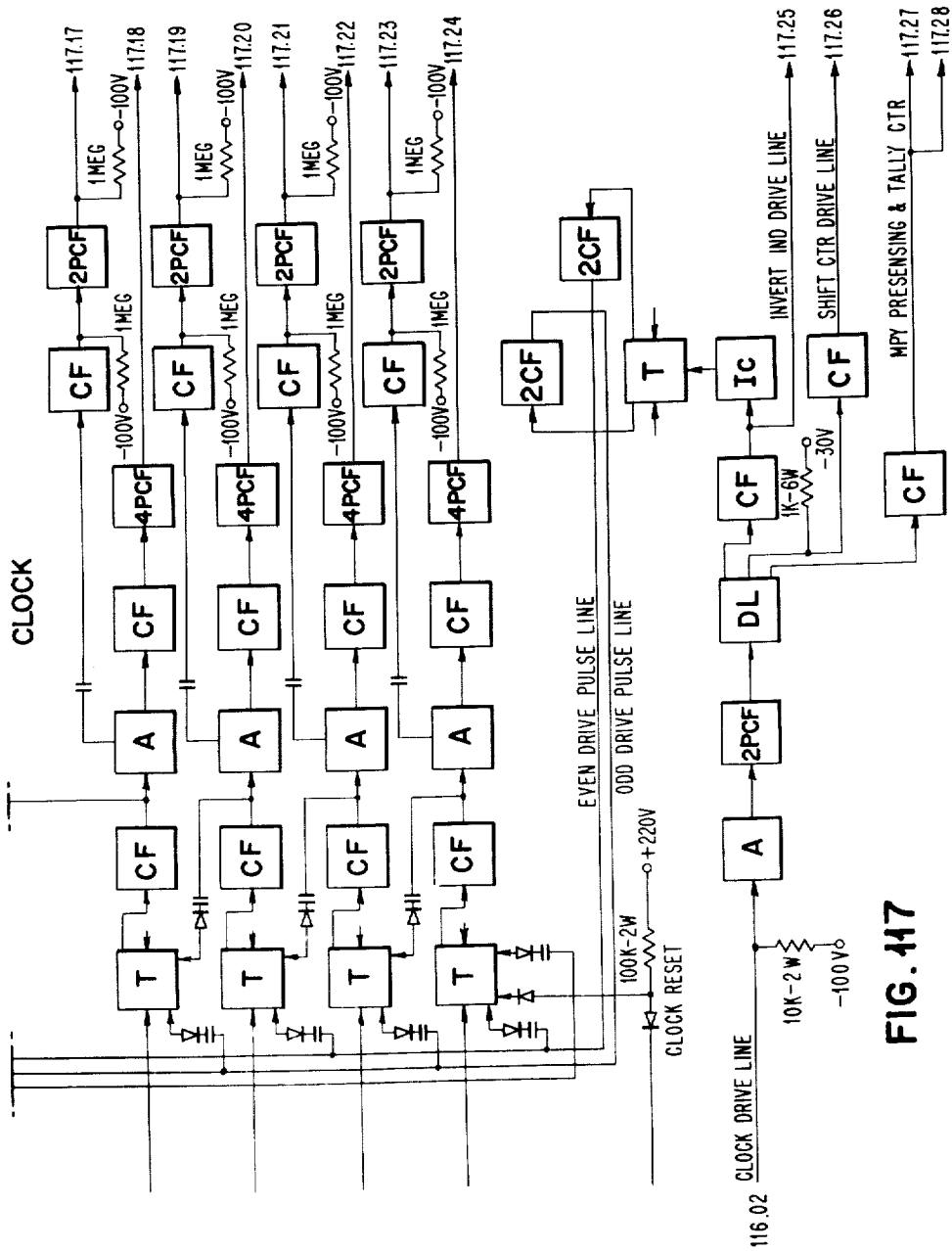


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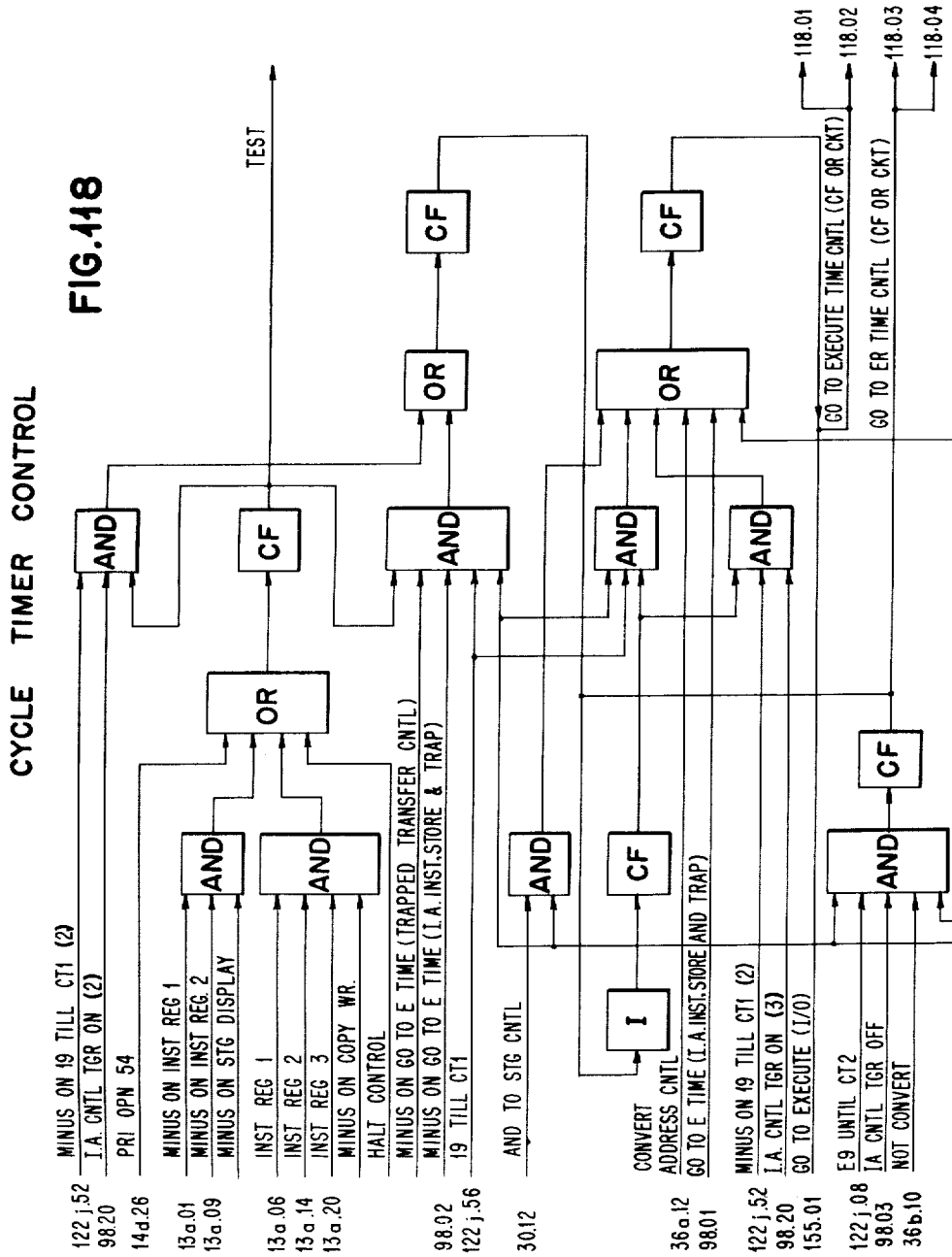
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[illegible]

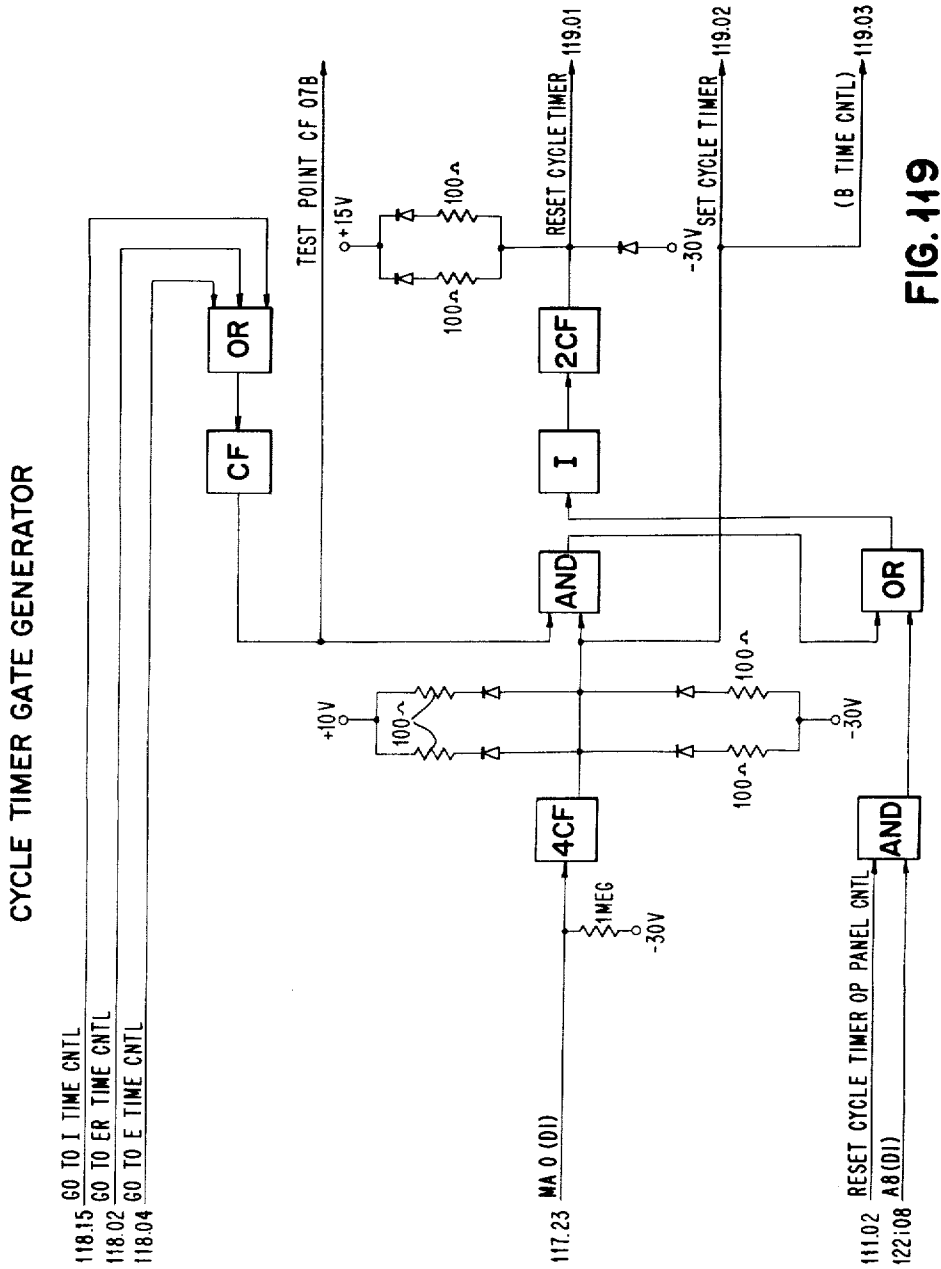
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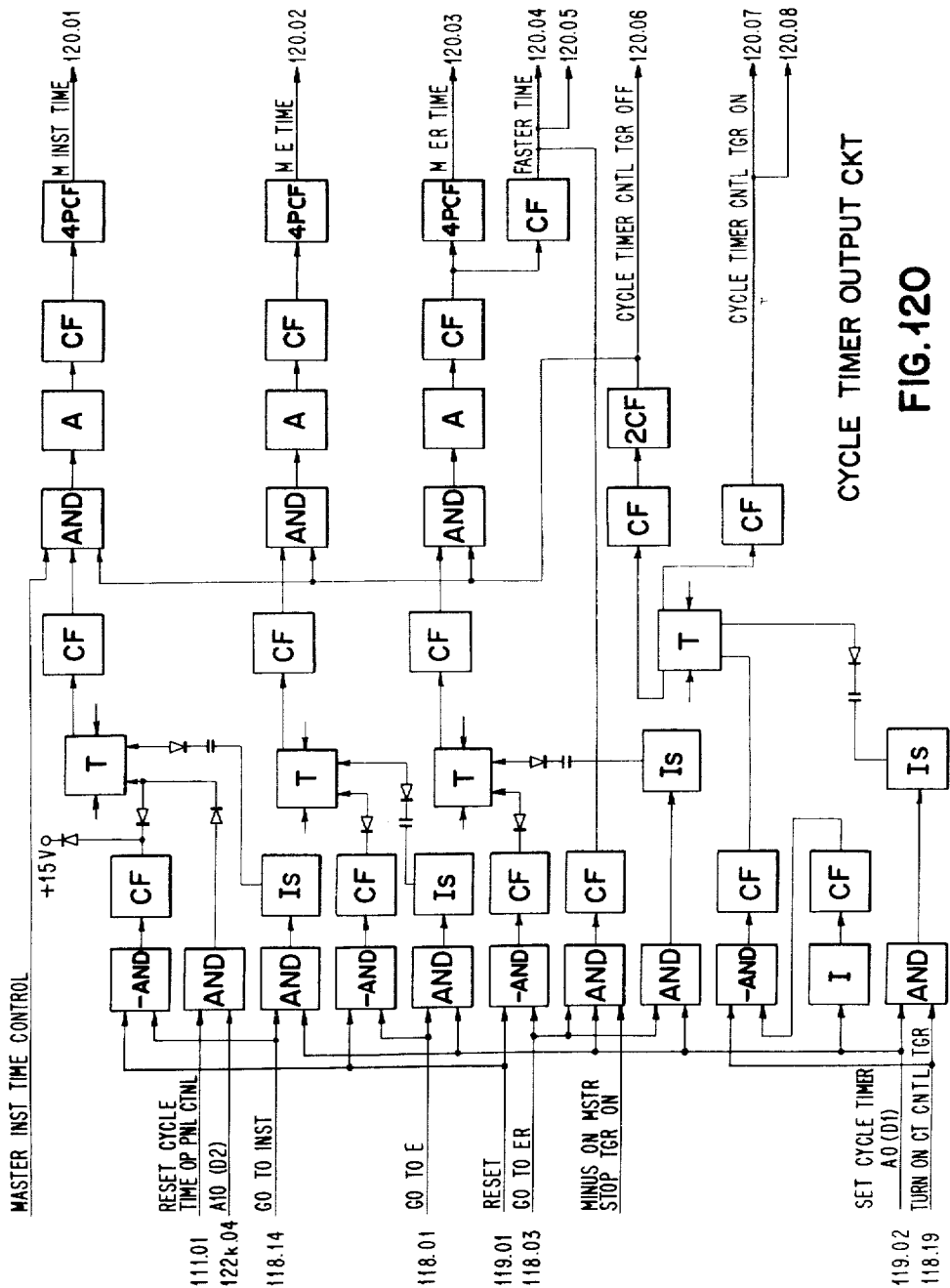
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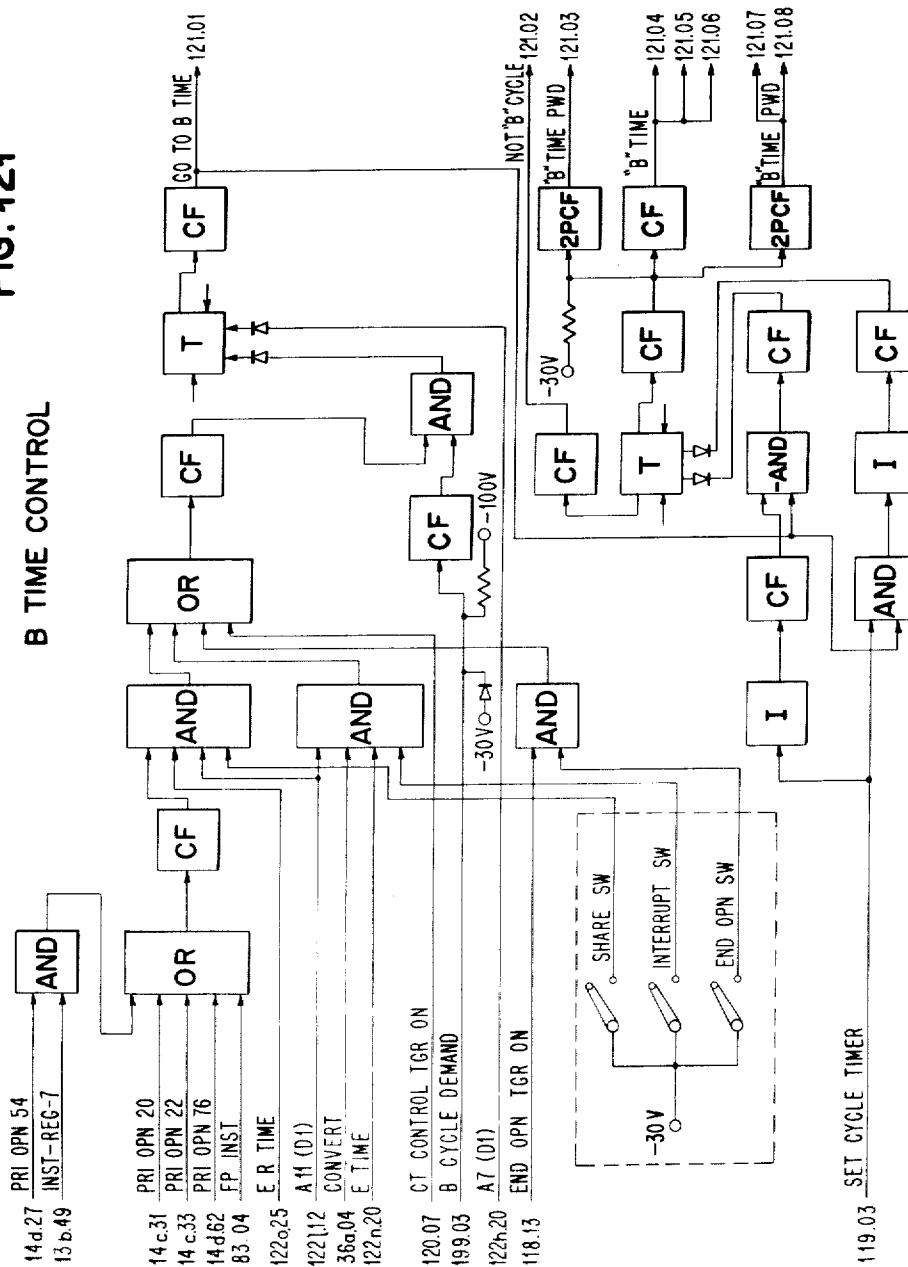
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**FIG. 121**



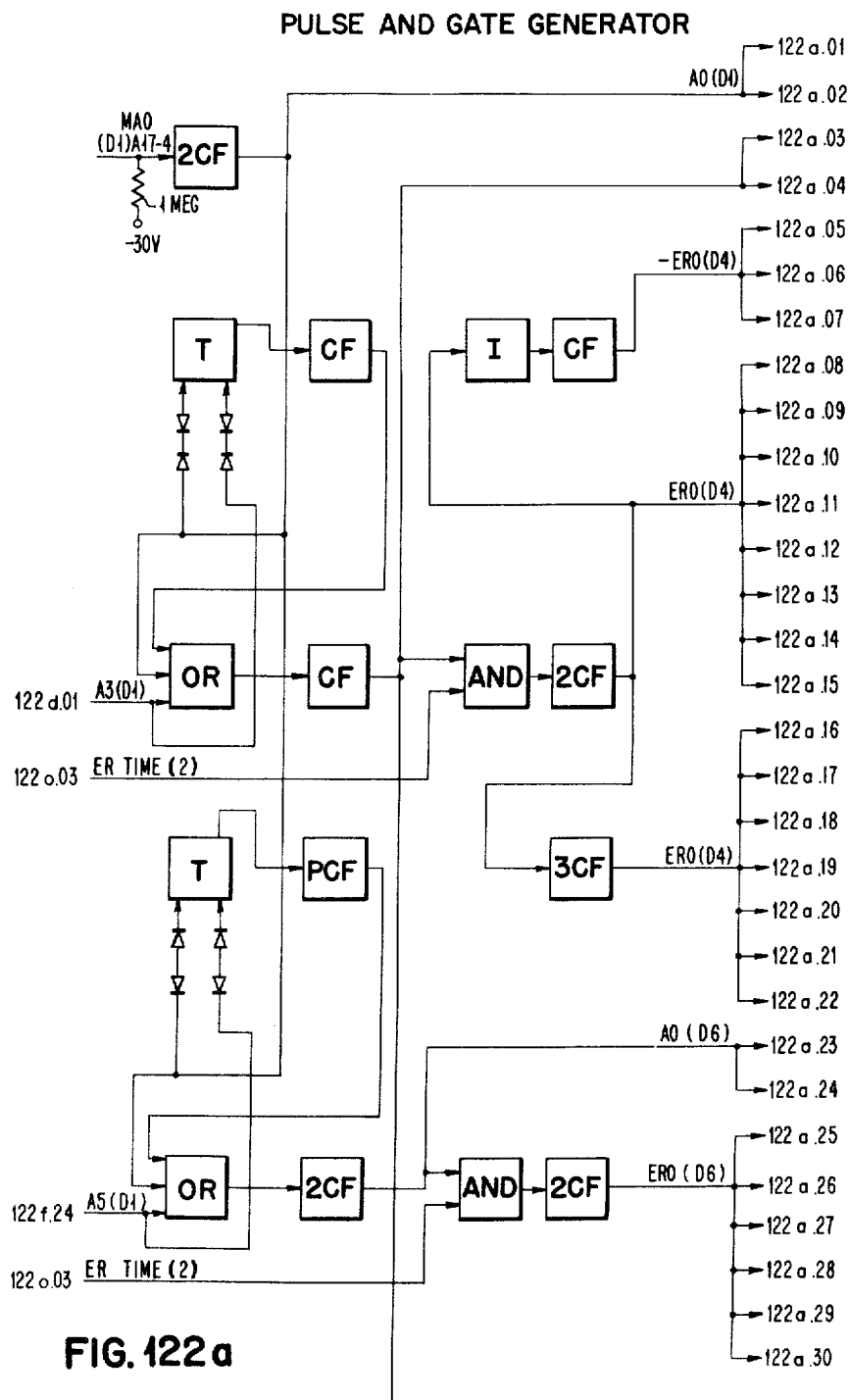
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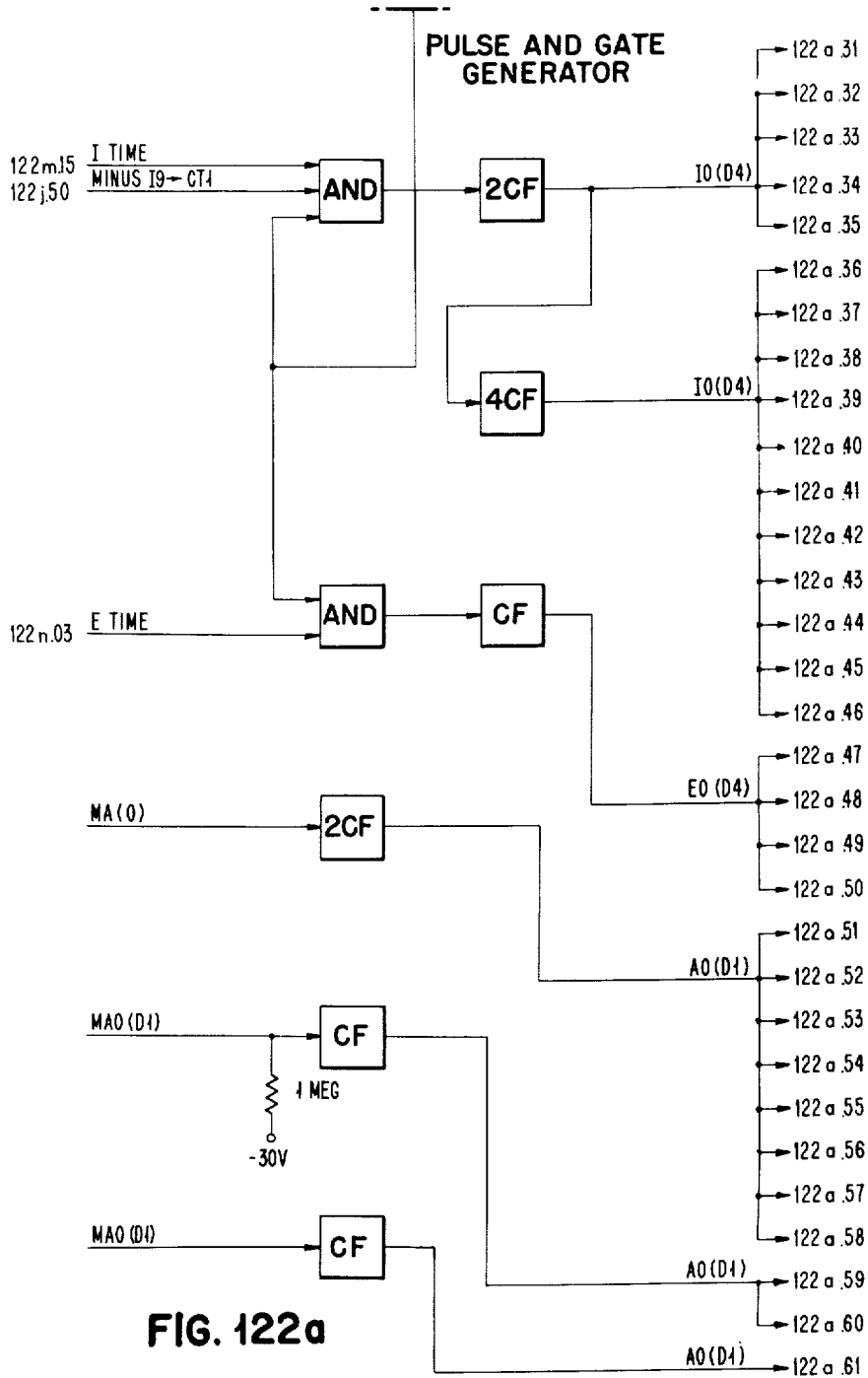


FIG. 122a

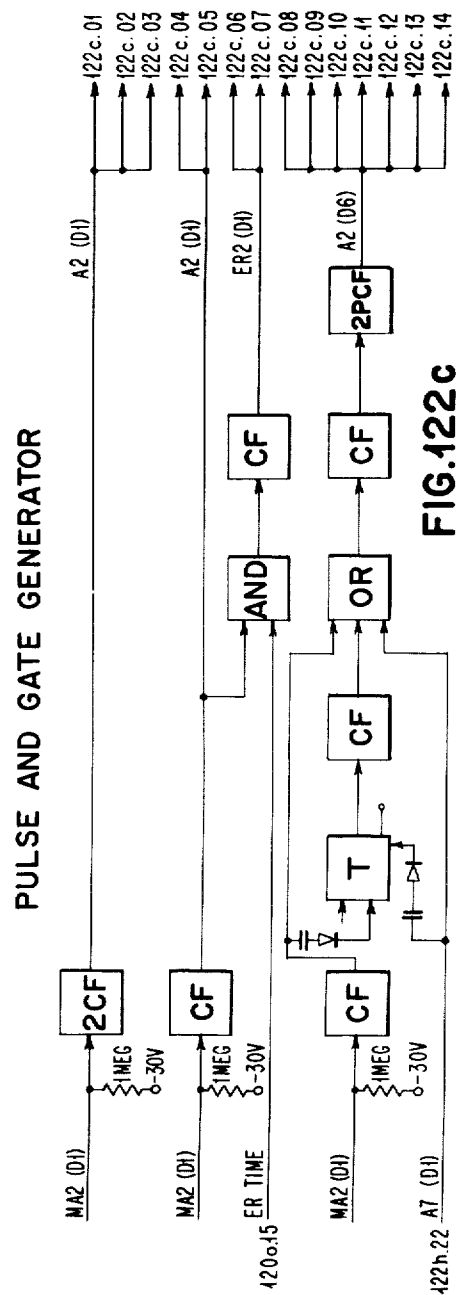
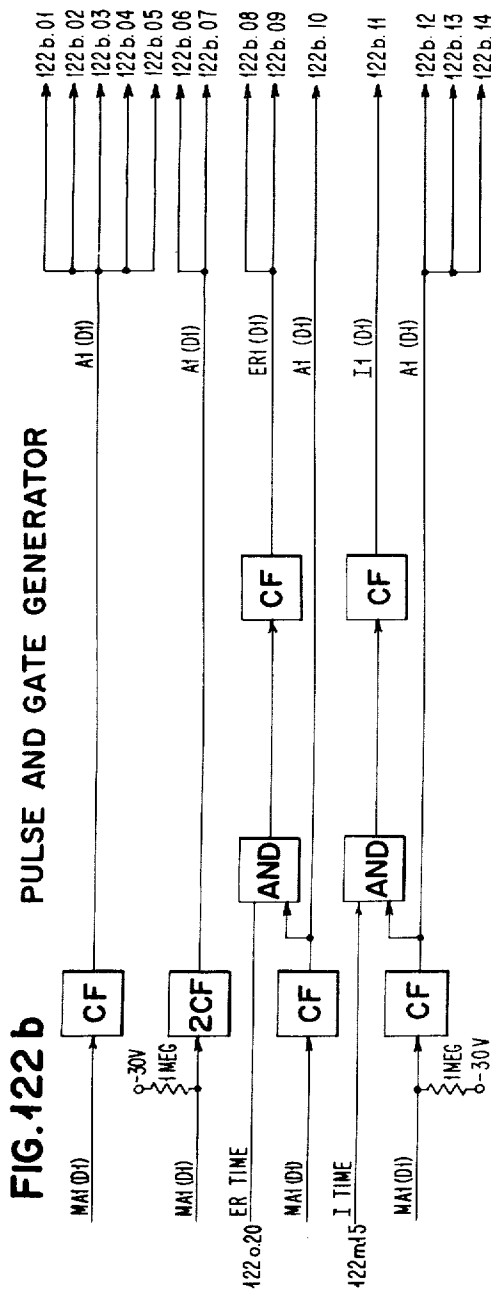
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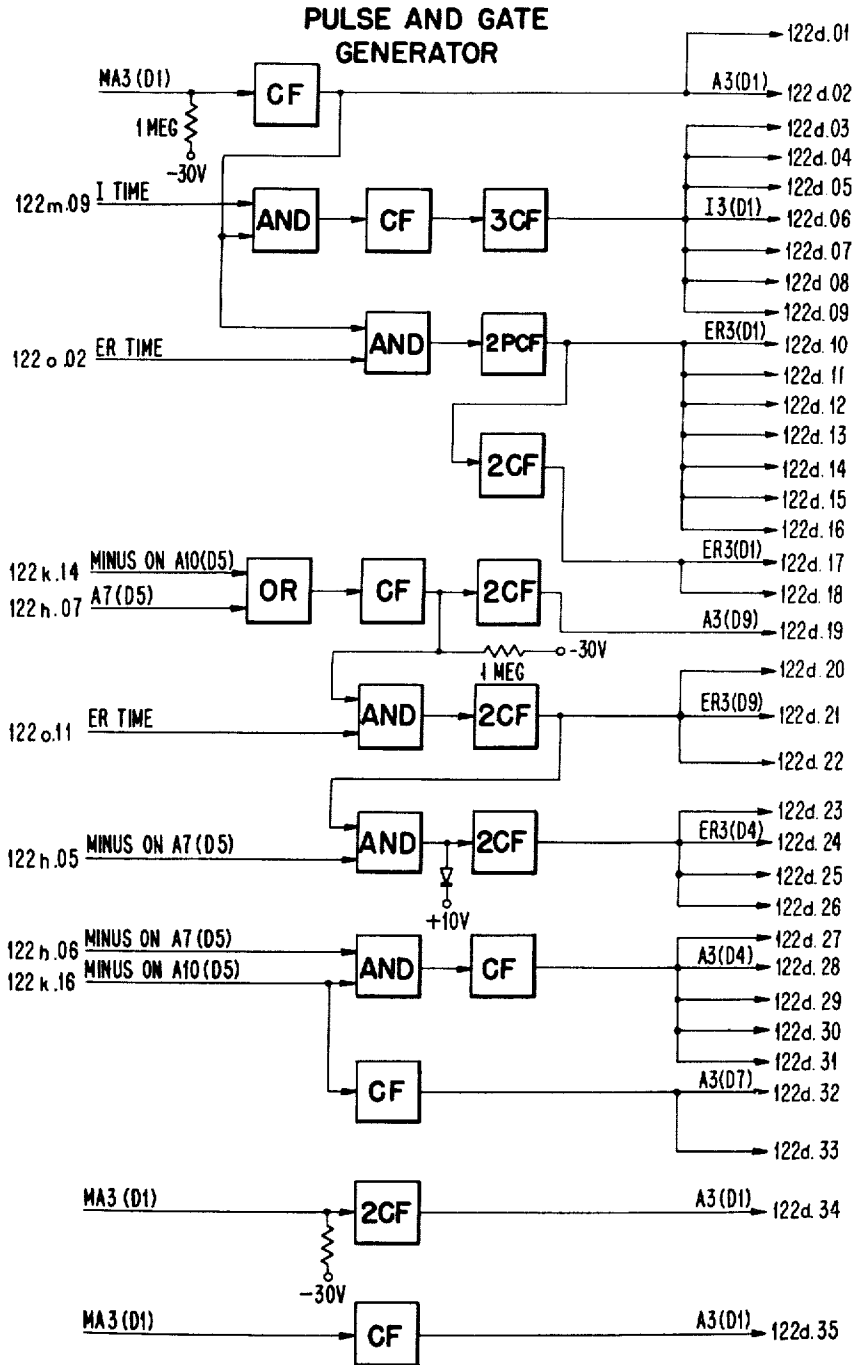


FIG. 122d

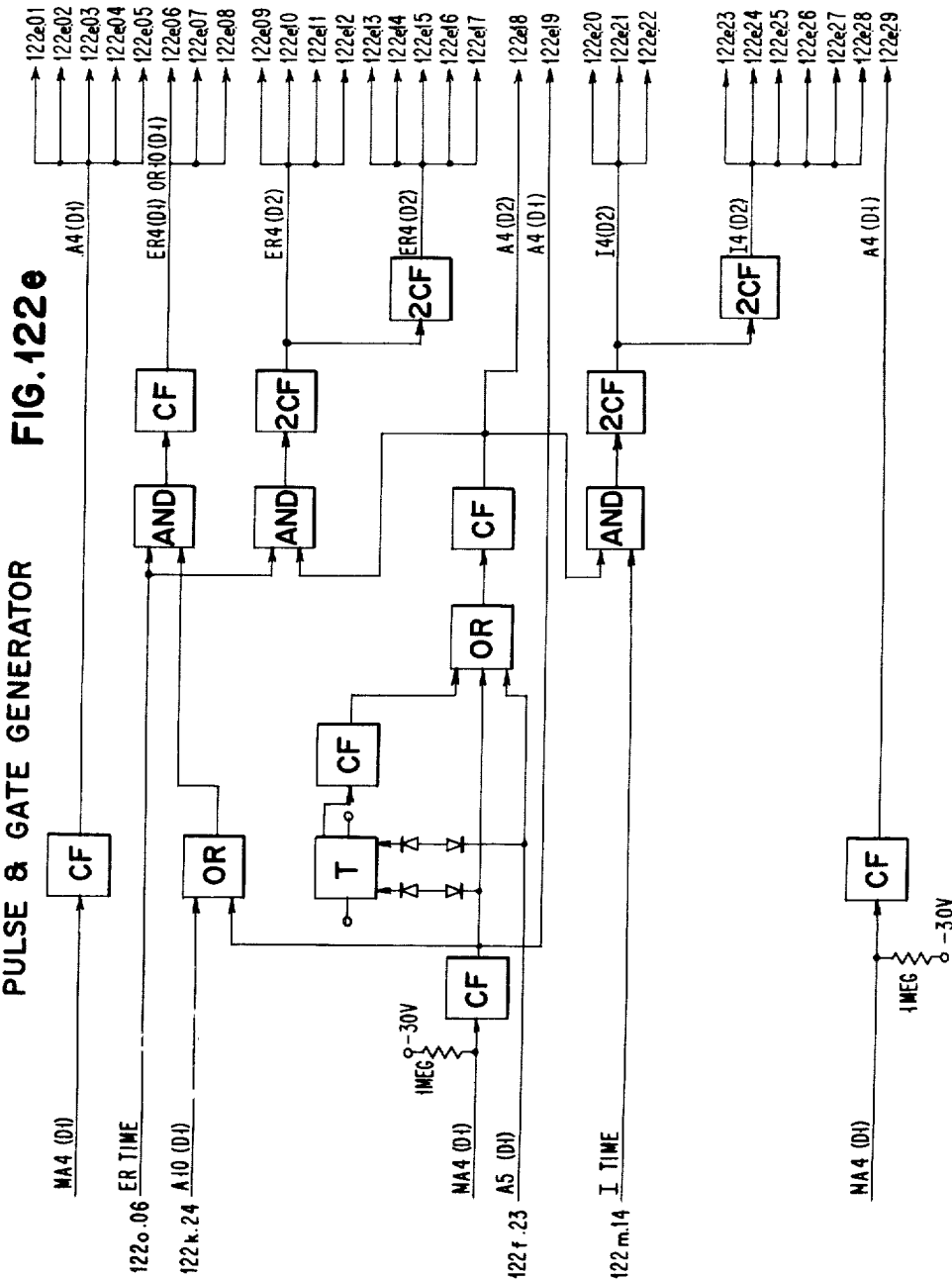
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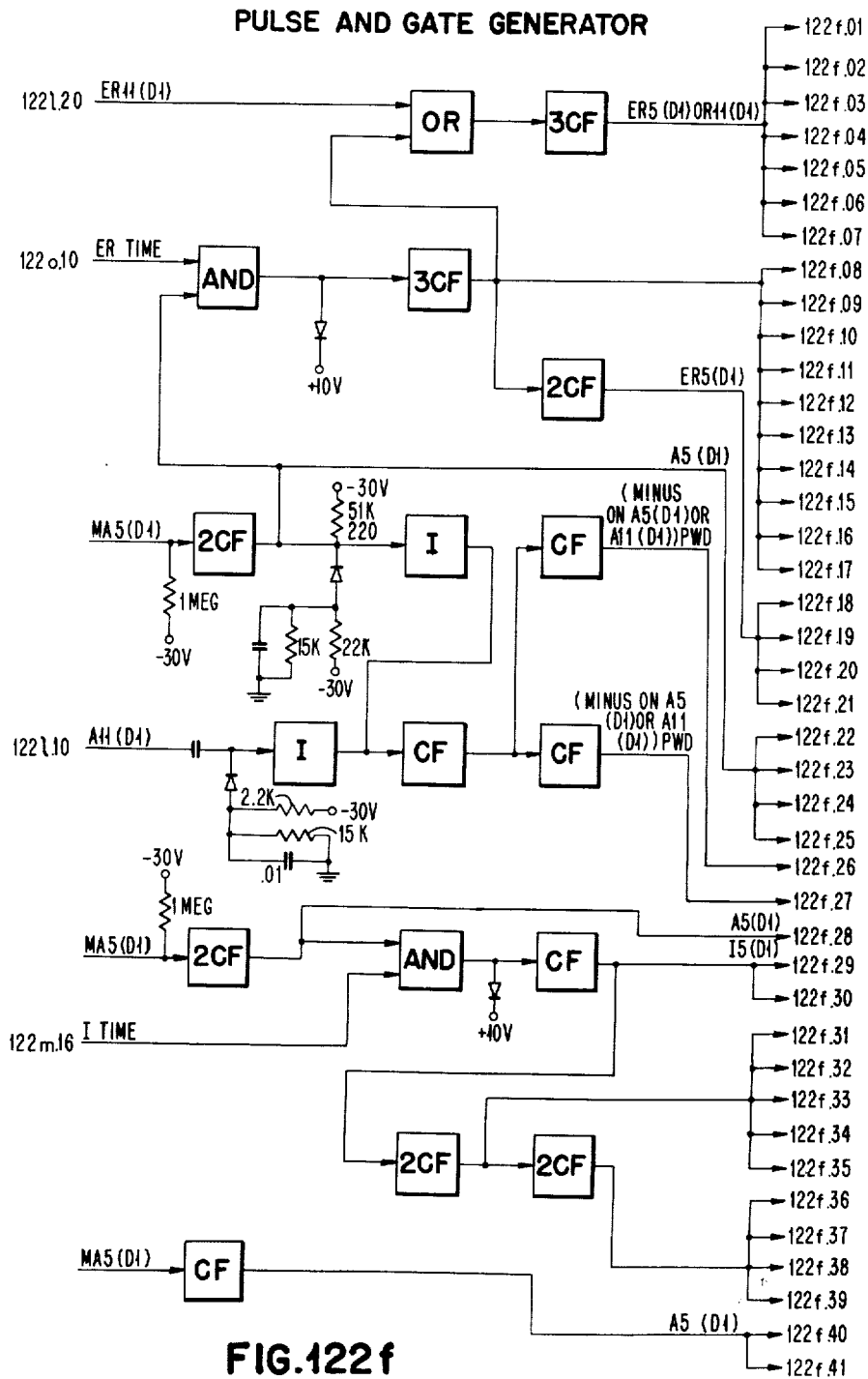
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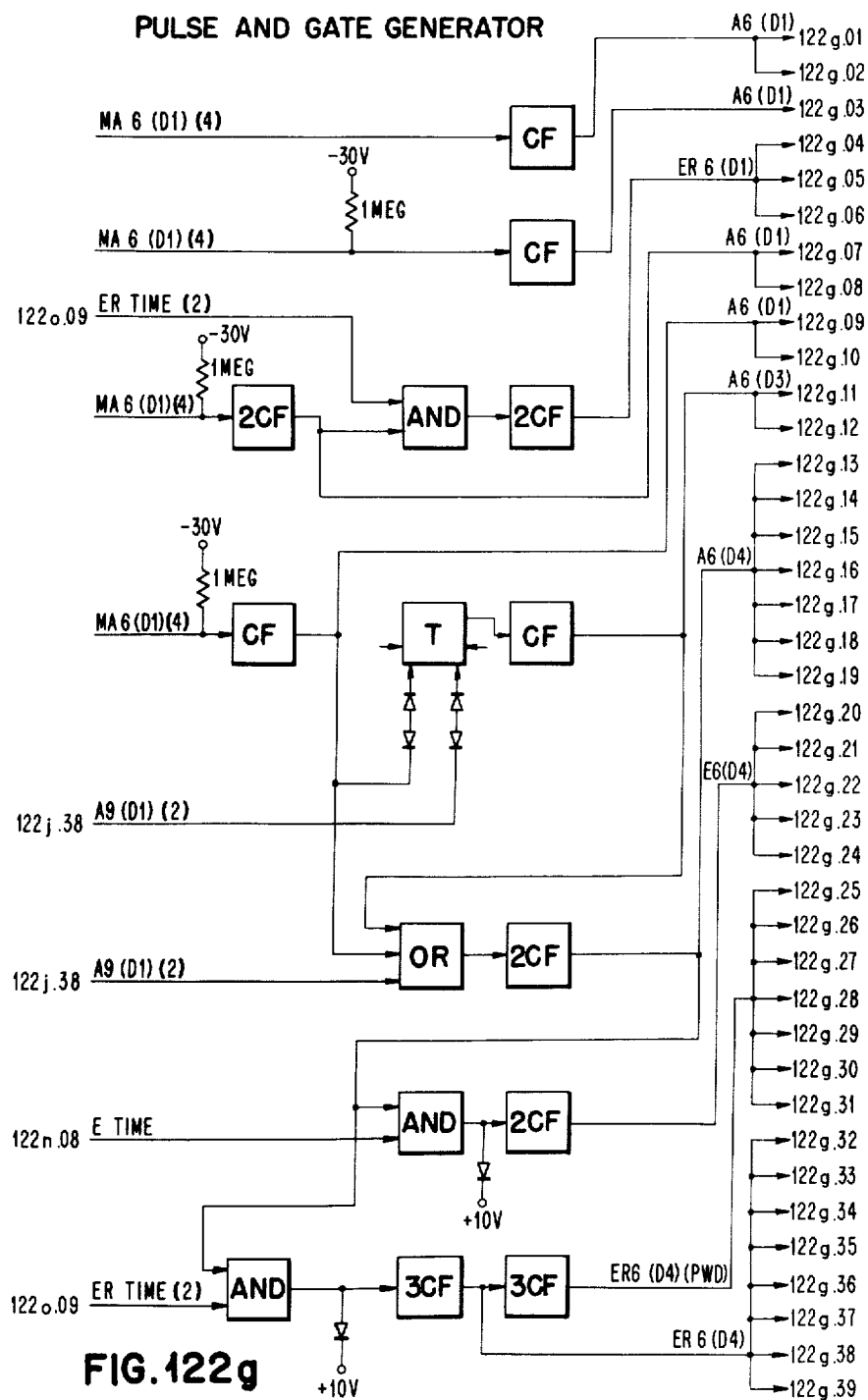
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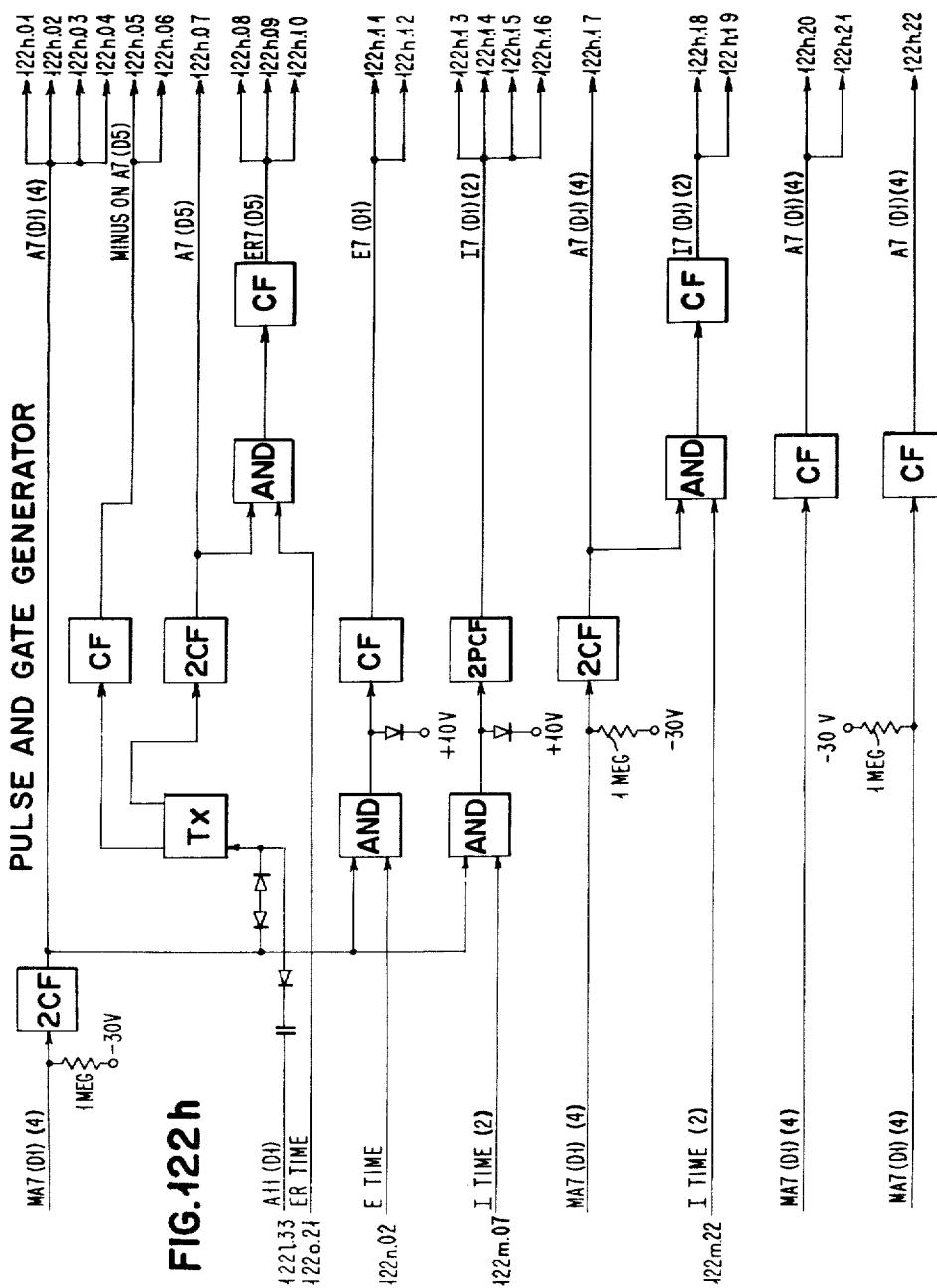
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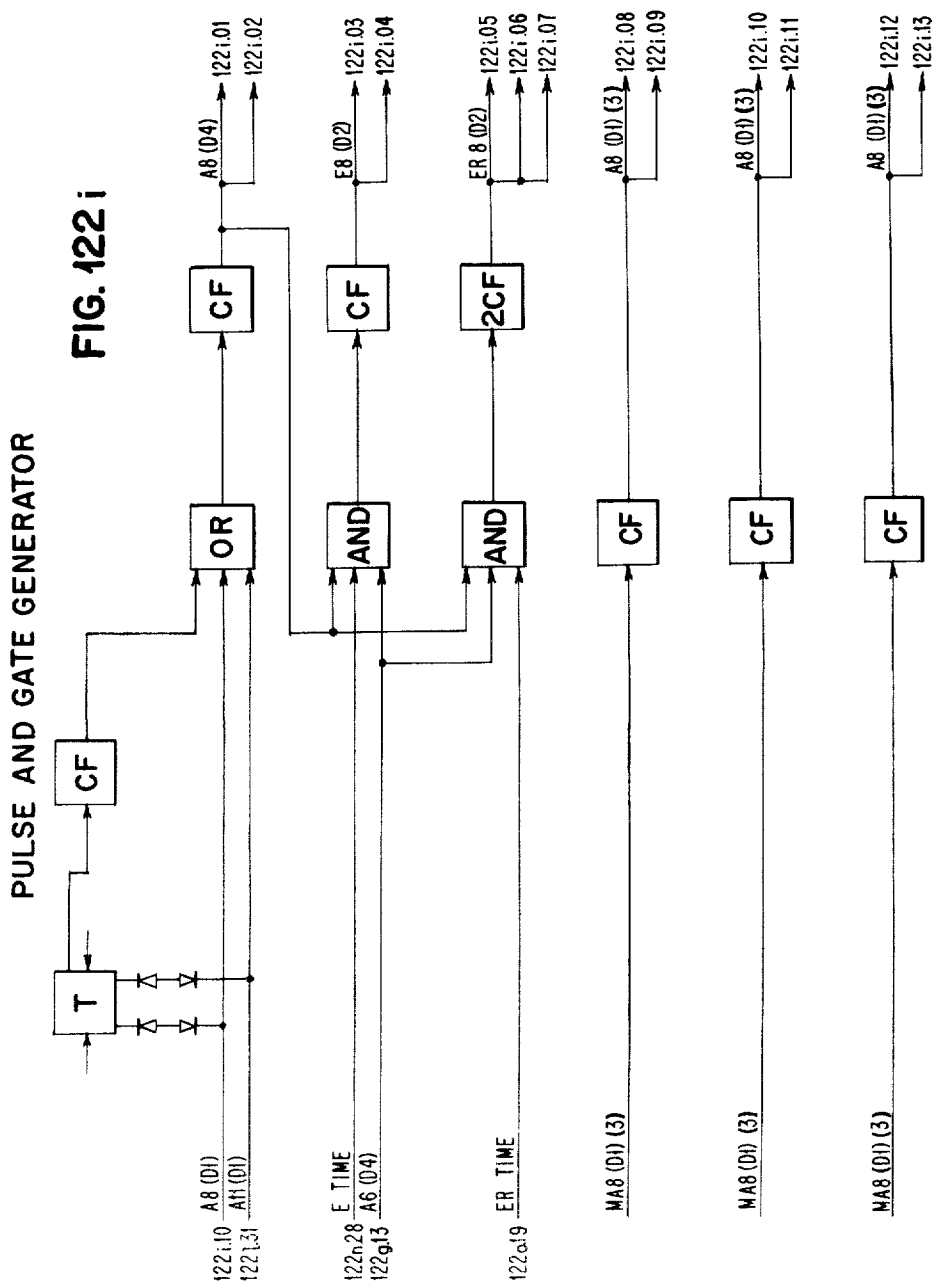
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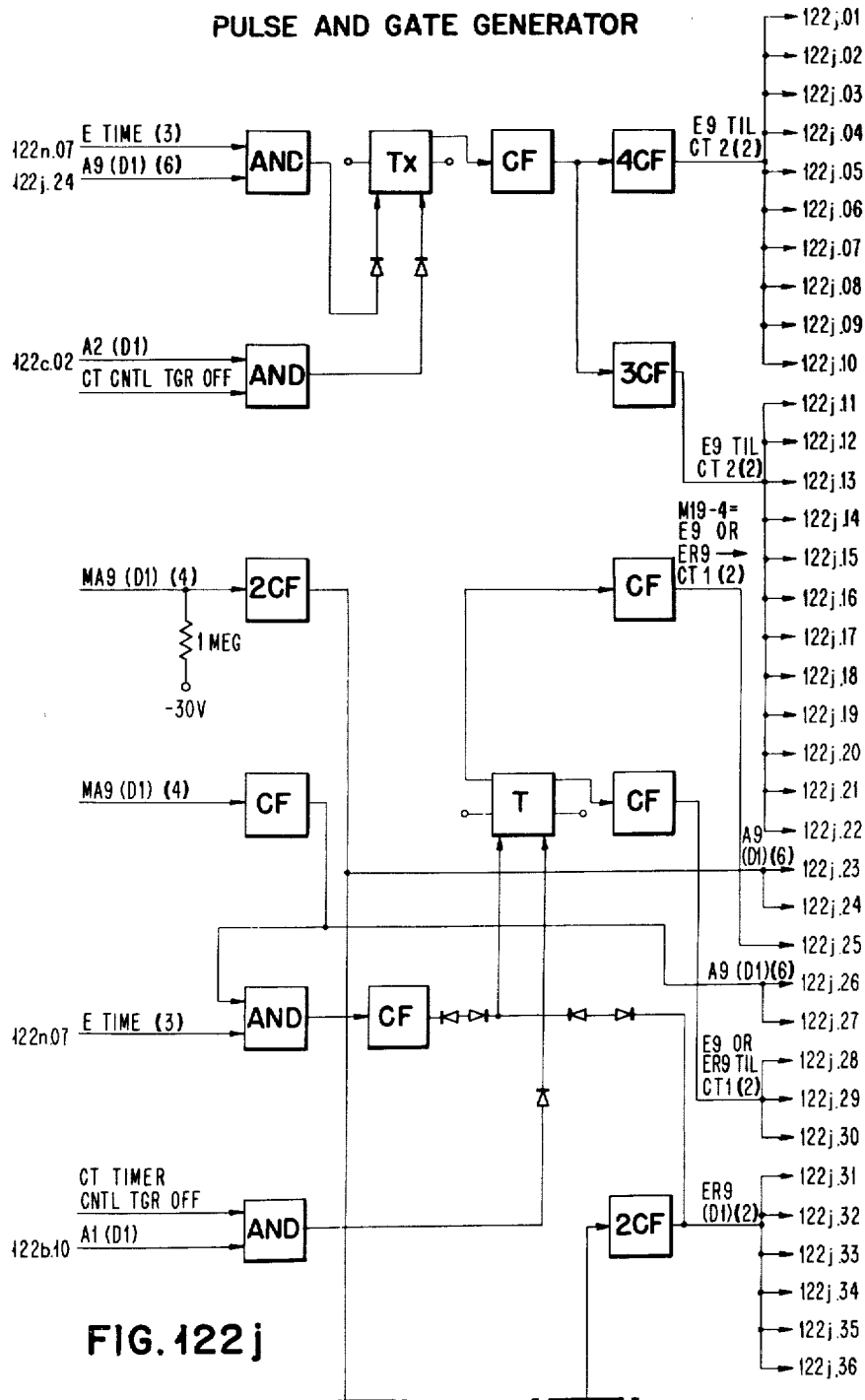
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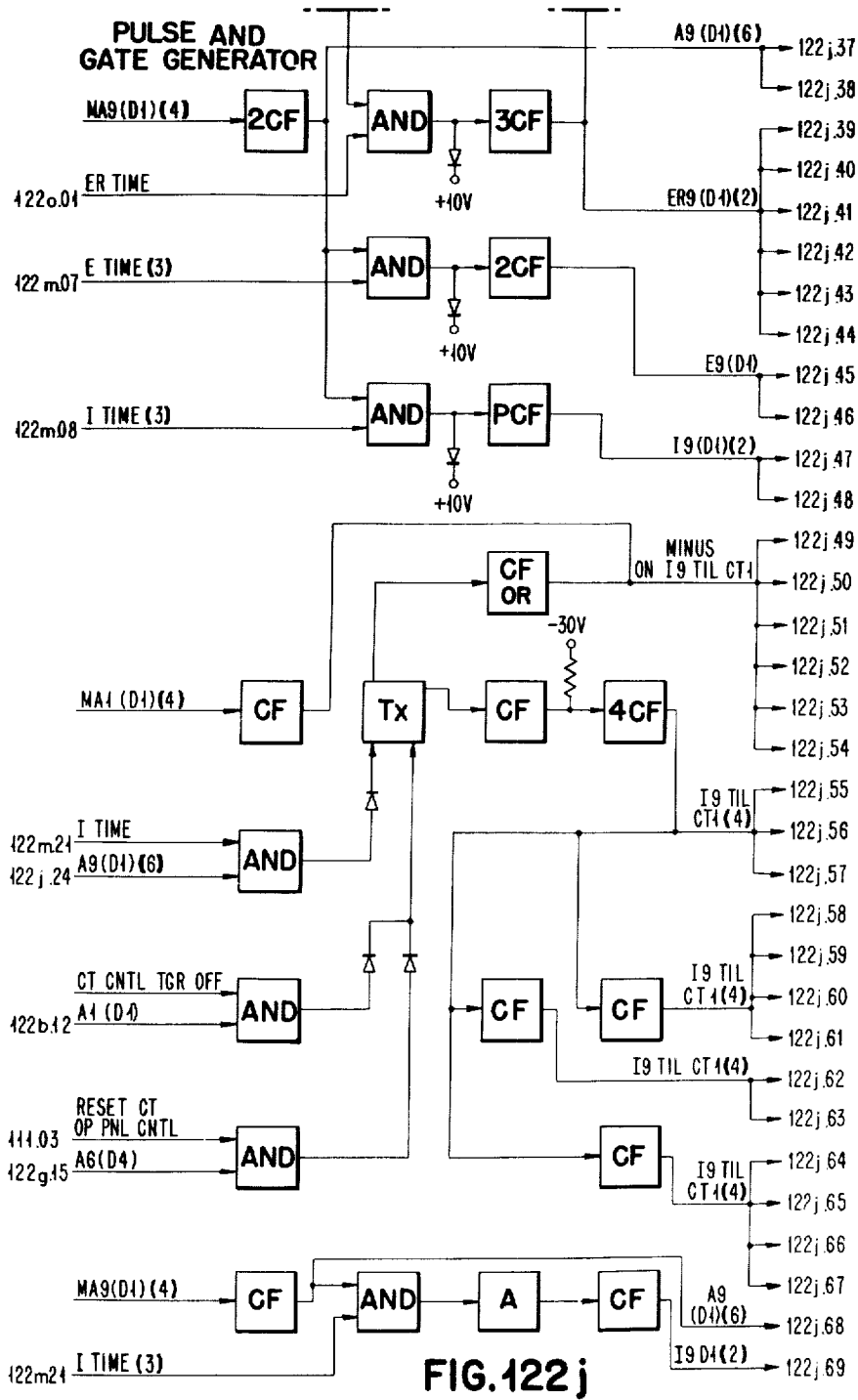
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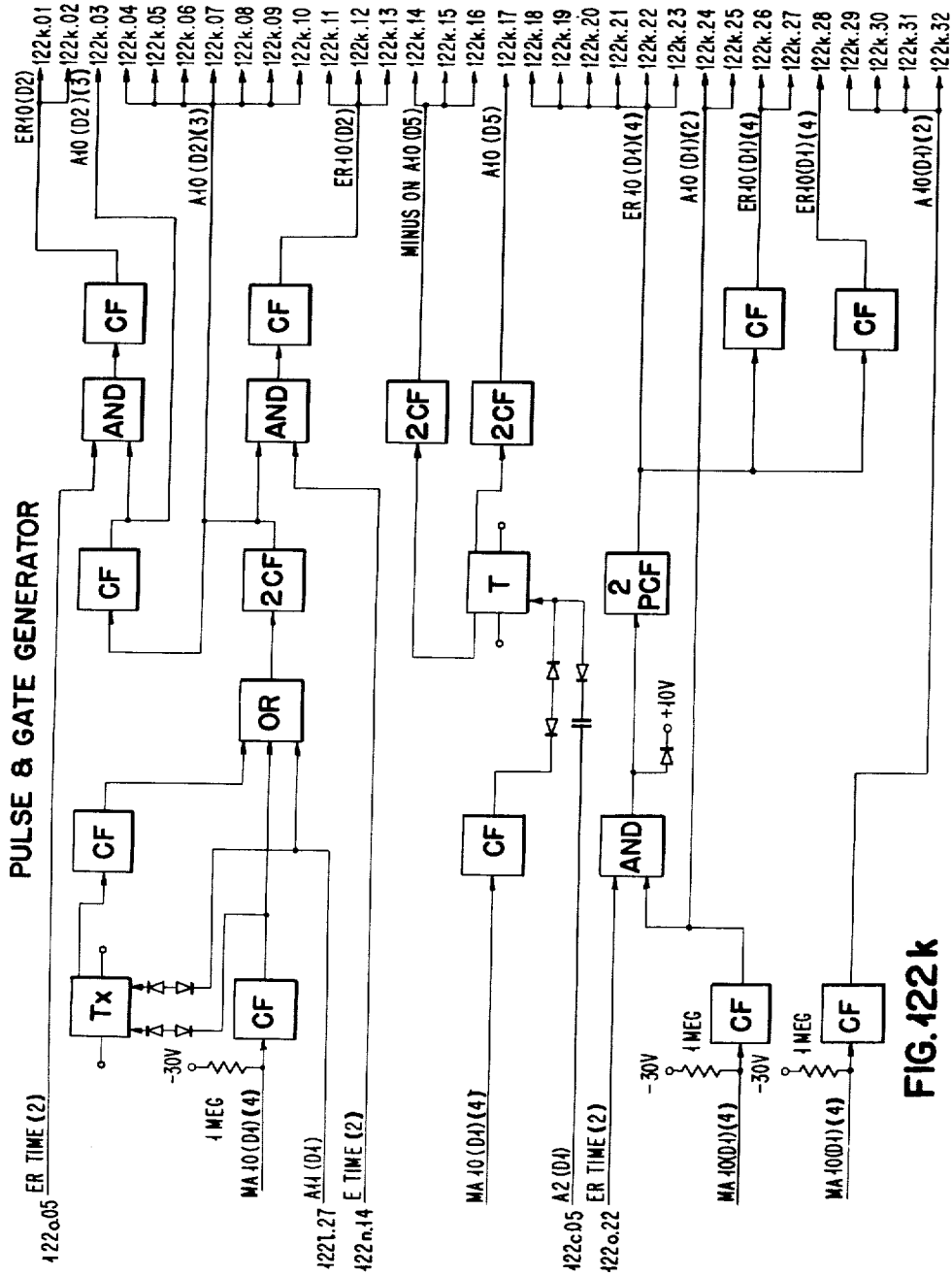
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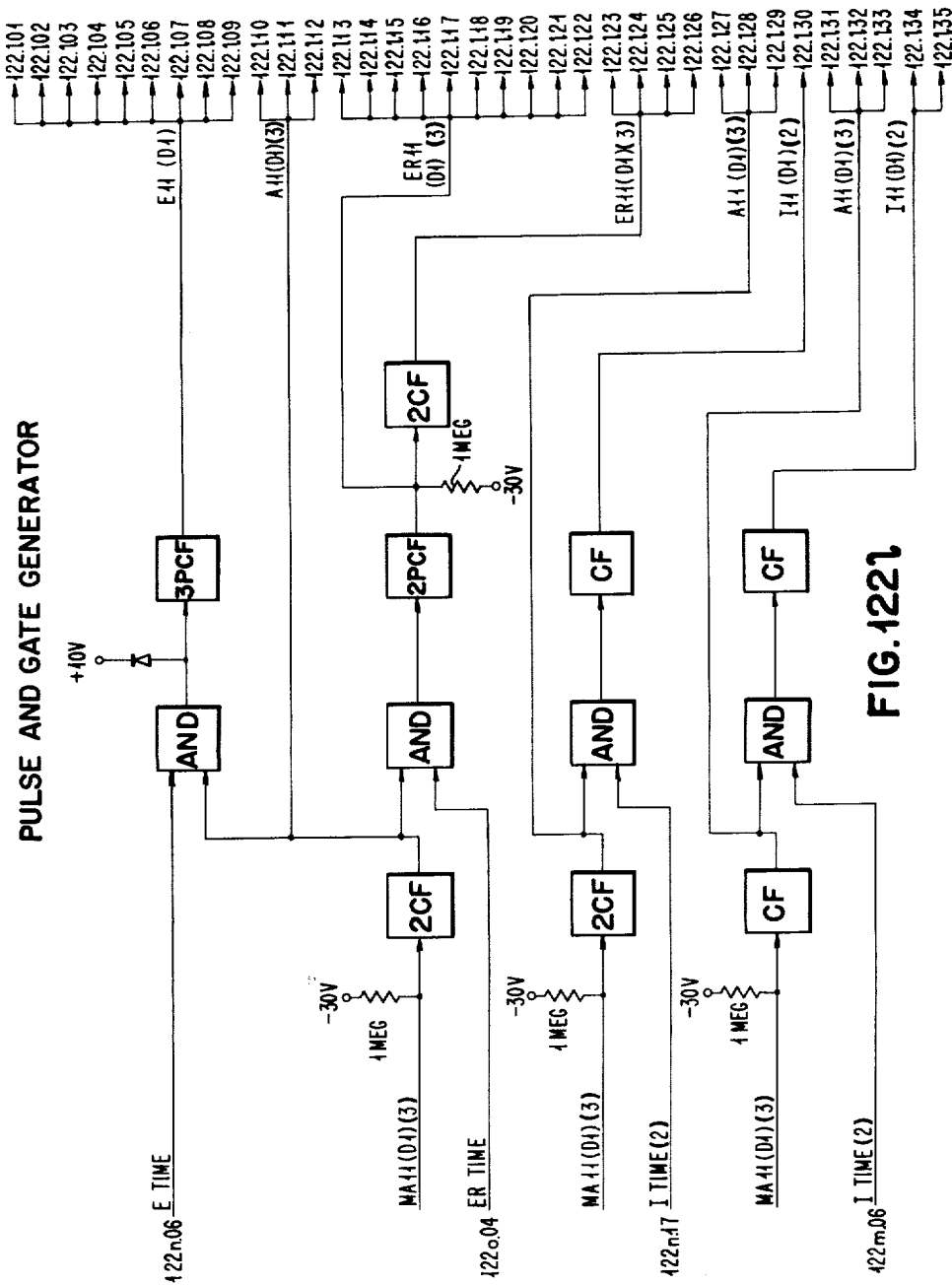
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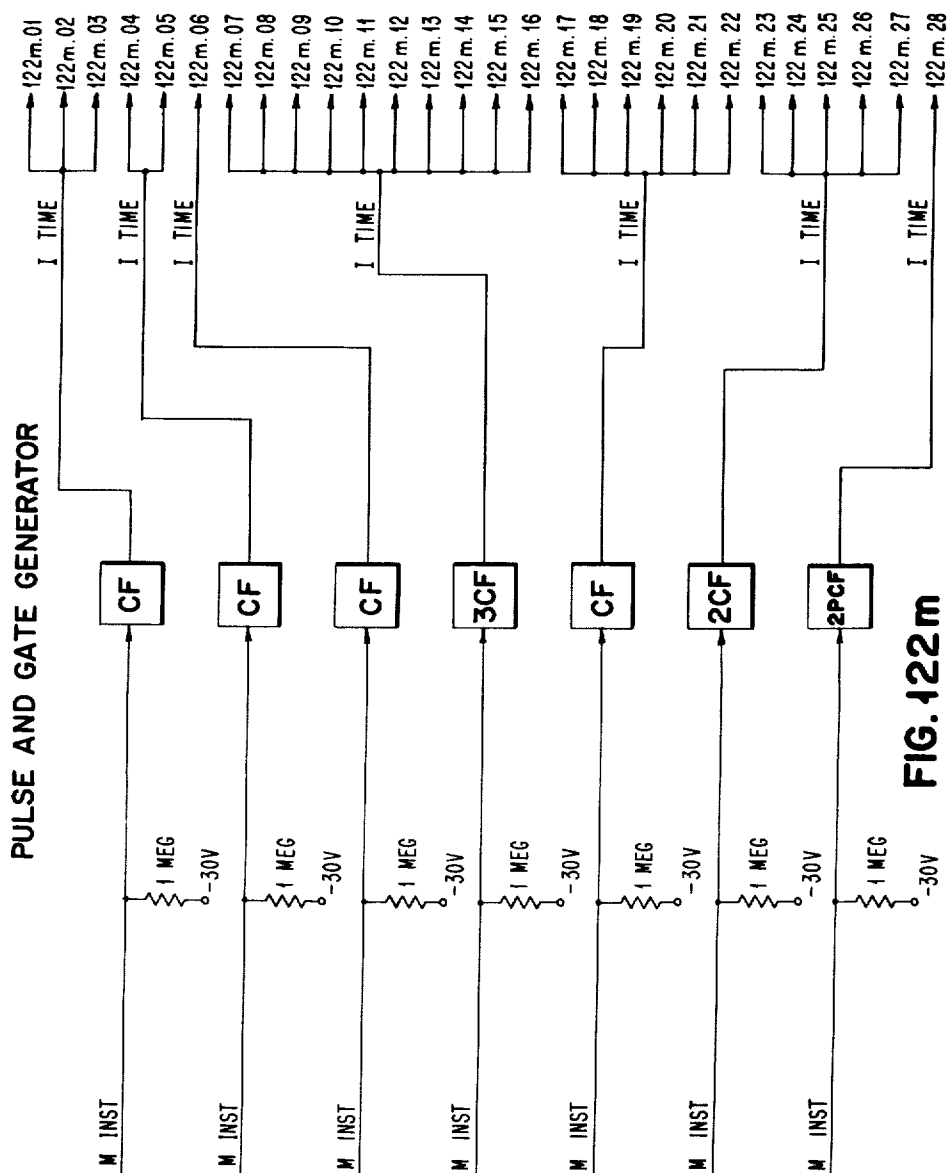
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DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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PULSE AND GATE GENERATOR

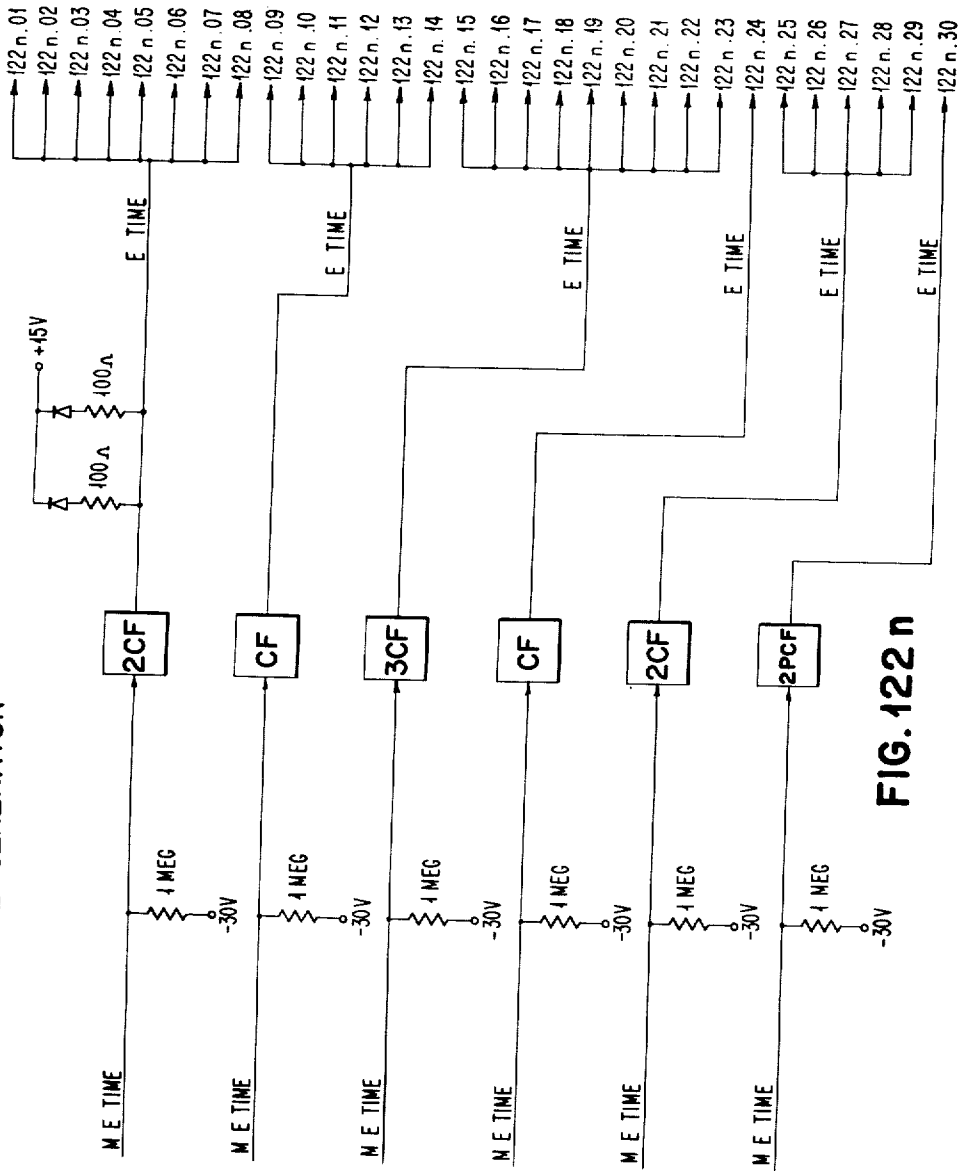


FIG. 122 n

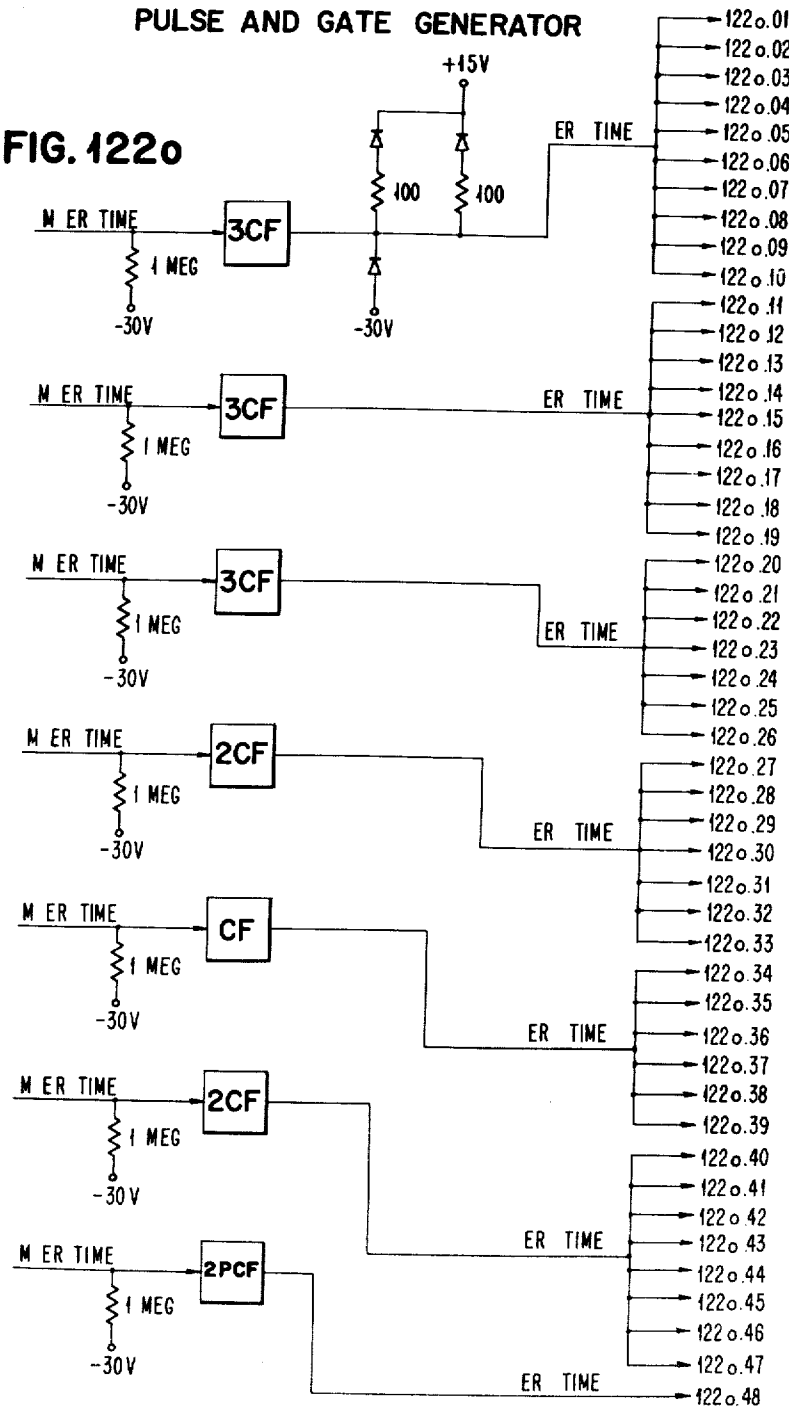
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

3,019,976

Filed Dec. 26, 1957

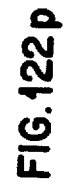
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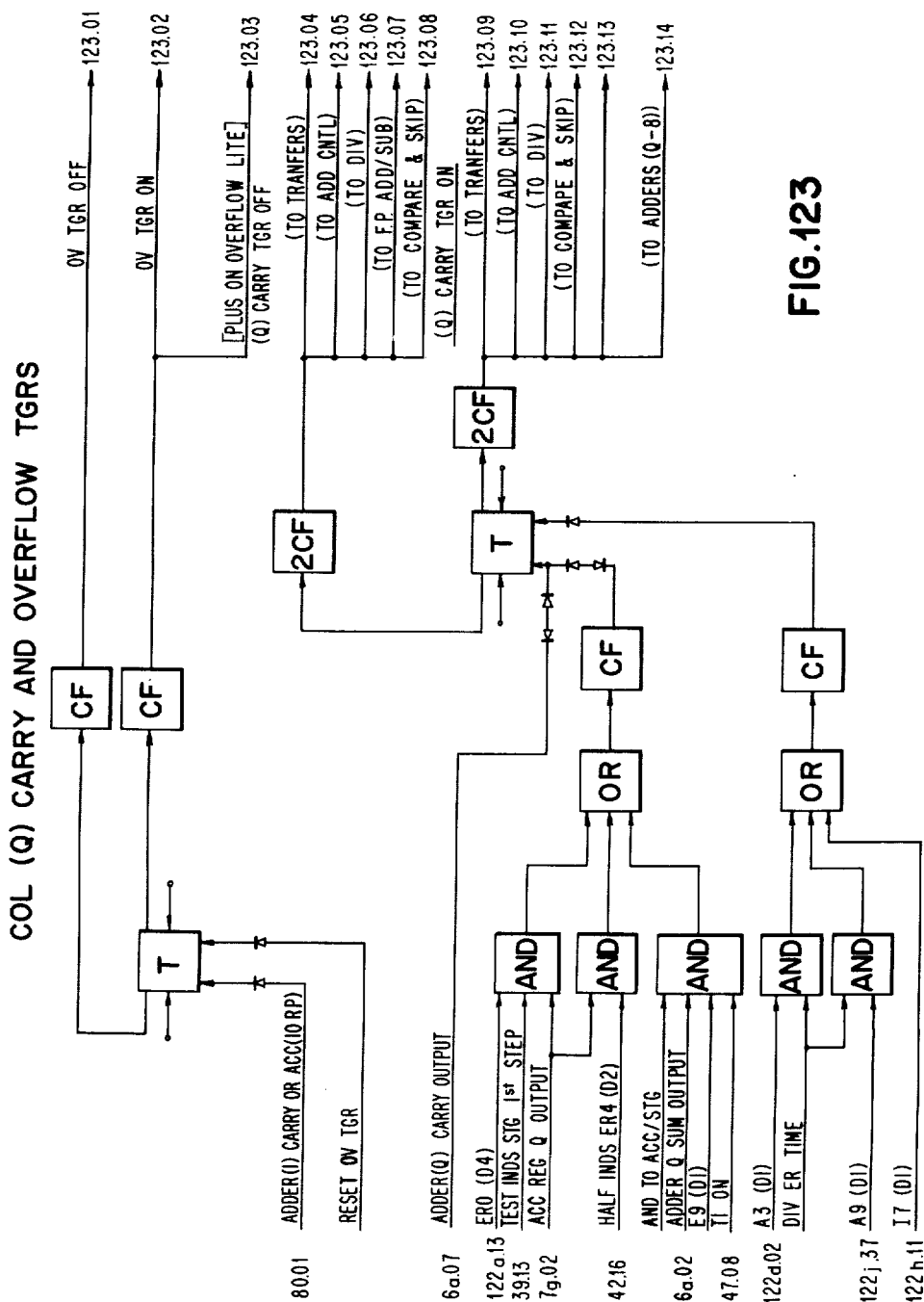
247 Sheets-Sheet 216



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**3,019,976**



**FIG. 123**

Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

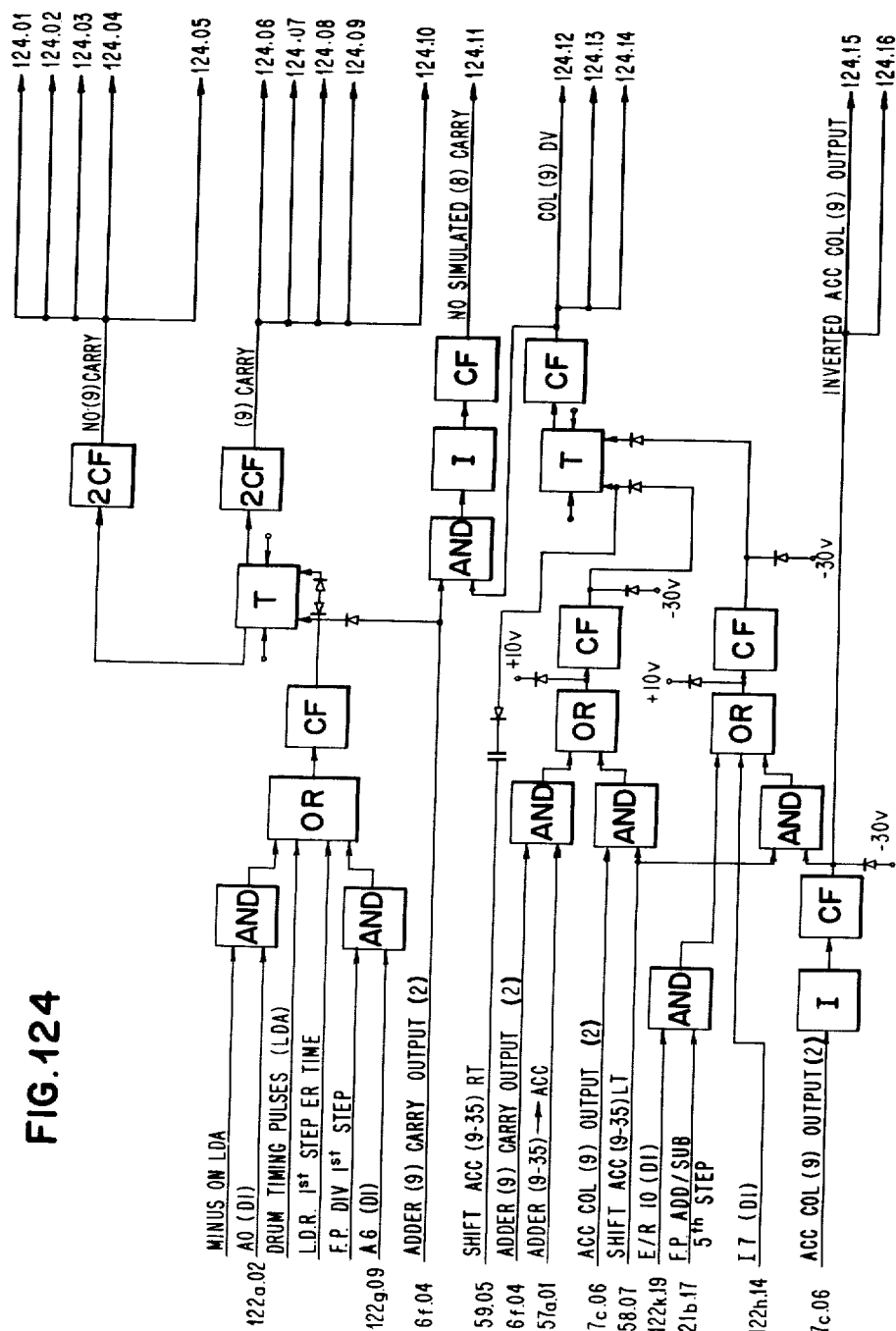
3,019,976

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COLUMN (9) CARRY & OVERFLOW TRIGGERS

FIG. 124



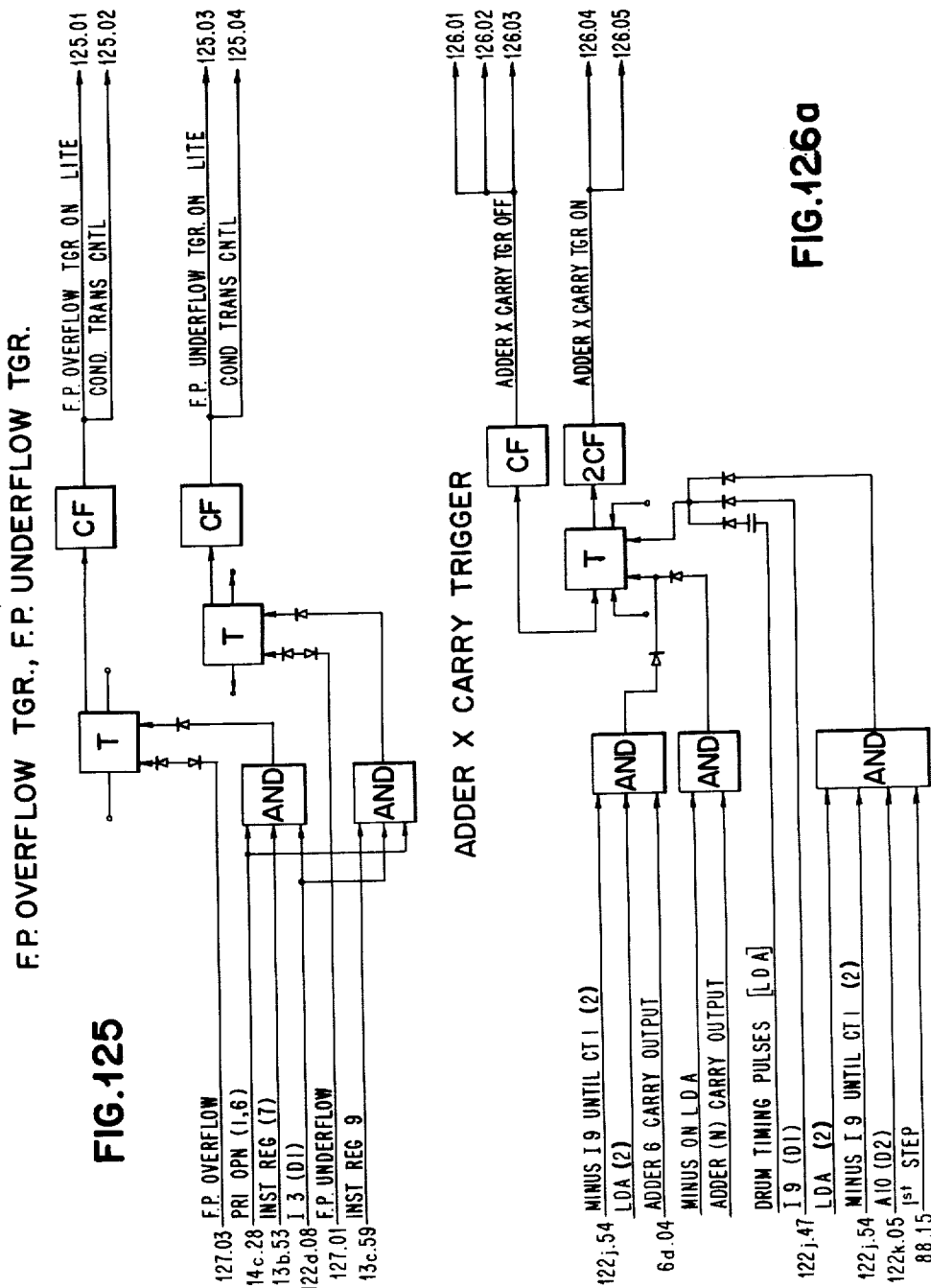
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

3,019,976

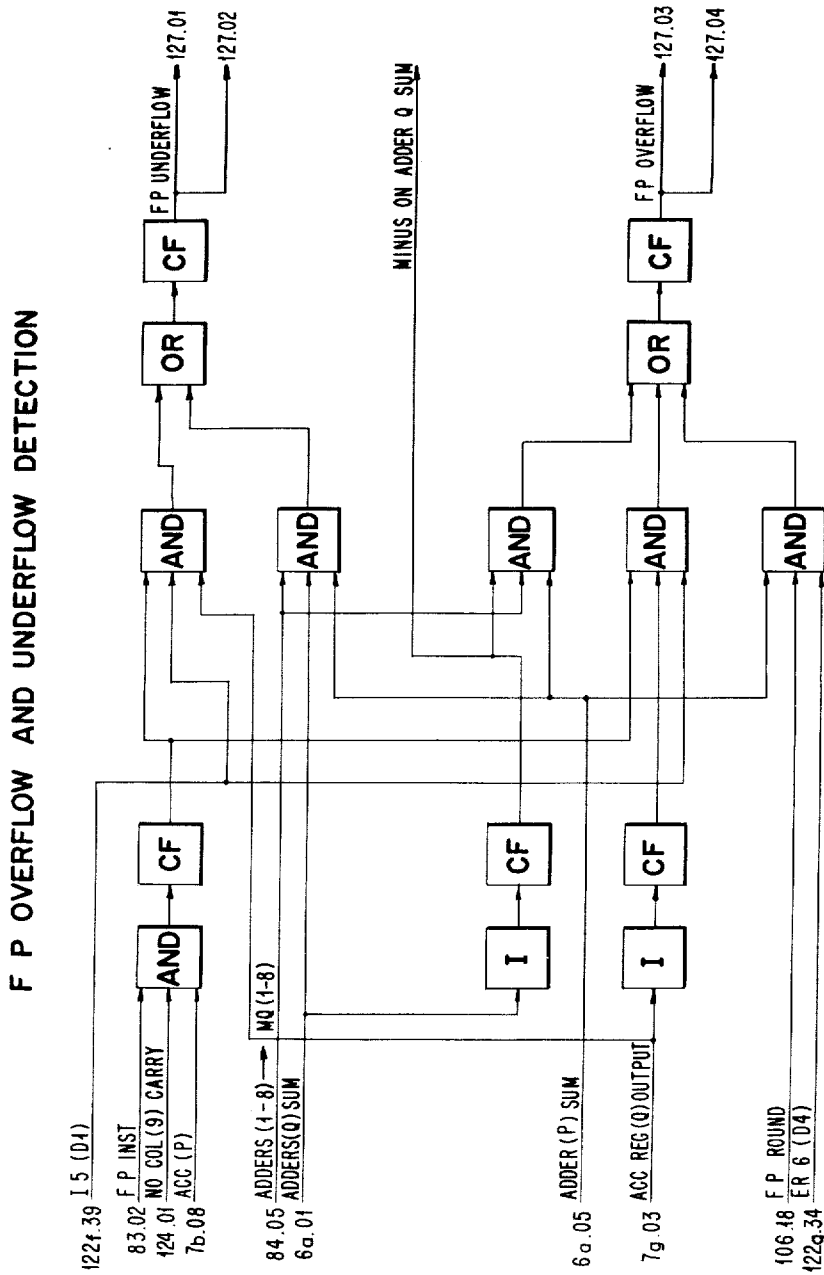
Filed Dec. 26, 1957

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**FIG. 127**

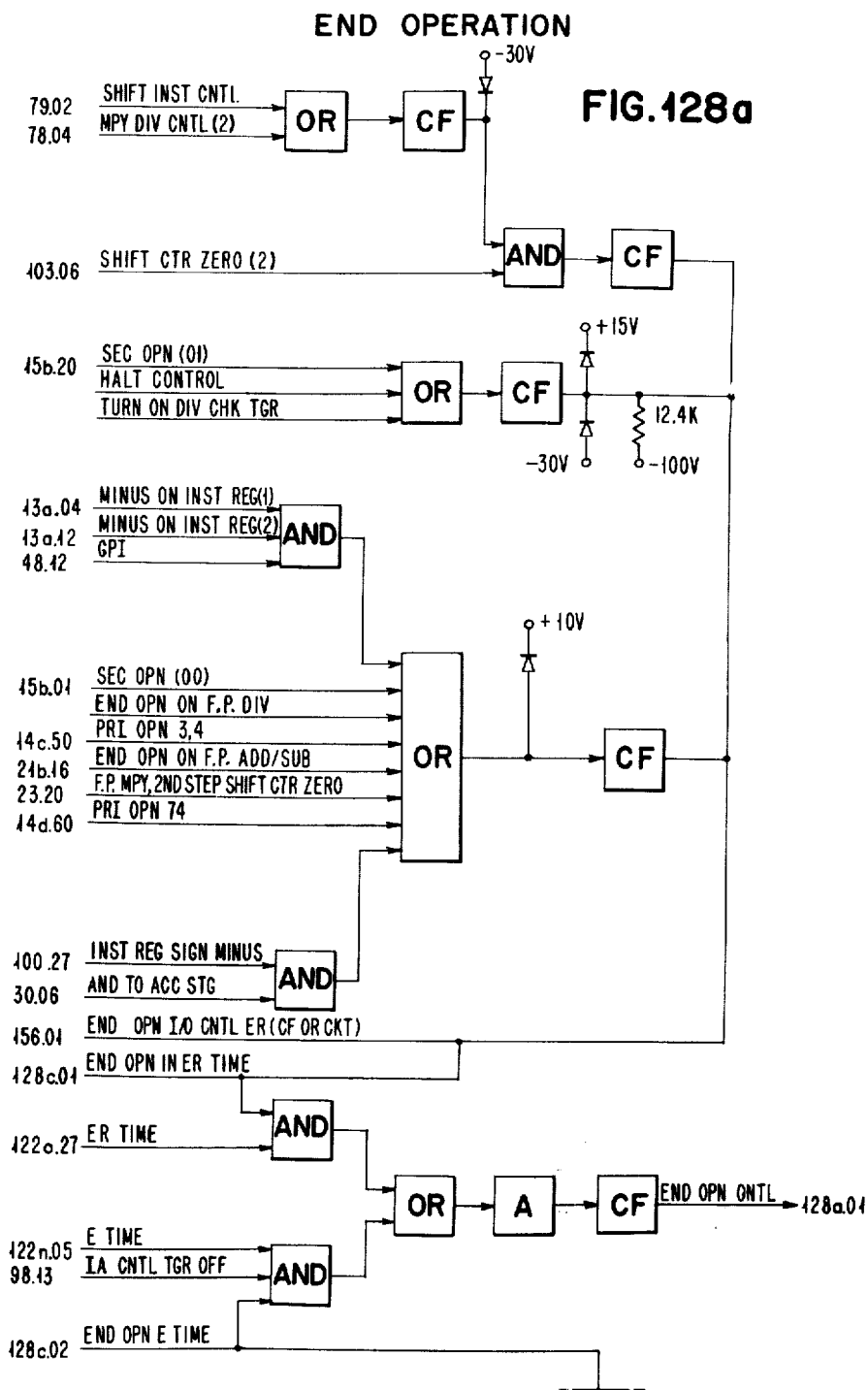
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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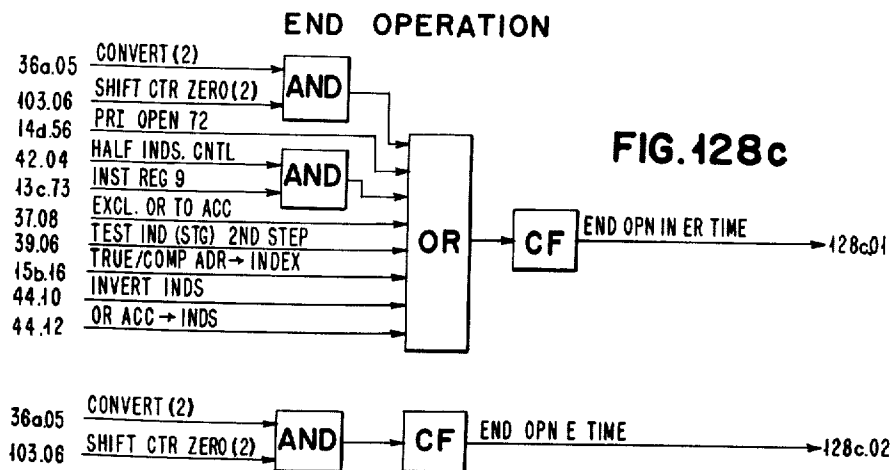
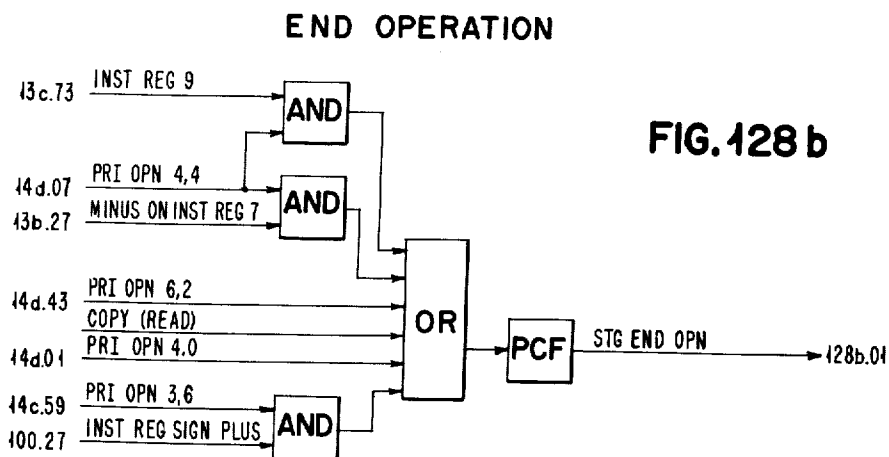
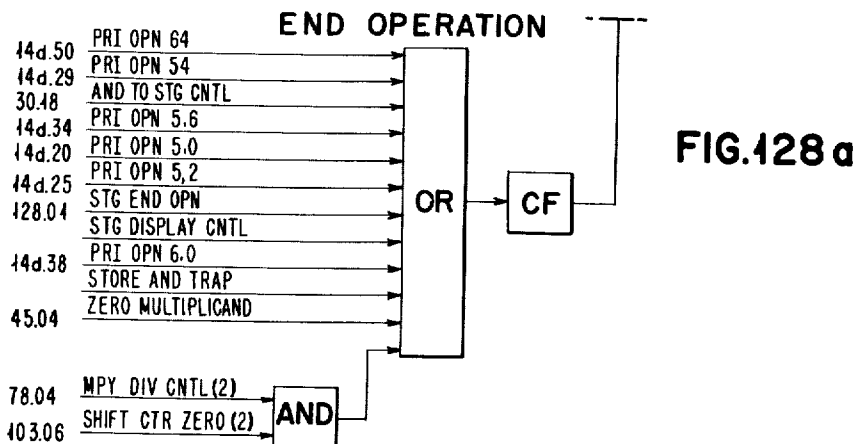
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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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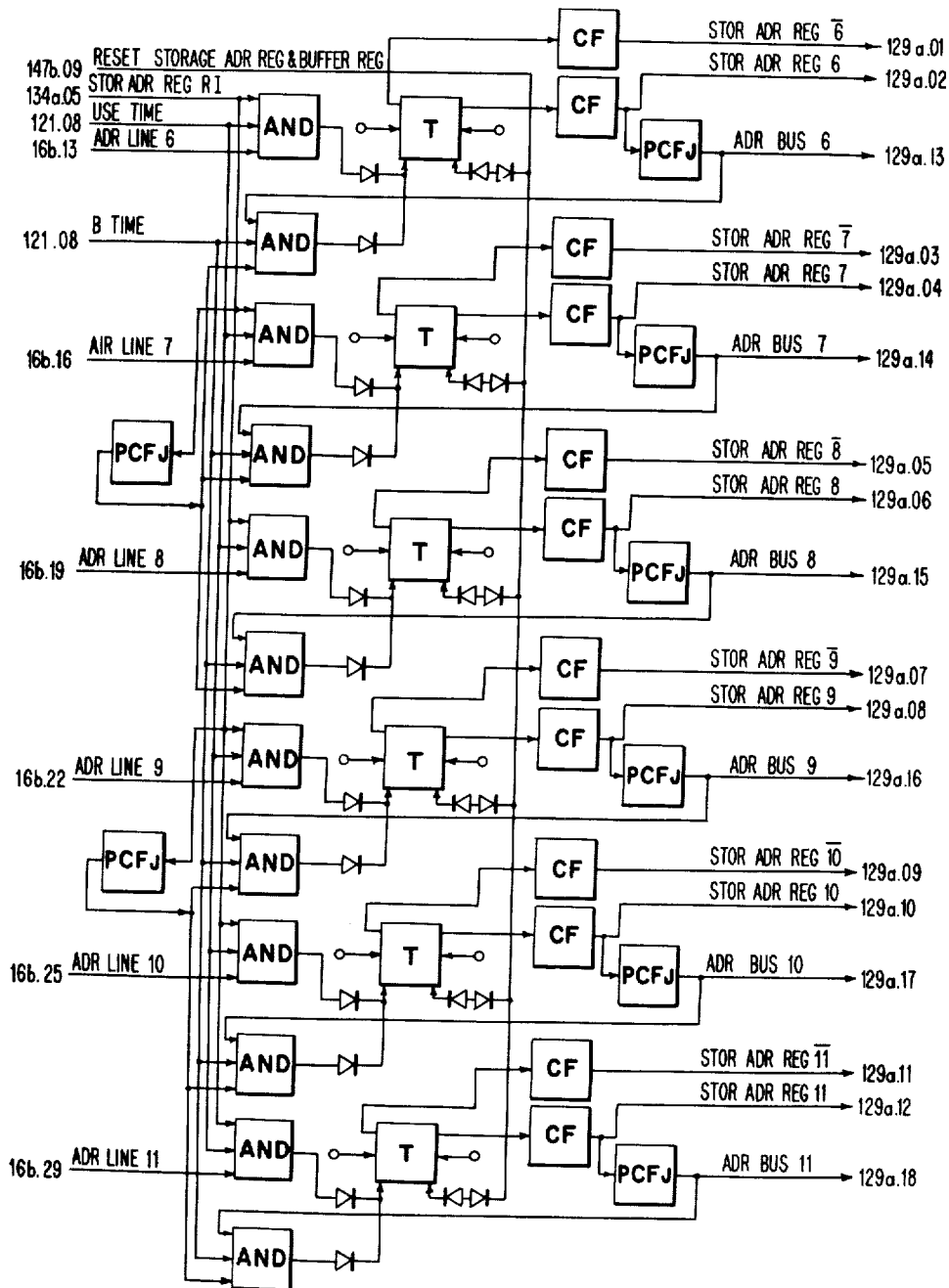
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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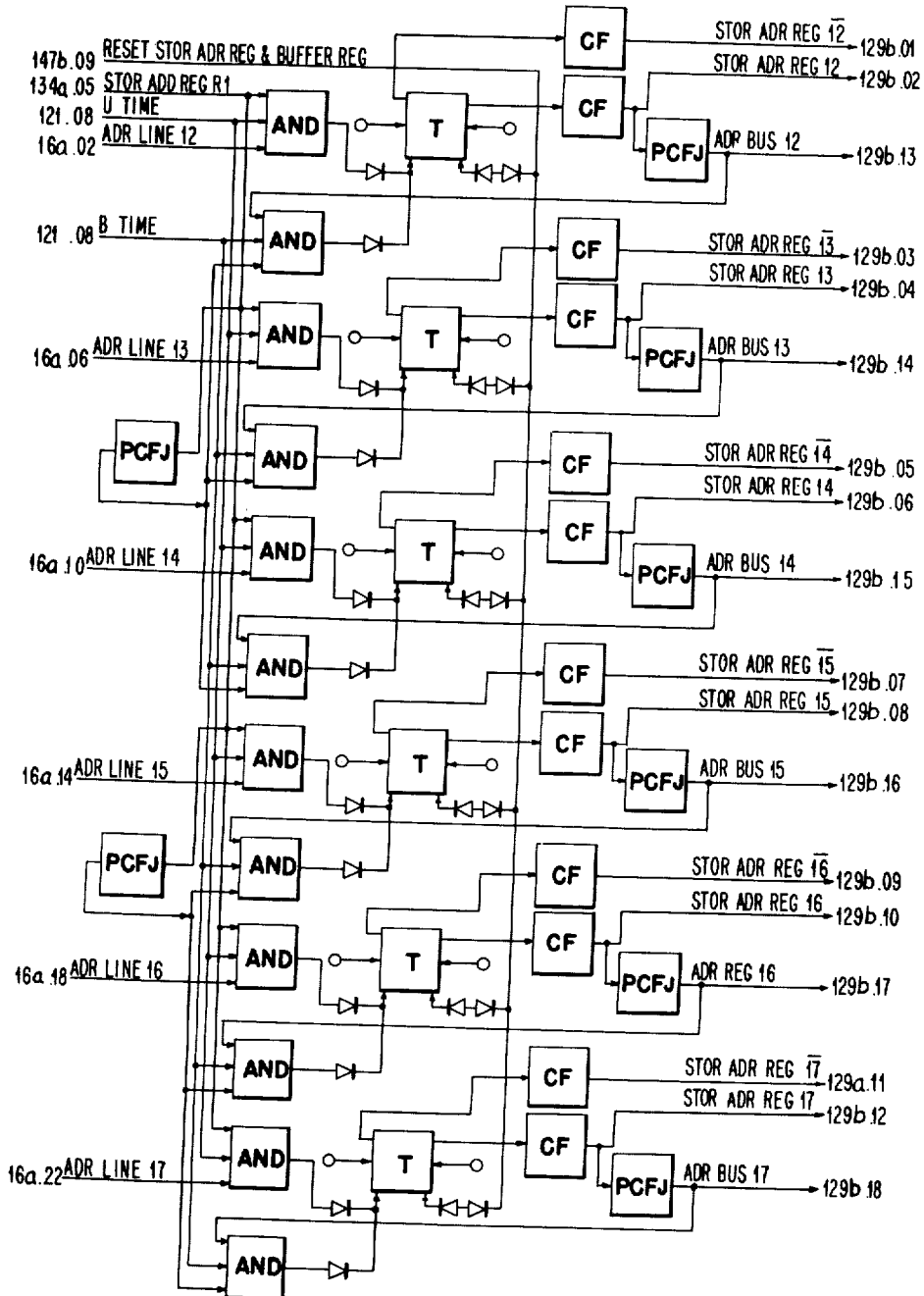
FIG. 129a STORAGE ADDRESS REGISTER



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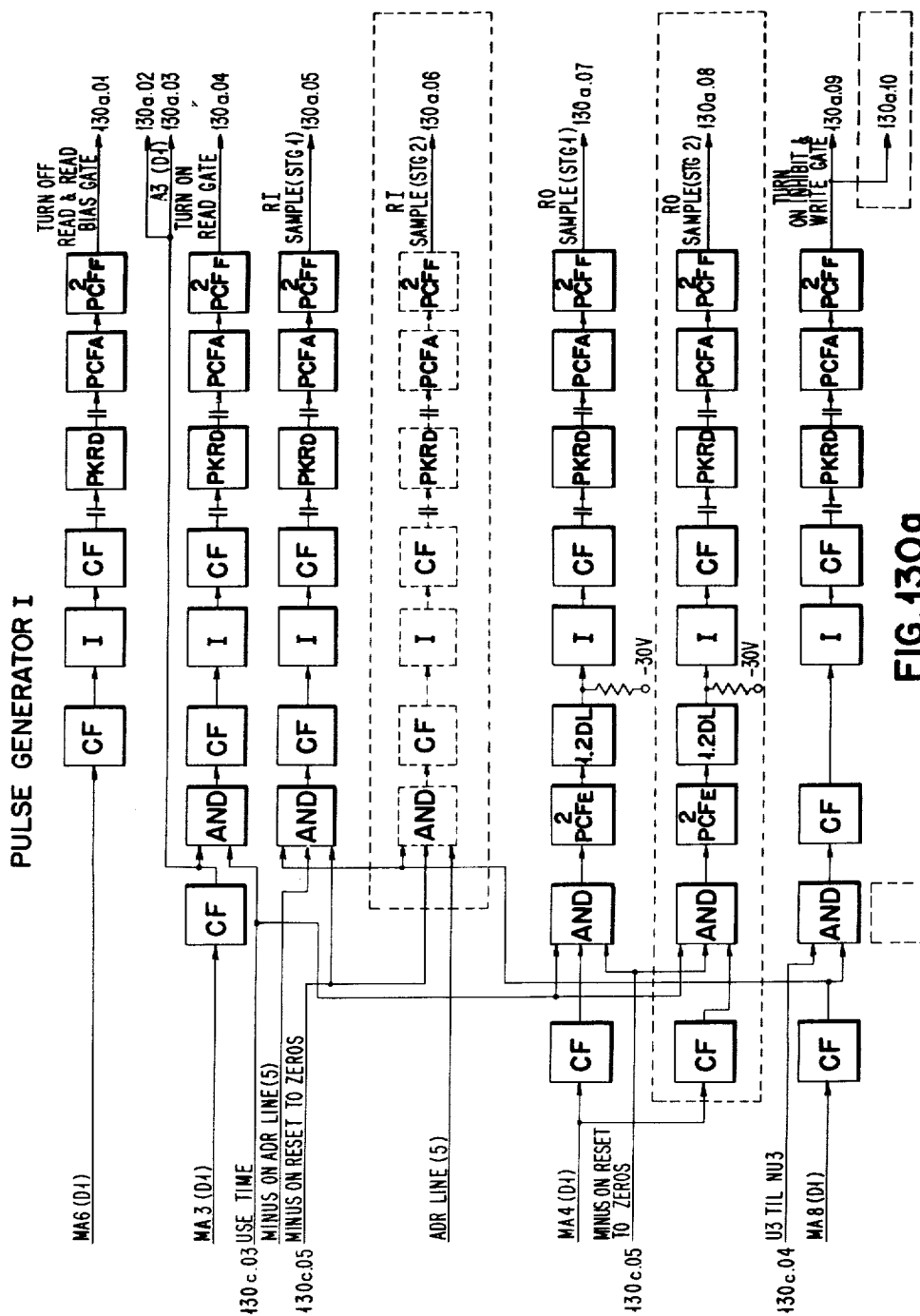
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**FIG. 129b** STORAGE ADDRESS REGISTER



**J. M. TAYLOR**  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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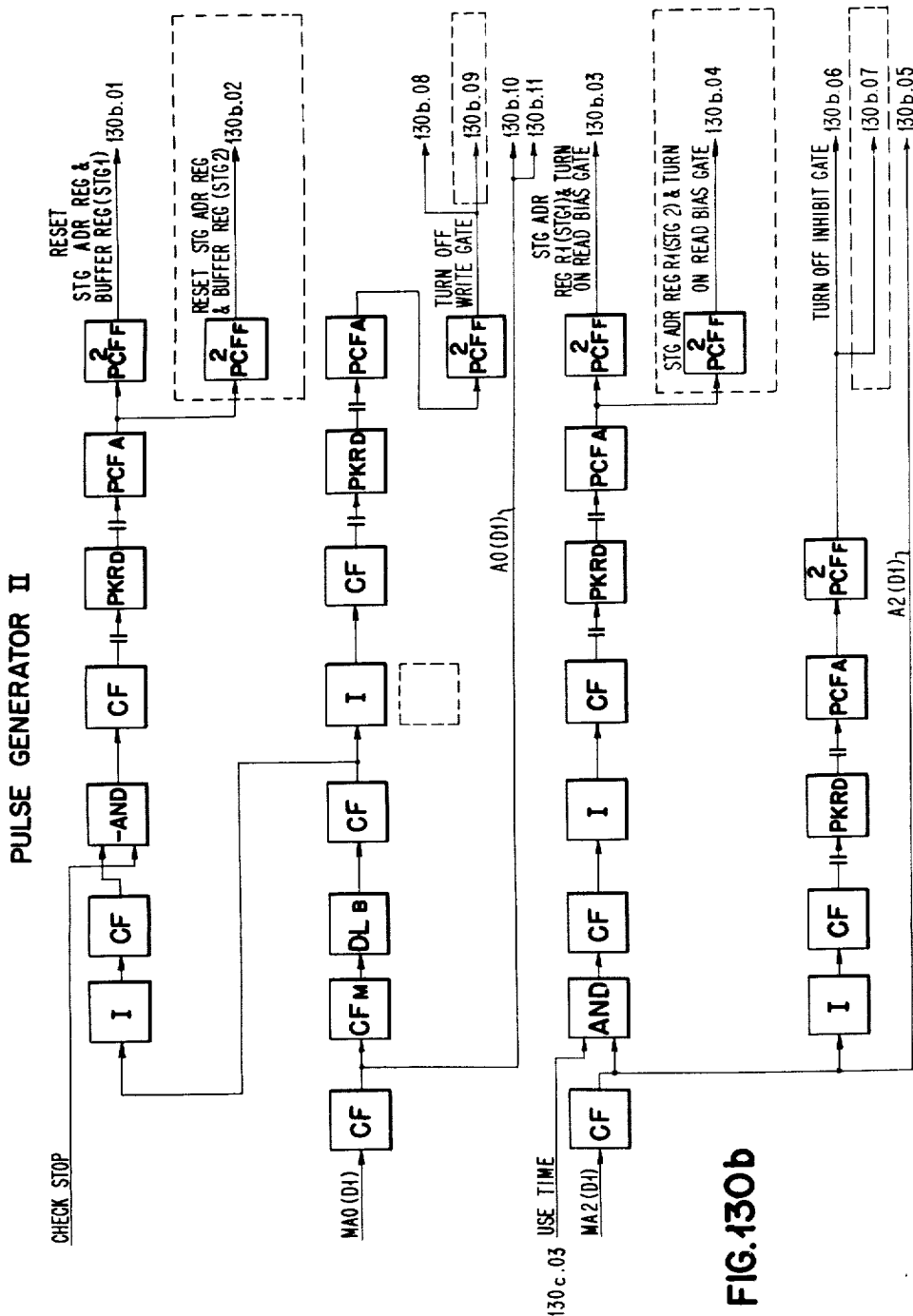
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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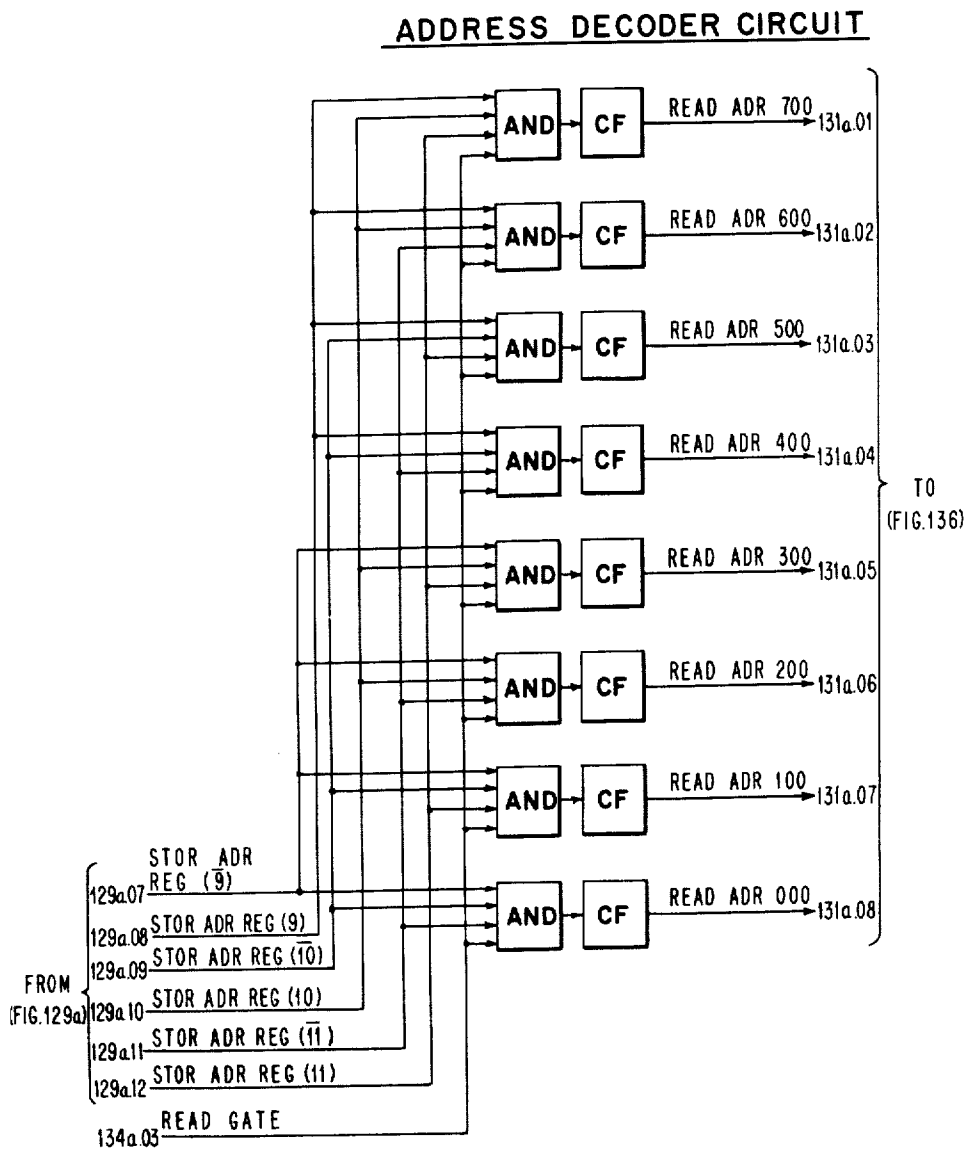
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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FIG. 131a



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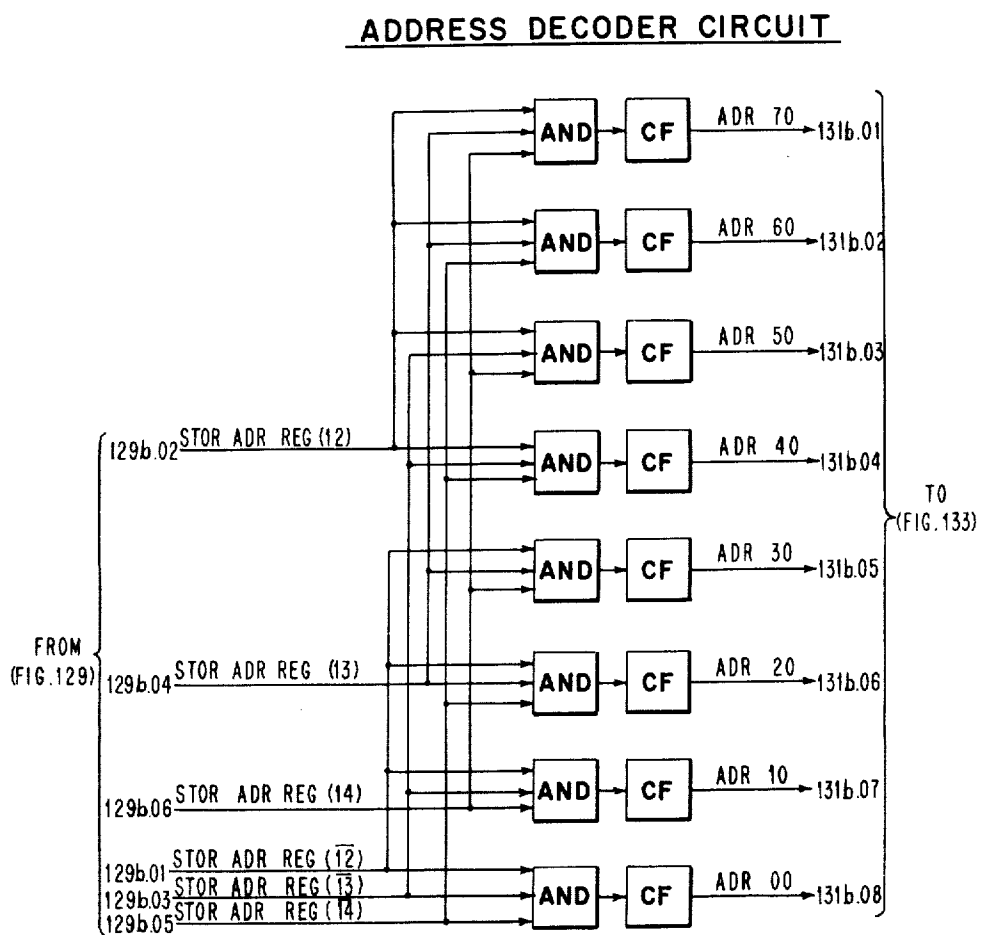
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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FIG. 131b



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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

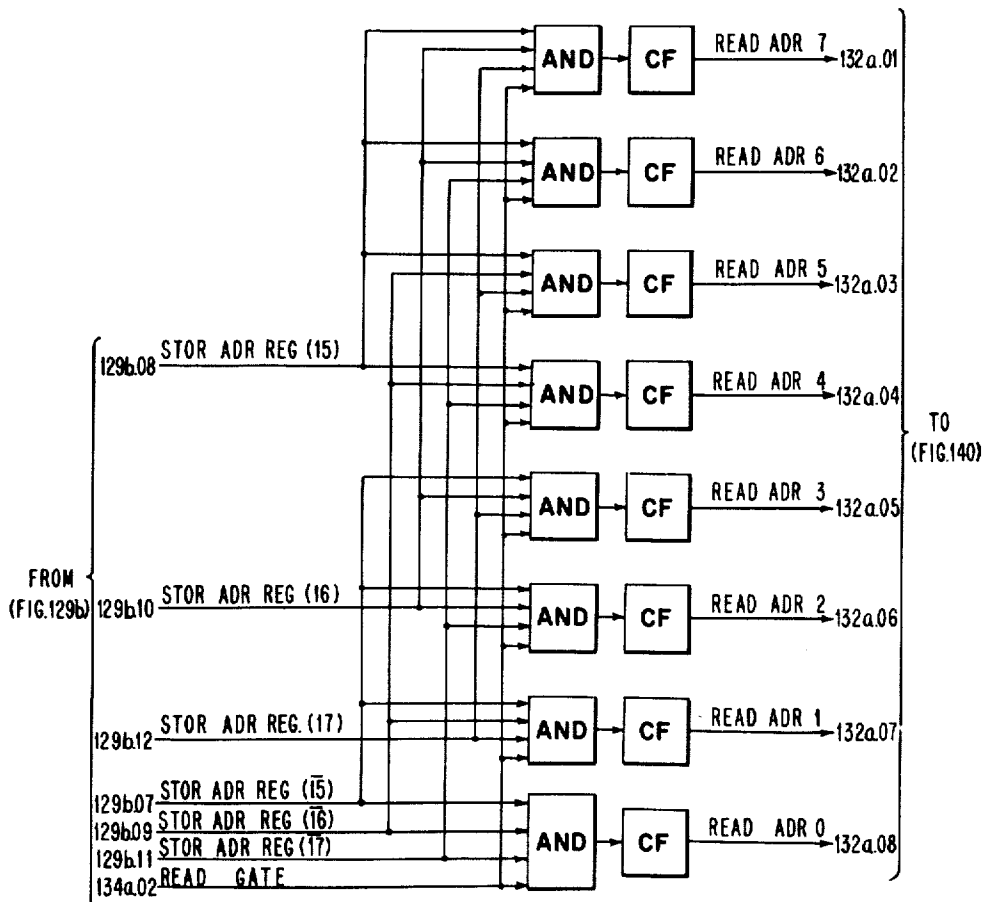
3,019,976

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FIG. 132a

ADDRESS DECODER CIRCUIT



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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

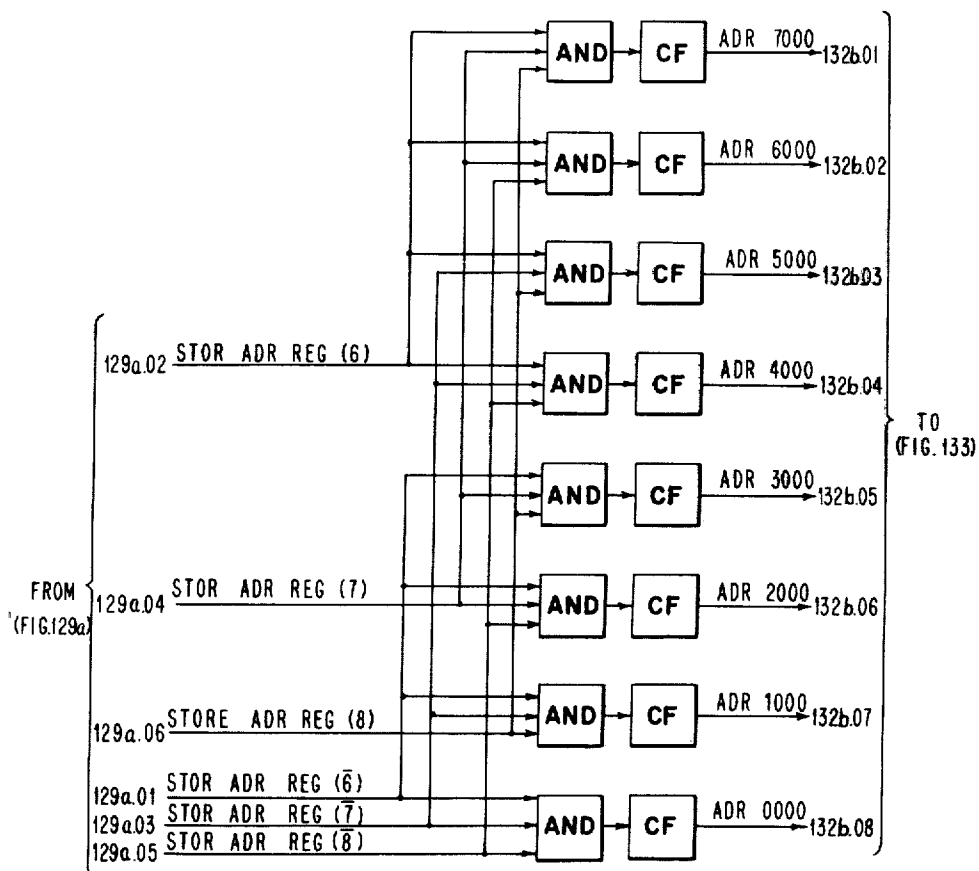
3,019,976

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FIG. 132b

ADDRESS DECODER CIRCUIT



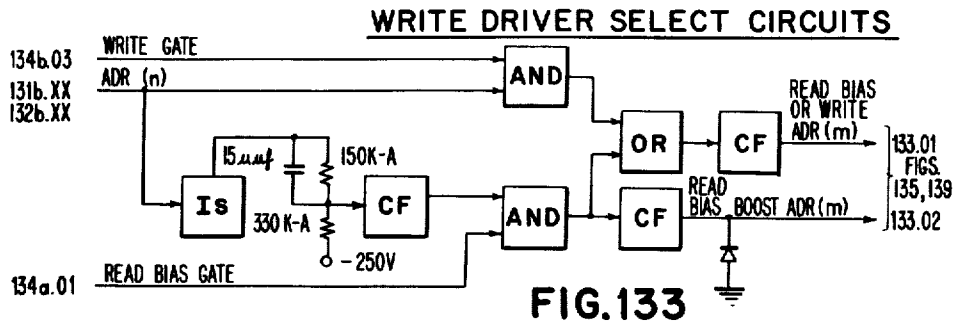
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

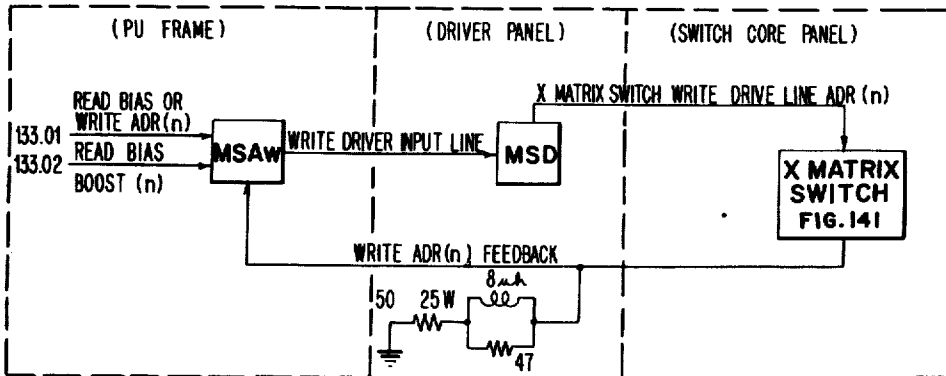
3,019,976

Filed Dec. 26, 1957

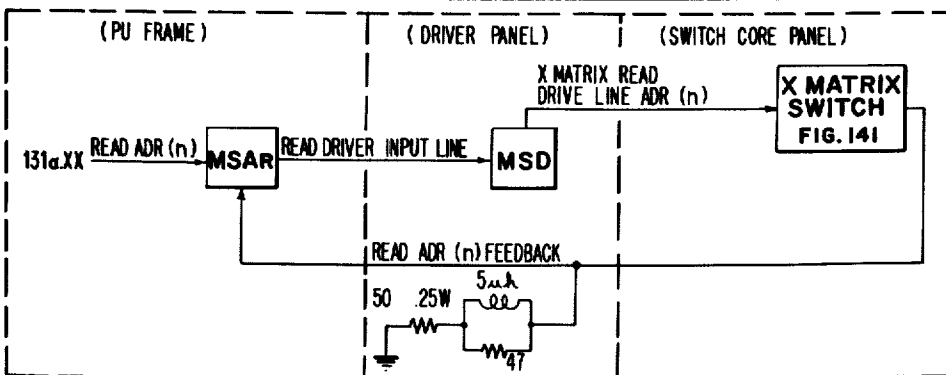
247 Sheets-Sheet 231



**FIG. 135** X MATRIX SWITCH WRITE DRIVER



**FIG. 136** X MATRIX SWITCH READ DRIVER



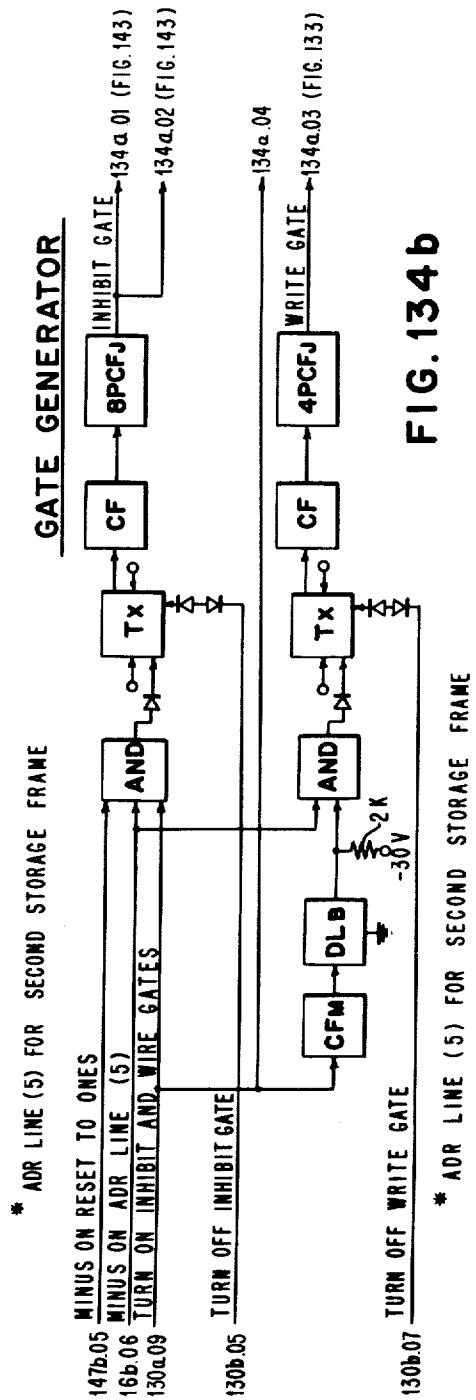
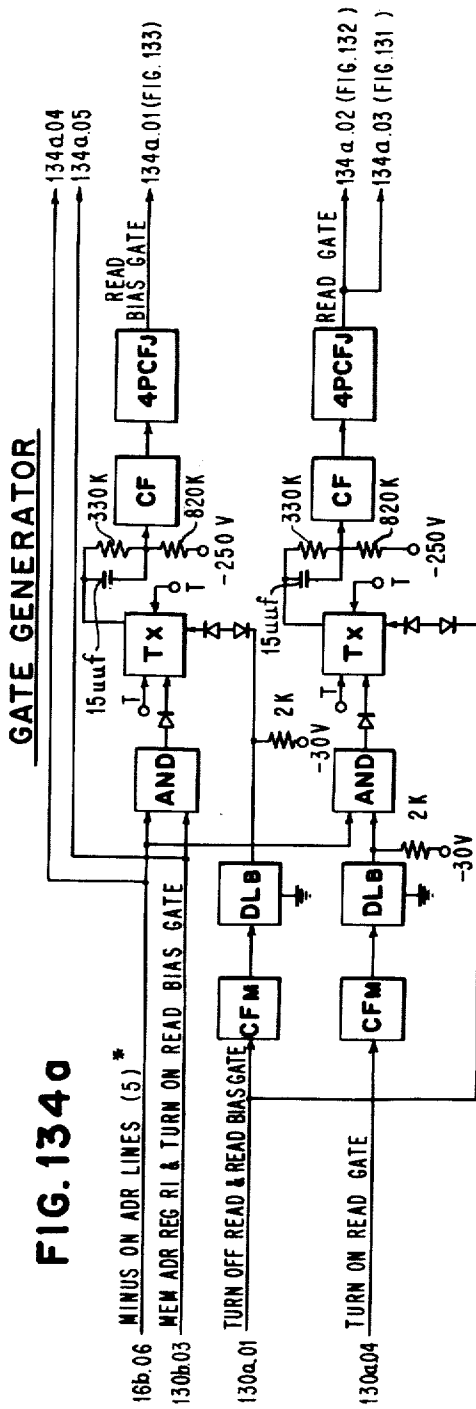
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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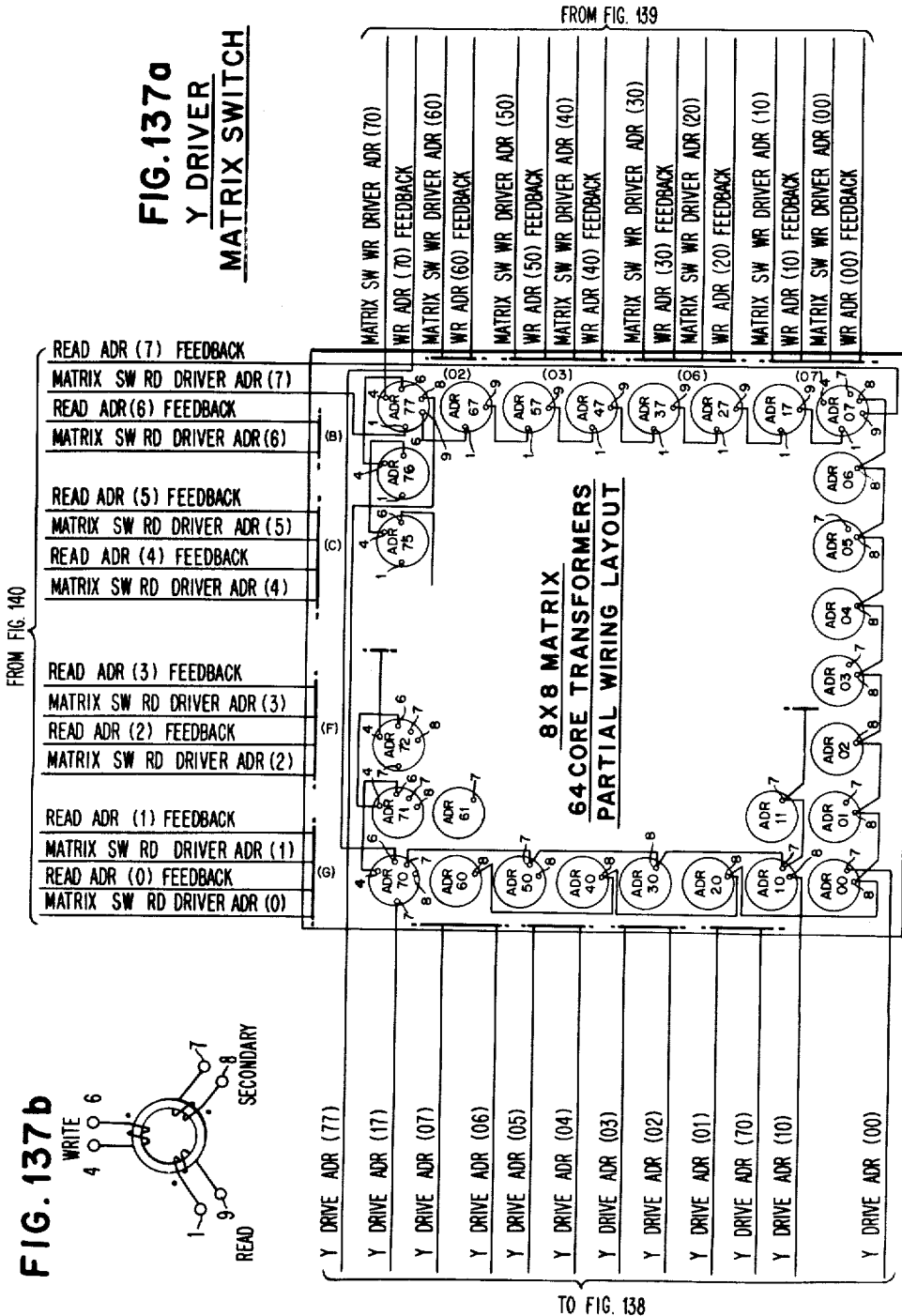
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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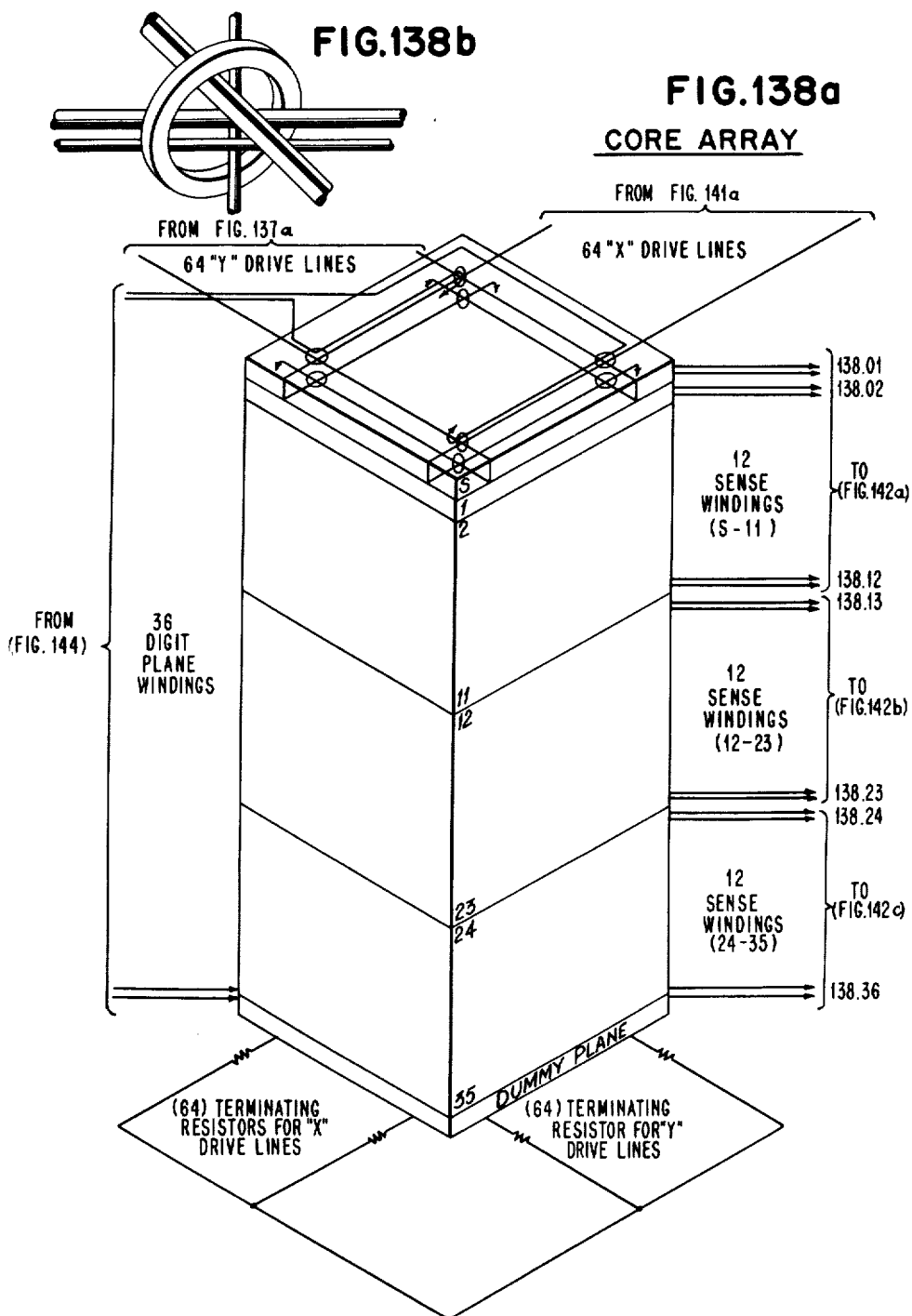
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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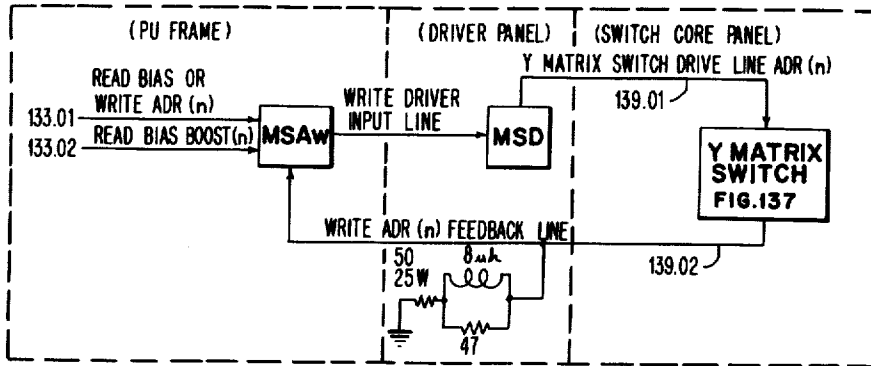
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

3,019,976

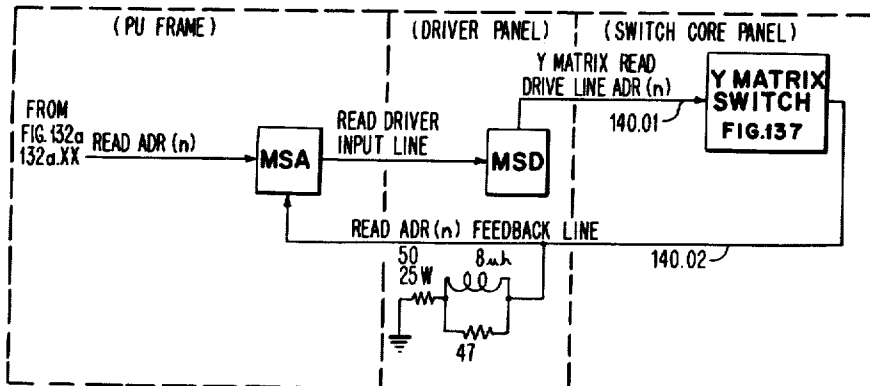
Filed Dec. 26, 1957

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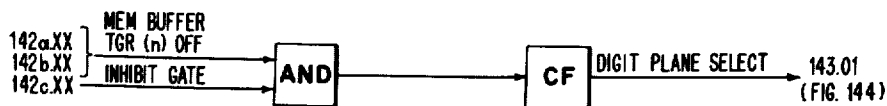
**FIG. 139** Y MATRIX SWITCH WRITE DRIVER



**FIG. 140** Y MATRIX SWITCH READ DRIVER



**FIG. 143** DIGIT PLANE SELECT CIRCUITS



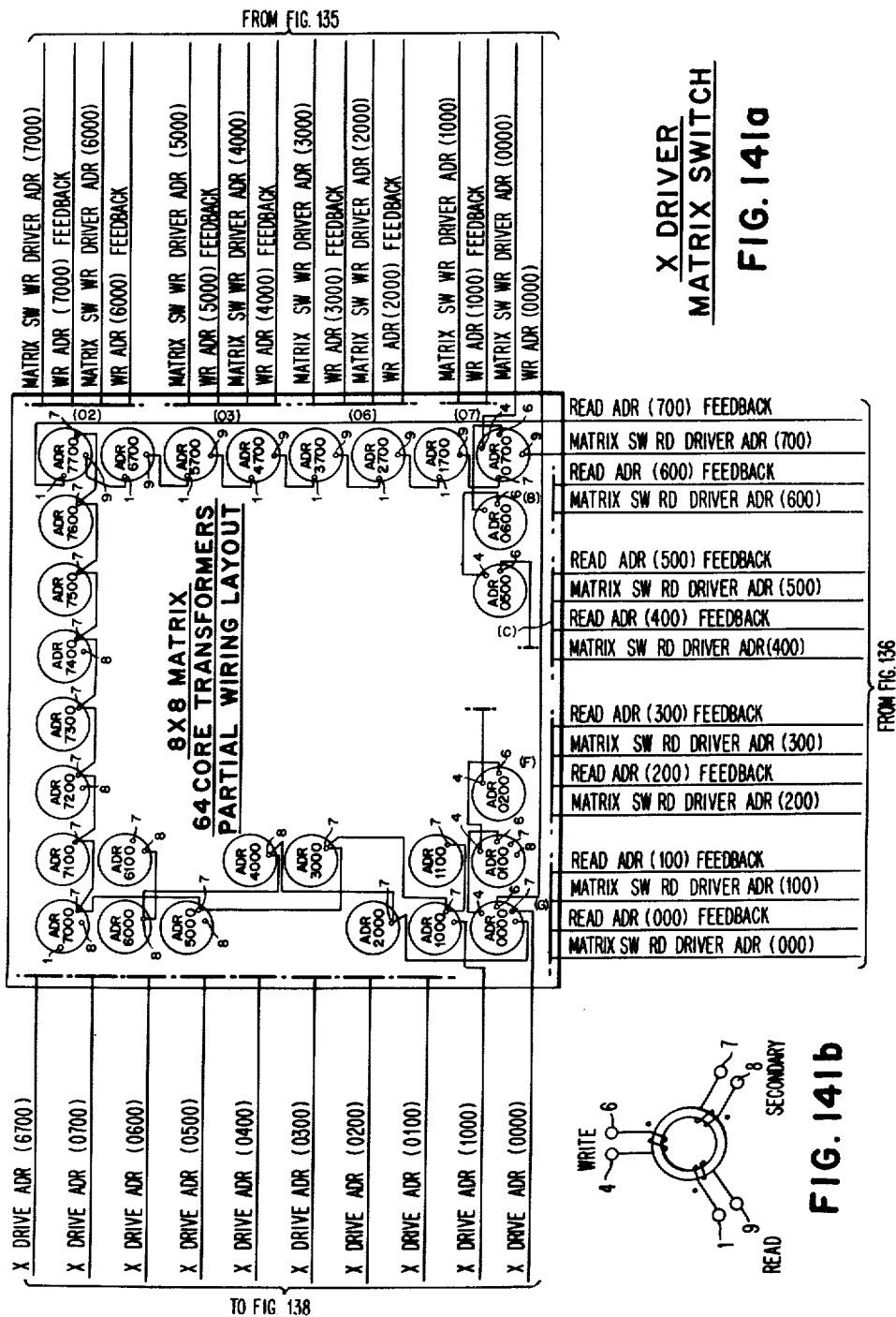
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

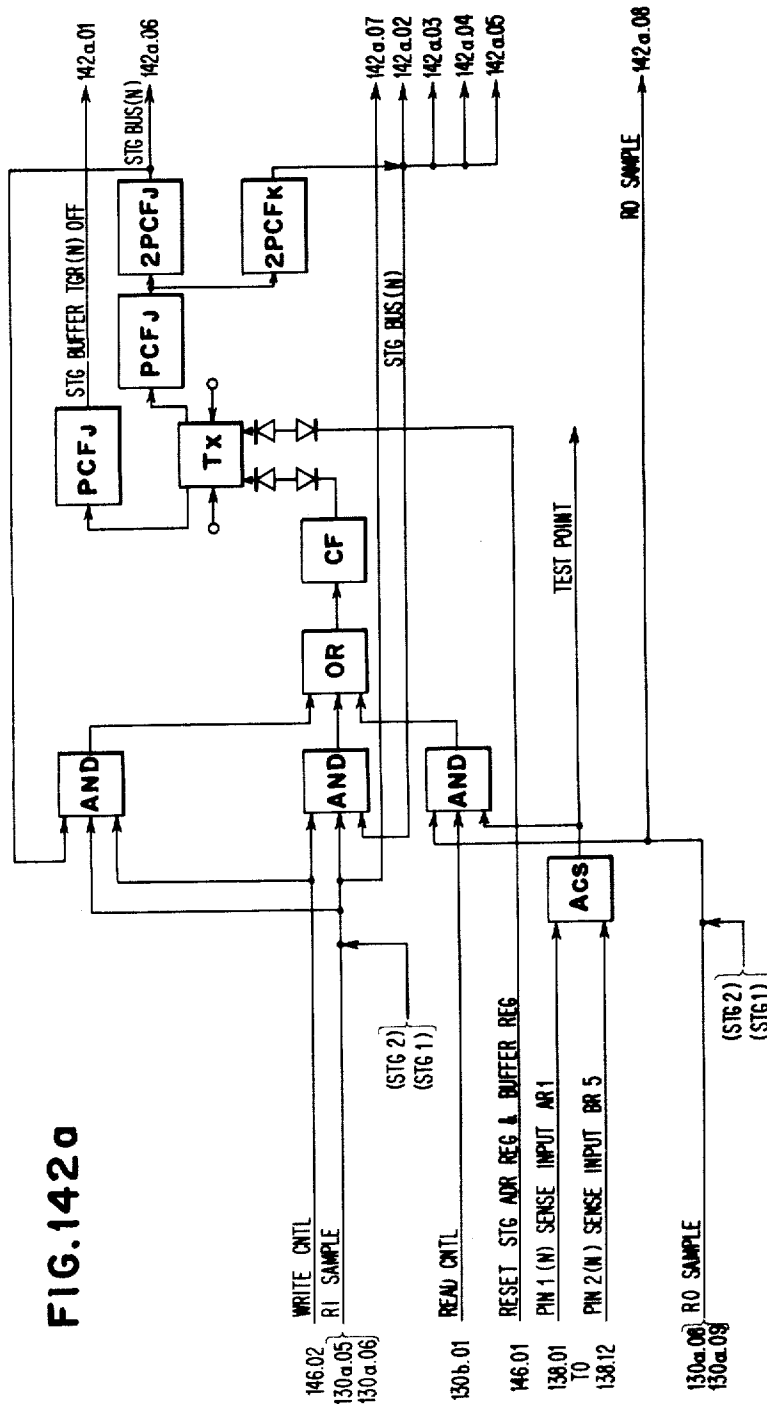
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247 Sheets-Sheet 237

SENSE AMP, BUFFER REGISTER & I/O SWITCHING

FIG. 142a



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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

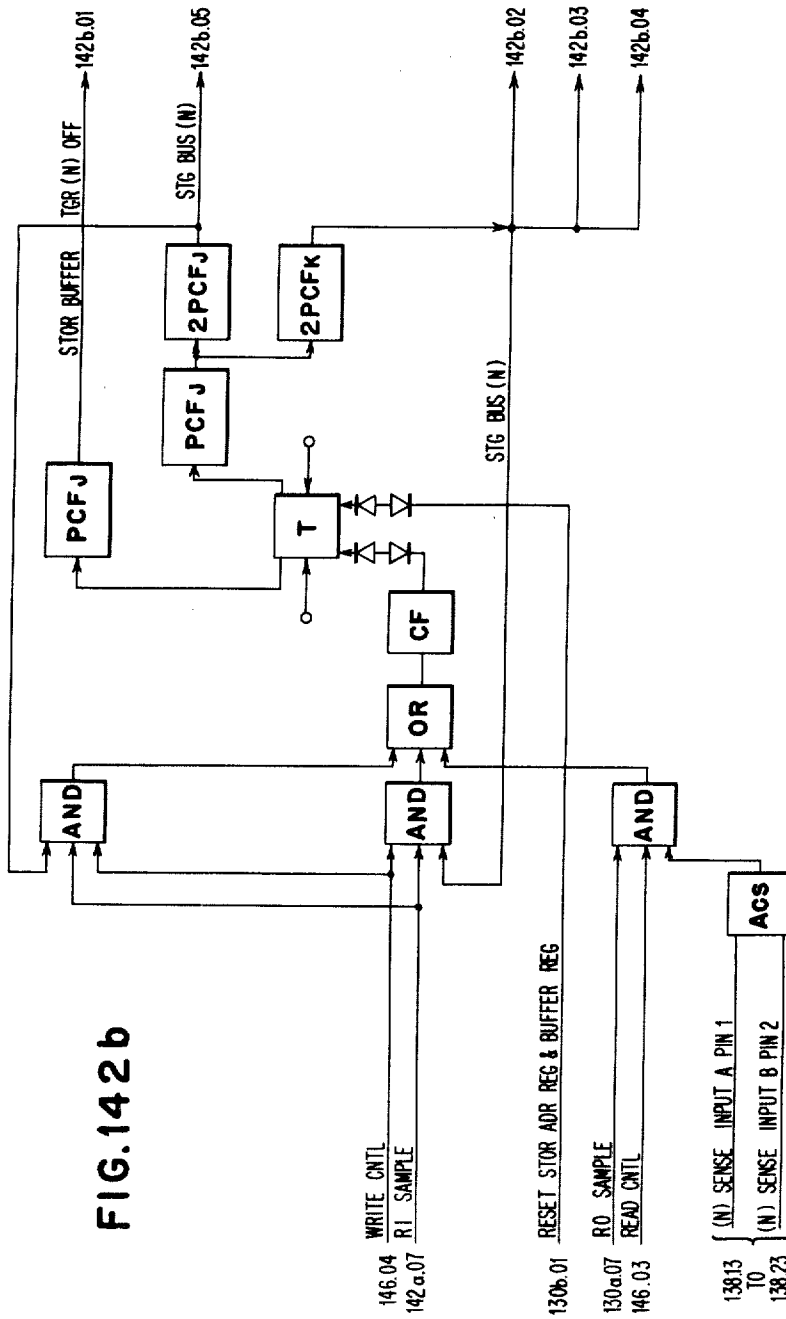
3,019,976

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SENSE AMP, BUFFER REGISTER & I/O SWITCHING

FIG. 142b



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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

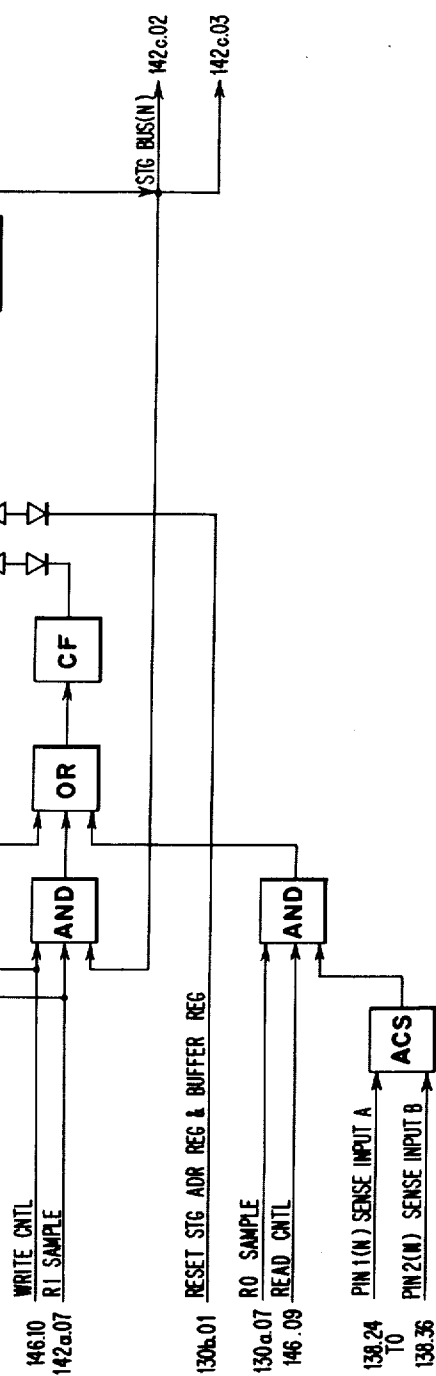
3,019,976

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SENSE AMP, BUFFER REGISTER & I/O SWITCHING

FIG. 142c



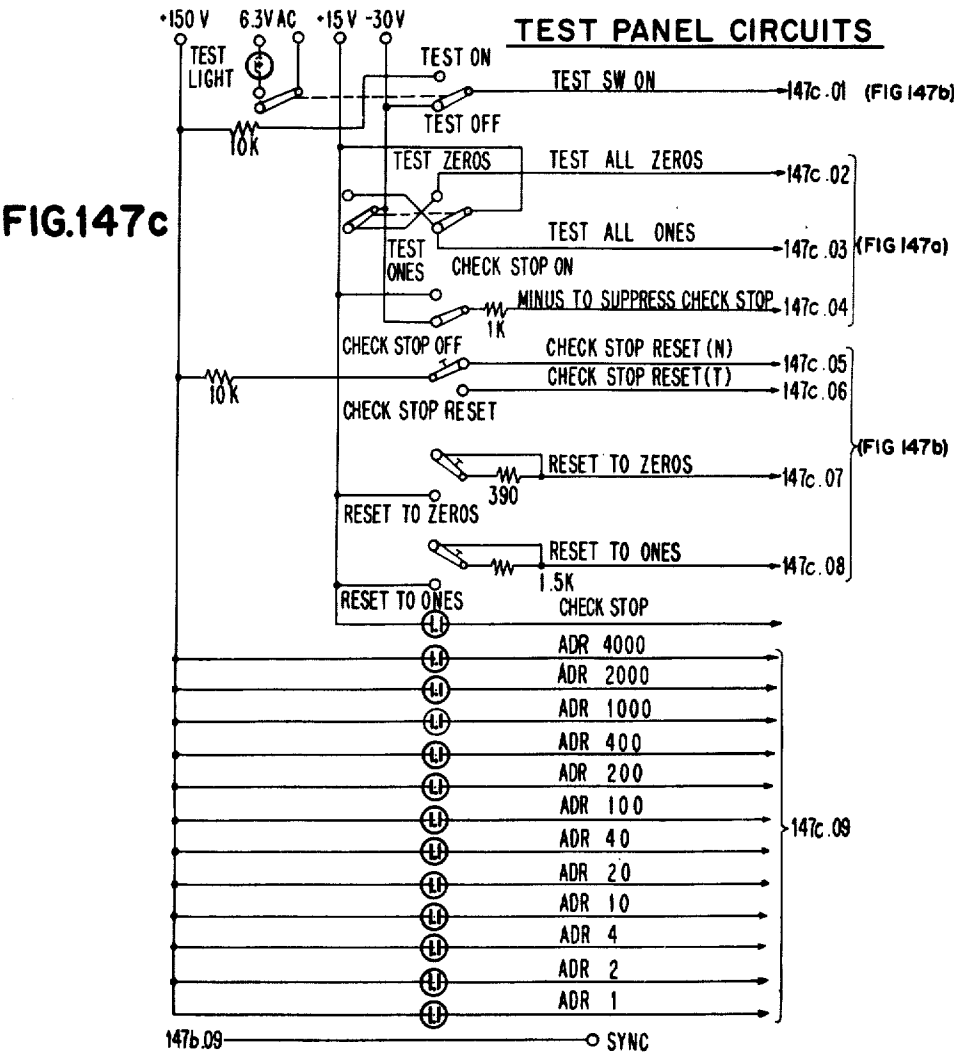
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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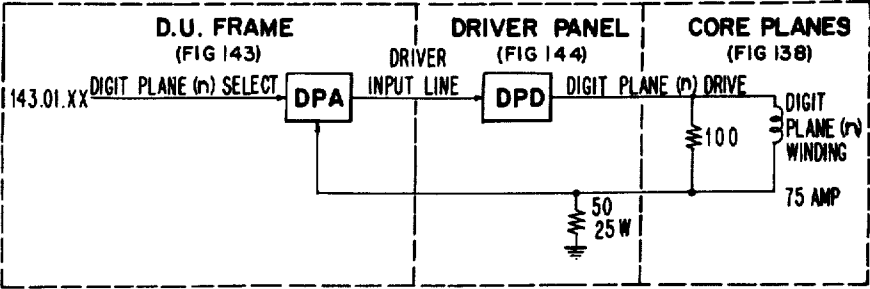
Filed Dec. 26, 1957

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**FIG.144**

**DIGIT PLANE DRIVER**



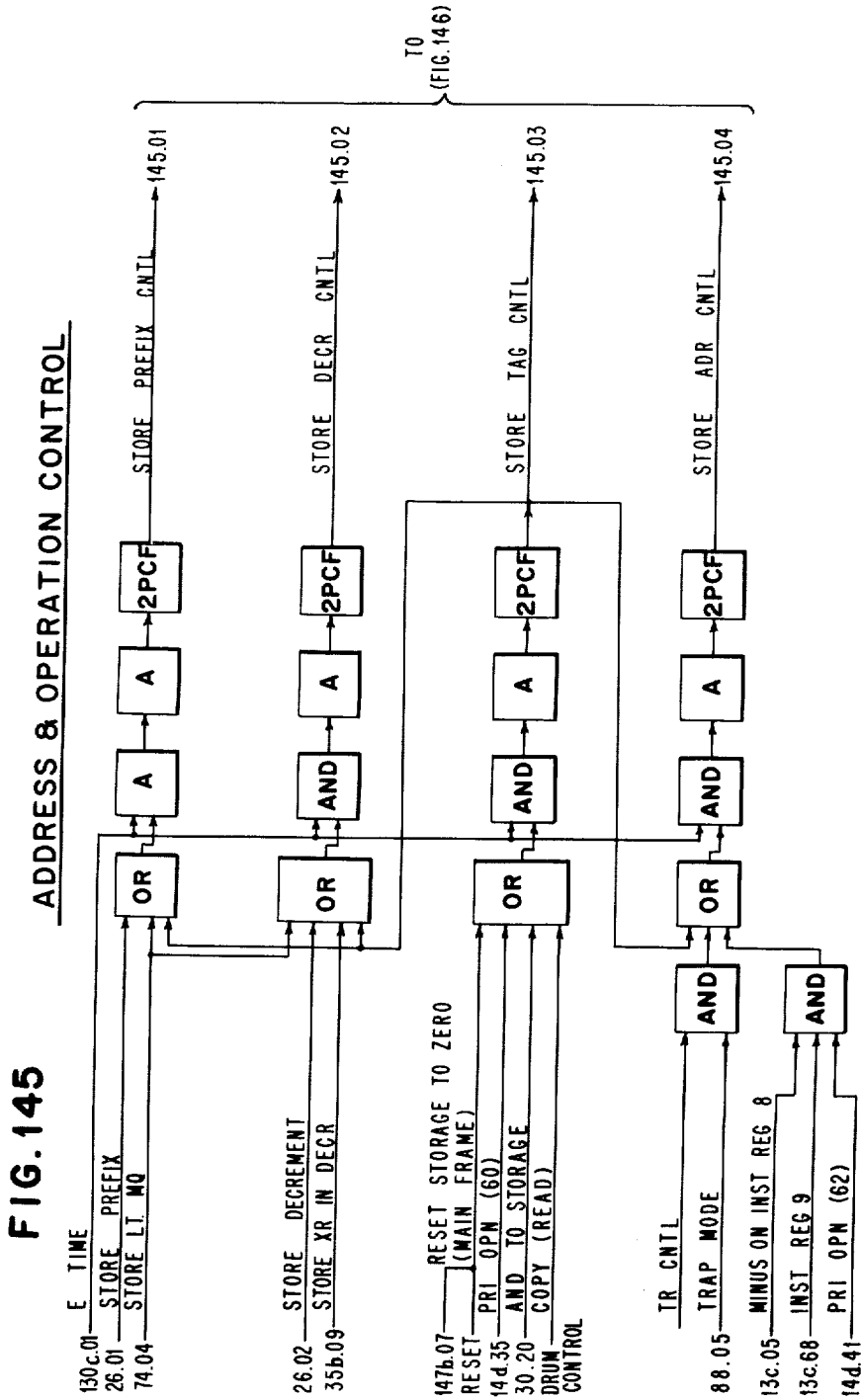
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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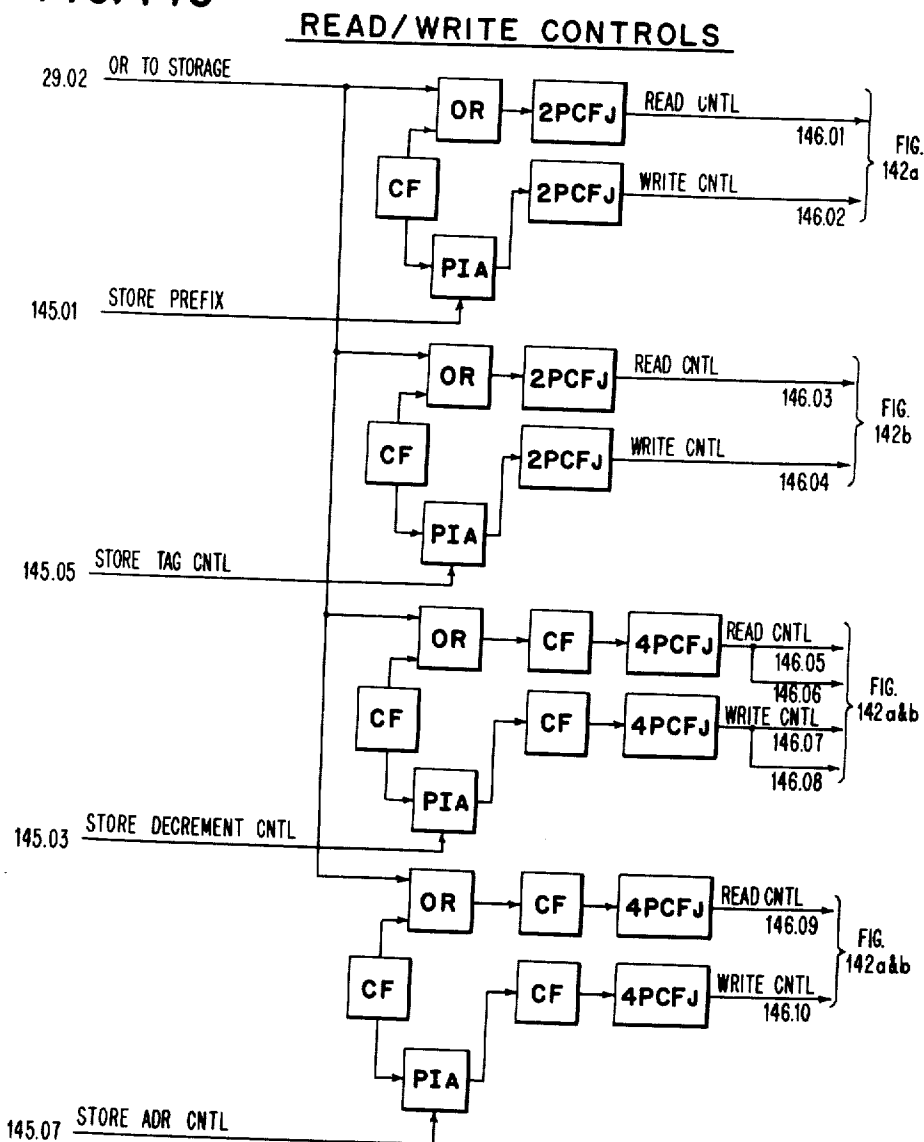
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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FIG. 146



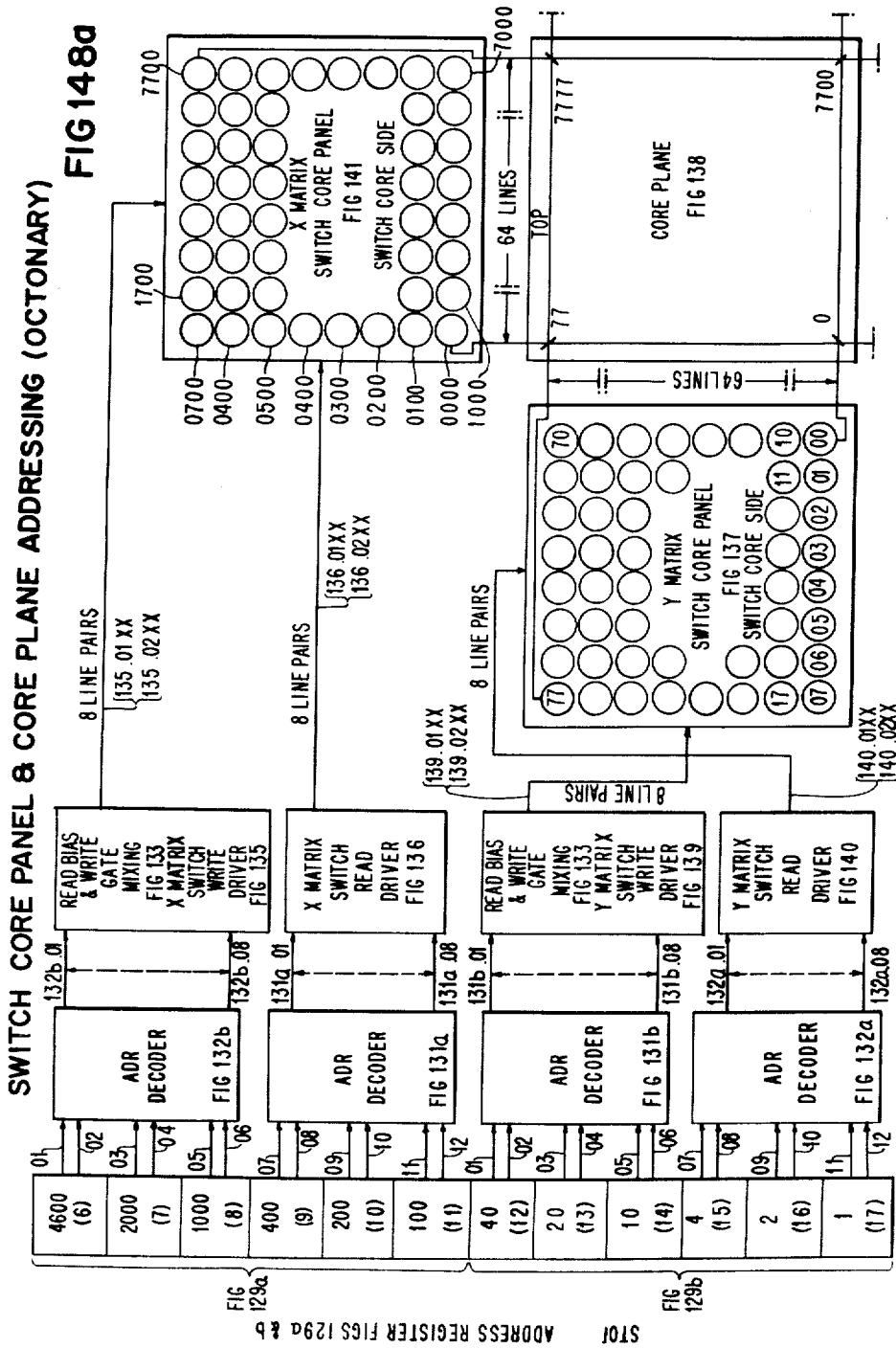
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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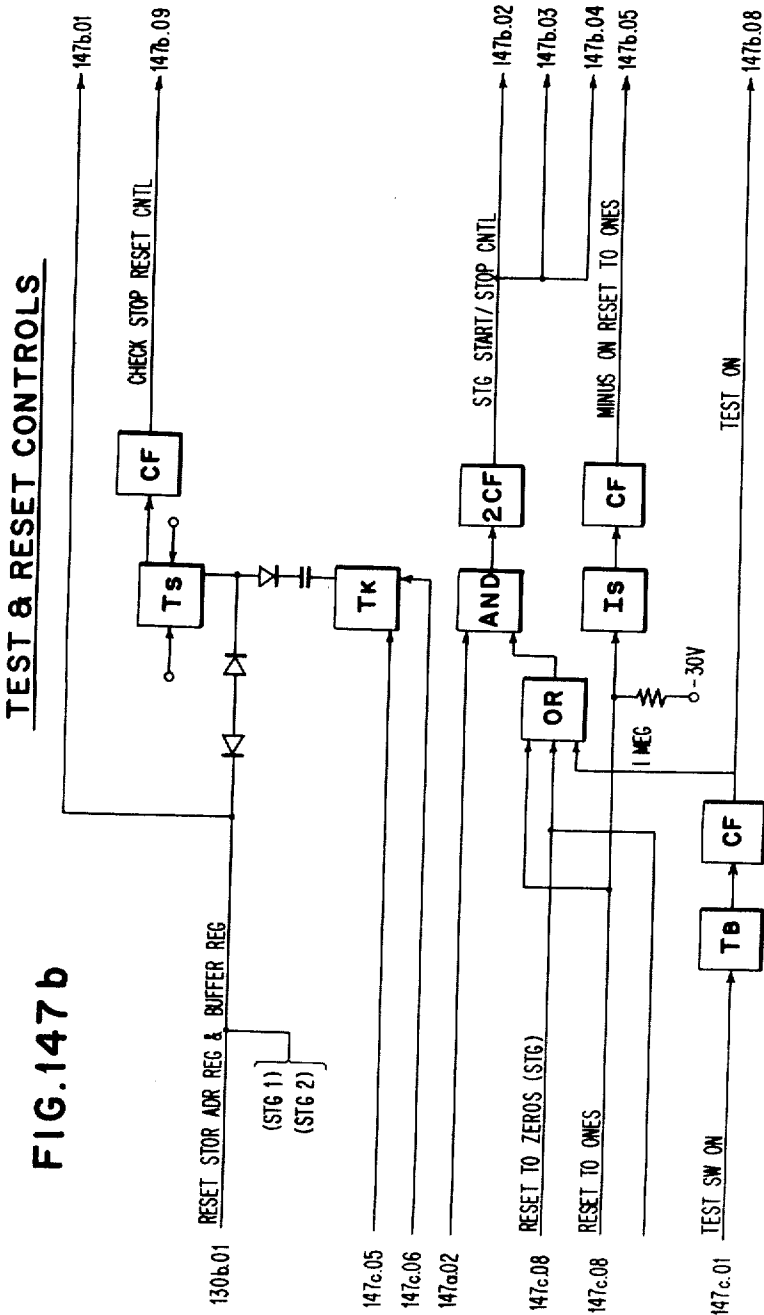
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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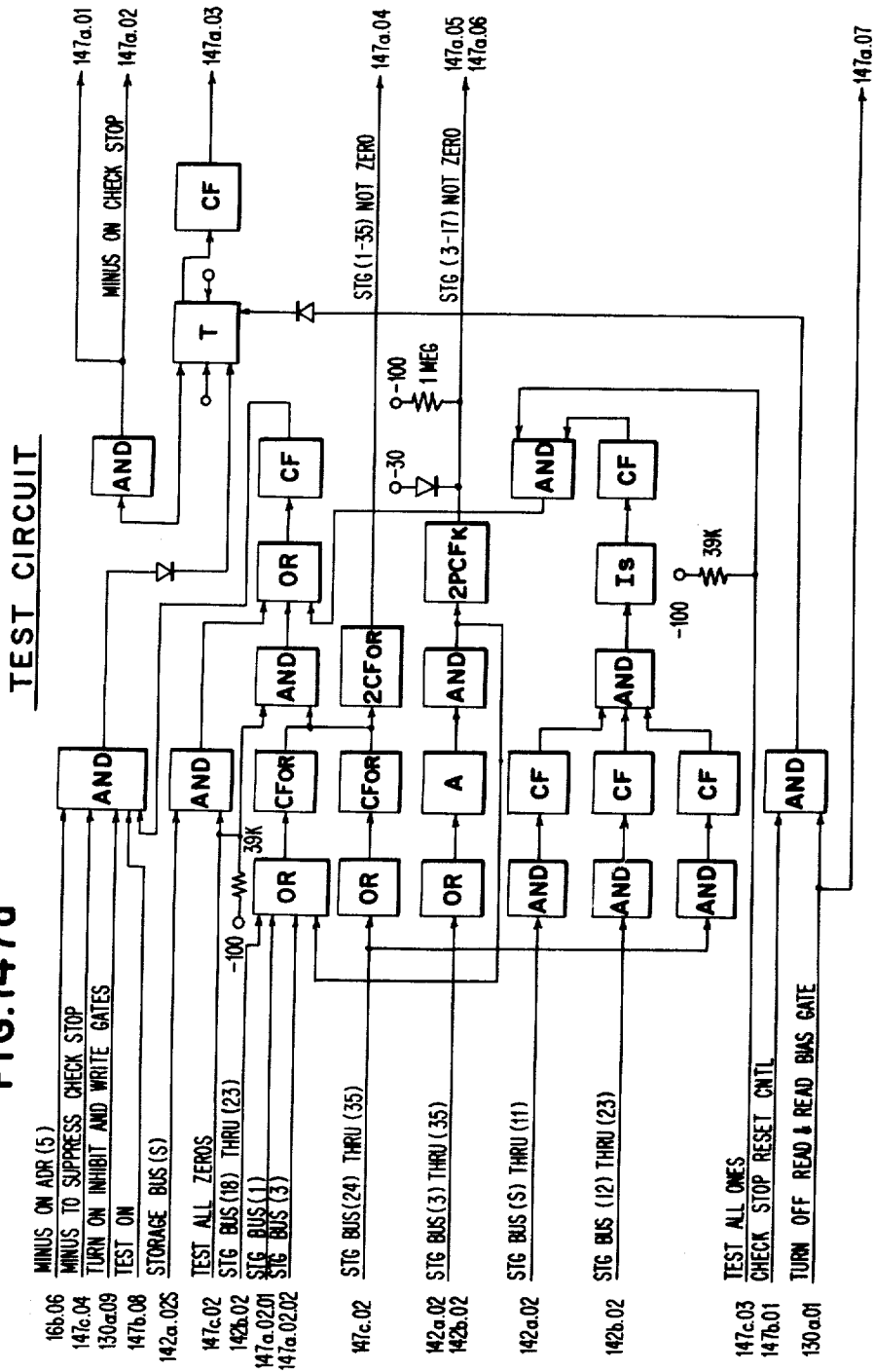
J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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FIG. 147a



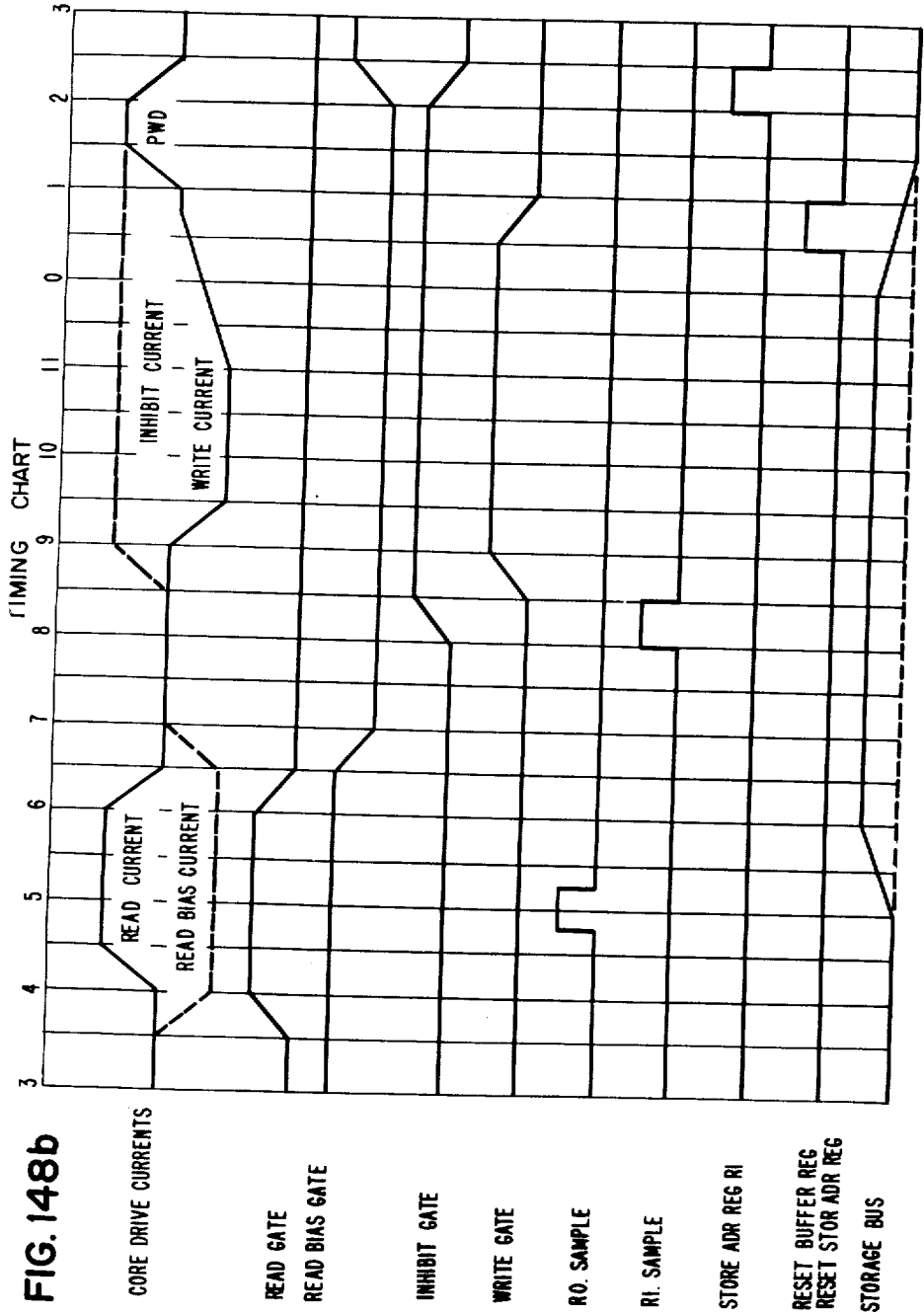
Feb. 6, 1962

J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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J. M. TAYLOR  
DATA PROCESSING SYSTEM INCLUDING  
AN INDICATING REGISTER

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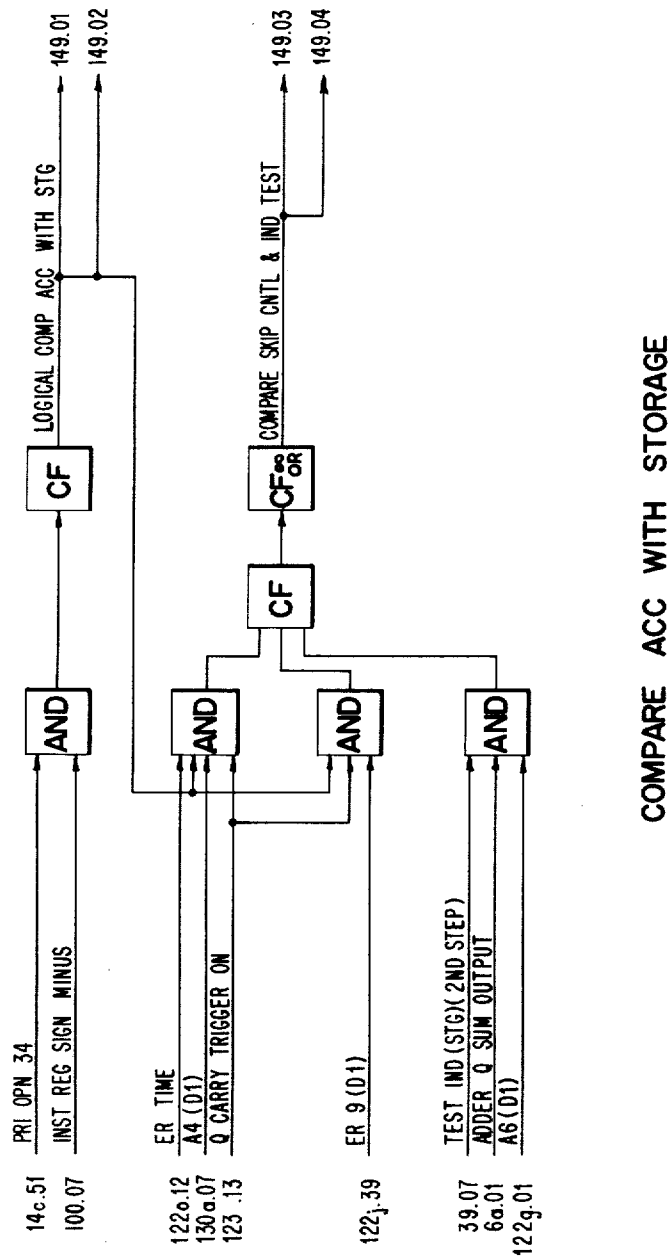


FIG. 149

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## DATA PROCESSING SYSTEM INCLUDING AN INDICATING REGISTER

Jordan M. Taylor, Poughkeepsie, N.Y., assignor to International Business Machines Corporation, New York, N.Y., a corporation of New York  
Filed Dec. 26, 1957, Ser. No. 705,444  
1 Claim. (Cl. 235—157)

This invention relates to digital computers of the parallel binary type and more particularly to a logical arrangement of registers including an indicator register for the examination of single bits and groups of bits to provide control over subsequent machine operations or construct words according to a predetermined plan.

In many applications of data processing machines, it is desirable to have indicators which can be set and tested in response to programmed operations. For maximum versatility the devices should be capable of assuming one or the other of a pair of stable states, zero or one, and singly or in groups be turned on or off and the contents inverted or tested by reference to zeros or ones in others of the registers, in storage locations, or in the instruction itself. Other than in operations involving program control, settable indicators are useful in extracting or inserting parts of words in another word or for testing fields within a word. Due to the nature of parallel binary computing machines, it is somewhat inconvenient to get at individual ones of the thirty-six bits in a word and due to the present nature of calculating processes, it is becoming increasingly necessary to have the ability to examine single or irregular groups of bits in a word. In some digit computing devices, individually bits are examined by shifting either to the right or to the left a predetermined number of positions as determined by a Counter having a count corresponding to the order of the bit and testing in the final position as to whether or not the digit was a binary one or zero. In some computers, this is readily accomplished in the sign position of one of the registers, which is normally adapted to provide a signal indicative of whether the sign bit is positive or negative, that is, a one or a zero. Accordingly, it is possible to determine the state of a specified order in a word but the shifting process requires a large number of serial shift operations which is time consuming. In the device of the present invention, an Indicator Register is provided in which these operations may be performed in a parallel fashion.

Briefly stated, thirty-six Sense Indicator Triggers are adapted to be used in programmed operations to alter the sequence of operations depending upon the status of these triggers individually, in groups, or in the entirety. These indicators are loaded from storage or an internal register or the contents thereof are transferred to storage or an internal register. Single or multiple indicators can be set, reset, inverted or tested by reference to a word in a register, in storage, or in the instruction itself. These indicators are used as program sense switches, sense lights, or selectors and by operation with the storage and arithmetic device in the computer may perform the logical operations as follows:

2

|            | A | B | A | B | A | B | A | B |                                    |
|------------|---|---|---|---|---|---|---|---|------------------------------------|
|            | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |                                    |
| 5 (1)----  | 1 |   | 1 |   | 1 |   | 1 |   | Trivial.                           |
| (2)----    | 0 |   | 1 |   | 1 |   | 1 |   | OR.                                |
| (3)----    | 1 |   | 0 |   | 1 |   | 1 |   | A or Not B (A implied by B).       |
| 10 (4)---- | 1 |   | 1 |   | 0 |   | 1 |   | B or Not A (A implies B).          |
| (5)----    | 1 |   | 1 |   | 1 |   | 0 |   | Not (A and B).                     |
| (6)----    | 0 |   | 0 |   | 1 |   | 1 |   | A.                                 |
| 15 (7)---- | 0 |   | 1 |   | 0 |   | 1 |   | B.                                 |
| (8)----    | 1 |   | 0 |   | 0 |   | 1 |   | If and Only If (Not Exclusive OR). |
| (9)----    | 1 |   | 0 |   | 1 |   | 0 |   | $\overline{B}$ .                   |
| 20 (10)--- | 1 |   | 1 |   | 0 |   | 0 |   | $\overline{A}$ .                   |
| (11)---    | 0 |   | 1 |   | 1 |   | 0 |   | Exclusive OR.                      |
| (12)---    | 1 |   | 0 |   | 0 |   | 0 |   | Neither A nor B (Sheffer Stroke).  |
| 25 (13)--- | 0 |   | 1 |   | 0 |   | 0 |   | (Not A) and B (Yes but).           |
| (14)---    | 0 |   | 0 |   | 0 |   | 1 |   | And.                               |
| (15)---    | 0 |   | 0 |   | 0 |   | 0 |   | Trivial.                           |

The contents A of the Sense Indicator Register are manipulated through the use of another word B which has a bit pattern composed of binary ones and zeros in any configuration desired by the programmer. Operations are performed in a manner such that each order of the word B is compared with a corresponding order of the contents A of the Sense Indicator Register. For the positions in the word B which contain a one, the corresponding position in the Sense Indicator Register is either modified or tested depending upon the type of Sense Indicator operation used. For the zero bits in the word B, the corresponding positions of the Sense Indicators are not affected. Four of the Sense Indicator operations, Place Accumulator in Indicators, Load Indicators, Place Indicators in Accumulators and Store Indicators are concerned with the transmission of full 36 bit words between the Sense Indicator Register and either the Accumulator or Magnetic Core Storage. The remaining twenty operations are used to test or modify the contents of the Sense Indicator Register. The twenty operations may be placed in five functional groups as follows:

### SET or LOGICAL OR

If the Sense Indicator Register contains word A, each order selected by the word B is replaced by a one.

### RESET

If the Sense Indicator Register contains word A, the contents of each Indicator position selected by the word B is replaced with a zero.

### INVERT

If the Sense Indicator Register contains word A, the contents of each Indicator position selected by the word B is replaced with its complement (ones are replaced by zero and zeros are replaced by ones).

### 3 ON TEST

If the Sense Indicator Register contains word A, the contents of each Indicator position is examined according to word B. If all examined positions contain ones, the calculator either transfers to a predetermined location in Core Storage or it skips the next instruction depending upon the testing operation used.

### OFF TEST

If the Sense Indicator Register contains word A, the contents of the Indicator Register are examined according to word B. If all examined portion contain zero, the Central Processing Unit either transfers to a predetermined location or skips the next instruction depending upon the testing operation.

A program is often written that deals with a problem in which several variations occur other than the usual transfer or branching, and it is decided to use a general program. This may be done with blocks of instructions and control in the general program is then transferred from block to block in the sequence determined by the particular variation being solved as interpreted by the configuration of the contents in the Sense Indicators using the operations described above.

The Sense Indicator Register may be used to monitor the program executed by the calculator by keeping a record of particular operations since bits in orders of the Sense Indicator Register may be set in accordance with those operations. Entire transactions in the form of a word may then be tested by the calculator or stored for subsequent reference at any other time by using the logical instructions and the store instruction.

It is a first object of this invention to provide improved apparatus for the logical operations upon individual orders of a binary word.

It is an object of this invention to provide improved apparatus including a register for extracting words from storage or other registers directly, as well as providing for the ability to program extracts.

It is an object of this invention to provide improved apparatus for performing logical operations other than but including AND, OR, and EXCLUSIVE OR.

It is another object of this invention to provide a plurality of switches which may be used singly or in groups as alternators and/or programmed counters.

It is an object of this invention to provide an improved data processing system including an additional register for the transfer of data words between the other registers for logical data manipulation including complementing, ANDing, and ORing of the data words.

It is an object to provide an improved device to collectively store unrelated manifestations of information in a single word within the data processing unit.

It is an object of this invention to provide an improved system including a register which is an extension of storage by a predetermined amount and is independently operable and accessible without a storage reference.

It is a still further object of this invention to provide apparatus for executing logical operations in response to instructions including a storage register, an adder, an accumulator, circuits connecting a portion of the storage register orders to a portion of said non-corresponding orders of the adder, an indicator register having true and complement outputs, and each order being a bistable device with a first input effective when the device is in a one state, second inputs effective when the device is in the zero state, and binary inputs, a storage device providing information to the registers, and circuits operable in response to the operations decoder for manipulating the information and operating inputs of the Indicator Registers.

Other objects of the invention will be pointed out in the following description and claim and illustrated in the accompanying drawings, which disclose, by way of ex-

### 4

ample, the principle of the invention and the best mode, which has been contemplated, of applying that principle.

In drawings:

FIGURE 1 is an overall block diagram illustrating the general arrangement and interconnections of the major components comprising the Central Processing Unit.

FIGURES 2a through 2ll form the logical block diagrams for the principal data portions of the Central Processing Unit and Magnetic Core Storage.

FIGURE 2mm illustrates how FIGURES 2aa through 2ll inclusive, may be placed to form a composite block diagram of the major data portions of the Central Processing System.

FIGURES 3a through 3k illustrate the Word Formats used in the Data Processing System.

FIGURE 4a is a Timing Chart of the Load Indicators Instruction.

FIGURE 4b is a Timing Chart of Place Accumulator in Indicator.

FIGURE 4c is a Timing Chart of ON Test for Indicators.

FIGURES 5a through 5f illustrate portions of the Storage Register and Storage Register Hold Circuits in logical block form.

FIGURES 6a through 6n illustrate the Adder and True Complement Controls in logical block form.

FIGURES 7a through 7g illustrate the Accumulator Register in logical block form.

FIGURES 8a through 8g illustrate the Multiplier Quotient Register and its associated hold circuits in logical block form.

FIGURE 9 illustrates the Index Register in logical block form.

FIGURE 10 illustrates the Indicator Trigger Register in logical block form.

FIGURES 11a, 11b and 11c illustrate the Storage Bus Switching, columns S through 35 in logical block form.

FIGURE 12 illustrates the Operator's Panel Entry Keys (S through 35).

FIGURES 13a, 13b, 13c (2 sheets) and 13d (3 sheets) illustrate positions 1 through 17 on the Instruction Register (Primary Operations Part) in logical block form.

FIGURES 14a through 14d illustrate the Primary Operation Decoder in logical block form.

FIGURES 15a and 15b illustrate the Secondary Operation Decoder in logical block form.

FIGURES 16a (2 sheets) and 16b (2 sheets) illustrate the Address Register in logical block form.

FIGURE 17 (2 sheets) illustrates the Instruction Counter in logical block form.

FIGURE 18 illustrates the Add and Subtract Execution Control in logical block form.

FIGURE 19 illustrates Clear and Add/Subtract Execution Control in logical block form.

FIGURE 20 illustrates MPY/MPYR EXEC CNTLS (Multiply Execution Controls) in logical block form.

FIGURES 21a (2 sheets) and 21b (2 sheets) illustrate Floating Point Add/Subtract Execution Controls in logical block form.

FIGURE 22 illustrates Floating Point Trap Trigger in logical block form.

FIGURE 23 illustrates Floating Point Multiply Execution Controls in logical block form.

FIGURE 24 (2 sheets) illustrates Conditional Transfer Execution and Control in logical block form.

FIGURE 25 illustrates Conditional Transfer Controls for transfer on Low MQ in logical block form.

FIGURE 26 illustrates Store Execution Controls in logical block form.

FIGURE 27 illustrates Long Left, Logical Left Execution Control in logical block form.

FIGURE 28 illustrates Long Right, Logical Right Execution Control in logical block form.

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FIGURE 29 illustrates OR to Storage Execution Control.

FIGURE 30 illustrates AND to Accumulator and to Storage Execution Control.

FIGURE 31 illustrates OR to Accumulator Execution Control.

FIGURE 32 illustrates Load Index Register Control.

FIGURE 33 illustrates Place Address in Index Register Control and Place Decrement in Index Register in logical block form.

FIGURE 34 illustrates Transfer with Index Raise Execution Control.

FIGURES 35a and 35b illustrate Indexing Execution Control in logical block form.

FIGURES 36a (2 sheets) and 36b illustrate Convert Control in logical block form.

FIGURE 37 illustrates EXCLUSIVE OR to Accumulator in logical block form.

FIGURE 38 illustrates Exchange, Transfer Sign Control in logical block form.

FIGURE 39 illustrates Test Indicators (Storage) Half Test Indicators in logical block form.

FIGURE 40 illustrates Transfer-Indicators (Accumulator) in logical block form.

FIGURE 41 illustrates Place Indicators in Accumulator and Reset Indicators from Accumulator in logical block form.

FIGURE 42 illustrates Half Indicator Register Controls in logical block form.

FIGURE 43 illustrates Multiply and Multiplier, Floating Point Multiply Trigger and Shift/Step controls in logical block form.

FIGURE 44 illustrates Place Accumulator in Indicators, Load Indicators, Invert Indicators or Accumulator Indicators in logical block form.

FIGURE 45 illustrates Storage and Multiplicand Zero Test in logical block form.

FIGURE 46 illustrates Interrupt Control in logical block form.

FIGURE 47 illustrates Execution Control Trigger (T1).

FIGURE 48 illustrates Inverter Trigger T2.

FIGURE 49 illustrates Index Register (N) Hold Lines Adder to Index Register (N).

FIGURE 50 illustrates Adders to Index Register (N) Gating Line Control.

FIGURE 51 illustrates Index Register to Adders Gating Line.

FIGURE 52 illustrates Index Register Mixing Unit in logical block form.

FIGURES 53a and 53b illustrate Storage Bus to Storage Register.

FIGURES 54a (2 sheets) and 54b (2 sheets) illustrate Storage Register (1-8) to Adder and Storage Register (9-35) to Adder.

FIGURES 55a (2 sheets), 55b, 55c (2 sheets) and 55d illustrate True Accumulator (Q, P, 1-8) to Adders; True Accumulator (9-25) to Adders.

FIGURE 56 illustrates Carry to Adder (35) in logical block form.

FIGURES 57a and 57b (2 sheets) illustrate Adder (Q, P, 1-8) to Accumulator; Adder (9-35) to Accumulator in logical block form.

FIGURE 58 illustrates Shift Accumulator Register Left Control.

FIGURE 59 illustrates Shift Accumulator Register Right Control.

FIGURE 60 illustrates MQ positions S, 1 or 9 to Accumulator 35, 1 to Accumulator 35 Control in logical block form.

FIGURE 61 illustrates Plus to Accumulator Register position S control.

FIGURE 62 illustrates Minus to Accumulator Register S Control.

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FIGURE 63 illustrates Storage Register S, 1 through 35 to MQ Register Controls in logical block form.

FIGURE 64 illustrates Shift MQ Right Controls in logical block form.

FIGURE 65 illustrates Shift MQ Left Controls in logical block form.

FIGURE 66 illustrates Clear MQ Register in logical block form.

FIGURE 67 illustrates Ring Shift MQ in logical block form.

FIGURE 68 illustrates 1 to MQ Register position 35 Control in logical block form.

FIGURE 69 illustrates I/O Bus, S through 35, to MQ Register Controls in logical block form.

FIGURE 70 illustrates Adders to Accumulator Controls in logical block form.

FIGURE 71 illustrates Minus to MQ position S controls in logical block form.

FIGURES 72a and 72b illustrate Accumulator to Storage Bus Controls.

FIGURE 73 illustrates operation Panel Keys to Storage Register Controls.

FIGURE 74 illustrates MQ Register S, 1 through 35 to Bus S, 1 through 35 and Storage MQ Register Store Control.

FIGURE 75 illustrates Address Switches to Storage Bus 3 through 17, 21 through 35 control.

FIGURE 76 illustrates Clear and Add/AND Control.

FIGURE 77 illustrates Ones to Storage Register S Control in logical block form.

FIGURE 78 illustrates 35 to Shift Counter Control in logical block form.

FIGURE 79 illustrates Step Shift Counter Controls in logical block form.

FIGURE 80 illustrates Adder (1) Carry or Accumulator (1 or P) to Overflow Trigger Controls.

FIGURE 81 illustrates Ones to Adders Q, P, 1 through 8 Controls in logical block form.

FIGURE 82 illustrates Carry to Adder Position 8 Controls in logical block form.

FIGURE 83 illustrates Floating Point Shift Control in logical block form.

FIGURE 84 illustrates Adders 1 through 8 to MQ 1 through 8 in logical block form.

FIGURE 85 illustrates Step Floating Point Tally Counter in logical block form.

FIGURES 86a and 86b illustrate Indexing Operation and Storage Register 18 through 35 to Adders P through 17.

FIGURES 87a and 87b illustrate Index Register to Adder Controls in logical block form.

FIGURE 88a illustrates Floating Point Tally Counter.

FIGURE 88b illustrates Trapping Control in logical block form.

FIGURES 89a and 89b illustrate Index Register Entry Control Carry One to Adder 16 and Carry One to Adder 17 Controls.

FIGURES 90a and 90b illustrate Indexing Controls.

FIGURES 91a and 91b illustrate Adder to Index Register.

FIGURE 92 illustrates Electronic Reset of Indicators.

FIGURE 93 illustrates Reset Indicators Controls in logical block form.

FIGURE 94 illustrates Set Indicators Controls in logical block form.

FIGURE 95a illustrates Invert Indicators Controls in logical block form.

FIGURE 95b illustrates Display Indicators.

FIGURE 96 illustrates Indicators to Storage Bus Controls in logical block form.

FIGURE 97 illustrates Complement Indicators to Storage Register Controls in logical block form.

FIGURE 98 illustrates Indirect Addressing Controls in logical block form.

FIGURE 99 illustrates Instruction Register Pulse Generator in logical block form.

FIGURE 100 (2 sheets) illustrates Instruction Register Sign, Plus and Minus Controls in logical block form.

FIGURE 101 illustrates Shift Counter Pulse Generator I in logical block form.

FIGURE 102 illustrates Shift Counter Pulse Generator II in logical block form.

FIGURE 103 illustrates Zero Address Controls.

FIGURE 104 illustrates Floating Point Entry to Shift Counter 10 through 17 Controls.

FIGURE 105 illustrates Subtract control in logical block form.

FIGURE 106 illustrates Sense Unit Address in logical block form.

FIGURE 107 (2 sheets) illustrates Advance Instruction Counter in logical block form.

FIGURE 108 illustrates Reset Instruction Counter Address Switch to Instruction Counter Control in logical block form.

FIGURE 109 illustrates Instruction Counter Transfer Control in logical block form.

FIGURES 110a and b illustrate Address Switch Input Controls in logical block form.

FIGURE 111 illustrates Enter MQ Control in logical block form.

FIGURE 112 illustrates the Primary Drive Circuits.

FIGURE 113 illustrates a Sign Mixing Controls.

FIGURE 114 illustrates the Master Oscillator.

FIGURE 115 illustrates the Inverted Sync Generator.

FIGURE 116 illustrates the Inverted Clamp Generator and Clock Drive.

FIGURE 117 (2 sheets) illustrates the Clock.

FIGURE 118 (2 sheets) illustrates Cycle Timer Control.

FIGURE 119 illustrates Cycle Timer Gate Generator.

FIGURE 120 illustrates Cycle Timer Output Circuit.

FIGURE 121 illustrates B Time Control.

FIGURES 122a (2 sheets) to p illustrate Pulse and Gate Generator Controls.

FIGURE 123 illustrates Column Q Carry and Overflow Triggers.

FIGURE 124 illustrates Column 9 Carry and Overflow Triggers.

FIGURE 125 illustrates Floating Point Overflow Trigger and Floating Point Underflow Trigger.

FIGURE 126a indicates Adder X Carry Trigger.

FIGURE 126b illustrates Divide Check Trigger.

FIGURE 127 illustrates Floating Point Overflow and Underflow Detection.

FIGURES 128a (2 sheets), b and c illustrate End Operation Control.

FIGURES 129a and b illustrate the Storage Address Register.

FIGURES 130a and b illustrate the Pulse Generator I and II.

FIGURE 130c illustrates Timing Pulse Control Circuits.

FIGURES 131a and b illustrate the Address Decoder Circuit.

FIGURES 132a and b illustrate the Address Decoder Circuit.

FIGURE 133 illustrates Write Driver Select Circuits

FIGURES 134a and b illustrate Gate Generator.

FIGURE 135 illustrates the X Matrix Switch Write Driver.

FIGURE 136 illustrates the X Matrix Switch Read Driver.

FIGURE 137a illustrates the Y Driver Matrix Switch Layout.

FIGURE 137b illustrates diagrammatically a Core with certain of its control Windings.

FIGURE 138a illustrates diagrammatically the Core Array Layout.

FIGURE 138b illustrates, in isometric a Core with Windings.

FIGURE 139 illustrates the Y Matrix Switch Write Driver.

FIGURE 140 illustrates the Y Matrix Switch Read Driver.

FIGURE 141a illustrates the X Driver Matrix Switch Layout.

FIGURE 141b illustrates diagrammatically a Core with certain of its Control Windings as in FIG. 137b.

FIGURES 142a, b, and c illustrate the Sense Amplifier, Buffer Register and I/O Switching.

FIGURE 143 illustrates the Digit Plane Select Circuits.

FIGURE 144 illustrates the Digit Plane Driver Circuits.

FIGURE 145 illustrates the Address and Operation Control.

FIGURE 146 illustrates the Read/Write Controls.

FIGURES 147a, b, and c illustrate Test Circuits, Test and Reset Controls and the Test Panel Circuits.

FIGURE 148a illustrates Switch Core Panel and Core Plane Addressing (Octonary).

FIGURE 148b is a timing chart illustrating the Timing of Magnetic Core Storage in sequence for one cycle from 3 time of a first cycle until 3 time of a second cycle.

FIGURE 149 illustrates Compare Accumulator with Storage.

The convention employed in numbering lines in the logical block diagrams is as follows: from left to right, the first numbers and the letter, if any, to the period or point is the figure number from which the line originated; the next two numbers to the second point refer to the output lines (generally numbered according to their positions on the sheet from top to bottom); and the last two numbers, when used, refer to the numerical position of the line with the word S, 1 through 35. Each input line in the block diagram bears the number derived from its point of origin. In the composite drawings, data flows generally into the block at the top and out of the block at the bottom, and control lines which cause the movement of data enter the block from the left.

In FIGURE 1, there is shown a Central Processing Unit of a high speed Data Processing system which is controlled by an internally stored program with instructions of the single address type which direct the machine to execute instructions at the rate of about 20,000 per second. The functions of transferring data in and out of the Central Processing Unit from Input-Output devices, Magnetic Core Storage, Magnetic Drum Storage, are controlled by the stored program as well. Internally, the Central Processing Unit operates in the binary number system, but the Input-Output number system may be those used in punched card systems, the decimal system, or the binary coded decimal (BCD) system to name a few. Many of the basic devices of the Central Processing Unit, shown generally in FIGURE 1, and more specifically in FIGURE 2, assume two stable states and are well suited to the binary system of notation where one specified state is indicative of a binary "one" and the other state is indicative of a binary "zero." The basic unit of information, the Word, consists of thirty-six binary digits and many be alphabetic, numeric, symbolic, an instruction, or any pattern of thirty-six bits desired by the programmer for any reason. The thirty-six positions of the word are shown schematically in FIGURE 3 where S refers to the sign position, 1 refers to bit position 1, 2 refers to bit position 2 and so forth. Only when a word is interpreted as numerical data does position S have any algebraic significance. Then, with position S con-

taining a "zero" the word is signified as positive and with position S containing a "one" the word is signified as negative. When a logical operation is performed upon a word, the word is interpreted as a thirty-six bit signless number.

Individual location in Magnetic Core Storage, Magnetic Drum Unit and individual units such as Magnetic Tape Units and all other Input-Output Units are identified by systems of numerical addresses, as described more fully in copending application, Serial No. 705,447, filed December 26, 1957. By means of a number contained in the Address part of the Instruction, it is possible to refer to the information contained in any location in Magnetic Core Storage or any Input-Output Unit of the system.

In FIGURE 1, the Central Processing Unit has data portions which comprise a thirty-six order Storage Register 1.01 comprising thirty-five orders and a sign order, a thirty-six order Adder 1.03 plus one overflow order, an Accumulator Register 1.05 of thirty-five orders plus two overflow orders P and Q and a sign order S, a Multiplier Quotient Register 1.07 comprising thirty-five orders and a sign order, three Index Registers 1.09 A, B, and C of fifteen orders and their associated Index Register controls, an Indicator Trigger Register 1.12 of thirty-six orders 0 through 35, Storage Bus Switching 1.14 of thirty-six orders connected to a Storage Bus 1.16 of thirty-six orders, the latter being connected to Magnetic Core Storage, and Operator's Entry Keys 1.18 of thirty-six orders. Associated with the data portion previously described is an Instruction Register 1.20 of eighteen positions S, 1 through 17, an Address Register 1.22, and an Instruction Counter 1.24 with related Storage Address Controls 1.26. Information may be placed in Core Storage from either the Accumulator Register 1.05, the Multiplier Quotient Register 1.07, or the Indicator Register 1.12. It is a function of the Storage Bus Switches 1.14 to switch the contents of the Accumulator Register, the MQ Register, or the Indicator Register onto the Storage Buses 1.16 in accordance with the execution of certain instructions which require that information be located in Storage.

The Central Processing Unit and Core Storage of the present invention may be employed in a data processing system which includes Data Synchronizers, Tape Control Units, Tape Drive Units, Printers, Perforating machines and Readers. The Data Synchronizers are used to control the flow of information from the input-output devices such as Tape Control Units, Tape Drive Units and Readers to Core Storage and to control the flow of information from Core Storage to the Tape Units, Printers, and Perforating machines. The Tape Control Unit controls all operations to be executed by the Tape Drive Units and assembles and disassembles 36 bit words as required in the transmission of data through the system.

A detailed description of general operations of a computer of this class which may be performed in response to well-known instructions is found in copending application Computer for 701, Serial No. 419,642, Haddad et al., filed March 30, 1954. Certain arithmetic, logical, and other operations may be performed by the device of the present invention in response to instructions tabulated immediately below in accordance with the principles set forth in Manual of Operations, Electronic Data Processing Machines, Type 704, Form No. 24-6661, copyright 1954, 1955, and printed in the U.S.A. by International Business Machines Corporation, the assignee of this application. The operation codes specify the particular operation to be performed and are tabulated in numeric form below. However, each numeric code must be translated into machine language which is in the binary code. For example, 0361 (octal) is expressed as 000011110001.

|    | Title                                 | Operation Code        |
|----|---------------------------------------|-----------------------|
|    | Add and Carry Logical Word.....       | ACL + 0361            |
|    | Add.....                              | ADD + 0400            |
| 5  | Add Magnitude.....                    | ADM + 0401            |
|    | Accumulator Left Shift.....           | ALS + 0767            |
|    | AND to Accumulator.....               | ANA - 0320            |
|    | AND to Storage.....                   | ANS + 0320            |
|    | Accumulator Right Shift.....          | ARS + 0771            |
|    | Backspace Tape.....                   | BST + 0764            |
|    | Clear and Add Logical Word.....       | CAL - 0500            |
| 10 | Compare Accumulator with Storage..... | CAS + 0340            |
|    | Change Sign.....                      | CHS + 0760 . . . 0002 |
|    | Clear and Add.....                    | CLA + 0500            |
|    | Clear Magnitude.....                  | CLM + 0760 . . . 0000 |
|    | Clear and Subtract.....               | CLS + 0502            |
|    | Complement Magnitude.....             | COM + 0760 . . . 0006 |
|    | Divide Check Test.....                | DCT + 0760 . . . 0012 |
|    | Divide or Halt.....                   | DVH + 0220            |
| 15 | Divide or Proceed.....                | DVP + 0221            |
|    | Enter Trapping Mode.....              | ETM + 0760 . . . 0007 |
|    | Floating Add.....                     | FAD + 0300            |
|    | Floating Divide or Halt.....          | FDH + 0240            |
|    | Floating Divide or Proceed.....       | FDP + 0241            |
|    | Floating Multiply.....                | FMP + 0260            |
|    | Floating Subtract.....                | FSB + 0302            |
| 20 | Halt and Proceed.....                 | HPR + 0420            |
|    | Halt and Transfer.....                | HTR + 0000            |
|    | Low Order Bit Test.....               | LBT + 0760 . . . 0001 |
|    | Locate Drum Address.....              | LDA + 0440            |
|    | Load MQ.....                          | LDQ + 0560            |
|    | Logical Left.....                     | LGL - 0763            |
|    | Long Left Shift.....                  | LLS + 0763            |
| 25 | Long Right Shift.....                 | LRS + 0765            |
|    | Leave Trapping Mode.....              | LTM - 0760 . . . 0007 |
|    | Load Index from Address.....          | LXA + 0534            |
|    | Load Index from Decrement.....        | LXD - 0534            |
|    | Multiply and Round.....               | MPR - 0200            |
|    | Multiply.....                         | MPY + 0200            |
|    | Minus Sense.....                      | MSE + 0760            |
|    | No Operation.....                     | NOP + 0761            |
| 30 | OR to Accumulator.....                | ORA - 0501            |
|    | OR to Storage.....                    | ORS - 0602            |
|    | Place Address in Index.....           | PAX + 0734            |
|    | P-Bit Test.....                       | PBT - 0760 . . . 0001 |
|    | Place Decrement in Index.....         | PDX - 0734            |
|    | Plus Sense.....                       | PSE + 0760            |
|    | Place Index in Decrement.....         | PXD - 0754            |
| 35 | Read Select.....                      | RDS + 0762            |
|    | Rewind.....                           | REW + 0772            |
|    | Round.....                            | RND + 0760 . . . 0010 |
|    | Rotate MQ Left.....                   | RQL - 0773            |
|    | Subtract Magnitude.....               | SBM - 0400            |
|    | Store Left Half MQ.....               | SLQ - 0620            |
|    | Store Logical Word.....               | SLW + 0602            |
| 40 | Set Sign Minus.....                   | SSM - 0760 . . . 0003 |
|    | Set Sign Plus.....                    | SSP + 0760 . . . 0003 |
|    | Store Address.....                    | STA + 0621            |
|    | Store Decrement.....                  | STD + 0622            |
|    | Store.....                            | STO + 0601            |
|    | Store Prefix.....                     | STP + 0630            |
|    | Store MQ.....                         | STQ - 0600            |
|    | Subtract.....                         | SUB + 0420            |
| 45 | Store Index in Decrement.....         | SXD - 0634            |
|    | Transfer on Index.....                | TLX + 2000            |
|    | Transfer on Low MQ.....               | TLQ + 0040            |
|    | Transfer on Minus.....                | TMI - 0120            |
|    | Transfer on No Overflow.....          | TNO - 0140            |
|    | Transfer on No Index.....             | TNX - 2000            |
|    | Transfer on No Zero.....              | TNZ - 0100            |
|    | Transfer on Overflow.....             | TOV + 0140            |
| 50 | Transfer on Plus.....                 | TPL + 0120            |
|    | Transfer on MQ Plus.....              | TQP + 0162            |
|    | Transfer.....                         | TRA + 0020            |
|    | Transfer and Set Index.....           | TSX + 0074            |
|    | Trap Transfer.....                    | TTR + 0021            |
|    | Transfer on Index High.....           | TXH + 3000            |
|    | Transfer with Index Incremented.....  | TXI + 1000            |
| 55 | Transfer on Index Low or Equal.....   | TXL - 3000            |
|    | Transfer on Zero.....                 | TZE + 0100            |
|    | Unnormalized Floating Add.....        | UFA - 0300            |
|    | Unnormalized Floating Multiply.....   | UFM - 0260            |
|    | Unnormalized Floating Subtract.....   | UFS - 0302            |
|    | Write End of File.....                | WEF + 0770            |
|    | Write Select.....                     | WRS + 0766            |

Still other instructions not described in this application cause operations to be performed in accordance with the principles described in copending applications, Serial No. 705,447, filed December 26, 1957; Serial No. 705,445, filed December 26, 1957; Serial No. 705,446, filed December 26, 1957; and Serial No. 705,442, filed December 26, 1957.

In FIGURE 4, there is illustrated the general timing relationship of machine operations performed in accordance with the principles of this invention. At this time, reference to the figure serves only to show generally the sequence of operations in order that a better understanding of the structure may be had while reading the description of the system to follow, after which the operations are described in detail.

The term "data" is used to describe transmission of information which is not destined for interpretation as an instruction or command even though ultimately it may, in some other program routine, be interpreted as an instruction or command or part of either subject to modification by the machine or the program or a combination thereof.

In FIGURE 2, data portions of the Central Processing Unit of FIGURE 1 are shown in FIGURES 2a through 2gg which comprise the Storage Register, FIGURES 2b through 2d, (FIGURES 5a-5f); the Adder, FIGURES 2j through 2u, (FIGURES 6a-6m); the Accumulator Register, FIGURES 2x through 2cc, (FIGURES 7a-7g); the Multiplier Quotient Register, FIGURES 2dd through 2gg, (FIGURES 8a-8g); the Index Registers, FIGURES 2f and 2g (FIGURE 9); the Indicator Register, FIGURE 2a (FIGURE 10); Storage Bus Switching, FIGURES 2w through 2y (FIGURE 11); the Storage Bus, FIGURES 2w through 2y; and the Operator's Entry Keys, FIGURE 2e (FIGURE 12). Associated with the data portion previously described is the Instruction Register, FIGURE 2h (FIGURE 13), the Primary and Secondary Operation Decoders, FIGURES 14 and 15, and the Address Register, FIGURE 2i, (FIGURE 16), and the Instruction Counter, FIGURE 2v. Magnetic Core Storage as a unit is shown in FIGURES 2hh through 2ll and Storage Address Controls are shown in FIGURES 2hh through 2kk.

#### ARITHMETIC CONTROL

The Arithmetic Control section of the CPU is to determine what operation must be performed for executing each instruction and to sequence these operations. In order to perform this function, there are Execution Controls illustrated in FIGURES 18 through 51 for each arithmetic instruction. Arithmetic Control Mixing Circuits or Command Circuits are illustrated in FIGURES 52 through 98 which take the information from the Execution controls and provide gates and pulses to perform each operation required.

#### PROGRAM CIRCUITS

The information received from Core Storage by the Central Processing Unit is initially placed in the Storage Register, FIGURES 2b through 2d, from the Sense Amplifier Buffer and I/O Switching of FIGURE 2ll prior to being operated on by the Program and Arithmetic circuits. The registers and counters used to receive and decode the instructions consist of the Instruction Register, FIGURE 13, the Instruction Counter, FIGURE 17, the Primary Operation Decoder, FIGURE 14, the Secondary Operation Decoder, FIGURE 15, and related control circuits, FIGURES 99-111. The Storage Address Register, FIGURES 129a and b, controls the addressing of the Core Storage Unit and is located in the unit it controls, that is, Magnetic Core Storage 1.12, illustrated functionally in FIGURES 2hh-2ii. Each of the registers and counters is described individually with reference to its function in the overall flow of information and both general and specific timings are set forth later in connection with the receiving and decoding of instructions.

The input information to the execution controls is primarily the output of the Instruction Register, FIGURE 13, which is routed through the Primary Operation Decoder, FIGURE 14, and the Secondary Operation Decoder, FIGURE 15. The decoder output is often mixed with an indication of one of the following conditions to provide conditional operation: (1) whether an overflow has occurred in the Accumulator, (2) whether the carry output from column Q of the adder is present, (3) whether the carry output from column 6 of the adder is present, (4) whether the contents of the sign position of the Accumulator Register, the Storage Register or the Quotient Register is negative, or (5) whether the Shift Counter is at "0" or not (The Shift Counter as described later, is used to count E/R (Execute-Route) cycles for a multiply

or a Divide instruction and is also used to count the number of shifts in a Shifting instruction.) The command circuits are provided with pulses or gates which circuits become the output command lines or control lines when they are conditioned by the outputs of the execution controls.

The Storage Register, FIGURES 2b-d, has inputs 12.01.01 through 12.01.36 to each of its positions S, 1 through 35 from respective ones of positions S, 1 through 35 of the Entry Keys, FIGURE 2e. The Storage Register also has inputs 11b.03 and 11c.03 to positions 1 through 35 from corresponding outputs of positions 1 through 35 of Storage Bus Switching, FIGURES 2w-y. Another set of inputs 10.01S through 10.01.35 is provided to the Storage Register Positions S, 1 through 35 from the outputs of the Indicator Register, FIGURE 2a, positions O, 1 through 35. Outputs 5a.04; 5b.06; 5c.04; and 5f.05 are provided from Storage Register, positions S, 1 through 35 to the input of positions O, 1 through 35 of the Indicator Register. Outputs 5b.04 are provided from the Storage Register positions 1, 2, 8 and 9 to *Indexing Controls*, FIGURE 90. Outputs 5b.07 from Storage Register positions 3 through 11 are provided to positions 1 through 9 of the Instruction Register, FIGURE 2h, with additional lines 5b.07.01 and 5b.07.02 from positions 1 and 2 to the Instruction Register Pulse Generator, FIGURE 99. Furthermore, an additional pair of outputs 5b.07 from Storage Register positions 1 and 2 are sent to the inputs 5b.07.01 and 5b.07.02 of the Instruction Register positions 8 and 9. Outputs 5a.02S; 5b.03; 5c.08; and 5f.08 from Storage Register positions S, 1 through 35 are provided to respective positions S, 1 through 35 of the MQ Register, FIGURES 2dd-gg. Outputs 5b.05 from positions 12 and 13 of the Storage Register, FIGURE 2c are provided to *Indirect Addressing Controls*, FIGURE 98. Outputs 5b.02; 5c.07; 5f.07 are provided from positions 1 through 35 of the Storage Register to respective inputs 1 through 35 of the Adder Register. Outputs 5a.01 and 5b.01 from positions S, 1 through 5 of the Storage Register, FIGURES 2b-2d are provided to the inputs of positions 30 through 35, FIGURE 2gg of the MQ Register. Outputs 5c.02; 5c.09; 5f.06 from positions 19 through 35 of the Storage Register are provided to the inputs of positions 1 through 17 of the Adder. Output 5c.01 for S position 18 of the Storage Register is provided to *Ones to Adder*, FIGURE 81. Outputs 5c.06 are provided from positions 18 through 20 of the Storage Register, FIGURE 2d, to *Index Register Hold Lines and Adder Control*, FIGURE 49. Outputs 5f.01; 5f.03 are provided from positions 24 through 26 of the Storage Register, FIGURE 2d to *Channel Select*, FIGURE 153. Outputs 5f.04 from Storage Register positions 24 through 26, FIGURE 2d, are provided to the Data Synchronizer Instruction Decoder, FIGURE 160 and outputs 5f.02.24-26 are provided from positions 24 through 26 of the Storage Register to *Sense Unit Address Control*, FIGURE 106. Outputs 5c.05.18-20 are taken from positions 18 through 20 of the Storage Register and are sent to *Index Registers to Address Gating Line*, FIGURE 51.

The Adder Register has positions Q, P and 1 through 35 as previously described and inputs 81.01 through 81.10 are provided to positions Q, P, 1 through 8 from *Ones to Adder Control*, FIGURE 81. Inputs 7g.01; 7b.02; 7c.02; 7d.02 are provided to positions Q, P and 1 through 35 of the Adder Register from positions Q, P and 1 through 35 outputs of the Accumulator Register, FIGURES 2x-cc. Inputs are provided to positions 3 through 17 of the Adder Register FIGURES 2k-2q, from positions 3 through 17 of the Index Register Mixing, FIGURE 2f. Inputs are provided to Adder positions 6 through 17 from Drum Control of Drum Unit 1.14. Inputs 7c.03.30-34; 7d.03.35 are provided to positions 12 through 17 of the Adder, FIGURES 2k-2q, from positions 30 through 35, FIGURE 4cc, of the Accumulator Register, and inputs 8a.06; 8b.06; 8c.03 are provided to

positions 12 through 17 of the Adder from positions 1 through 5, FIGURE 2dd, of the MQ Register. Outputs are provided from the Adder as inputs to positions Q, P and 1 through 35 of the Accumulator Register. Outputs 6b.02; 6c.01; 6d.02; 6e.02 are provided from the Adder positions 1 through 8 to the input of positions 1 through 8 of the MQ Register. Outputs are provided from the Adder positions 3 through 17 to the inputs of each of the Index Registers A, B and C, FIGURE 9. Outputs are provided from the Adder positions 3 through 17 to the inputs of the Address Register, FIGURE 2i.

An output is provided from each lower order Adder position, FIGURES 2i-u, to the input of each higher order position as illustrated. For example, the carry output 6h.03, FIGURE 2u, of position 34 of the Adder is connected to the input of position 33 of the Adder, the carry output of position 33 of the Adder is connected to the input of position 32 of the Adder, and in like manner similar carry lines are connected through position Q.

Output lines are provided from positions 3 through 17 of the Address Register, FIGURE 2i (FIGURES 16a and 16b) as inputs to positions 3 through 17 of the Storage Bus Switches.

Inputs are provided to the Storage Bus Switching, FIGURES 2w-y, positions S, 1 through 35 from the output of the MQ Register positions S, 1 through 35 and inputs are provided to Storage Bus Switching positions S, 1 through 35 from the outputs of the Indicator Register. An input 7i.01S, FIGURE 2w, is provided to positions S of Storage Bus Switching from the output of position P, FIGURE 2aa, of the Accumulator Register. Inputs are provided to the Storage Bus Switching positions 1 through 35 from positions 1 through 35 of the Accumulator Register and there is a connection 7b.01P between the output of position P, FIGURE 2aa, of the Accumulator Register to the input of the S position, FIGURE 2w, of the Storage Bus Switching.

An output 11a.04S is provided from position S, FIGURE 2w, of Storage Bus Switching to Minus on Storage Register, FIGURE 77. Outputs 11a.02; 11b.04; 11c.04 are provided from the Storage Bus Switching positions S, 1 through 35 to Memory Buffer Register, FIGURE 142. Outputs 11a.03; 11b.01; 11c.01 are provided from Storage Bus Switching positions S, 1 through 5, FIGURES 2w-2x to position P, 1 through 5, FIGURES 2j-2l, of the Accumulator Register. Positions P, 1 through 35 of the Accumulator Register have outputs from each lower order position connected to the next adjacent higher order position terminating at the input of position P for the purpose of shifting left. There are outputs from positions Q, P, 1 through 34 of the Adder to the inputs of the next adjacent lower order position terminating with the output position 34 entering as an input of position 35 for shifting right. Position Q of the Accumulator Register has an output 7g.02Q to the Carry Overflow Trigger, FIGURE 123, and another output 7g.03Q to 2, Floating Point Overflow/Underflow Detection, FIGURE 127. An output line 7b.07P is provided from position P of the Accumulator Register to Test Sense Input (not shown in the drawings) and another output 7b.08P to Floating Point Overflow/Underflow Detection Controls, position 1 of the Accumulator Register has an output 7b.01.01 to Adder 1 Carry to Accumulator Overflow Trigger, FIGURE 80. Outputs are provided from the Accumulator Register positions P, 1 through 35 to the input of Storage Bus Switching positions S, 1 through 35 as previously described. Position 9 of the Accumulator Register has two output lines 7c.06.08 and 7c.07.09 to Column 9 Carry and Overflow Trigger, FIGURE 124, and to Floating Point Add/Subtract Execution Controls, FIGURES 21a and 21b. An output 7d.08.35 from position 35, FIGURE 2cc, of the Accumulator Register is connected to the input of position S, FIGURE 2dd, of the Multiplier Quotient Register, and another output

7d.07.35 is connected to position 1 of the MQ, FIGURE 2dd.

Position S, FIGURE 2dd, of the MQ Register has an output line 8a.06S to Adder and True Complement Controls, FIGURE 6k, an output 8a.05S to Floating Point Shift Control, FIGURE 83, and another output 8a.01.S to Sign Mixing, FIGURE 113. Position 1 of the MQ Register, FIGURE 2dd, has an output 8b.03.01 to Floating Point Shift Control, FIGURE 83, has an output 8b.02.01 to Multiply Execution Control, FIGURE 20, and an output 8b.01.01 to Sense Unit Address, FIGURE 106; Position 8, FIGURE 2ee, of the MQ Register has an output 8d.01.03 to Floating Point Shift Control, FIGURE 83. Position 9, FIGURE 2ff, has an output 8e.02.09 to the Floating Point Shift Control, FIGURE 83, and an output 8e.01.09 that goes to Floating Point Round, FIGURE 106. Outputs 8e.06.34 and 8f.03.35 are provided from position 34 and position 35 to Multiply Floating Point Trigger Shift Step, FIGURE 43. Output lines are provided from positions S, 1 through 35 for entry of the Drum 1.10 in FIGURE 1. The output of each lower order position of the MQ Register is connected as an input to the next higher order position, for example, the output 8f.01.35 of Position 35, FIGURE 2gg, is connected to the input of position 34 and so forth in like manner until the final connection is made between the output of position 1 and the input of position S, FIGURE 2dd, of the MQ Register for left shifting. Furthermore, outputs are provided from each higher order position of the MQ Register to each adjacent lower order position beginning with the output 8a.04S of position S to the input of position 1 and ending in like manner with connections from the final one of the outputs 8e.03.34 to the input of position 35. A single input 68.01, FIGURE 2gg, is supplied to position 35 of the MQ Register from One to MQ Register, FIGURE 68.

Output lines are provided from positions 3 through 17 of the Address Register, FIGURE 2i, to positions 3 through 17 of the Instruction Counter, FIGURE 2v, and outputs are provided from positions 3 through 17 of the Address Register. Inputs are provided from Address Register, FIGURE 2i, positions 10 through 17 to the Instruction Register positions 10 through 17. An input is provided to position S of the Storage Register from 3.10.01 Primary Operation Decoder, FIGURES 14a through 14d.

#### CONTROL OF DATA FLOW

With reference to the Central Processing Unit, FIGURES 2a-gg, the flow of data is controlled in the following manner: Operator's Entry Keys S, 1 through 35, FIGURE 2e, via cable 12.01, then in parallel by the individual wires of the cables 12.01.S, 12.01.01, etc. to the Storage Register positions S, 1 through 35, FIGURES 2b-d, to Operator Panel Keys to Storage Register Control, FIGURE 73, which controls entry into positions S, 1 through 35 of the Storage Register, FIGURES 2b-d, or instead under control of Complement Indicators to Storage Register, FIGURE 97; the Indicator Register S, 1 through 35 are fed from the outputs of the Storage Register positions S, 1 through 35 via a cable under control of the Reset Indicators, FIGURE 93 (see also FIG. 2a), Set Indicators, FIGURE 94, or Invert Indicators, FIGURE 95, controls. Electronic Reset of Indicators Control is also provided in FIGURES 92 (see line 92.01) and 2a).

Data may also be transferred from positions 1 through 35 of the Storage Bus Switching, FIGURES 2w-y, via a cable to respective inputs of the Storage Register, FIGURES 2b-d, under control of Storage Bus to Storage Register Control, FIGURE 53. Data is transferred via cable from positions S, 1 through 35 of the Storage Register, FIGURES 2b-d, to positions S, 1 through 35 of the MQ Register, FIGURES 2dd-gg, under control of Stor-

age Register to MQ Register Controls, FIGURE 63. Outputs from positions S, 1 through 35 of the Storage Register, FIGURES 2b-d, are connected to positions P, 1 through 35 of the Adder Register, FIGURES 2j-u, for entry of data in response to operation of *Storage Register to Adder Control*, FIGURE 54. Data are also transferred between positions 18 through 35 only of the Storage Register, FIGURES 2c and d, to positions P through 17 of the Adder under control of *Storage Register (18-35) to Adder (P-17) Control*, FIGURE 86a. Six positions of data (1-5) contained in positions S, 1 through 35 of the Storage Register, FIGURES 2b-d, may be entered into positions 30 through 35 of the MQ Register, FIGURE 2gg, by means of *Convert Controls*, FIGURE 36. The negative of the contents of selected ones of the orders of the Index Register, FIGURES 2f and g, are provided to positions 3 through 17 of the Adder by means of *Index Register to Adders Gating Line*, FIGURE 51. True outputs of positions Q, P, 1 through 35 of the Accumulator Register, FIGURES 2z-cc, are transferred to positions Q, P, 1 through 35 of the Adders by means of the *True Accumulator to Adders Control*, FIGURES 55a and b. The complement of the Accumulator positions Q, P, 1 through 35 are provided to positions Q, P, 1 through 35 of the Adder under control of *Complement Accumulator to Adder*, FIGURES 55c and d. Carry output of position P, of the Adder is provided to the input of position 35 of the Adder by means of *Carry to Adder 35*, FIGURE 56. The contents of positions 3 through 17 of the Adders are supplied to selected ones of the Index Registers, FIGURES 2f and g, in response to operation of *Adders to Index Register Gating Line*, FIGURE 50. The contents of Adder positions 3 through 17 are transferred to the Address Register, FIGURE 2i, in response to operation of *Address Switch Input Controls*, FIGURE 110. The contents of positions 1 through 8 of the Adders are transferred to positions 1 through 8 of the MQ Register, FIGURES 2dd, 2ee, in response to operation of the Adders 1-8 to MQ 1-8 Controls, FIGURE 84. The contents of the Accumulator positions 30 through 35, FIGURE 2cc, are transferred to the Adder positions 12 through 17, FIGURES 2o-2q, in response to operation of *Convert Controls*, FIGURES 36a and b. The contents of positions S, 1 through 5 of the Storage Bus, FIGURE 2u, are entered in positions P, 1 through 5 of the Accumulator, FIGURES 2aa-2bb, in response to operation of *Convert Controls*, FIGURES 36a and b, which contents of Storage Bus Switching may be from Accumulator Register, the MQ Register or the Indicator Register as specified by the controls of Storage Bus Switching. Storage Bus Switching, FIGURES 2w-y, is not a storage device in the sense that a register is and it merely transfers information from the Accumulator Register, the MQ Register and the Indicator Register to the Storage Busses. The contents of the Address Register, positions 3 through 17, FIGURE 2i, may be placed in positions 3 through 17 of positions 21 through 35 of Storage Bus Switching, FIGURES w-y, in response to operation of *Address Switches to Storage Bus 3-17 and 21-35* of FIGURE 75. The contents of the MQ Register may be transferred to the Storage Busses via Storage Bus Switching by means of *MQ Registers S, 1-35 to Storage Bus S, 1-35 Control*, FIGURE 74. The contents of the Accumulator may be placed on the Storage Busses via Storage Bus Switching by means of *Accumulator to Storage Bus*, FIGURE 72. The Instruction Register, FIGURE 2h, is controlled by means of Shift Counter Pulse Generator I or Shift Counter Pulse Generator II, FIGURES 101 and 102. Data on the Storage Bus may be entered into the MQ by means of *I/O Bus S, 1-35 to MQ Register Control*, FIGURE 69. A word from the Drum, FIGURE 1.14 may be entered into the MQ Register positions S, 1 through 35 by way of the I/O Bus in response to operation of *I/O Bus, S, 1-35 to MQ Register S, 1-35*, FIGURE 69. The contents of the Address Register, FIGURE 2i, may be placed in the Address Register by

means of the *Control Address Switch Input*, FIGURE 110.

## CONTROL FLOW

There are two general types of control words, namely, an Instruction and a Command, both having an operation part and an address part. For the decoder of the purposes of explanation an Instruction is defined as a configuration of thirty-six bits which is decoded by the Central Processing Unit for the purpose of controlling an operation to be performed by the Central Processing Unit. This operation, if it be an Instruction for an Input-Output type of operation, is transmitted to a Data Synchronizer channel. The second type of control word is known as a Command, and is similar to an Instruction except it enters Transmission Registers of the Data Synchronizer Channel through which it acts like an Instruction and controls that kind of an operation dealing with the transmission of data between a Data Synchronizer Channel and Core Storage. Commands are decoded by the Transmission Register in a DSC. The difference between the two is that Instructions enter and are decoded by the Central Processing Unit whereas Commands enter and are decoded by the Data Synchronizer Channel.

For a better understanding of the operation of the system, control is divided into two sub-control levels, namely, initial control and operational control. Initial control means those control functions necessary to initiate an Input-Output operation and originates in the Central Processing Unit while operational control comprises those control functions necessary to maintain operation once started and to insure a proper completion. For example, during a system operation a Central Processing Unit instruction is needed to initiate any tape operation. Once started, initial control is then passed to the Data Synchronizer concerned, then to the Tape Control Unit, and finally to the Tape Drive Unit selected. Once each unit has satisfied its initial requirement, the control is then held by the units necessary to complete the operation desired. It is seen here, that except for initial operation, the Central Processing Unit is needed in the tape operation for one purpose only, which is to provide the Data Synchronizer Channel access to Core Storage, when such access is needed. For any one tape system (Tape Control Unit and connected Tape Drive Units), this will occur no more frequently than once every 400 microseconds. The Central Processing Unit is otherwise free during this time to pursue its other activities while operational control rests with the Data Synchronizer, the Tape Control Unit and the Tape Drive Unit.

The major function of the operational control is to determine when the other units involved will perform their specific functions to accomplish the given over-all operation. The function of the control logic circuits between the Data Synchronizer Unit and the Central Processing Unit is to determine when the Central Processing Unit will provide the Data Synchronizer needs access to Core Storage, to store or obtain a word. The function of the control logic circuits between the Tape Control Unit and the Data Synchronizer unit is multiple: (a) It indicates to the Data Synchronizer Unit when the Tape Control Unit has a word ready or needs a word, (b) it indicates when an operation is completed and whether completed by the Data Synchronizer or the Tape Control Unit, and (c) it also indicates the occurrence of special conditions, such as an error. The function of the control logic circuits between the Tape Drive Unit and the Tape Control Unit is to indicate to the Tape Control Unit when the Tape Drive Unit is ready to perform an operation, when it is performing an operation, and when it has completed an operation. In each of the operational control functions, a complete interlock between all units involved is maintained until the operation is complete.

## MACHINE TIMING

The fundamental machine cycle of the Central Process-

ing Unit (CPU) is 12 microseconds. One cycle is the duration of Core Storage access time which is the time required by the Central Processing Unit to transmit to or receive a word of information from Core Storage. The time required to transmit information between the Core Storage and any of the Input-Output units via one of the Data Synchronizers is given later when the timing relationship of the Input-Output devices in relation to the basic machine cycles are discussed. The fundamental machine cycles may be Instruction (I) cycles, Execution (E) cycles, Execute-Route (E/R) cycles and B cycles, each of 12 microseconds' duration. I cycles are required to make references to Memory to obtain Instructions and to distinguish instruction words from data words. Execution (E) cycles are required for the Central Processing Unit and the Data Synchronizer Unit to make reference to Memory in order to bring data from Core Storage into the units or to enter words into Storage. E/R cycles are required by the CPU for operations *without* references to Memory. B cycles are references to Core Storage by the Data Synchronizer channel and differ from E cycles only in the manner in which they arise and the fact that the Central Processing Unit may not make reference to Core Storage during this time. There are particular cycles where references are made to Core Storage for the Central Processing Unit's purpose, but *Control Word* data is also stored in the Data Synchronizer Channel. Simply stated, the CPU and DSC do have access to memory at the same time for certain instructions during I and E times but, of course, the only time that this is true is when the same information can be used or if it is common to both units.

The timing circuits comprise an Oscillator, FIGURE 114, which oscillates at a frequency of 1 megacycle and provides signals to an Inverted Sync Generator, FIGURE 115. The Inverted Sync Generator provides inverted sync pulses on one output and pulses on another output to the Inverted Clamp Generator and Clock Drive, FIGURE 116, the latter having 2 outputs, an inverted clamp line and a drive line to the Clock, FIGURE 117. The Clock provides the 12 master timing pulses, labelled Master A0 through Master A11 under control of the 1 megacycle oscillator by using a ring of 12 triggers fed by the oscillator in a manner well known in the art. The signals on the Inverted Clamp Line from FIGURE 116 and the Inverted Sync Line, FIGURE 115, are special signals required by the Microsecond Delay and Storage Units in the Storage Register, Accumulator Register and MQ Register. The Inverted Synchronizing pulse on line 115.01 is a positive pulse having a duration of approximately 0.3 of a microsecond and the clamp pulse on line 116.01 is a negative pulse having duration of approximately .02 microsecond. Both pulses are repeated at the megacycle rate of the Oscillator, FIGURE 114, and are in phase with each other which is necessary for proper operation of the Microsecond Delay Units as described hereafter. A Cycle Timer Control, FIGURE 118, utilizes inputs from various command controls and operation controls for providing outputs to a Cycle Timer Gate Generator, FIGURE 119, and to Cycle Timer Output Circuits, FIGURE 120. The Cycle Timer Output Circuits provide outputs 120.01, 120.02 and 120.03 indicative of the type of cycle that the machine is to operate in, that is, whether the cycle shall be an instruction (I) cycle, Execution (E) cycle or Execute-Route (E/R) cycle and one and only one of the outputs indicative of I, E, or E/R time is up at any time. Each output stays up for a minimum duration of one 12 microsecond clock cycle. The Cycle Timer Control, FIGURE 118, provides instruction signals to the Cycle Timer Output Circuits, FIGURE 120, labeled Go to E Time, 118.01, Go to E/R Time 118.03, and Go to I Time 118.14. Other inputs are provided to the Cycle Timer Gate Generator, FIGURE 119, having outputs Reset Cycle Timer 119.01, Set Cycle Timer 119.02, and B Time Control circuits 119.03.

The B Time Control, FIGURE 121, has inputs from the Primary Operation Decoder, Instruction Register and certain other control and timing units for generating outputs concerning B time. A Pulse and Gate Generator, FIGURE 122, generates output signals in response to master timing pulses, type of cycle, and instruction controls.

When the Input-Output units are not being used the Cycle Timer Control follows this sequence: During the last machine cycle pertaining to a previous instruction, a signal is sent to the Cycle Timer Control, FIGURE 118, indicating that the previous operation is complete and that the Central Processing Unit is to proceed to I time for the purpose of interrogating Core Storage for the next instruction according to usual stored program techniques. When this has been accomplished, at Lead-In Instruction time (around 10 time in I time), the new instruction is decoded. Immediately following the decoding of this instruction, its type of instruction is known as well as whether or not another reference to Core Storage is required. For instance, if the instruction is Add this requires another reference to Core Storage to bring in the data to be added. Therefore, the Central Processing Unit is so controlled that its next machine cycle is an E cycle which provides a reference to Core Storage. In case of a store instruction, the same would apply, except that this time the references to Memory would cause information to be moved from a register in the Central Processing Unit to Core Storage. During execution of some instructions, references to Memory may not be required as in the case of multiply, which does not require more than the initial reference to memory to get the multiplicand after which a series of E/R cycles are required in order to actually carry out the iterative addition and shifting by the Central Processing Unit in order to perform the multiplication. Only the initial reference to Storage is required.

In addition to the three basic cycles I, E and E/R there is the B (Buffer) cycle referred to previously which results from the inter-action between a Data Synchronizer Channel and the CPU requiring a reference to Storage. B cycles do not provide data simultaneously to the DSU and CPU but frequently data is sent to a DSC simultaneously with control information being sent to the CPU and vice versa.

#### INSTRUCTION COUNTER

The Instruction Counter, FIGURE 2v, determines the address in Core Storage involved during an Instruction cycle. In the normal progress of the program, sequential addresses in storage are interrogated during successive I times because the Instruction Counter normally receives a pulse at the end of each operation to step it up 1 so that a succeeding higher numbered address is referred to on the next Instruction cycle. The orders of the counter are labelled 3 through 17 in order to agree with the corresponding orders of the Address Register, FIGURE 2i. The loading of the instruction counter occurs at the beginning of each Instruction cycle as will later be described and determines the address of the word comprising the next Instruction *except* in those I times following a Halt, a successful Transfer or Branch and in certain operations such as Skip which advances the Instruction Counter more than one to cause skipping of instructions.

#### INSTRUCTION REGISTER

The Instruction Register, FIGURE 2h, stores and operates on the information normally received from Magnetic Core Storage as a result of an Instruction cycle until the instruction is completely executed when it is reset during the early part of the next instruction cycle prior to receiving a new instruction. At every I8 time of the Instruction cycle, a one microsecond pulse (abbreviated D1) (see FIG. 2h) causes positions S, 1-9 of the Instruction Register to be reset to 0 and at the same time positions 10 through 17, and the Shift Counter of the Indicator Register, are reset to 1. The layout of the In-

struction Register is as follows: Sign in position S, primary operation, positions 1 through 5; secondary operation, positions 6 through 9; and advance or shift counter data, positions 10 through 17. The information read from the Storage Register, FIGURES 2b-d, into the Instruction Register includes the sign, the primary operation part, and the secondary operation part of the Control Word, while positions 10 through 17 of the Instruction Register receive information from the Address Register, FIGURE 2i.

On a type A instruction (those that contain a prefix), bits 1 and 2 of the Storage Register are read into positions 8 and 9 of the Instruction Register. All B type instructions (those that do not contain a prefix) read positions 3 through 11 of the Storage Register into positions 1 through 9 of the Instruction Register. During the Instruction cycle, the sign bit in the Storage Register is transferred into the S position of the Instruction Register, where it has no algebraic significance but is used only to expand the capacity of the register, and, thus make it possible to decode more instructions.

#### PRIMARY OPERATION DECODER

Orders 1-5 of the Instruction Register, FIGURE 13, store the primary operation part of the instruction to be performed. The double outputs of each of these orders are analyzed in the Primary Operation Decoder, FIGURE 14, which resolves the five conjugate pairs of signals into one signal on one of 32 possible decoder output lines. Since only 32 outputs are available from the primary Operation Decoder and 189 computer operations must be provided for, it is necessary to further employ the output of the Primary Operation Decoder by combining it with bits stored in other orders of the Instruction Register to expand the number of instructions over that offered by the Primary Operation Decoder.

#### SECONDARY OPERATION DECODER

A sense type instruction has its primary code stored in the primary operation part of the Instruction Register while the type of Sense is stored in the secondary operation part. For example, in Read Select 0762, the 7 and 6 are represented by bits in orders 1 through 5 of the Instruction Register while the 2 is indicated by a binary bit in column 8. Whenever an instruction with a primary operation code 7, 6 is decoded the secondary operation part of the instruction is sampled into the Secondary Operation Decoder, FIGURE 15, to bring up a secondary operation output of (0, 2). On the non-indexable instruction, columns 8 and 9 of the decoder contain the prefix which was transferred from columns 1 and 2 of the Storage Register. Like the primary part of the Instruction Register, the secondary part is reset at I8(D1) and read at I9 time.

#### ADDRESS PART OF THE INSTRUCTION REGISTER (SHIFT COUNTER)

The 8 positions of the address part, FIGURE 2i, of the Instruction Register form a count-down counter of eight triggers which has a capacity of 255 places. This counter is reset to 1 every I8(D3) and on a Shift Instruction the number of places to be shifted is placed in the Shift Counter by turning OFF the appropriate triggers at I12 time. The shift counter is impulsed every microsecond under a machine cycle gate and as the counter goes to 0, it signals the end of the shifting operation. Similarly, shifting during Multiply, Divide and Floating Point operations are controlled by the Shift Counter.

When using a Sense of an Input-Output Union Instruction, the Address part of the instruction is read into the Shift Counter at I12 time through the address Switch Controls and the output of the Shift Counter during this type of an Instruction are fed to the Class and Unit Select Matrices, FIGURES 149, 150, which in turn feed the Class and Unit Selectors, FIGURES 151-160. It is

pointed out that the Shift Counter is reset with all triggers ON and that zeros are then set into the counter since to set it to its proper setting the counter is of the count-down type and the normal reset and set of the counter would cause an erroneous carry.

#### ADDRESS SWITCHES

The Address Switches, FIGURE 110, sample either the Instruction Counter outputs or Adder outputs of positions 3 through 17. In order to store the Index Register in the decrement portion of the Storage Register or to display the effective address, it is necessary to route the Adder outputs 3 through 17 through the Address Switches to the Storage Bus Switches, FIGURES 2w-y.

#### SIGN MIXING CIRCUITS

The Sign Mixer Circuits, FIGURES 113, combine all outputs from the sign bits of the Storage Register, FIGURES 2b-d, the Accumulator Register, FIGURES 2z-22, and the MQ Register, FIGURES 2dd-gg to provide signals indicating that the signs are alike or unlike, and also provide signals from the Instruction Register, FIGURE 2h, indicating when the Address counter reaches the desired count during a Multiply or Divide operation.

#### SUMMARY OF TIMING CONSIDERATIONS

Every I time the information from Storage is operated on as an Instruction and the location interrogated during the Instruction cycle is selected by the Instruction Counter, FIGURE 2v. When the End Operation Trigger comes on near the end of the last cycle of the previous operation the contents of the Instruction Counter are gated through to the Address Register, FIGURE 2i, at I0(D1) time. The contents of the Address Register at this time indicate the location in Storage that is to be interrogated for a new Instruction. At I2(D1) time, the contents of the Address Register are delivered to the Storage Address Register, FIGURE 2hh (FIGURE 129), of the Core Storage Unit.

When the Storage Address Register has received the address and instruction, it controls the interrogation of the specified location and at I4¾(D½) time places the contents on the Storage Bus I5 to CT 0.5 of next cycle. At I7(D1) the information on the Storage Buses is referred into the Storage Register, FIGURES 2b, c, d. In preparation for the decoding of this Instruction, the Instruction Register is reset at I8 time. If there is a bit in Storage Register positions 1 or 2 then data from positions 1 and 2 are placed in the Instruction Register positions 8 and 9 at I9(D1). However, if no bit is present in Storage Register positions 1 or 2, then the bits in Storage Register orders 3 through 11 are set into the Instruction Register at positions 1 through 9 I9(D1) time. Regardless of the condition of orders 1 and 2, the content of the sign (S) position of the Storage Register is sent into the Instruction Register S position at I9(D1). The instruction code is received by the Instruction Register at I9 time and is decoded by the Primary Operation Decoder, FIGURE 14, from I9.5 until the succeeding I8 time. The output of the Primary Operation decoder prescribes commands for various arithmetic and logical operations and because of the large number of types of Instructions and the limited capacity of the Primary Operation Decoder, it is necessary to use also outputs 6 through 9 of Instruction Registers along with the outputs of the Primary Operation Decoder for decoding purposes.

The number stored in the Instruction Counter, FIGURE 2v, is advanced by 1 at I11(D1) to effect the interrogation of the next sequential Core Storage address during the succeeding I cycle. This is the normal advance and the advance is only suppressed in special cases as stated above. By this time the program circuits have caused the decoding of the Instruction which controls the types of cycles to follow I time and the Instruction Counter is set for the next sequential address.

When the instruction has been completed, a command line End of Operation control, FIGURE 128, is brought up to turn ON the End Operations Trigger, FIGURE 118, at 10 times of the last cycle of the operation which signals the Cycle Timer to proceed to I time and bring out the next instruction.

#### OVERFLOW AND CARRY TRIGGERS AND CONTROLS

In FIGURE 123 there is shown two triggers, one for storing the fact that an Overflow has occurred and the other for storing the fact that a Carry out of column Q of the Adder has occurred. A pair of triggers are used in FIGURE 124, one for indicating the presence or absence of a carry into position 9 of Adder and another trigger for indicating the carry out of column 9. In FIGURE 125, there is shown a pair of triggers, one for indicating Floating Point Overflow and the other for indicating Floating Point Underflow. There is shown a trigger in FIGURE 126 which has an input from a predetermined Adder depending upon the size of Core Storage that is used in the system. In this instance, there is a Carry output from Adder 6 to this trigger. Although Locate Drum Address, LDA, is not used in the explanation of this embodiment of this invention and is not explained in detail, the fact that Locate Drum Address is not used is pertinent to the extent that the associated controls are down.

In connection with Floating Point Overflow and Underflow detection circuits of FIGURE 127 provide outputs indicative of Floating Point Overflow and Minus on Adder Q sum. In FIGURES 128a, b and c, there is shown the control circuits for End Operation, Storage End Operation in E R time and End Operation in E time.

#### WORD FORMAT

FIGURE 3a shows the layout of a type A instruction. These instructions use positions S, "1," and "2" for an operation code and are characterized by having a "1" in positions 1 and/or 2. All other instructions contain zeros in both positions "1" and "2." Instructions Transfer on Index TIX, Transfer on No Index TNX, Transfer on Index High TXH, Transfer with Index Incremented TXI, and Transfer on Index Low or Equal TXL use positions 3 through 17 as a decrement part, positions 18 through 20 as an index tag, and bits 21 through 35 as an address part. The index tag selects the Index Register, FIGURES 2f and g, as the one whose contents are to be modified and tested by the instruction. The decrement contains the modifications or test amount and the address specifies the storage location of the next instruction if the test condition is met. Another of these instructions uses only S, 1 and 2 and bits 3 through 35 have no effect on the execution of the instruction.

The format of a type B instruction is shown in FIGURE 3b, the shaded part representing the field not used by all type B instructions. These instructions are characterized by having an operation part in S, 1 through 11 (1 and 2 contains 0's), an index tag in 18 through 20 and an address part in 21 through 35 for Shift Instructions. Positions 12 and 13 are used as an indirect address tag by all type B Instructions except non-indexable, shift, input-output, variable multiple and variable divide instructions. Positions 14 and 15 are not used by type B instructions.

FIGURE 3c shows the format of the type C instructions. Type C instructions use S, 1 through 9, as an operation part (1 and 2 contains 0's), 10 through 17 as a count, 18 through 20 as an index tag and 21 through 35 as an address part. Three of these instructions, Variable Length Multiply (VLM), Variable Length Divide or Halt (VDH) and Variable Length Divide or Proceed (VDP) are indexable and use the index tag for address modification. Convert by Replacement from Accumula-

tor, (CVR), Convert by Replacement from MQ, (CRQ) and Convert by Addition from MQ, (CAQ) are not indexable and use position 20 of the index tag to indicate that the base address of a count cycle is to replace the contents of index register A. The number of convert cycles, the number of bits in the multiplier, or the number of bits to develop in the quotient is specified by the count. While the count field has a capacity of 255, a count larger than 47 may cause indirect addressing to take effect on VLM, VDH, VDP but not on Convert Instructions since such a count places bits in positions 12 and 13. Bits through 21 and 35 specify the storage location of the operand or the base address of the first convert cycle.

FIGURE 3d shows the format of type D instruction. Type D instructions operate in conjunction with columns 0 through 17 or 18 through 35 of the Indicator Register, FIGURE 2a. The 18 bit mask used in Sense Indicator instructions is contained in the positions 18 through 35 of the instruction. Positions S, 1 through 11 contain the operation part with 1 and 2 containing zeros. Position S is used to denote whether the Columns left (0 through 17) or columns right (18 through 35) positions of the Indicator Register are used in the instruction. If S contains a "1," the left positions are used, and if S contains a "0," the right positions are used.

In FIGURE 3e, the format of type E instructions is shown. These are defined by plus or minus 0760 in positions S, 1 through 11, do not contain an address part, and use positions 24 through 35 as part of the operation code. Address modification through an index register is specified by positions 18 through 20, is not prohibited but may cause the operation to be changed.

Data Synchronizer operation makes use of three word formats as shown in FIGURES 3f and 3g and 3h. Word formats of FIGURES 3f and 3g illustrate an instruction word (Control Word) sent to DSC from storage and FIGURE 3h illustrates a word sent from a DSC to storage. The normal DSC control word specifies the number of words to be transmitted (Word Count) in positions 3 through 17 and specifies the initial storage location in positions 21 through 35 to which data is to be sent or taken from. DSC control is specified by positions S, 1, 2 and 19 and the use of these positions for DSC control are described in detail hereafter. The special DSC control word in FIGURE 3g is a word which modifies the sequential location of other control words for the Data Synchronizer as described later. Positions S and 1 contain 0's, position 2 must contain a 1 and position 19 contains a zero. Positions 21 through 35 give the location of the next control word to be used by the DSC.

FIGURE 3h shows the format of an instruction word when a store DSC instruction is executed. The storage location from which the next control word is taken is specified in positions 3 through 17 (location). The storage address of the next word of data is specified in positions 21 through 35 (Address).

FIGURE 3i illustrates the layout of a Floating Point instruction. The magnitude of the binary fraction is given by positions 9 through 35 and the sign of the binary fraction is given in position S. The binary characteristic of the fraction (binary exponent +128) is stored in positions 1 through 8.

In FIGURE 3j, a Fixed Point instruction is illustrated. In fixed-point arithmetic, the 36 bit word in storage is interpreted as containing a sign in S and a 35 bit magnitude in positions 1 through 35. In logical operations, the word is treated as a 36 bit unsigned quantity.

In FIGURE 3k, a six character binary coded data (BCD) word format is indicated. It will be discussed in some detail later.

The Central Processing Unit distinguishes between instructions and data information by the type of cycle selected. Words read out of memory during an instruction cycle are channeled to the Instruction Register where

the stored manifestations of the bits comprise a representation of the instruction. Information read from memory during an execute cycle is always handled as numeric data.

### AUTOMATIC ADDRESS MODIFICATION

When an iterative program operates on different items of data during each step of the iteration, it is necessary to change the addresses of instructions which further refer to this data before each iteration. Without the use of automatic address modification, instructions which change the addresses of other instructions may constitute a large number of instructions in a given program. When the address of the instruction is brought to the Storage Address Register, it passes first through the Adders and Address Switches. If indexing (address modification) is desired the 2's complement of the amount in one of a chosen of the Index Registers is brought into the Adders at the same time in positions 3-17. The results of this address operation is that the Address Switches receive the difference between the address and the contents of the selected Index Register and this difference is known as effective address. The execution of the instruction proceeds in the usual manner using the effective address. Each index register serves as an accumulator register so that its contents can be increased and decreased by the execution of certain indexing instructions. The Index Register can receive information from either the decrement portion or the address portion of the instructions, from the Accumulator or from the Instruction Counter and it can send information to Adders for address modification, to the Accumulator or to Storage. Selection of an Index Register is made by bits in Storage Register locations 18, 19 and 20. Further address modifications may be had by providing bits in positions 12 and 13 in the Storage Register. By means of controls, FIGURE 98, the contents of the Storage location referred to are not added, but instead the address found at this Storage location specifies the location from which data are to be added to the Accumulator. Both of these addresses may be indexed by the same or different Index Registers, each word containing its own tag in positions 18, 19 and 20. Indirect addressing may be used with all indexable transfer instructions and with all other indexable instructions which make a reference to storage.

### MAGNETIC CORE STORAGE ORGANIZATION

Referring now, in general, to FIGURES 2hh through 11 and specifically to FIGURES 129 through 147, the Data Processing System employs a three dimensional Magnetic Core Storage Device and associated storage controls. Outputs from the Address Register, FIGURE 2i, and DSU Address Switches, FIGURE 2ww, are provided as inputs to a Storage Address Register shown in FIGURE 2hh, the specific logical contents of which are shown in FIGURE 129. Certain timing pulses are provided to a Pulse Generator shown generally in FIGURE 2jj and specifically in FIGURES 130a, b and c which provides output signals to the Memory Address Register, FIGURE 2hh. The Memory Address Register provides outputs to an X Address Decoder, FIGURES 131a and 132b, and to Y Address Decoder, FIGURES 132a and 131b. Both the X and Y Address Decoders have outputs to respective ones of a pair of Read Bias and Write Gate Mixing Circuits, FIGURE 133. Timing pulses are provided from a Read-Write Gate generator, FIGURES 134a and b, to the Gate Mixing Circuits; to the X and Y Address Decoders, FIGURES 131a and 132b and 132a and 131b, respectively; and to the Read Bias and Write Gate Mixing controls, FIGURE 133. Output lines 133.01 and 133.02 are provided from Read Bias and Write Gate Mixing circuits to the inputs of an X Matrix Switch Write Driver, FIGURE 135. Outputs 131A.01-08 are provided

from the X Address Decoder to an X Matrix Smith Read Driver, FIGURE 136, and outputs 131b.0-08 are provided from FIG. 131b to Read Bias and Write Gate Mixing Circuits, FIGURE 133. Connections are made according to FIGURE 135 between Gate Mixing, FIGURE 133, and an X Driver Matrix Switch, FIGURE 141a. The 64 output lines of this X Driver Matrix Switch are provided as inputs to the Core Array, FIGURE 138a, each output drives one of 64 X drive lines in the array as indicated in FIGURE 138a when that driver line has been addressed. Outputs are provided from a Read Bias and Write Gate Mixing, FIGURE 133, to the Y Matrix Switch Write Driver, FIGURE 139, and outputs are provided from the Y Address Decoder to the Y Matrix Switch Read Driver, FIGURE 140. Connections are made according to FIGURE 133 between the Address Decoder, FIGURE 131a, and an Y Matrix Switch, FIGURE 139. Outputs 132A.01-08 are provided as inputs to the Y Matrix Switch Read Driver, FIGURE 140, and connections are made according to FIGURE 140 to the Y Driver Matrix Switch, FIGURE 137a. Sixty-four Y Drive lines of Y Matrix Driver Switch, FIGURE 137a, are provided to the Core Array, FIGURE 138. Thirty-six digit windings shown in FIGURE 138 are provided to inhibit the writing of a "1" in a selected core as will be described in detail later.

Communications with Core Storage from either the Central Processing Unit or Input-Output devices are made through a Sense Amplifier Buffer and Input-Output Switching Register, FIGURES 2-11 (FIGURE 142). Outputs 142A.03; 142A.04; 142A.05; 142B.03; 142B.04; 142C.03 and provided to Storage Bus Switching, FIGURES 2w-y (FIGURES 11b, c, d) and 36 output lines 142.01 are provided as inputs to a Digit Plane Select Circuits FIGURE 143. Thirty-six outputs of the Digit Plane Select Circuits are provided to a Digit Plane Driver Unit, FIGURE 144; the latter having 36 digit plane drive outputs which are connected to the Core Array, FIGURE 138, as previously described. With the energization of a selected X and Y line, outputs from cores at the selected address are present at the Sense windings of the Core Array to the input of the Sense Amplifier Buffer and I/O Switching, FIGURE 142. Control lines are provided to the Sense Amplifier Buffer and I/O Switching, FIGURE 142, by way of an Address and Operations Control, FIGURE 145 and, in turn, by way of Read-Write Control, FIGURE 146. (Adders and operations control are part of CPU.) (Inputs to the Adders and Operations Control are from the Central Processing Unit and are shown specifically in FIGURE 145.) Inputs are provided to the Test Circuits shown generally as FIGURES 147a, b and c from the Sense Amplifier Buffer and I/O Switching Register and from the Pulse Generator, FIGURES 130a and b. An understanding of the Test Circuits is not necessary for an understanding of the invention. Accordingly, no specific details are mentioned except in those instances where a control line is operated as an incident to the operation of Core Storage.

In FIGURE 138, there is shown a diagrammatical view of a Core Array in which cores are arranged in square arrays such that each core is situated at the junction of two mutually perpendicular single turn windings that are called the X and Y windings. If I is the minimum current necessary to change a core from the "zero" state to the "one" state then if current

$$\frac{I}{2}$$

is supplied to the single X and a single Y winding, the only core which can change state is the one at the intersection of these two windings. Four windings actually pass through each core and are called the X, Y Digit and Sense Windings as shown in FIGURE 138b. The planes are stacked vertically to form a three dimensional array of 36 planes, each X or Y winding being connected in series with

the corresponding X or Y winding in the planes above or below it. Currents of

$$\frac{I}{2}$$

are applied to one X and one Y winding and a vertical line of cores is selected at the intersection of the planes at which the X and Y windings lie. The Digit and Sense windings, however, are not connected between the various planes. The process of reading information from the selected vertical line of cores leaves that line of cores of 36 positions in "zero" state and, therefore, to prevent the loss of the information read out it becomes necessary to write "ones" in those cores which has previously contained "ones." This process is accomplished producing magnetizing currents for writing "ones" in the entire line of cores, but whenever a "zero" should appear, an inhibit signal is returned to the plane associated with that digit from the digit winding to cancel a portion of the magnetizing effect which suppresses the writing of a one in that plane. More specifically, during the Write cycle the Core Plane Address to be written first receives a Read pulse which changes the full address of 36 positions to zero. The Sense winding output is suppressed at the output of the Sense Amplifier which prevents setting the Storage Buffer triggers to the contents of the Address which has been read from. At Write time the Read in sample together with the Storage Bus outputs either turns on the Buffer Triggers for those outputs containing a "one" or leaves it off as in the case of reading a "zero." After the Buffer Triggers have been set, the Write current is sent to all 36 cores of the Address to be written tending to cause all "ones" to be read into that Address. Where "zero" is to be written into a particular core the writing of the "one" is suppressed by the Storage Buffer Lines 142a.01S through 142a.01.11; 142b.01.12; 142b.01.23; 142c.01.24; 142c.01.35 which go to the Digit Plane Select circuits of FIGURE 143 to bring up the Digit Plane Select lines 143.01S through 143.01.35 to inhibit "ones" from being written into respective planes associated with each Digit Plane Select winding. Since a Write operation is always preceded immediately by a Read operation during any selection of a Memory Address, the selected core is always in a "zero" state when writing starts. To write a "zero" into a core the X and Y windings are each pulsed simultaneously with current of

$$+\frac{I}{2}$$

and the Digit Plane winding receives an inhibit pulse of

$$-\frac{I}{2}$$

which results in a net of

$$+\frac{I}{2}$$

to the core which is insufficient to switch the core from "zero" to the "one" state.

#### READ AND WRITE OPERATION

A Store Instruction is one that writes the contents or partial contents of a Central Processing Unit Register at an address in Core Storage specified by the Store Instruction. This is commonly referred to as Writing. Other instructions cause the contents of some Addresses in Core Storage to read out and sent to the CPU for the purpose of adding, subtracting and so forth, depending upon the instruction, and this is referred to as Reading. For example, the instruction Store +0601 with an Address of 0700 (octal) is assumed to be located at Address 0777 (octal) in Core Storage. The Instruction Counter in the Central Processing Unit, FIGURE 2v, normally tells the machine where to go in Core Storage during an Instruction cycle and get the next instruction and in this example, con-

tains the Address 0777 (octal) in the positions indicated below:

| Instruction Counter |          | Positions |   |   |   |   |   |   |    |    |    |    |    |    |    |    |   |
|---------------------|----------|-----------|---|---|---|---|---|---|----|----|----|----|----|----|----|----|---|
| 5                   | Contents | 3         | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |   |
|                     |          | 0         | 0 | 0 | 0 | 0 | 0 | 1 | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 |

Until 16 time the output of the Instruction Counter feeds the Address Register, FIGURE 2i, in the Central Processing Unit and the contents thereof are transferred into the Address Register at 10(D1) time. At 12 time, the contents of the Address Register positions (FIGURE 2i) 6 through 17 or the contents of the DSU location Register are transferred to the Storage Address Register, FIGURE 2hh, located in Magnetic Core Storage. Each position of the Storage Address Register, FIGURE 129, has three outputs, making the total of thirty-six and is divided into four major divisions as shown schematically in FIGURE 148a: the group of bit positions 6, 7 and 8 is the Thousands position; 9, 10 and 11 comprise the Hundreds; the group of bit positions 12, 13 and 14 comprise the Tens; and the group of bit positions 15, 16 and 17 comprise the Units. Each of these four groups has six outputs 129a.01-129a.12 and 129b.01-129b.12, labeled 6, 7, 8 and so forth. The Address Decoder, FIGURE 132b, decodes positions 6, 7, and 8; Address Decoder, FIGURE 131a, decodes positions 9, 10 and 11; Address Decoder, FIGURE 131b, decodes positions 12, 13 and 14; and Address Decoder, FIGURE 132a, decodes positions 15, 16 and 17. The address contained in the Storage Address Register and placed in the Address Decoders is 0777 (octal) and accordingly, in FIGURE 132a, Storage Address 15 line 129b.08 is up; Storage Address Register 16 line 129b.10 is up; Storage Address Register 17 line 129b.12 is up; Storage Address Register 15 line 129b.07 is down; Storage Address Register 16 line 129.09 is down; Storage Address Register 17 line 129b.11 is down; and when the Read Gate line 134a.02 comes up, Read Address 7 line 132a.01 is up since all inputs to its AND circuit are up. In FIGURE 131b, Storage Address Register 12 line 129b.02 is up; Storage Address Register 13 line 129b.02 is up; Storage Address Register 14 line 129b.04 is up; Storage Address Register 12 line 129b.01 is down; Storage Address Register 13 line 129b.03 is down; Storage Address Register 14 line 120b.05 is down. Address 70 line 131b.01 is up since all the inputs are up to its AND circuit. In FIGURE 131a, Storage Address Register 9 line 129a.07 is down; Storage Address Register 9 line 129a.08 is up; Storage Address Register 10 line 129a.09 is down; Storage Address Register 10 line 129a.10 is up; Storage Address Register 11 line 129a.11 is down; and Storage Address Register 11 line 129a.12 is up. When the Read Gate line 134a.03 comes up, an output is provided on Read Address 700 line 131a.01, since all the inputs to its AND circuit are up. In FIGURE 132b, the Storage Address Register 6 line 129a.02 is down; the Storage Address Register 7 line 129a.04 is down; the Storage Address Register 8 line 129a.06 is down; Storage Address Register 6 line 129a.01 is up; Storage Address Register 7 line 129a.03 is up; Storage Address Register 8 line 129a.05 is up. Accordingly, an output is provided on Address 000 line 132b.08 since all of the inputs to its AND circuit are up. The outputs from the Tens and Thousands Decoders, FIGURES 131b and 132b, respectively, are available as soon as the Storage Address Register is read into at 12(D1). However, the Units and Hundreds Decoders await a Read Gate pulse on lines 134a.02 and 134a.03 from the Read and Write Gate Generator before their outputs are up. This allows time to set up the biasing of the Switch Cores before the Selected Switch Cores are actually transferred. The outputs 131b.01 and 132b.08 for the Tens and Thousands Address Decoders are sent to Read Bias and Write Gate Mixing circuits, FIGURE 133, and here their outputs are logically inverted for providing from each of these circuits seven lines which are up and one which is down. The seven

lines that are up from the Read Bias and Write Gate Mixing circuits for the Thousands Address Decoder are sent to the X Switch Core Matrix, FIGURE 135, and the seven lines which are up from the Mixing circuits from the Tens Decoder are sent to the Y Switch Core Matrix, FIGURE 139. As shown in Timing Chart, FIGURE 148b, both Switch Core Matrices are biased and a Read Gate Line comes up at approximately 13.5 time which allows the Units and Hundreds Address Decoders, FIGURES 132a and 131a, to select the correct Switch Core in both the X and Y Matrix.

With reference to FIGURE 138, the Read-Out of a 36 bit word from the 36 sense windings to the Buffer Register, FIGURE 142, is accomplished by the use of Switch Cores shown in FIGURES 137 and 141. Since each of the 36 Core Planes in the Core Storage Unit is a 64 x 64 Array the Two Switch Core Matrix Panels are used to provide 64 X Drive lines and 64 Y Drive lines as shown in FIGURE 138, at the top of the figure. FIGURE 137a shows an 8 x 8 Switch Core Matrix having 64 Y Drive Address lines which go to the Core Array shown in FIGURE 138. The cores shown diagrammatically in FIGURE 137a are each identified by an Address shown thereon and are illustrated in detail in FIGURE 137b. The Switching Cores have a substantially rectangular hysteresis loop with a Read winding having terminals identified by the numbers 1 and 9, a Write winding having terminals identified as 4 and 6 and a Secondary winding having terminals 7 and 8 with the polarities as indicated by the dots shown in the figure. When the Write winding is energized, the switch core remains magnetized in the state representative of "zero"; and when current is provided to the Read winding, the switch core is magnetized in the opposite sense indicative of a "one." A switch core is said to switch when current is provided in the Reading winding sufficient to cause a residual magnetism to change from "zero" to "one." Likewise, sufficient current in the Write winding switches the core from "one" to "zero." A magnetizing force applied through the Write winding has very little effect on the core already magnetized in that direction and a magnetizing force applied to the Read winding has little effect on a core already magnetized in that direction. The Write winding provides the biasing force which, when used simultaneously with a magnetizing force applied on the Read winding, prevents the core from switching due to cancellation of the flux.

The line pairs coming from the Y Matrix Switch Read, FIGURE 140, are related to the Units position, of the Address as previously mentioned, FIGURE 148a, so that the lines associated with the Units position Address are up and the other seven pairs of lines associated with the Non-Selected Units Address are down. For example, the Read Address 7 line 132a.01 is up providing an input to the Matrix Switch Read Amplifier of FIGURE 140 bringing up the Read Driver input line to the Matrix Switch Driver, which provides current through the line 140.01. In FIGURE 137a, the Matrix Switch Read Driver Address (7) line 140.01 is up which provides current through the series Read coils of the Switch Cores terminals 1 and 9 of Address Cores 77, 67 and so forth through terminals 1 and 9 of Address (07) Switch Core and from the 9 terminal back to the Read Address 7 Feedback line 140.02. The Read Address Feedback line is returned to the Y Matrix Switch Read Driver of FIGURE 140. In this regard, it is pointed out that current flows from a negative D.C. potential at the cathode to plate of the Matrix Switch Driver through the Read windings in series and through the Feedback line to the cathode of the Matrix Switch Read Amplifier and to ground through the lines 140.03, shown in FIGURE 140. Since the cathode of the Matrix Switch Driver is at a negative potential of 130 volts essentially positive B+ is provided to the Matrix Switch Driver. Thus, the Read windings of the Switching Cores Address 77, 67, 57, 47, 37, and 27, 17 and 7 are carrying magnetizing current sufficient to cause a residual

magnetism to change the state of from "zero" to "one."

Referring now to FIGURE 131b, the Tens Address Decoder, Address line 131b.01 for Address 70 is up to the Write Driver Select circuits, FIGURE 133, but the Write Gate line 134b.03 is not up until about 19 time. However, the Address 70 line is up and inverted to an AND circuit at the more negative level. Even though the Read Bias Gate line 134a.01 is up there is no output from the AND circuit since the inverted Address 70 line is down.

With reference to the Address Decoder, FIGURE 131b, it will be noted that although the 131b.01 line is up that the other seven lines 131b.02 through 131b.08 are down. Accordingly, in the Write Driver Select circuits of FIGURE 133, the output of the Write Driver Select circuits for the Address 70 is down, but the outputs of the Write Driver Select circuits for the Addresses 60, 50, 40, 30, 20, 10 and 0 are down. Therefore, with reference again to FIGURE 133, the Address lines 131b.02-08 being down provides outputs which are up from the inverters and the Read Bias Gate line 134a.01 is up at I2 near the beginning of the cycle providing outputs on lines 133.01 and 133.02 for Matrix Switch Write Driver lines for the Addresses 60, 50, 40, 30, 20, 10 and 0 as shown in FIGURE 137a. In FIGURE 137a, it will be noted that the Matrix Switch Write Driver Address line 70 is connected to the 4 terminal of the Address 77 core and that the 4 and the 6 terminals are those terminals for the Write coils which are connected in series from the Address 77 core through the Address 70 core. The 6 terminal of the last mentioned core is connected to the Write Address 70 Feedback line as shown. As previously mentioned, the Matrix Switch Write Driver Address 70 line is down and accordingly, current is not provided to the Write coils of the series-connected Switching Coils of Addresses 77-70. However, current is supplied to the Write coils of the other rows of Address Switching cores by way of the Matrix Switch Write Drive Address 60, 50, 40, 30, 20, 10 and 0 lines as mentioned previously with regard to the Write Driver Select circuits of FIGURE 133. In summation, the Address Switching cores 77, 67, 57, 47, 37, 27, 17 and 07 have their Read coils energized; the Switching Cores Address 67, 57, 47, 37, 27, 17 and 07 also have their Write coils energized; the net effect on the last mentioned cores is that they are not switched, but the Address Core 77 is switched since it has only read current supplied. The switching Cores 66-60; 56-50; 46-40; 36-30; 26-20; 16-10; and 6-0 receive current through their Write Coils which tends to switch the core from a "one" to a "zero." However, since the last mentioned cores are already at the state the magnetizing force is ineffective to change that state. The Switching Core Addresses 76, 75, 74, 73, 72, 71 and 70 have neither the Read nor the Write coils energized so that no change of state takes place. The Switch Core Address 77 has only the Read coil energized as previously described and is switched from "zero" to "one." This change of state from a "zero" to a "one" in effect induces a voltage in the secondary winding which is felt on the Y Drive Address 7 line which goes to Core Plane, FIGURE 138, and provides

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Similarly, the Hundreds Address is decoded, FIGURE 131a, and provides an input on line 131a.01 to the X Matrix Switch Read Driver, FIGURE 136, to bring up the Read Address 700 Matrix Driver. The Thousands Address Decoder of FIGURE 132b inverts the Selected output 132b.08 in FIGURE 133 to provide one pair of output lines associated with the Address 0000 which is down and seven pairs associated with Addresses 7000-1000 which are up to the X Matrix Switch Core panel, FIGURE 141. Specifically, Matrix Switch Write Driver Addresses 7000, 6000, 5000, 4000, 3000, 2000 and 1000 are up whereas the Matrix Switch Write Driver Address 0

is down and the Switch Core Address 0700 is the only core which can change from the "zero" to the "one" state. This change is felt on the X Drive Address 0700 line which provides

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to the Selected X Drive line. Thirty-six cores are acted upon since each X or Y winding is connected in series with the corresponding X or Y windings in the planes above or below it. A sense winding is threaded through all the cores in each plane so that in FIGURE 138 there are two terminals for the Sense winding for each plane and there are two terminals provided to the Sense Amplifier Buffer Register, FIGURES 142a, b and c. More specifically, two terminals from each of the thirty-six planes are applied to the input of the primary of the transformer, as shown in FIGURE 62, U.S. patent application Serial Number 592,545, filed July 6, 1956, title: Data Coordinator. For each plane having a "1" an output is provided from the Sense Amplifier to the AND circuit having two other inputs Read Control 146.03 and Read-Out Sample 130a.07. For a "1," an output is provided through the OR circuit and Cathode Follower to turn on the Buffer Register Trigger. When a "0" is being read, there is no output from the Sense Amplifier and accordingly, the trigger remains in a state indicative of a "zero." Since the Read-out is destructive and the location (0777) specified by the Address now contains "zero," it is required that the word written out into the Buffer Register be read back into the Address specified (0777).

It will now be described how "ones" are written in those cores of Address 0777 which had previously contained "ones" and which are now contained in the Storage Buffer Register, FIGURE 211 (FIGURES 142a, b, c). This operation is accomplished by setting up circuits for writing "ones" in the entire line of cores, but in those positions in which a "zero" should appear, an inhibit signal is returned to those planes associated with the "zero" digits by way of the individually associated Digit Plane windings, which causes suppression of the writing of "ones" in those planes. The timing of the Inhibit Gate is shown in the Timing Chart, FIGURE 148b. After the Read-Out Operation, the X and Y Switching Cores corresponding to the Address from which the information was read are in the "one" state. That is, they have been switched to provide an output in the Secondary which drives the cores in the Selected vertical line, FIGURE 138, from the "one" to the "zero" state to provide an output from the Sense windings indicative of the values contained in the selected thirty-six cores. To write the information contained in the Buffer Register back into the Core Array, advantage is taken of the fact that the Switch Cores for the Address Read-Out are now in the "one" state. During Write time all inputs to the Read Windings, FIGURES 136 and 140, of the Switch Core Matrices (FIGURES 137 and 141) are suppressed by a Read Gate lines 134a.02 and 134a.03 (FIGURES 132a and 131a). This is to say that the Read Gate provided on the line 134a.02 to the Address Decoder circuit in FIGURE 132a and the Read Gate provided on the line 134a.03 to the Address Decoder circuit in FIGURE 131a are down. Accordingly, there will be no output from either the Address Decoder, FIGURE 131a, or the Address Decoder, FIGURE 132a. The outputs of the Thousands Address Decoder, FIGURE 132b, and the Tens Address Decoder, FIGURE 131b, are not inverted. With reference to FIGURE 133, for example, the Read Bias Gate on line 134a.01 is down which prohibits the passage of the inverted output from the Address line, but the Write Gate on the lines 134b.03 is up which brings up the selected one of the Read Bias or Write Address lines which output is provided to the X Matrix Switch Write

Driver Address (0000) lines of FIGURES 135 and 141. Similarly, the output of the Tens Address Decoder, FIGURE 131b, is passed through Read Bias and Write Gate Mixing, FIGURE 133, and is provided as an input to the Y Matrix Switch Write Driver Address (70) line of FIGURES 139a and 137a. With reference now to the Y Driver Matrix Switch, FIGURE 137a, it will be noted that the inputs from Y Matrix Switch Read Driver, FIGURE 140, are all down and that the only input to the Y Driver Matrix Switch is on the Matrix Switch Write Driver Address 70 from FIGURE 139. Recalling now that the Address (77) Switch Core was the only one which was changed from the "zero" to the "one" state, it is apparent that the application of current to the Write coil causes the Address Switch core 77 to switch from the "one" to the "zero" state. However, other Switch cores are not affected in this manner since they are already in the "zero" state and the magnetizing force applied is therefore ineffectual to cause a significant voltage in the Sense Output winding or Secondary Output winding. These, of course, are the cores having Addresses 76, 75, 74, 73, 72, 71 and 70. Accordingly, an output is provided on the Y Drive Address 77 line of FIGURE 137a to FIGURE 138. Similarly, with reference to the X Driver Matrix Switch, FIGURE 141a, the inputs from the X Matrix Switch Read Driver, FIGURE 136, are down and the only input from X Matrix Switch Write Driver, FIGURE 135, is provided on the Matrix Switch Write Driver Address (0000). It is pointed out that this provides the Write current to the Write coil of Switching Core Address 0700 which is the only core in the X Driver Matrix Switch Array which has been changed from the status of "zero" to "one." Therefore, this core when provided with a Write current in the absence of the Read current switches from "one" to "zero" and the voltage induced in the Secondary winding is provided on the X Drive Address line 0700 to the Core Array of FIGURE 138. Since a current of

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is provided to a selected one of the Y Drive lines and a current of

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is provided to selected one of the X Drive lines shown in FIGURE 138 each of the thirty-six cores in the vertical line selected would normally be switched from the "zero" to the "one" state. However, through the use of the thirty-six digit plane windings, selected ones of the cores which were normally in the "zero" state prior to reading out will be preserved in the "zero" state in the following manner:

With reference to the Sense Amplifier Buffer Register and I/O Switching, FIGURES 142a, b and c, it will be noted that there is provided a line 142a.01, 142b.01 and 142c.01 which is Storage Bus Trigger (N) Off. Accordingly, when each Trigger in the Buffer Register is in the OFF condition as indicated by conduction of the right-hand side of the Trigger, the left-hand side is OFF with the plate at its higher positive potential which is interpreted on the output lines Storage Buffer Trigger (N) OFF as the "OFF" condition, and these outputs are provided from the Buffer Register to the Digit Plane Selector circuits, FIGURE 143. The inhibit Gate comes up at 18.5 and for each of the thirty-six positions containing a "zero" in the Buffer Register an output is provided from the Digit Plane Select circuit on selected ones of the lines 143.01.S through 043.01.35. The outputs are provided to the Digit Plane Driver in the manner shown in FIGURE 144 for driving the Digit Plane windings shown in FIGURE 138 for those of the thirty-six positions containing "zeros." The current provided to the Digit windings is sufficient to

cancel the total effect of the current provided to the Y and X Drive lines since

$$\frac{I}{2}$$

is provided to each of the X and Y Drive lines (which is the current required to switch the core) and the current provided to the Digit Plane winding is sufficient to overcome at least a portion of this current thereby prohibiting the switching of the core from the "zero" to the "one" state on Writing operation. When a word is to be written into Core Storage in response to a Store instruction, the operation proceeds almost as previously described with respect to a Read instruction. However, before a Write pulse can be generated from the Switch Cores, the Switch Cores associated with the selected address must be placed in a Write status and this can be done by causing the proper Switch Cores to first provide a Read current. Therefore, for a Write cycle the Core Plane Address to be written first receives a Read pulse which causes the contents at the Address specified to be all "zeros" in all 36 positions. Output signals will be present on those Sense Windings having a core change from the "one" to the "zero" state but these are suppressed at the output of the Sense Amplifier since the Read-Out Sample line 130a.07 is down. At this time the selected Switching Cores of the X Matrix Switch and the Y Matrix Switch have been switched from the "zero" to the "one" for providing outputs to the Selected vertical line of cores causing them to change from a "one" to a "zero." Information is present on the lines 142a.02, 142b.02 and 142c.02 from the Storage Bus or in the alternate is present on the DSU Storage Bus 142a.06, 142b.05, 142c.04. When the Read-In Sample signal is provided on the line 130a.05 together with the Write Control signal on 164.02 the trigger is turned ON for those positions having "ones" present at the inputs (that is, having the input lines up).

After the Buffer trigger has been set, the Write current is sent to all thirty-six cores of the Address to be written which causes all "ones" to attempt to read into that Address. Where "zero" is to be written into a particular core the writing of a "one" is suppressed by the Storage Buffer Trigger OFF line 142a.01, 142b.01 or 142c.01 in the manner previously described. The Buffer Register triggers are reset by way of the lines 130b.01, Reset Storage Address Register and Buffer Register between 0.5 and 1.0 time.

### COMPONENT CIRCUITS

A detailed description of the principles of operation of a Magnetic Core Storage device may be had in U.S. patent application, Serial Number 592,545, filed July 6, 1956, and referred to previously. A detailed description of a Central Processing Unit of the parallel binary type is described in Computer for 701, copending application Serial No. 419,642, Philip E. Fox, filed March 30, 1954, and includes basic instructions and typical circuits for causing their performance. Especially applicable are FIGURES 1b, 1d, 1f and 1g, which correspond generally to devices employed in the present invention. Other operations, particularly those utilizing Input-Output units such as magnetic tapes are disclosed in the copending application, Serial No. 401,648, Bartelt et al., filed December 31, 1953, and in the copending application, Serial No. 401,502, of Bartelt et al., filed December 31, 1953. Further description may be had with reference to similar arithmetic elements in "IBM" Type 701 Computer, by H. D. Ross, Proceedings of the I.R.E., vol. 41, pages 1287-1294, October 1953.

The Storage Register, Accumulator Register, and Multiplier Quotient Register are composed of microsecond delay units which are storage units having the particular capacity of being able to accept information and transmit information at the same time. These units are described in detail in U.S. Patent Re. 23,699. The Adder

and True Complement controls comprise thirty-five full Adders and two half Adders of the type explained in detail with reference to FIGURES 7b and 7c of application, Serial Number 419,642 referred to previously. The True Complement controls are those circuits that control the input to the Adders and consist of switching circuits and inverters. The switches control the time of entry of a word into the Adder and also determine whether the digits pass through the Inverter or not. Thus, a word entered into the Adders may be either true or complement. The Indicator register is composed of triggers of the bistable multivibrator type which remain in one or the other of two stable states until forced by external signals to assume the other state. The trigger is said to be ON when its left side is conducting, and therefore its left side is called the "ON side" and the right side is the "OFF Side." In this instance, a trigger is said to be storing a "1" when ON and a "0" when OFF. In this embodiment of the invention, circuits are arranged to operate at voltage levels at a -30 volts and a +10 volts. When a line is referred to as being in the Down condition, it is to be assumed that the line is at a -30 volts, and conversely when a line is said to be in the UP condition it is to be assumed that the line is at a +10 volts potential.

Circuits employed in the practice of this invention have been designed to function in a one microsecond period which has been the usual period employed in similar machines by the assignee of this application since the Type 701 Computer was introduced. Computer type circuits are used throughout the patent applications to which reference is made and a detailed explanation of the circuits themselves and of the modifications thereof are not considered necessary because of the present state of the art. Throughout the description of operation no reference is made to passive elements such as cathode followers, level setters and the like. It is obvious that the characteristics of these elements vary and are largely determined not only by the component load but also by the length of conductors coupling one circuit to another.

Indicator instructions are as follows:

| Title                                   | Operation Code |
|-----------------------------------------|----------------|
| Invert Indicators from Accumulator..... | IIA + 0041     |
| Invert Indicators of Left Half.....     | IIL - 0051     |
| Invert Indicators of Right Half.....    | IIR + 0051     |
| Invert Indicators from Storage.....     | IIS + 0440     |
| Load Indicators.....                    | LDI + 0441     |
| Left Half Indicators, Off Test.....     | LFT - 0054     |
| Left Half Indicators, On Test.....      | LNT - 0056     |
| Off Test for Indicators.....            | OFT + 0444     |
| On Test for Indicators.....             | ONT + 0446     |
| Or Storage to Indicators.....           | OSI + 0442     |
| Place Accumulator in Indicators.....    | PAI + 0044     |
| Place Indicator in Accumulator.....     | PIA - 0046     |
| Right Half Indicators, Off Test.....    | RFT + 0054     |
| Reset Indicators from Accumulator.....  | RIA - 0042     |
| Reset Indicators of Left Half.....      | RIL - 0057     |
| Reset Indicators of Right Half.....     | RIR + 0057     |
| Reset Indicators from Storage.....      | RIS + 0445     |
| Right Half Indicators, On Test.....     | RNT + 0056     |
| Set Indicators of Left Half.....        | SIL - 0055     |
| Set Indicators of Right Half.....       | SIR + 0055     |
| Store Indicators.....                   | STI + 0604     |
| Or Accumulator to Indicators.....       | OAI + 0043     |
| Transfer When Indicators On.....        | TIO + 0042     |
| Transfer When Indicators Off.....       | TIF + 0046     |

### INVERT INDICATORS FROM ACCUMULATOR IIA + 0041

Word B is in the Accumulator and word A is in the Sense Indicator Register. Each order of the Accumulator P, 1 through 35 is matched with a corresponding order of the Sense Indicators 0 through 35. When the bit in the Accumulator Order is a "1," the contents of that position in the Sense Indicator Register is complemented. When the bit in the Accumulator is a "0," the contents of that position in the Sense Indicator Register is unchanged. The contents of the Accumulator are unchanged. This operation is accomplished by placing the contents of the Accumulator Register, word B, in the Stor-

age Register and then applying the contents of the Storage Register in parallel to binary inputs of each order of the Sense Indicator Register. Since the Storage Register is made up of microsecond delay units, no outputs are obtained from those Storage Register positions containing "0." Accordingly, only the Storage Register positions containing "1" are effective to set the corresponding Sense Indicator Triggers. Since the inputs are binary, if the state of the Trigger is "0," a "1" will cause it to change state to a "1." Whereas if its state is a "1," a "1" input causes it to change to "0." Assuming that word B is brought from Storage and placed in the Accumulator and that word A is placed in the Indicators with the Load Indicator Instruction, the operation code of the Invert Indicators from Accumulator Instruction (+0041) is contained in positions S, 1 through 11 of the Storage Registers. Positions 3 through 11 of the Storage Registers are placed in positions 1 through 9 of the Instruction Register by means of control lines 99.05 and 99.06. In the Instruction Register, FIGURE 13a, Storage Register 3 output line is down providing outputs on Minus on Instruction Register 1 lines 13a.01 through 13a.04. Storage Register 4 output line is down providing outputs on the lines 13a.09 through 13a.12. Storage Register 5 output line is down thus providing outputs on Minus on Instruction Register 3 lines 13a.17 and 13a.18. Storage Register 6 output line is up providing outputs on the lines 13a.23 and 13a.24. Storage Register 8 output line is down providing an output on the line 13a.25.

In FIGURE 13b, Storage Register 8 output line is down providing outputs on Minus on Instruction Register 6 lines 13b.01 through 13b.13. Storage Register 9 output line is down providing outputs on Minus on Instruction Register 7 lines 13b.25 through 13b.37. In FIGURE 13c, Storage Register 10 output line is down providing outputs on the line Minus on Instruction Register 8 lines 13c.01 through 13c.19. Storage Register 11 output line is up providing outputs on the lines 13c.55 to 13c.76. In FIGURE 100, Instruction Register sign Plus and Minus, position S of the Storage Register contained a 0 therefore the Instruction Register Sign Plus lines 100.01 through 100.41 are up.

Referring now to the Primary Operation Decoder, FIGURE 14a, the Instruction Register lines 1, 2, 3, 4 and 5 are up to provide an output 0, 4 indicative of the tens and hundreds position of the Operation Code. In FIGURE 14c, the lines 14c.12 through 14c.19 are up. In FIGURE 15a, Secondary Operation Decoder, additional decoding is provided. In Place Accumulating Indicators, FIGURE 44, Primary Operation (0, 4) line 14c.13 is up and the lines Minus on Instruction Register 6, Minus on Instruction Register 7, Minus on Instruction Register 8 and Instruction Register 9 are up providing outputs on the lines 44.07 through 44.10. The line 44.09 goes to Accumulator Storage Bus, FIGURE 72b, and when an I0(D4) pulse comes in, an output is provided on the line 72b.01 to Accumulator positions S, 1 through 35 to Storage Bus positions S, 1 through 35, FIGURE 72a, causing outputs to be provided on the lines 72a.01 through 72a.05. These lines go to Storage Bus Switching, FIGURE 2x (FIGURES 11a, 11b and 11c) to gate the contents of the Accumulator on to the Storage Buses. In FIGURE 44, the line 44.07 goes to Storage Bus to Storage Register Control, FIGURE 53b where it is combined with an I3(D1) line to provide an output on Storage Bus to Storage Register line 53b.02 which goes to FIGURE 53a to provide outputs on the lines 53a.01 through 53a.08. These lines go to Storage Register, FIGURES 2b through 2d (FIGURES 5a through 5f) to store the contents of the Storage Buses in the Storage Register. In FIGURE 44, the line 44.08 goes to Invert Indicators, FIGURE 95a, where the Tally Counter Drive line 117.25 is up due to the Clock Line Drive line 116.02, FIGURE 117. When the I5(D1) line comes up, an output is provided on the Invert Indicator line 95a.01 which goes to Indicator Trig-

ger Register, FIGURE 2a (FIGURE 10) to gate the Storage Register outputs into the binary input of the Triggers of the Indicator Trigger Register. Thus, for every Storage Register position containing a 1, the respective trigger is complemented. The line 44.10 goes to End Operation Control, FIGURE 128c, where it provides an output on the line 128c.01 to End Operation Control, FIGURE 128a.

#### INVERT INDICATORS—LEFT HALF ILL — 0051

This instruction is a type B instruction where the operation is contained in positions S, 1 through 11 and positions 1 and 2 contain "zeros." A control field F is contained in positions 18 through 35 and each position within field F is matched with a corresponding bit of the contents of the Sense Indicator Register positions 0 through 17. When a position in field F contains a "one," the contents of the corresponding position in the Sense Indicator, positions 0 through 17, is complemented. For each position in control field F containing a "zero," the contents of the corresponding position in the Sense Indicator positions 0 through 17 is unchanged. Contents of positions 18 through 35 of the Indicator Register are unchanged. Invert Indicator Left-Half is accomplished in the following manner: The instruction is placed in the Storage Register, FIGURES 2b through 2d, positions 18 through 35 of the Storage Register contain the field F and the contents of these positions are placed in the Adder positions P through 17, FIGURES 2j through 2q. The contents of the Adder are then placed in the Accumulator Register. Then, positions S through 17 of Storage Bus Switching, FIGURES 2w and 2x, are transferred to the Storage Register. It is pointed out that the result of this operation is to have moved positions 18 through 35 of the Storage Register into positions S through 17 of the Storage Register, and this is permissible since the operations portion of the control Word is placed in the Instruction Register during the Instruction Cycle and decoded there. During the ER cycle, which follows, manipulations take place which transfer the field from positions 18 through 35 of the Storage Register to positions P through 17 of the Adder. At the beginning of the next Instruction Cycle, following the ER cycle, the Invert Indicator Controls come up and the outputs of Storage Registers, positions S through 17, are applied as binary inputs to the Indicator Register, FIGURE 2a. Since positions 18 through 35 of the Storage Register now contain "zeros," there is no effect upon the contents of the Indicator Register positions 18 through 35, but for every position of the Storage Register which contain a "one," the corresponding position in the Indicator Register 0 through 17 is complemented. The instruction is brought into the Storage Register in the usual manner in response to the line Storage Bus to Storage Register and positions 3 through 11 of the Storage Register are placed in the Instruction Register, FIGURE 2h (FIGURE 13). The Sign position of the Storage Register goes to Instruction Register Sign Plus and Minus, FIGURE 100. Since position S contained a "one," the trigger is set bringing up the Instruction Register Sign Minus lines 100.43 through 100.103. In FIGURE 13a, Instruction Register, Storage Register 3 output line is down and the lines 13a.01 through 13a.04 are up; Storage Register 4 output line is down providing outputs on the lines 13a.09 through 13a.12. Storage Register 5 output line is down providing outputs on the lines 13a.17 and 13a.18. Storage Register 6 output line is up providing outputs on the lines 13a.23 and 13a.24. Storage Register 7 output line is down providing outputs on the line 13a.25. In Instruction Register, FIGURE 13b, Storage Register 8 output line is up providing outputs on the lines 13b.15 to 13b.24. Storage Register 9 output line is down providing outputs on the lines 13b.25 to 13b.37. In FIGURE 13c, Instruction Register, Storage Register 10 output line is down providing outputs on the lines 13c.01 through 13c.19. Storage Register 11 line is

up providing outputs on the lines 13c.55 through 13c.76. In FIGURE 14a, the Primary Operation Decoder, Instruction Register lines 1, 2, 3, 4 and 5 are up to provide an output on the line (0, 4) which goes to Primary Operation Decoder, FIGURE 14c, to bring up the lines 14c.12 to 14c.19. In FIGURE 42, Half Indicator Register Controls, Primary Operation (0, 4) line is up, Instruction Register 6 line is up, and Test Indicators Off Half Control line 39.01 is up. Since the trigger in Test Indicator Storage Half Test Indicator, FIGURE 39, is OFF, the lines 42.01 through 42.12 are up for one ER cycle, in FIGURE 42.

With reference to the Cycle Timer Control, FIGURE 118, the lines Minus on Instruction Register 1, Minus on Instruction Register 2 and Minus on Storage Display are up. The lines Minus on Go to E Time (Trap, Transfer Control), Minus on Go to E Time, IA Instruction (Store and Trap), are up and the End Operation Trigger is OFF so when the I9 to C1 line comes up, an output is provided on the lines 118.03 and 118.04. The line 118.01 goes to Cycle Timer Output circuits, FIGURE 120, where it sets the Master ER Time Trigger. The line 118.02 goes to the Cycle Timer Gate Generator, FIGURE 119, to provide a Reset Cycle Timer output on the line 119.01. The machine goes into ER time and at ER4(D2) lines 42.13 through 42.16 are brought up in Half Indicator Registers controls, FIGURE 42. The line 42.15 goes to Storage Registers 18 through 35 to Adders P through 17, FIGURE 86b, where it is combined with Instruction Register Sign Minus to provide an on Storage Register positions 18 through 35 to Adder positions P through 17 on the line 86b.01. This line goes to Indexing Operation Storage Registers 18 through 35 to Adder positions P through 17, FIGURE 86a, to provide an output on the lines 86a.01 through 86a.12.

In FIGURES 2j through 2q and more specifically in FIGURES 6a through 6l, the contents of the Storage Register, positions 18 through 35, are placed in positions P through 17 of the Adder. At ER4(D2), the line 72b.01 in Accumulator to Storage Bus, FIGURE 72b, is brought up to place the contents of the Accumulator positions S through 35, on the Storage Bus. With reference to the Half Indicator Register Controls, FIGURE 42, at ER5 outputs are provided on the lines 42.17 through 42.20. The line 42.20 goes to Adder to Accumulator Controls, FIGURE 57b, where it provides an output on the line 57b.01 to Adders to Accumulator Control, FIGURE 70, where the line 70.01 is brought up. The line 70.01 goes to Adder to Accumulator Controls, FIGURE 57a, to bring up the lines 57a.01 through 57a.04 to place the contents of the Adder in the Accumulator (FIGURES 2z through 2cc). The line 42.19 goes to Storage Bus to Storage Register Controls, FIGURE 53b, where it brings up the Storage Bus to Storage Register line 53b.02 at ER5(D1) which transfers the Storage Bus positions S through 35 to Storage Register, positions S through 35.

In Indexing Controls, FIGURE 90b, the Half Indicator Control line 42.06 is up and at ER3(D4) Drop Hold Tag Bits line 90b.01 is up. The line 42.06 goes to Indexing Controls, FIGURE 90a where it turns OFF the trigger to bring up the Minus on Hold Tag Bits lines 90a.04 and 90a.05. At this time, positions P through 17 of the Accumulator Register contain what was formerly in field F of the Instruction and was originally placed in positions 18 through 35 of the Storage Register. The present contents of the Storage Register is the contents of the Accumulator Register at the beginning of the ER cycle. In FIGURE 54b, Storage Register to Adders, Half Indicators Controls line 42.13 is up and at ER10(D2) an output is provided on the lines 54b.01 and 54b.02 to place the contents of the Storage Register positions S through 35 in the Adders. In FIGURE 57b, Adder to Accumulator control, the line 42.20 is up at ER11(D1) to bring up the line 57b, Adders to Accumulator, and cause the con-

tents of the Adder to be placed in the Accumulator. It is emphasized, however, that at the same time that the Storage Register contents are going through the Adder to the Accumulator, namely, ER10 to ER0, the contents of the Accumulator positions P through 17 or the contents of field F are being placed in the Storage Register, positions S through 17 in the following manner. In FIGURE 72b, Accumulator to Storage Bus, the Half Indicator Control line 42.14 is up and at ER10(D2) the line Accumulator to Storage Bus 72b.01 is brought up. In FIGURE 53a, Storage Bus to Storage Register, the Half Indicators to Register line 42.05 is up and Instruction Register Sign Minus line 100.07 is up which brings up the lines 53a.01 through 53a.05 causing the contents of the Accumulator positions P through 17 to be placed in Storage Register, positions S through 17. At this point, Storage Bus positions 18 through 35 to Storage Register positions 18 to 35 line is down. The line 42.04 of Half Indicator Register Controls goes to End Operation Control, FIGURE 128c, where Instruction Register 9 is up to provide an output on the End Operation in the ER time line 128c.01. This line goes to End Operation Control, FIGURE 128a, where it is combined with ER time to produce an End Operation Control on the line 128a.01. In the Cycle Timer Control of FIGURE 118, End Operation Control Line is up, and at A10(D2) the end Operation trigger is turned ON providing outputs on the lines 118.06 through 118.15. The lines 118.14 and 118.15 prescribe Go to I Time on the next cycle. The line 42.08 goes to Invert Indicator Controls, FIGURE 95a, where the Minus on Instruction Register 7 line is up at I3(D1) and line 95a.01 is up to Indicator Trigger Register, FIGURE 10, where it provides a gate for those orders of the Storage Register containing "ones." Therefore, for every order of the Storage Register containing a "one," the corresponding trigger in the Indicator Trigger Register is complemented for those orders containing "zeros" the status of the trigger is unchanged. It is pointed out also that positions 18 through 35 of the Storage Register now contain "zeros" so there is no effect upon positions 18 through 35 of the Indicator Register.

#### INVERT INDICATORS OF RIGHT-HALF IIR + 0051

This instruction is a Type B Instruction in which the operation is contained in positions S through 11 and a Control Field F is contained in positions 18 through 35. Each order of the Field F of this instruction is matched with a corresponding order of the Sense Indicator Register in positions 18 through 35. For each position of the field containing a "1," the corresponding position in the Sense Indicator Register is complemented. When the bit is a "0," the contents of the corresponding positions in the Sense Indicator Register is unchanged. The contents of the Sense Indicator Register, positions 0 through 17 are unchanged. It will be noted the similarity between the Invert Indicator Right-Half and the previously described Invert Indicators Left-Half. In so far as the operation is concerned the only difference is that the operation code of the Invert Indicators Right-Half is plus. The Control Field F contained in positions 18 through 35 is now placed in positions 18 through 35 of the Adder, whereas in Invert Indicators Left-Half, positions 18 through 35 of the Storage Register were transferred to positions P through 17 of the Adder in order that the Control Field could be moved into position whereby it could be matched with positions 0 through 17 of the Indicator Register. Because of the similarity, only the differences in the control lines will be discussed.

In FIGURE 86b, Storage Register positions 18 through 35 to Adder positions P through 17, it will be noted that the Instruction Register Sign minus line is down, thus preventing Storage Register positions 18 through 35 to Adder positions P through 17 line 86b.01 from being up. In FIGURE 54b, Storage Registers to Adders, the Half-Indicators ER4(D2) line 42.13 is up, and the Instruction

Register Sign in plus for the IIR Instruction. Thus, an output is provided on line 54b.01 to FIGURE 54a where lines are brought up to transfer the entire contents of the Storage Register into the Adders. This means of course, that the operation part is entered into the Adders and from there into the Accumulator. However, it is gated out by the transfer of Storage Bus positions 18 through 35 to Storage Register positions 18 through 35 hereafter, and when the control field F finally reaches positions 18 through 35 of the Storage Register, positions S, 1 through 17 of the Storage Register will be vacant. The operation code is, of course, retained in the Instruction Register, FIGURE 2h, and in the Sign Plus and Minus controls.

With reference to FIGURE 53a, Storage Bus to Storage Register Controls, the Half Indicators to Register line 42.19 is up, Instruction Register Sign plus line is up so that the Storage Bus positions 18 through 35 to Storage Register positions 18 through 35, lines 53a.06 to 53a.08 are up. Accordingly, the Storage Register, FIGURES 2b to 2d, positions 18 through 35, contain the control field F and positions S through 17 are 0. The Invert Indicator line 42.08 comes up and Invert Indicator Control, FIGURE 95a at I5(D1) Invert Indicators line 95a.01 is up to the Indicator Trigger Register, FIGURE 10, causing the positions 0 through 17 of Indicator Register to be complemented provided a corresponding "one" is entered on the Storage Register output lines from position 18 through 35 of the latter.

#### INVERT INDICATORS FROM STORAGE IIS OPERATION CODE PLUS 0040

This instruction is a Type B Instruction which contains an address, an operation part, and an index tag. The instruction is decoded and the Address specified in the Instruction is entered into the Storage Address Register, FIGURE 2hh. The word at that location in Storage is brought up to the Sense Amplifier, Buffer, and I/O Switching, FIGURE 2ll, during the following Execute Cycle and is placed in the Storage Register. Each order of the Storage Register is then matched with the corresponding bit of the Sense Indicator Registers, positions 0 through 35 when the bit in the Storage Register is a 1, the corresponding positions in the Sense Indicator Register is complemented. When the bit in the corresponding order of the Storage Register is a "zero," the contents of the position in the Sense Indicator is unchanged. The contents of the location in Core Storage specified is likewise unchanged.

In FIGURE 100, Instruction Register Sign Plus and Minus, the sign is positive, and the lines 100.43 through 100.103 are up. In the Instruction Register, FIGURE 13a, Storage Register 3 output is up providing output from the lines 13a.05 through 13a.08. Storage Register 4 output line is down providing outputs Minus on Instruction Register 2 lines 13a.09 through 13a.12. Storage Register 4 output line is down thus providing outputs on Minus on Instruction Register 3, lines 13a.17, and 13a.18. Storage Register 6 output line is up providing outputs on Instruction Register 4 lines 13a.23 and 13a.24. Storage Register 7 output line is down, thus providing an output on Minus on Instruction Register 5 line 13a.25.

In FIGURE 13b, Storage Register 8 output line is down providing outputs from the lines 13b.01 through 13b.13. Storage Register 9 line output is down providing outputs on the minus on Instruction Register 7 lines 13b.25 through 13b.37. In FIGURE 13c, Storage Register 10 line is down providing outputs on the minus on Instruction Register 8 lines 13c.01 through 13c.19. Storage Register 11 line is down providing outputs on the Minus on Instruction Register 9 lines 13c.37 through 13c.53.

In the Primary Operation Decoder, FIGURE 14b, the Instruction Register 1, 2, 3, 4 and 5 lines are up and the IA Trigger is OFF, thus providing an output on the line (4, 4) indicative of the tens and hundreds operation code of the Instruction 0440. In FIGURE 14d, outputs are thereby provided on the lines 14d.07 through 14d.12.

Since this Instruction required a reference to Storage, an Execute Cycle must be taken to bring out the word at the location specified by the Address contained in the Instruction. The Address of the location in Storage is specified by the contents of positions 21 through 35 of the Storage Register which is placed in positions 3 through 17 of the Adder from I9 until CT1 from the line 122j.59 which causes the contents of the Storage Register positions 18 through 35 to be placed in the Adder, positions P through 17 via the lines 86a.01 through 86a.12. The contents of positions 3 through 17 of the Adder are then gated through the Address Register, to the Storage Address Register, FIGURE 129, by way of an Adder to Address Switch Control, FIGURE 110. The word at the location specified by the Address is brought from the Core Array and placed in the Storage Buffer Register, FIGURE 11, in the manner described previously.

In FIGURE 53a, the Minus on And to Storage Control line 30.10 is up, the Minus on Transfer and Trapping Mode line 110.03 is up, and at E7(D1) outputs are provided on the lines 53a.01 through 53a.08 to cause the contents of the storage Buffer Register, FIGURE 2ll, to be entered into the Storage Register, FIGURES 2b through 2d. With reference to FIGURE 95a, Invert Indicators, the Primary Operation (4, 4) line is up, Minus on Instruction Register 7 line is up, Minus on Instruction Register 8 line is up, Minus on Instruction Register 9 line is up, and at E11(D1), Invert Indicators, line 95a.01 is up to the Indicator Trigger Register, FIGURE 2a (FIGURE 10), and the contents of the Storage Register positions S, 1 through 35 are gated through to the binary inputs of the Indicator Triggers. Therefore, for each position of the Storage Register containing a "1," the corresponding position of the Indicator Trigger Register is complemented.

#### LOAD INDICATORS (LDI + 0441)

The contents of the location in Storage specified by the address in the LDI Instruction is placed in the Indicator Register. With reference to the Instruction Register positions 1 through 5, FIGURE 13a, Storage Register 3 output line is up and Instruction Register 1 lines 13a.06, 13a.07 and 13a.08 are up. Storage Register 4 output is down and Minus on Instruction Register 2 lines 13a.09, 13a.10, 13a.11 and 13a.12 are up, Storage Register 5 line output is down and Minus on Instruction Register 3 output lines 13a.17 and 13a.18 are up. Storage Register 6 line output is up so Instruction Register 4 line 13a.24 is up, Instruction Register 7 output is down and Minus on Instruction Register 5 line 13a.25 is up. With reference to the Instruction Register, FIGURE 13b, Storage Register 8 line output is down and Minus on Instruction Register 6 lines 13b.01 through 13b.13 are up. Storage Register 9 line output is down and Minus on Instruction Register 7 lines 13b.25 through 13b.37 are up. With reference to Instruction Register, FIGURE 13c, Storage Register 10 line is down, and Minus on Instruction Register 8 lines 13c.01 through 13c.19 are up. Storage Register 11 line is up and Instruction Register 9 lines 13c.55 through 13c.76 are up. In FIGURE 100 Instruction Register Sign Plus and Minus, Instruction Register Sign Plus lines 100.01 through 100.41 lines are up. In the Primary Operation Decoder, FIGURE 14b the lines 1, 2, 3, 4 and 5, and Indirect Addressing Trigger Off lines are up, and an output is provided from the line (4, 4) indicative for Primary Operation code of 4, 4 or the tens and hundreds position of the Operation code. In FIGURE 14d, the lines 14d.07 through 14d.12 are up. The line 14d.07 goes to End Operation, FIGURE 128b, the line Minus on Instruction Register 7 is up providing Storage End Operation on the line 128b.01, which goes to End Operation, FIGURE 128a. The IA control trigger is OFF and at E time an output is provided on End Operation Control line 128.01 to Cycle Timer Control, FIGURE 118, for causing an End Operation at the end of the Execute

Cycle as shown in FIGURE 4a. The line 14d.10 in FIGURE 14d is provided to Reset Indicators, FIGURE 93, where Instruction Register 7 line is not up, and therefore the Reset Indicator line 93.01 remains down. In FIGURE 14d, the line 14d.09 is up to Invert Indicators, FIGURE 95a, where the line Minus on Instruction Register 9 is down and an output is prevented on the Invert Indicators line 95a.01. In FIGURE 14d, the line 14d.12 is up to Set Indicators, FIGURE 94, where the line Instruction Register 8 is down and an output on Set Indicators line 94.01 is prevented. The line 14d.08 goes to Test Indicators Storage, Half Test Indicator, FIGURE 39, where the Minus on Storage Register 9 is down preventing a Test Indicator Storage T2 line 39.02 from being up.

In FIGURE 86a, the Storage Register 18-35 to Adders P-17 lines 86a.01 through 86a.12 are up from I9 until CT1 by way of the line 122j.59. In FIGURE 110, the Minus on Transfer in Trapping Mode line 110.02 is up and combines with the I9 until CT1 line to bring up the Adder to Address Switch Control line 110.04. The line 110.04 of the Address Register, FIGURE 16a to gate Adder positions 3 through 17 onto the Address Switch lines to the Storage Address Register, FIGURE 129. The contents of the location specified by these address lines is placed in the Storage Buffer Register, FIGURE 142, and at E7 the contents thereof are placed in the Storage Register via lines 30.10, 110.03 and E7(D1) in FIGURE 53a and the Hold Storage Register lines of FIGURES 5d and 5e.

In FIGURE 92, the Load Indicators line 44.06 is up from FIGURE 44 since Primary Operation 44, Minus on Instruction Register 7, and Instruction Register 9 lines are up. In FIGURE 92, the E0(D4) and A2(D6) lines cause the Indicator Triggers to be reset by the line 92.01.

In FIGURE 94, the Load Indicators line 44.06 is up and from E9 until CT2 the contents of the Storage Register are entered into the Indicators via the line 94.01.

#### PLACE ACCUMULATOR IN INDICATORS (PAI + 0044)

The instruction contains an operations part +0044 and an address. The contents of the location specified by the address replace the contents of the Sense Indicator Register. The contents of the location in Storage remains unchanged.

In FIGURE 13a, Storage Register 3 output line is down and outputs are provided on the lines 13a.01 through 13a.04. The line Storage Register 4 output is down providing outputs on the lines 13a.09 through 13a.12, the line Storage Register 5 line is down providing outputs on the lines 13a.17 and 13a.18, and the line Storage Register 6 output provides an output on the line 13a.24. The Storage Register 7 output line is down providing an output on the line 13a.25. In FIGURE 13b, Storage Register 8 line is down providing outputs on the lines 13b.01 through 13b.13 and Storage Register 9 line is up providing outputs on the lines 13b.39 through 13b.55. In FIGURE 13c, Storage Register line 10 is down providing outputs from the lines 13c.01 through 13c.19, and Storage Register 11 line is down providing outputs on the Minus on Instruction Register 9 lines 13c.37 through 13c.53. In FIGURE 14a, Primary Operation Decoder the Instruction Register lines 1, 2, 3, 4 and 5 are up providing an output on the line (0, 4). In FIGURE 14c, the Primary Operation (0, 4) line is up to provide outputs on the lines 14c.12 through 14c.19. The line 14c.12 goes to Transfer Indicator to Accumulator, FIGURE 40, where an output is not provided since Instruction Register 8 line is down. The line 14c.13 goes to Place Accumulator and Indicators, FIGURE 44, where Primary Operation (0, 4) line 14c.13 is up Instruction Register 7 line is up, Minus on Instruction Register 8 line is up, and Minus on Instruction Register 6 line is up to provide outputs on the Place Accumulator in Indicators, Storage Bus to Storage Register line

44.01, Accumulator to Storage Bus line 44.02, Set Indicators line 44.03, Electronic Reset of Indicators line 44.05, and Set Indicators line 44.06.

The line 44.04 goes to Electronic Reset of Indicators, FIGURE 92, where it is combined with A2(D6) and I0(D4) to provide an output on the Electronic Reset of Indicators line 92.01, the latter going to the Indicator Trigger Register, FIGURE 10, to reset the indicators to "zero." The line 44.04 goes to Accumulator to Storage Bus, FIGURE 72b, where it provides an output I0(D4) on the Accumulator to Storage Bus line 72b.01. The line 44.01 goes to Storage Bus to Storage Register, FIGURE 53b, where at I0(D4) an output is provided on Storage Bus to Storage Register line 53b.02. The line 44.03 goes to Set Indicators, FIGURE 94, and combines with the line 14(D2) to provide an output Set Indicators on the line 94.61. The line 94.01 goes to the Indicator Trigger Register, FIGURE 10, where it gates the Storage Register outputs to set the Indicator Triggers. In this manner the contents of the Accumulator are placed in the Sense Indicator Register.

It is pointed out with reference to the timing chart of FIGURE 4b that the End Operation Go to I Time control comes up at the end of the Instruction cycle when the Instruction PAI was brought into the Central Processing Unit from Storage. A second reference to Memory is not required for data since the Accumulator contents are to be placed in the Indicator. Therefore, an E/R cycle is taken and a reference is made to Storage for the next instruction after the E cycle. The Instruction Counter has been advanced, an Instruction cycle follows and a new instruction is brought in to the Storage Register as indicated in the timing chart without interference with the operation of placing the contents of the Accumulator Indicator.

In FIGURE 40, Transfer Indicators Accumulator, the line 14c.12, the Instruction Register Sign Plus line 100.22, Minus on Instruction Register 6 line 13b.06, Instruction Register 8 line 13c.26 and Minus on Instruction Register 9 line 13c.43 are up to bring up the line 40.01. The line 40.01 goes to Invert Trigger T2, FIGURE 48, where it is combined with the I9 until CT1 line 122j.62 to turn ON T2 trigger. Also in FIGURE 48 the Primary Operation (0, 4) line is up, but Instruction Register 6 and Instruction Register 9 lines are down. The line 40.02, Transfer Indicators Accumulator (GPI) line is not up until T2 is ON so previous to this signal on line 48.12 goes to End Operation Control, FIGURE 128a, where it is combined with Minus on Instruction Register 1 and Minus on Instruction Register 2 and GRI line 48.12. However, the E/R time lines is not up at this time to provide an End Operation Control.

As stated previously with T2 ON, the lines 40.02 through 40.08 are up to gate the contents of the Accumulator on to the Storage Bus and to bring the contents of the Storage Bus in the Storage Register and then set the indicators with the contents of the Storage Register by the line 94.01 at I7(D1). The contents of the Storage Buffer Register, FIGURE 211, contains the instruction which immediately follows the PAI instruction. It is placed in the Storage Bus at I7(D1) placed in the Storage Register, the operation part of the instruction is taken from Storage Register to Instruction Register at I9(D1), the instruction PAI is removed from the Instruction Register at I8 and at I9.5 the instruction which follows the PAI instruction is decoded.

#### RESET INDICATORS OF LEFT HALF (RIL — 0057)

This instruction has a Primary Operation code 04. Since details of operation decoding has previously been explained it is considered to be unnecessary to name specific lines by number which are not used in connection with the operation code (0, 4) of this instruction. It suffices to say that in the Storage Register, Storage Register lines 6, 8, 9, 10 and 11 are up and Storage Register lines 3, 4, 5 and 7 are down. Accordingly, Instruction Register lines

1, 2, 3, 4, 5, 6, 7, 8, 9 are up to the primary operation decoder. In FIGURE 14a, the line indicative of the tens and hundreds positions of the operation code is up, namely (0, 4). In FIGURE 14c, the lines 14c.12 to 14c.19 are up.

This is a type B instruction having the operation contained in positions S through 11 with "zeros" in positions 1 and 2. Positions 18 through 35 contain a Control Field F and each order of the field F is matched, with a corresponding order of the Sense Indicator Register positions 0 through 17. When the bit in positions 18 through 35 of the instruction is a "one," a "zero" replaces the contents of that position with contents of the corresponding position in the Sense Indicator Register and when the bit in a corresponding position of the field F is a "zero," the contents of the corresponding positions the Sense Indicator Register is unchanged. The contents of Indicator Register positions 18 through 35 is unchanged. This is accomplished in the following manner; the instruction RIL is loaded into the Storage Register of the Magnetic Core Storage and positions 18 through 35 of the Storage Register are placed in positions P through 17 of the Adder, the contents of the Adders are then placed in the Accumulator and the contents of the Accumulator positions S through 35 are placed in the Storage Register positions S through 35. The result is that the initial contents of the Accumulator which was contained therein at the start of the operation is now in the Storage Register and the contents of positions 18 through 35 of the Storage Register is now in positions P, 1 through 17 of the Accumulator. During the latter part of the ER cycle, the contents of the Storage Register (formerly the contents of the Accumulator) is sent through the Adders to the Accumulator at the same time that the contents of the Accumulator, namely, positions P through 17 (the field F) and positions 18 through 35 which contains "zeros" are sent to the Storage Register. Then the contents of the Storage Register are sent to the Indicators to reset them according to the ones in the orders of the Control Field F. In Test Indicator Storage Half Test Indicators, FIGURE 39, the test Indicators Off Storage line 39.01 is up and in Half Indicator Register Control, FIGURE 42, the primary operation (0, 4) line is up. Instruction Register 6 line is up and Test Indicators Off Half Control line 39.01 is up to bring up the lines 42.01 through 42.12. These lines are up throughout the E/R cycle which is taken in response to the Cycle Timer Control, FIGURE 118. In Storage Register positions 18 through 35 to Adder positions P through 17, FIGURE 86b, a line 42.15 is up at E/R 4 for 2 microseconds and Instruction Register Sign Minus line is up, so that an output is provided on the line 86b.01 to FIGURE 86a where the lines 86a.01 to 86a.12 are up. Therefore, the outputs of positions 18 through 35 are gated into the Adders positions P through 17. In FIGURE 57b, the Adder to Accumulator Half Indicators to Register, line 42.20 is up to provide outputs on the Adder to Accumulator line 57b.01 at E/R(D1) to place the contents of the Adders in the Accumulator. Coincidentally with the operation of moving Storage Register positions 18 through 35 to the Accumulator Register, the contents of the Accumulator Register are moved into the Storage Register in the following manner. In the Accumulator to Storage Bus Controls, FIGURE 72b, the Half Indicators line 42.14 is up at ER4(D2) to provide an output on the line 72b.01 to the Accumulator positions S, 1 through 35 to Storage Bus positions S, 1 through 35 controls of FIGURE 72a. In FIGURE 72a, the lines 72a.01 through 72a.04 are brought up to put the contents of the Accumulator Register on the Storage Buses. In Storage Bus to Storage Register Controls, FIGURE 53b, the line 42.19 is up and the ER5(D1) line is up to provide an output on the line 53b.02 to the Storage Bus to Storage Register, FIGURE 53a, where the output lines 53a.01 through 53.08 are brought up, thus placing the contents of the Storage Bus in the Storage Register.

Later in the E/R cycle, the contents of the Storage Register positions S through 35 are loaded into the Accumulator and the contents of the Accumulator positions S, 1 through 17 are loaded into the Storage Register in the following manner. Since in Storage Register to Adders, FIGURE 54b, the Half Indicator Control line 42.13 is up and ER10(D2) line is up, outputs are provided on the lines 54b.01 through 54b.02 to transfer the contents of the Storage Register positions S through 35 to the Adders. In Adder to Accumulator Controls, FIGURE 57b, the line 42.20 is up at ER11(D1) to provide an output on the line 57b.01 to the Adders to Accumulator Control, FIGURE 70, where the Adder to Accumulator control line 70.01 is brought up. In FIGURE 57a, the line 70.01 provides outputs on the lines 57a.01 to 57a.04, and the contents of the Storage Register positions S through 35 are now in the Accumulators. Coincidentally, the contents of the Accumulator are sent to the Storage Register in the following manner. In Accumulator Storage Bus Controls, FIGURE 72b, a Half Indicator control line 42.14 is up and at ER10(D2), the Accumulator to Storage Bus line 72b.01 is up. In FIGURE 72 outputs are provided on the lines 72a.01 through 72a.05 to cause the contents of the Accumulator to be placed on the Storage Buses. The line 42.19 goes to Storage Bus to Storage Register Control, FIGURE 53a, where it is combined with an Instruction Register Sign Minus line to provide outputs on the lines 53a.01 through 53a.05 to gate the contents of the Storage Register positions S through 17. The line 42.04 goes to End Operation Controls, FIGURE 128c, where it is combined with Instruction Register 9 line to provide end operation in E/R Time control on the line 128c.01. During E/R time End Operation Control line 128a.01 goes to the Cycle Timer initiates End Operations and directs the machine to go to Instruction time. The line 22.07 from Half Indicator Register controls goes to Reset Indicators FIGURE 93 where it is combined with Instruction Register 8 line to bring up the Reset Indicators line 93.01 to the Indicator Trigger Register, FIGURE 10. The line 93.01 gates the Storage Register outputs where each order of the Indicator Trigger Register is turned OFF in response to a "one" being stored in the Storage Register since the Storage Register outputs are provided to the input of a trigger which turns the latter OFF in response to the Storage of a "one." Obviously those orders in the Storage Register containing "zeros" are ineffective to change the status of the Indicator triggers and as pointed out earlier, the present contents of the Storage Register positions 18 through 35 are ineffective and they contain "zeros."

#### ON TEST FOR INDICATORS ONT + 0446

The status of each order of the Sense Indicator Register for which there is a "one" in the corresponding position of a word taken from storage at the location specified by the Address of this instruction is examined. Indicators from which there is a "zero" in the corresponding position of the word from Storage are not examined. If all examined Indicator orders are not "ones," the Calculator takes the next instruction in sequence. If all are "ones," the Calculator skips the next instructions and proceeds from there. This instruction takes four cycles, an Instruction Cycle, an Execute Cycle, and two E/R Cycles. During the Instruction Cycle, the ONT instruction is decoded and the address specified by the instruction is then used during the Execute Cycle to bring the word at the location specified by the address into the Central Processing Unit. Thereafter during two successive E/R Cycles, the ON Test is performed. FIGURE 4c illustrates the timing sequence and shows the manipulations within the various registers to accomplish the test. Assuming that the instruction ONT is now in the Storage Register, positions 3, 6, 9 and 10 of the Storage Register contain "ones" and positions 4, 5, 7, 8 and 11 contain "zeros." The Instruction Register lines 1, 4, 7 and 8 are up and the

lines  $\bar{2}$ ,  $\bar{3}$ ,  $\bar{5}$ ,  $\bar{6}$  and  $\bar{9}$  are up. In the Instruction Register Sign Plus and Minus Control, FIGURE 100, the lines indicating Instruction Register Sign Plus are up. In the primary operation decoder, FIGURE 14b, the lines Instruction Register 1,  $\bar{2}$ ,  $\bar{3}$ , 4,  $\bar{5}$  are up providing an output on the line (4, 4) which goes to FIGURE 14d and brings up the lines 14d.01 through 14d.02. The line 14d.08 goes to Test Indicators Storage, FIGURE 39, where the Primary Operation (4, 4) line is up, Instruction Register 7 line is up and Minus on Instruction Register 9 is up to provide an output on Test Indicators (Storage). The line 39.02 goes to Inverter Trigger T2, FIGURE 48, where the line is combined with E time line 122m.19 to turn T2 ON and bring up the lines 48.06 through 48.10. The address contained in the instruction in Storage Register positions 21 through 35 and just placed in positions 3 through 17 of the Adders is gated through the Address switches to the Storage Address Register, FIGURE 129, and in response to this Address, the contents of the location thereby specified are brought from the Storage Buffer Register, FIGURE 211, into the Storage Register by way of the controls of FIGURE 53 at E7(D1). In Test Indicators Storage and Half Test Indicators, FIGURE 39, T2 is ON during E/R Time and the Test Indicator Storage First Step lines 39.08 to 39.13 are up. The lines 39.02 are up and the line 39.09 goes to Storage Register to Adders, FIGURE 54b, where ER0(D4) the lines 54b.01 and 54b.02 are up also. In FIGURE 54a, Storage Register positions 1 through 35 to Adder lines 54a.01 through 54a.13 are up to transfer the contents of Storage Register to Adder. The line 54b.01 goes to FIGURE 81 where the contents of position S of the Storage Register are caused to be placed in position P to the Adder. The line 39.10 goes to Adder to Accumulator controls FIGURE 57d, where it is combined with ER3(D1) to provide an output on Adder to Accumulator line 57b.01 to Address to Accumulator line 57b.01 to Address to Accumulator Control, FIGURE 70, which passes the output on to the Adders on the Adders to the Accumulator line 70.01. The line 70.01 goes to Adder positions P, 1 through 35 to Accumulator, FIGURE 57a, to bring up the lines 57a.01 through 57a.04 and transfer the contents of the Adder to the Accumulator. Coincidentally with the transfer of the contents of the Storage Register to the Accumulator, the contents of the Accumulator are transferred to the Storage Register in the following manner. The line 39.11 goes to Accumulator to Storage Bus Control, FIGURE 72b, where it is combined with an ER0(D4) line to bring up a Accumulator Storage Bus line 72b.01, the latter going to FIGURE 72a to bring up the lines 72a.01 through 72a.05 and cause the contents of the Accumulator to be placed on the Storage Bus. The line 39.08 goes to Storage Bus to Storage Register Controls, FIGURE 53b, where it is combined with an ER3(D1) line to bring up the Storage Bus to Storage Register line 53b.01, the latter going to Storage Bus to Storage Register Controls, FIGURE 53a, to bring up the lines 53a.01 through 53a.08 and cause the contents of the Storage Bus to be placed in the Storage Register. The line 39.12 goes to complement Accumulator to Adder Controls FIGURE 55b, where it is combined with an ER6(D4) line to bring up Complement Accumulator Adder line 55b.01, the latter going to FIGURE 55c which brings up the lines 55c.01 through 55c.05 and 55c.07 through 55c.13. The line 39.10 goes to Adder to Accumulator controls FIGURE 57b where at A7(D1) of this E/R cycle an output is provided on the Adder to Accumulator line 57b.01. The line 57b.01 goes to Adders to Accumulator Control, FIGURE 70, where it brings up to Adder to Accumulator Control on the line 70.01. This line goes to Adder positions Q, P, 1 through 35 to Accumulator, FIGURE 57a, to bring up the lines 57a.05 to 57a.08 causing the Adders to be placed in the Accumulator. The line 39.16 goes to Accumulator to

Storage Bus Controls, FIGURE 72b, where it brings up the line 72b.01 which goes to FIGURE 72a to bring up the lines 72a.01 to 72a.05 at ER/10 for the duration of two microseconds to place the Accumulator on the Storage Bus. The line 39.14 goes to Storage Register to Adders, FIGURE 54d, to bring up the lines 54b.01 and 51b.02 to place the contents of the Storage Register in the Adders. The contents of the Accumulator are now on the Storage Bus and are entered in the Storage Register at ER11(D1) by means of the Storage Bus to Storage Register Controls of FIGURE 53b. In FIGURE 53b, the Test Indicator Storage First Step line is up from FIGURE 39 and it is combined with the line ER11(D1) to bring up the line 53b.02. The contents of the Adders are placed in the Accumulator at ER11(D1) by the Adder to Accumulator controls of FIGURE 57b to the Test Indicator Storage line 39.10. In summation the contents of the Accumulator and the Storage Register are exchanged. The initial contents of a Storage Register when the operation began are complemented. The result of that the original contents of the Storage Register have been complemented.

Referring now to Test Indicators Storage and Left Test Indicators, FIGURE 39, the Test Indicator Storage Second Step lines must now be brought up. With reference to FIGURE 39, the line 39.02 is up from I9.5 until I8, T2 is ON from E time until ER0 and Test Indicator Storage First Step is up during the first ER cycle. T2 is turned OFF by the fall of the ER11(D1) pulse, and turn OFF at T2 identifies the second ER cycle and initiates this sequence of operations by bringing up the lines 39.03 through 39.07. The line 39.15 is up the very last part of the first ER cycle and goes to Indicators to Storage Bus, FIGURE 96, where Instruction Register 8 line is up to bring up the indicators to Storage Bus lines 96.01 through 96.03. Coincidentally with the last operation, the line 39.03 Storage Register to Adders is up and goes from Storage Register to Adders, FIGURE 54b, to bring up the lines 54b.01 and 54b.02. The latter goes to Storage Register to Adder controls, FIGURE 54a, to bring up the lines 54a.01 through 54a.13. The present state is that the contents of the Accumulator and the contents of the Indicator Register are ORed into the Storage Register and the previous contents of the Storage Register are placed in the Adders and then the Accumulators. Since the Storage Register now contains the ORed contents of the Accumulator, the Indicator Registers On test is now performed by causing a "one" to be placed in Adder position 35. The carry to Adder 35 line 39.05 goes to Carry to Adder 35 Controls, FIGURE 56, where it is combined with the A3(D4) line to bring up the Carry to Adder 35 line 56.01. The line 56.01 goes to position 35 of the Adder, FIGURE 6h.

Recalling for the moment that the status of each order of the Sense Indicator Register in which there is a "one" in a corresponding position of the contents of the Storage Register is examined and if all examined Sense Indicator Triggers are not "ones" the calculator skips the next instruction in sequence, or if all "ones," the calculator skips the next instruction and proceeds from there, consider the following example in which only six binary positions are used, although it is to be understood that the operation applies to 36 positions: The Indicator Register has the number 101001 in positions 31 through 35 and the Storage Register has the number 001000 in positions 30 through 35. Since there is only one 1 in the Storage Register in position 32 only the Indicator position 32 will be examined. As previously described the contents of the Storage Register is complemented which gives the number 110111, and then the contents of the Indicator and the Storage Register complemented are ORed together in the Storage Register which gives the number 111111 which are then placed in the Adder. A one is added into position 35 which causes a carry to ripple from position 35 on through the higher order positions.

Assuming that the contents of Storage Register contain "zeros" in positions S, 1 through 29 that corresponding positions of the Indicator Trigger Register are "zero" then the one ripples into the Q position of the Adder. In FIGURE 39, the Skip Control line 39.07 goes to Compare Accumulator with Storage, FIGURE 149, and the output from Adder line 6a.01 is combined with Test Indicators lines at A6(D1) to Compare Skip Control and the Indicator Test line comes up. The Compare Skip Control and Indicator Test line goes to Advance Instruction Counter, FIGURE 107 where at ER6(D1) it causes an output Advance Instruction Counter to provide an output on Instruction Counter 17 binary input on the line 107.03. The signal on the line 107.03 Instruction Counter advances the counter by "one." Since the position tested had a one, the calculator skips the next instruction and proceeds. This is accomplished since this one added to the Instruction Register is in addition to the one which is added normally. Therefore, the next instruction in sequence is skipped. End Operation and Go to I Time is provided in FIGURE 128.

#### OFF TEST FOR INDICATORS (OFT + 0444)

For each bit of the contents of the location in Storage specified by the OFT instruction containing a "one," a corresponding position of the Sense Indicator Register positions 0 through 35 is examined. If all of the examined positions are "zero," the calculator skips the next instruction and proceeds from there. If all of the examined positions are not "zeros," the calculator takes the next instruction in sequence. The contents of the location specified in storage, and the contents of the Sense Indicators are unchanged. Consider the example wherein positions 30 through 35 of the Storage Register contain the binary number 010010 and all other positions of the Storage Register are 0. Positions 30 through 35 of the Indicator Register contain the binary number 101101 and all other positions of the Register are 0. The complement of positions 30 through 35 of the Storage Register is 101101 and the complement of the positions 30 through 35 of the Indicator Register is 010010. If these two numbers are Ored together, the sum is all ones. Since positions 31 and 34 of the Storage Register contain ones, and these same positions are examined in the Indicator Register, both being zero, then conditions are satisfied for a skip and a one is entered into positions 35 of the Adder to get a carry into position Q of the Adder. The difference between the ONT + 446 instruction and the Off Test for Indicators +0444 is that in the latter operation code, Instruction Register position 8 is not one. In FIGURE 14d the Primary Operation (4, 4) Indicator instruction line is up, providing outputs on the lines 14d.07 through 14d.12. In the Secondary Operation Decoder, FIGURE 15a, the line Minus on Instruction Register 9 is up, the line Minus on Instruction Register 6 is up, the line Minus on Instruction Register 7 is up, and the line Minus on Instruction Register 8 is up to provide an output on the Secondary Operation (0, 4) line 15a.03 to Secondary Operation Decoder, FIGURE 15d, to bring up the lines 15b.07 and 15b.08. Positions 21 through 35 of the Storage Register are placed in positions 3 through 17 of the Adders by way of Controls of FIGURE 86a at I9 and the contents of positions 3 through 17 of the Adder are gated through the Address Switches by way of the controls of FIGURE 110. The Instruction Counter is advanced in the normal manner by way of Circuits of FIGURE 107. The word in the location specified by the Address in the Off Test for Indicators is placed in the Storage Bus, and at E7 the Storage bus to Storage Register controls of FIGURE 53a cause the contents of the Storage Busses to be placed in the Storage Register. In FIGURE 39, Primary Operation (4, 4) line, Instruction Register 7 line, and Minus on Instruction Register 9 line, are up and bring up the Test Indicator line 39.02. In FIGURE 48, Test Indicators Storage line and E time line

122n.19 combine to turn ON T2. The line 48.07 goes to FIGURE 39 where it is combined with Test Indicators line 39.02 ER time and T2 ON to bring up the lines 39.08 through 39.13. The Storage Register to Adder line 39.09 goes to FIGURE 54b to cause the contents of the Storage Register to be placed in the Adders. The line 39.11 Accumulator to Storage Bus goes to FIGURE 72b to place the contents of the Accumulator Register on the Storage Bus. The line 39.08 causes the contents of the Storage Bus to be placed in the Storage Register. The line 39.10 causes the contents of the Adder to be placed in the Accumulator. The result of this operation is that the word brought from Storage from the location specified by this instruction is now in the Accumulators. The line 39.12 Complement Accumulators to Adders comes up at ER6(D2) and the word brought from Storage in response to the Off Test Indicators instructions has now been complemented. The line 39.10 causes the contents of the Adders to be placed in the Accumulator, FIGURE 57b. In FIGURE 39, at A10(D2) the line 39.16 Accumulator to Storage Bus comes up to place the complemented Accumulator contents on the Storage Bus. Storage Register to Adder line 39.14 goes to FIGURE 54b to place the contents of the Storage Register in the Adder, and the line 39.10 goes to FIGURE 57b to cause the contents of the Adders to be placed in the Accumulator. In FIGURE 48, Test Indicators to Storage line is combined with ER11(D1) to turn Off T2 which signifies the end of the first ER cycle. The line 48.02 goes to Test Indicators, FIGURE 39, where it is combined with ER time and Test Indicators line 39.02 to bring up the lines 39.03 through 39.07. The line 39.04 goes to Complement Indicators Storage Register, FIGURE 97, where it is combined with ER0(D4) and Minus on Instruction Register 8 line to bring up the lines 97.01 through 97.04 to cause the complement of the information stored in the Indicators to be placed in the Storage Register. It is pointed out at this time that Minus on Instruction Register 8 line is up in this instance whereas in the On Test for Indicators this line is down. The hold on the Storage Registers is now dropped since it is desired to OR the contents of the Storage Register and the complement of the Indicators. The line 39.05 goes to Carry to Adder position 35, FIGURE 56, to cause a carry into that Adder position. The Carry ripples through all positions of the Adder into position Q. The line 39.07 goes to Compare Accumulator with Storage, FIGURE 149, where it is combined with Adder Q Sum Output which is up at A6(D1) to bring up the lines 149.03 and 149.04. The line 149.03 goes to Advance Instruction Counter Controls, FIGURE 107, where it is effective to advance Instruction Counter by one more than is usual in the ordinary operation, and this causes one instruction to be skipped. The line 39.06 goes to End Operation Controls to cause an end operation in the usual manner.

#### LEFT HALF INDICATORS OFF TEST (LFT - 0054)

The status of each position of the Sense Indicator Register positions 0 through 17 of which there is a "one" in the corresponding position of the Field F of this instruction is examined. Indicators for which there is "zero" in the corresponding position of the Field F of this instruction are examined and the contents of the Sense Indicators positions 18 through 35 are not examined. If all of the examined Sense Indicator positions are not "zeros," the calculator takes the next instruction in sequence. If all are "zeros," the calculator skips the next instruction and proceeds from there. The contents of the Sense Indicators in the Field F are unchanged. This instruction takes an Instruction cycle and three ER cycles. The Instruction cycle and the first ER cycle are the same as the Reset Indicators of Left Half (RIL - 0057) except that the Indicators are not reset during the next Instruction cycle. The second and third ER cycles of the Left

Half Indicators Off Test Instruction are the same as the two ER cycles of the Off Test for Indicators (OFT + 0444). These steps are provided by the Test Indicators Storage Half Test Indicators, FIGURE 39, and the Half Indicator Register Controls of FIGURE 42.

#### LEFT HALF INDICATORS ON TEST (LNT - 0056)

The status of each position of the Sense Indicator Register positions 18 through 35 for which there is a "one" in the corresponding positions of Field F of this instruction is examined. Indicators for which there is a "zero" in the corresponding position of the Field F of this instruction and the contents of the Sense Indicators positions 0 through 17 are not examined. If all the examined Sense Indicator positions are not "ones," the calculator takes the next instruction in sequence. If all are "ones," the calculator skips the next instruction and proceeds from there. The contents of the Sense Indicators Register and the Field F are unchanged. This instruction takes an I cycle and three ER cycles. The I cycle and the first ER cycle are the same as the Reset Indicators of Left Half (RIL - 0057) except that the Indicators are not reset during the next Instruction cycle. The second and third ER cycles of this instruction are the same as the On Test for Indicators (ONT + 0446) which takes only two ER cycles.

#### RIGHT HALF INDICATORS ON TEST (RNT + 0056)

The status of each Sense Indicator position 0 through 17 for which there is a "one" in the corresponding position of the Field F of this instruction is examined. Indicators for which there is a "zero" in the corresponding positions of the Field F and the contents of Sense Indicators positions 18 through 35 are not examined. If all of the examined Sense Indicator positions are not "ones," the calculator takes the next instruction in sequence. If all are "ones," the calculator skips the next instruction and proceeds from there. The contents of the Sense Indicator Register are not changed. The instruction cycle and the first ER cycle are the same as the Reset Indicators of Right Half (RIR + 0057) except that the Indicators are not reset during the next Instruction cycle. The second and third ER cycles of this instruction are the same as On Test for Indicators (ONT + 0446). The latter instruction taking only two ER cycles.

#### OR STORAGE TO INDICATORS (OSI + 0442)

Each bit of the contents of the location specified by the Address in the OSI instruction is matched with the contents of the Sense Indicator Register positions 0 through 35. When the corresponding position of either the Accumulator or the Sense Indicator is a "one," a "one" replaces the contents of that position in the Sense Indicator. The execution of this instruction takes an I cycle and one Execute cycle. During the latter part of the Instruction cycle the operation is decoded at E7(D1). The contents of the Storage Bus, which is the contents of the location in Storage specified by the Address part of the OSI instruction, are sent to the Storage Register by way of Storage Bus to Storage Register, FIGURE 53a, Minus on AND to Storage Control line 30.10, Minus on Transfer Trapping Mode line 110.03, and E7(D1). In FIGURE 94, Set Indicators, the lines Primary Operation (4, 4) Minus on Instruction Register 7 and Instruction Register 8, and E9 until CT2 which brings up the Set Indicator line 94.01 to the Indicator Trigger Registers, FIGURE 10, Storage Register AND outputs and Set Indicators turn ON the trigger of corresponding positions for each position of the Storage Register containing a "one." The effect of this then is to OR the contents of the location at the Address specified in the instruction with the contents of the Indicator Trigger Register.

#### PLACE INDICATORS IN ACCUMULATOR (PIA - 0046)

The contents of the Sense Indicator Register replaces the contents of positions P, 1 through 35 of the Accumulator and the contents of positions S and Q are cleared. The contents of the Sense Indicator Register is unchanged. This instruction takes an Instruction cycle and an ER cycle. The Instruction is decoded at 19.5 for the Instruction Cycle and at I0(D4) the contents of the Indicators is placed on the Storage bus by way of Place Indicators in Accumulator, FIGURE 41. In FIGURE 41, the Primary Operation (0, 4) line, Instruction Register Sign Minus line, Minus on Instruction Register 6 line, Instruction Register 7 line, and Minus on Instruction Register 9 line are up to bring up the lines 41.01 through 41.05. The line 41.02 goes to Indicators to Storage Bus, FIGURE 96, where it is combined with I0(D4) to bring up the lines 96.01 through 96.03 which go to Storage Bus Switching, FIGURE 11, to gate the contents of the Indicators onto the Storage Bus. The line 41.01 goes to Storage Bus to Storage Register FIGURE 53b, where it brings up the line 53b.02 to Storage Bus to Storage Register, FIGURE 53a, to bring up the lines 53a.01 through 53a.08 and thereby enter the contents of the Storage Buses and the Storage Register. The line 41.03 goes to Storage Register to Adders, FIGURE 54b, to place the contents of Storage Register in the Adders. In Ones to Adder positions Q, P, 1 through 8, FIGURE 81, a "one" is caused to be entered to Adder position P. The line 41.04 goes to Adders to Accumulator Control, FIGURE 70, where at I5(D1) the contents of the Adders are placed in the accumulator.

#### RIGHT HALF INDICATOR OFF TEST (RFT + 0054)

For each bit in positions 18 through 35 of this instruction containing a "one," a corresponding position of the Sense Indicator Register 18 through 35 is examined. If all of the examined positions contain "zero," the calculator skips the next instruction and proceeds from there. If any of the examined positions do not contain a "zero," the calculator takes the next instruction in sequence. The contents of the Sense Indicator Register and the contents of positions 18 through 35 of the Instruction are unchanged. This instruction takes an Instruction cycle and three ER cycles. The Instruction cycle and the first ER cycle are the same as the Reset Indicators of Right Half (RIR + 0057) except that the Indicators are not reset during the next Instruction cycle. The second and third ER cycles are the same as the two ER cycles of the Off Test Indicator Instruction +0444. The steps are provided by way of the Half Indicator Register Controls of FIGURE 42.

#### RESET INDICATORS FROM ACCUMULATOR (RIA - 0048)

The Accumulator contains word B and the Sense Indicator Register contains word A. When the bit in an order of the Accumulator is a "one," a "zero" replaces the contents of the corresponding order in the Sense Indicator Register. When the bit in an order of the Accumulator is "zero," the contents of the corresponding order of the Sense Indicator is unchanged. This Instruction takes an Instruction cycle and an ER cycle. The instruction is decoded at 19.5 of the Instruction cycle. At I0(D4), the contents of the Accumulator are placed in the Storage Buses. In Place Indicators and Accumulator and Reset Indicators from Accumulator, FIGURE 41, the Primary Operations (0, 4) Minus on Instruction Register 6, Minus on Instruction Register 7, and Instruction Register Sign Minus lines are up to bring up the lines 41.06 through 41.08. The line 41.07 goes to Accumulator to Storage Bus, FIGURE 72b, to bring up the Accumulator to Storage Bus line 72b.01 to Accumulator to Storage Bus, FIGURE 72a. This line brings up the lines 72.01

through 72a.05 which gate the contents of the Accumulator onto the Storage Buses. The line 41.06 Storage Bus to Storage Register goes to Storage Bus to Storage Register Controls of FIGURE 53 to put the contents of the Storage Buses into the Storage Register at ER3(D1). The line 41.08 goes to Reset Indicators, FIGURE 93, where it is combined with I4(D2) to bring up the Reset Indicators line 93.01 which goes to Indicator Trigger Register, FIGURE 10, to gate the Storage Register outputs into the Trigger Register. For each position of the Storage Register containing a "one," a corresponding "one" in the Indicator Trigger Register is turned OFF. For those positions of the Storage Register having "zeros," corresponding triggers in the Sense Indicator Register are not affected.

#### RESET INDICATORS OF RIGHT HALF (RIR + 0057)

This instruction takes an Instruction cycle and ER cycle. The operation is decoded from I9.5 until 18 of the following I cycle. The Primary Operation code is (0, 4), Instruction Register is plus, and Instruction Register lines 6, 7, 8 and 9 are up. Each bit of positions 18 through 35 of this instruction is matched with a corresponding bit of the contents of the Sense Indicator positions 18 through 35. When the bit in positions 18 through 35 of the Instruction is a "one," a "zero" replaces the contents of that position in the Sense Indicator Register. When the bit in positions 18 through 35 of the Instruction is a "zero," the contents of that position in the Sense Indicator Register is unchanged. The contents of the Sense Indicator positions 0 through 17 and positions 18 through 35 of the Instruction are unchanged.

In Half Indicator Register Controls, FIGURE 42, Primary Operation (0, 4) line, Instruction Register 6 line, and Test Indicator Off Half Control line 39.01 are up, and the line 42.02 goes to Storage Register to Adder where it is combined with Instruction Register Sign Plus to bring up Storage Register to Adder lines. The line 42.03 goes to Accumulator to Storage Bus, FIGURE 72a, to cause the contents of the Accumulator to be placed on the Storage Bus at ER4 to ER6. The line 42.05 goes to Storage Bus to Storage Register, FIGURE 53, and at ER5(D1) the contents of the Storage Buses are placed in the Storage Register. In FIGURE 42, at ER5(D1) the line 42.20 is up to Adder to Accumulator controls, FIGURE 57. The line 42.06 goes to Indexing controls, FIGURE 90, where the Drop Hold Tag line is brought up from ER3 through ER7. In Half Indicator Register Controls, the line 42.03 goes to Accumulator to Storage Bus where it is combined with ER10(D2) to bring up the line 72b.01 which places the contents of Accumulator on the Storage Bus. The line 42.19 goes to Storage Bus to Storage Register Controls, FIGURE 53a, where it is combined with Instruction Register Sign Plus to bring up the Storage Bus positions 18 through 35 to Storage Register positions 18 through 35 lines 57a.06 through 57a.08. In FIGURE 41, the line 41.08 goes to Indicator Trigger Register, FIGURE 10, where it gates the outputs of the Storage Register to the Triggers. For each Storage Register an output containing a "one," the trigger is turned OFF if it is ON. For those positions of the Storage Register containing "zeros," the corresponding trigger is not affected.

#### RESET INDICATORS FROM STORAGE (RIS + 0445)

A word B is located in Storage at the address specified by the Instruction. A word A is in the Sense Indicator Register. Each order of the word B is matched by the corresponding order of the Sense Indicators. If the corresponding order of the word B is "zero," the contents of that order in the Sense Indicator Register is unchanged. If the bit in the order of word B is a "one," "zero" replaces the contents of the corresponding order in the Sense Indicators. The execution of this instruction takes

an Instruction cycle and an Execute cycle. During the Execute cycle the word is brought from Storage at ER7(D1) and the location specified in Address portion of the RIS Instruction by way of controls of FIGURE 53, Storage Bus to Storage Register. In FIGURE 41 in Reset Indicators, FIGURE 93, Primary Operation (4, 4) line is up, Instruction Register 7 line is up, Instruction Register 9 line is up and I0(D4) and A2(D6) lines combine to bring up the Reset Indicators line 93.01 which goes to Indicator Trigger Register, FIGURE 10, where the outputs of the Storage Register are used to reset the Indicators.

#### SET INDICATORS OF LEFT HALF (SIL - 0055)

This is a type B instruction with a Field F in positions 18 through 35. Each bit contained in the Field F is matched with the contents of positions 0 through 17 of the Sense Indicator Register. When the corresponding order of either the Field F or Sense Indicator Field is a "one," a "one" replaces the contents of that order in the Sense Indicator Register. If neither is a "one," a "zero" replaces the contents of the position in the Sense Indicator. In FIGURE 86b, Storage Register positions 18 through 35 to Adder positions P through 17, ER4(D2) line 42.15 is up, the Instruction Register Sign is Minus and an output is provided on the line 86b.01 to Storage Register positions 18 through 35 to Adder positions P through 17, FIGURE 86, to bring up the lines 86a.01 through 86a.12 to Storage Register positions 18 through 35 Adder positions P through 17 to place the Field F in Storage Register positions P through 17 of the Adder. In Accumulator to Storage Bus, FIGURE 72b, Half Indicator ER4(D2) line 42.14 is up to bring up the line 52b.01 to cause the contents of the Accumulator to be placed in the Storage Buses. The line 42.19 goes to Storage Bus to Storage Register, FIGURE 53a, to cause the contents of the Storage Bus to be entered into the Storage Register. The line 42.20 goes to Adder to Accumulator Control, FIGURE 57b, to cause the contents of the Adder to be placed in the Accumulator. The line 42.03 goes to Accumulator to Storage Buses, FIGURE 72b, where it is combined with ER10(D2) to bring up the Accumulator to Storage Bus line 72b.01 which goes to Accumulator to Storage Bus, FIGURE 72a, to cause the contents of the Accumulator to be entered on the Storage Buses. The line 42.19 goes to Storage Bus to Storage Register Controls, FIGURE 53a, to cause the contents of the Storage Buses to be placed in the Storage Register. The line 42.02 goes to Storage Register to Adder Controls, FIGURE 54b, to place the contents of the Storage Register in the Adders. The line 42.20 goes to Adder to Accumulator, FIGURE 57b, to cause the contents of the Adders to be entered into the Accumulator at ER11(D1). The line 42.04 goes to End Operation and go to I Time, FIGURE 128. In Set Indicators Controls, FIGURE 98, Half Indicator Controls line is up, Minus on Instruction Register 8 line is up, Instruction Register 9 line is up, Instruction Register 7 line is up, and the combination of I0(D4) and A2(D6) lines brings up the Set Indicators line 94.01 which goes to Indicator Trigger Register FIGURE 10 and gates the output of the Storage Register into the Indicator Trigger Register, FIGURE 10. The line 42.06 goes to Indexing Controls, FIGURE 90b, to Drop Hold Tag bits on the line 90b.01 from ER3 through ER7.

#### SET INDICATORS OF RIGHT HALF (SIR + 0055)

Each bit of the Field F in this instruction is matched with the contents of the Sense Indicator positions 18 through 35 when the corresponding position of either the Field F or the Sense Indicator position is a "one," a "one" replaces the contents of that position in the Sense Indicator. If neither is a "one," a "zero" replaces the contents of that position in the Sense Indicator. This instruction operates in the same manner as the Set Indicators of Left Half with the exception that Storage Register positions S through 35 are transferred to the Adder,

whereas in Set Indicators of Left Half Storage Register positions 18 through 35 are transferred to the positions P through 17. With reference to Storage Register to Adders, FIGURE 54b, Half Indicator ER4(D2) line 42.13 is up and Instruction Register sign is Plus so the line 54b.01 is up to cause the contents of the Storage Register to be entered into the Adders. The remaining portion of operation is performed in the manner illustrated in connection with Set Indicators of Left Half Instruction.

#### STORE INDICATORS (STI + 0604)

In this Instruction the contents of the Sense Indicator Register replace the contents of the location in Storage specified by the Address part of this instruction, and the contents of the Sense Indicator is unchanged. The Address portion of this instruction is entered into Address positions P through 17 and is gated through the Address Switches to Storage Address Register in the manner previously described in connection with Magnetic Core Storage organization. The contents of the Indicator or Trigger Register is placed on the Storage Buses where it entered Storage Buffer Register and, in turn, is stored in the Core Array in the location specified by the Address. With reference to Indicators to Storage Bus, FIGURE 96, Primary Operation (6, 0) line is up, Instruction Register 7 line is up, E time line is up to provide outputs on the lines 96.01 through 96.03 which causes the contents of the Indicators to be placed on the Storage Bus and read into the Storage Buffer Register as previously explained.

#### OR ACCUMULATOR TO INDICATOR (OAI + 0043)

Each bit of positions P, 1 through 35 of the Accumulator is matched with the corresponding bit in the Sense Indicator Register positions 0 through 35. When the corresponding bit of either the Accumulator or the Sense Indicator is a "one," a "one" replaces the contents of that position in the Sense Indicator. When the corresponding bit of both the Accumulator and the Sense Indicator is a "zero," a "zero" replaces the contents of that position in the Sense Indicator. The contents of the Accumulator are not changed. The execution of this instruction takes an Instruction cycle and an ER cycle. The instruction is decoded at I9.5 until I8 time in the following Instruction cycle. The contents of the Accumulator are placed in the Storage Buses at I0(D4) by way of OR Accumulator to Indicators, FIGURE 44. Primary Operations (0, 4) line is up, Minus on Instruction Register 7 is up, Instruction Register 8 is up, and Instruction Register 9 is up to provide outputs on the lines 44.11 through 44.14. The line 44.13 goes to Accumulator to Storage Bus, FIGURE 72b, to bring up the line 72b.01. The line 72b.01 goes to FIGURE 72a to cause the contents of the Accumulator to be placed on the Storage Buses and the line 44.12 goes to End Operation Controls, FIGURE 128. The line 44.11 goes to Storage Bus to Storage Register Controls to cause the contents of the Accumulator on the Storage Buses to be entered into the Storage Register. The line 44.14 goes to Set Indicators Controls, FIGURE 94, where it is combined with an I4(D2) pulse to bring up the Set Indicators line 94.01. The line 94.01 goes to Indicator Trigger Register, FIGURE 10, where it gates the Storage Register outputs into the Indicator Triggers. Since this input is to be on the ON side of the Trigger, those Storage Register positions containing a "zero" are ineffective to turn ON the trigger. This effectively accomplishes an OR operation.

#### TRANSFER WITH INDICATORS ON (TIO + 0042)

The status of each Sense Indicator for which there is a "one" in the corresponding position of the Accumulator is examined. Indicators for which there is a "zero" in the corresponding position of the Accumulator are not examined. If all of the examined Sense Indicator positions contain a "one" the calculator takes the next Instruc-

tion from Location specified by the address part of the Instruction and proceeds from there. If all are not "ones," the calculator proceeds to the next instruction in sequence. The contents of the Accumulator and the contents of the Sense Indicator are unchanged. This instruction is performed by ORing the complement of the Accumulator with the Indicators. Assume that positions 30 through 35 of the Accumulator Register contain 010101 and all other positions contain "zero" and that the contents of the Sense Indicators Register positions 30 through 35 contain 110111 and all other positions contain "0." According to the Instruction, the Sense Indicator positions 31, 33 and 35 are examined since positions 31, 33 and 35 of the Accumulator contain "ones." If all of the positions examined in the Sense Indicator Register are "ones," a transfer results in which the calculator goes to the location in Storage specified by the Address portion of this instruction, and takes its instruction from that position. Therefore, if positions 30 through 35 of the Accumulator are complemented and then ORed with the contents of the Sense Indicators Register it is apparent that the sum is all "ones." A "one" is entered into position 35 and causes a carry to ripple through to position Q.

This instruction takes an Instruction cycle and two ER cycles. The instruction is decoded from I9.5 until I8 and Transfer Indicators Accumulator, FIGURE 40, Primary Operation (0, 4) line 14c.12 is up, Instruction Register Sign Plus line 100.22 is up, Minus on Instruction Register 6 line 13b.06, Instruction Register 8 line 13c.27 and Minus on Instruction Register 9 lines are up to bring up the line 40.01 to turn ON T2 in FIGURE 48. When T2 comes ON the lines 40.02 through 40.09 are up. In FIGURE 55d, Complement Accumulator to Adders, the line 40.08 combines with ER4(D2) to bring up the Complement Accumulator to Adder line 55b.01 which causes the Complement of the Accumulator to be entered into the adder. The line 40.07 goes to Adder to Accumulator, FIGURE 57b, to bring up the line Adder to Accumulator 57b.01. In Accumulator to Storage Bus, FIGURE 72b, Transfer Indicator to Accumulators and ER6(D4) lines are up to bring up the Accumulator to Storage Bus line 72b.01. The line 40.05 goes to Storage Bus to Storage Register, FIGURE 53b, where are ER9(D1) it brings up the Storage Bus to Storage Register line 53b.02. In Indicators to Storage Bus, FIGURE 96, Transfer Indicators, ER6(D4), and Minus on Instruction Register 7 are up to bring up the Indicator to Storage Bus lines 96.01 through 96.03. This places both the contents of the Accumulator and the contents of the Indicators on the Storage Buses and at ER9(D1) the contents of the Storage Buses are placed in the Storage Register by way of Transfer Indicators to Accumulator in ER9(D1) as previously explained. T2 is turned OFF by the fall of the ER11(D1) line and the contents of Storage Register are placed in the Adders in FIGURE 54b by the Transfer Indicators to Accumulator second step line 40.09. The line 40.10 goes to Carry to Adder 35, FIGURE 56. If the test is successful as explained in the example and a Carry ripples through into position Q of the Adder in Compare Accumulator with Storage Controls, FIGURE 149, then the calculator goes to the location in storage specified by the Address in the instruction.

#### TRANSFER WHEN INDICATORS OFF (TIF + 0042)

For each bit of the contents of the Accumulator Register positions P, 1 through 35 containing a "one," the corresponding position of the Sense Indicator Register position 0 through 35 is examined. If all of the examined positions contain "zero," the calculator takes the next instruction from location specified by the Address portion of the instruction and proceeds from there. If any of the examined bits do not contain a "zero," the calculator proceeds to the next instruction in sequence. The contents of the Accumulator and the contents of the Sense Indicator Register are unchanged. Assume for the

purposes of illustration that the contents of the Accumulator positions 30 through 35 are 001100. The contents of the Indicator Register positions 010001 and all other positions of both the Accumulator Register and the Indicator Register are 0. In this instance, positions 32 and 33 of the Indicator Register are examined since positions 32 and 33 of the Accumulator contain "ones." Since positions 32 and 33 of the Indicator Register contain "zeros" then the calculator takes the next instruction from the location specified by the Address and the transfer with indicators OFF instruction. By complementing the contents of the indicator and ORing the same, a sum is provided of all "ones." Then, by providing a "one" into position 35, a Carry ripples through to position Q of the Adder where it is tested and the transfer operation is performed. The contents of the Accumulator are complemented in the manner previously described with reference to the Transfer of Indicators On. In this instance, the Complement Indicators to Storage Register must be provided. With reference to Complement Indicators to Storage Register, FIGURE 97, Transfer Indicators to Accumulator First Step line is up, Instruction Register 7 line is up at ER9(D1) and Complement Indicators to Storage Register lines 97.01 through 97.04 are up. These lines gates the Complement of the Indicator into the Storage Register where the Complement of the Accumulator is now entered. The result is that the Complement of the contents of the Indicator and the Complement of the contents of the Accumulator are ORed together in the Storage Register. The tests are performed in the same manner as the transfer of Indicator On was performed.

#### DEFINITIONS OF SYMBOLS

A<sub>1</sub> MEG, A<sub>C</sub>, A AND are AND circuits; A<sub>S</sub> is a Slow Amplifier; —AND and —A are OR circuits; A<sub>D</sub> is a Drum Amplifier; A<sub>CS</sub> is a Sense Amplifier; and ATA is a Read Preamplifier.

CF is a cathode follower; CF (infinite), CF<sub>OR</sub><sup>R</sup>, CF<sub>OR</sub> (infinite), CF<sub>OR</sub> are cathode follower OR circuits; CF<sub>T</sub> is a tapped cathode follower; CF<sub>ER</sub> is a cathode follower used for the electronic reset of triggers; CF<sub>M</sub>, CF<sub>OR</sub> (R) are cathode follower OR circuits having the cathode clamped so as not to go below ground; CF<sub>T</sub> is a cathode follower with tapped load for reduced output; CG<sub>M</sub> is a Clamp Generator; and CPA is a Clamp Power Amplifier.

D is a Microsecond Delay Unit; DG is a Diode Gate; DL is a Delay Line, DPQ is a Digit Plane Amplifier; DPD is a Digit Plane Driver, and DL<sub>B</sub> is Delay Line. GA and GAF are Grounded Grid Amplifiers.

K and K<sub>FP</sub> are Cathode Followers; K<sub>RA</sub> and K<sub>RA</sub> are Reset Cathode Followers; K<sub>O</sub> is a Power Cathode Follower OR; K<sub>C</sub> is Power Cathode Follower with very small load resistor suitable for low duty cycle use; K<sub>O</sub> is Cathode Follower OR; K<sub>J</sub> is a Power Cathode Followers; and K<sub>JO</sub> is a Power Cathode Follower OR.

MV is a Multivibrator; MSAW is a Matrix Switch Amplifier, Write; MSAR is a Matrix Switch Amplifier, Read; and MSD is a Matrix Switch Driver.

O, O<sub>1</sub> MEG and OR are OR circuits; O<sub>C</sub> is a cascaded OR circuit; —OR is an AND; and OSC is a Master Oscillator. R is a Relay Driver (essentially an inverter with a relay coil as a plate load).

SS<sub>F</sub> is a Single Shot (fast recovery); ST is a Switch Timer; SS<sub>E</sub> is a Single Shot (fast recovery); SS<sub>H</sub> is a Single Shot (holdover); SS<sub>D</sub> is a Single Shot (short duration); SR is a Switch Read; SG is a Sync Generator; SC is a Sync Clipper; and SPA is a Sync Power Amplifier.

T is a High Speed Trigger; T<sub>WR</sub> is a Write Trigger; T<sub>KX</sub> is a Key Trigger with reset (X denotes reset); T<sub>K</sub> is a Key Trigger; T<sub>T</sub>, T<sub>U</sub>, T<sub>V</sub>, T<sub>W</sub>, T<sub>Y</sub>, T<sub>XA</sub> and T<sub>XB</sub> are Triggers where the subscripts denote different resets; TH is Thyatron; T<sub>A</sub> is a Trigger with particular output dividers; T<sub>S</sub> is a slow Triggers; T<sub>AXA</sub>, T<sub>AXB</sub>, T<sub>AZ</sub>, T<sub>AW</sub>, T<sub>W</sub>, and T<sub>C</sub> are Slow Triggers having various output

dividers; T<sub>KA</sub> is a Key Trigger and T<sub>B</sub> is a Schmitt Trigger.

WD is a Write Driver.  $\times T_{KA}$  and  $\times T$  are Key Triggers reset off;  $\times T_D$  is a Key Trigger with a large crossover capacitance; and xtal is a crystal.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the invention therefore, to be limited only as indicated by the following claim.

What is claimed is:

In a data processing system operable to act upon data manifestations in response to a program of instruction manifestations, the manifestations representative of each instruction including an operations part and address part; apparatus for performing a logical comparison, test and branch in response to manifestations representative of a Test Indicators instruction, including: storage means having addressable locations for storing as states manifestations representative of instructions and data; addressing means for obtaining access to specified locations in said storage; sequential program means for indicating as states the address of a Test Indicators instruction; means for transferring manifestations representative of said Test Indicators instruction states from said program means to said addressing means, for causing said storage means to emit signals representative of said Test Indicators instruction; decoding means for receiving said emitted signals representative of said operations part of said Test Indicators instruction and emitting output signals in accordance with said operations part; routing means for generating routing signals in accordance with said decoding means output signals; first means controlled by said routing signals for transferring said emitted signals representative of said address part of said Test Indicators instruction to said addressing means, for causing said storage means to emit signals representative of masking data; a storage register having a plurality of orders; an accumulator register having a plurality of orders; an adder having a plurality of orders; second means controlled by said routing signals interconnecting said storage register, accumulator register and adder in a manner to permit orders of data manifestations stored as states in said storage register to be summed in said adder with corresponding orders of data manifestations stored as states in said accumulator, the sum being stored as states in said accumulator register; third means controlled by said routing signals for complementing the data manifestations stored as states in said accumulator before said summation commences; an indicator register having a plurality of orders, each order comprising a bistable device having a true output for indicating the state stored therein, a complement output for indicating the complement of the state stored therein; a set input for causing said bistable device to assume a one state, a reset input for causing said bistable device to assume a zero state and a binary input for causing said device to assume an opposite state; fourth means controlled by said routing signals for selectively transferring signals representative of said indicator register true and complement states from selected ones of said bistable devices true and complement outputs to said storage register; fifth means controlled by said routing signals for entering signals representative of data to be tested into said indicator register; sixth means controlled by said routing signals for storing as states in said storage register said emitted signals representative of said masking data; seventh means controlled by said routing signals for entering signals representative of said storage register masking data representative states into said adder for transfer to said accumulator register as states;

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eighth means controlled by said routing signals for entering signals representative of said accumulator masking data representative states into said adder for the transfer of the complement back to said accumulator as states; ninth means controlled by said routing signals for entering as states into said storage register; signals representative of said indicator register test data representative states and signals representative of said accumulator register complemented masking data, said storage register combined states assuming a one condition for each order corresponding to a one signal from the corresponding order of either the indicator register or the accumulator register; tenth means controlled by said routing signals for making said seventh means operative to enter said storage register combined states into said adder and operative to cause a one to be simultaneously summed in said adder; eleventh means controlled by said routing signals and associated with said adder for generating an end carry signal if the combined states of the storage register entered into the adder are

all ones; twelfth means controlled by said routing signals operative by said end carry signal for causing said program means to indicate states representative of a non-sequential instruction address.

#### References Cited in the file of this patent

##### UNITED STATES PATENTS

|           |                       |               |
|-----------|-----------------------|---------------|
| 2,719,670 | Jacobs et al. -----   | Oct. 4, 1955  |
| 2,767,908 | Thomas -----          | Oct. 23, 1956 |
| 2,796,219 | Hill -----            | June 18, 1957 |
| 2,846,142 | Strachey et al. ----- | Aug. 5, 1958  |

##### FOREIGN PATENTS

|         |                     |              |
|---------|---------------------|--------------|
| 749,836 | Great Britain ----- | June 6, 1956 |
|---------|---------------------|--------------|

##### OTHER REFERENCES

E.R.A.—24-Digit Parallel Computer With Magnetic Drum Memory, PX 29136, Engineering Research Associates, Inc., St. Paul, Minn., 1949, pages 23 to 36.