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(54) Data packet switching

(57) A data packet switching arrangement wherein data packets are switched into a transmission pathway according to their priority. Data packet priority is consequently determined in a ring and a priority token attributed thereto. A high priority token ensures its data packet is switched into the transmission pathway when next available. Lower priority tokens are held by respective packets until all data packet priorities have been determined and no higher priority tokens attributed, whereupon the respective data packet is switched into the transmission pathway when next determined. Correctible errors include; more than one token of given priority in the ring; device error; and excessive time between tokens. The arrangement may function in a self-timed manner, or be timed in a bit multiplex manner, especially for multiple priority levels.

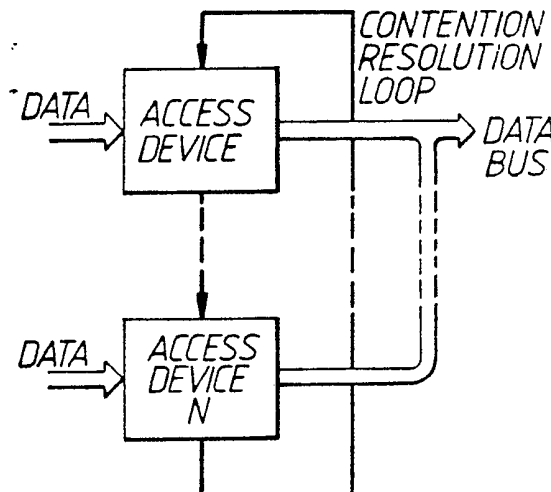


FIG. 1.

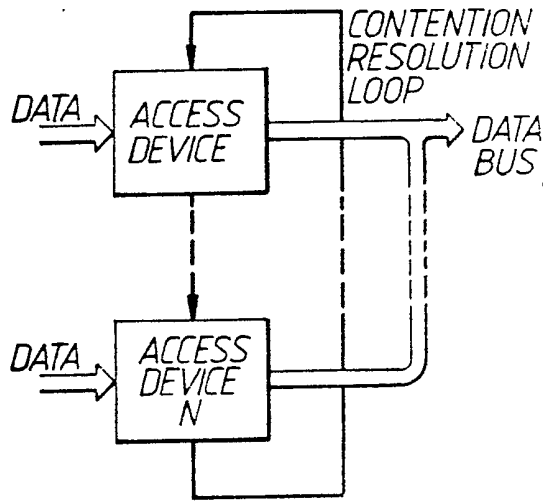


FIG. 1.

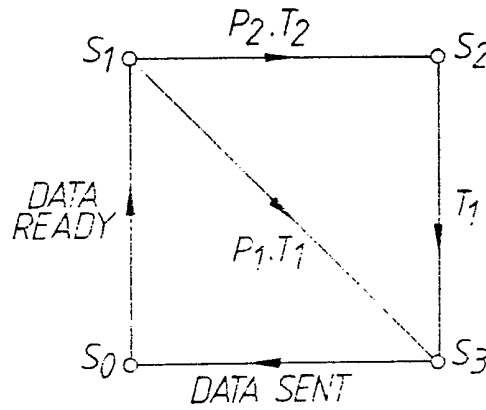


FIG. 2.

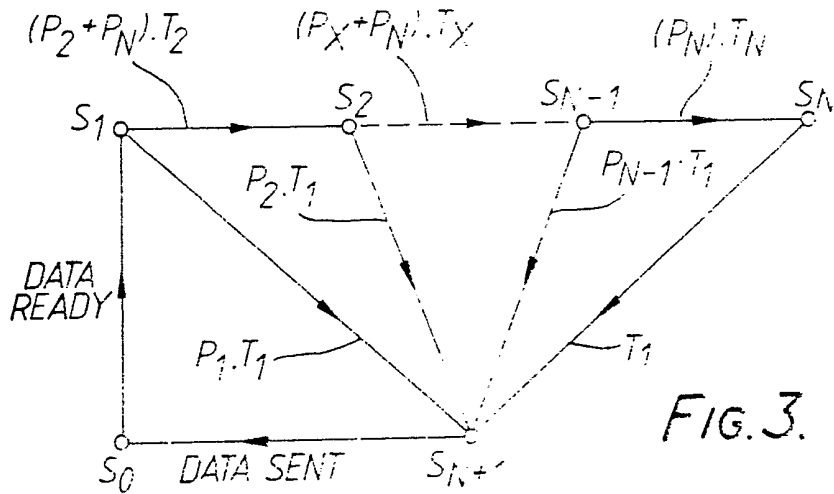


FIG. 3.

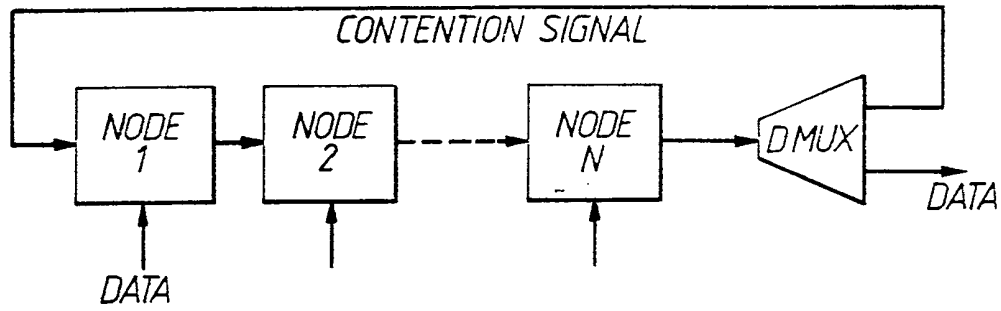


FIG. 4A.

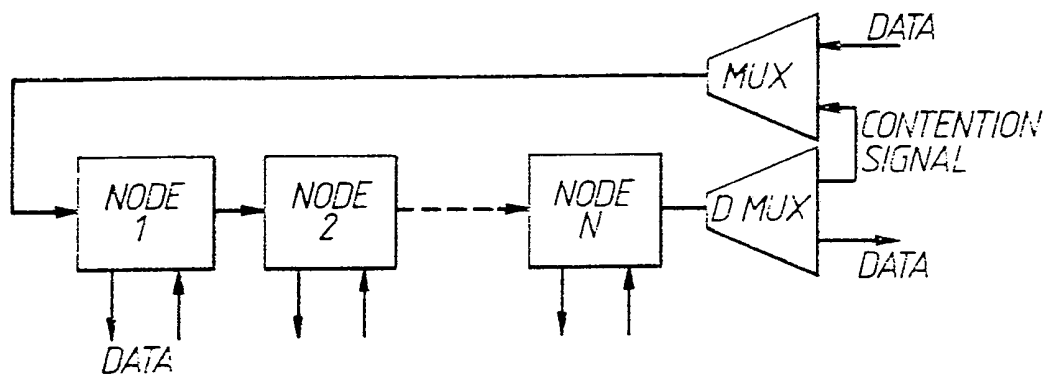


FIG. 4B.

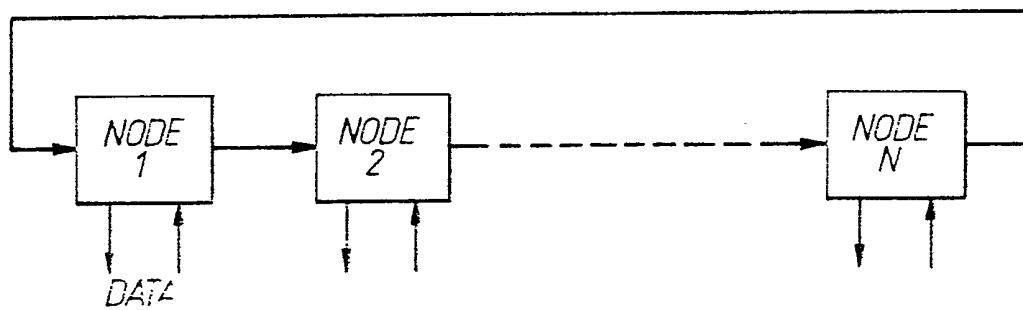


FIG. 5.

NOTE 1 IN THESE CASES THE DEVICE WILL RELEASE T1 AND T2 TOGETHER

PRIORITY (P) HIGH PRIORITY LOW PRIORITY	OLD STATE				TOKENS IN		NEW STATE				TOKENS OUT			
	P1 P2	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	T <sub>1</sub>	T <sub>2</sub>	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	T <sub>1</sub>		T <sub>2</sub>
2	✓					0	0	✓				0	0	
2	✓					0	1	✓				0	1	
2	✓					1	0	✓				1	0	
2	✓					1	1	✓				1	1	
2		✓				0	0		✓			0	0	
2		✓	✓			0	1		✓			0	1	
2		✓	✓			1	0			✓		1	0	
2		✓	✓	✓		0	0			✓	✓	0	0	ERROR 2
2			✓	✓		1	1			✓	✓	0	0	ERROR 2
2			✓	✓	✓	0	0			✓	✓	0	0	ERROR 2
2				✓	✓	1	0				✓	0	0	ERROR 1
2				✓	✓	1	1			✓	✓	1	1	ERROR 1, ERROR 2
1	✓					0	0	✓				0	0	
1	✓					0	1	✓				0	1	
1	✓					1	0	✓				1	0	
1		✓				0	0		✓			0	0	
1		✓	✓			0	1		✓			0	1	ERROR 3
1			✓			1	0			✓		0	0	ERROR 3
1			✓			1	1			✓	✓	0	0	ERROR 3
1				✓		0	0				✓	0	0	NOTE 1
1				✓		0	1				✓	0	0	NOTE 1
1				✓		1	0				✓	0	0	ERROR 1
1				✓		1	1				✓	0	0	ERROR 1, NOTE 1

ERROR 1 = DUPLICATE T1  
 2 = DUPLICATE T2  
 3 = FAULT IN DEVICE

S<sub>0</sub> = QUIESCENT  
 S<sub>1</sub> = READY  
 S<sub>2</sub> = STEADY  
 S<sub>3</sub> = GO

FIG. 6.

**POOR QUALITY**

## DATA PACKET SWITCHING

The present invention relates to data packet switching.

When a number of independent devices need to write to a common data bus it is necessary to provide means to equitably share the bus capacity between the devices. Devices having data to send on the bus will contend for access and the means for choosing which should gain access is referred to as contention resolution.

In many cases the group of devices having access to a bus will include some which have a higher priority of access and should have first choice in use of the bus. In some situations more than two levels of priority may be required in which case access should be ordered according to the priority levels.

Previous mechanisms have had contention resolution on the common transmission bus, i.e. one I/O port only per device which taps onto a common contention resolution path. This form of contention resolution must always suffer from a fixed order of priority (e.g. determined by the source address) or on an uncertainty (e.g. who gives up first or who has the faster clock). Ring (loop or 'daisy chain') contention resolution, where the devices are arranged in a ring about the bus, substantially removes the above defects. When the device has finished, the next device in the loop gets first chance and so on.

An example of such a mechanism is given in GB 1,250,352 (Suensha Handelsbonken).

It is an objective of the present invention to provide a data packet switching arrangement wherein a multitude of priority levels

for data packets can be attributed whereby device positional anomalies are substantially relieved and general transmission efficiency improved.

According to the present invention, there is provided a data packet switching arrangement for switching data packets into a transmission pathway including means arranged to determine data packet priority and to attach a priority token thereto, there being a single high priority token attachable to a data packet to ensure that packet is next to be switched into the transmission pathway, and lower priority tokens attachable to respective data packets in order and, there being no tokens of higher priority extent, are switched into the transmission pathway in said order, and upon a data packet being switched into the transmission pathway, its priority token is released.

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings, in which:-

Figure 1 illustrates an access device arrangement according to the present invention;

Figure 2 is a state diagram for the access device arrangement as shown in Figure 1 having two levels of priority for data packets;

Figure 3 is a state diagram for the access device arrangement as shown in Figure 1 having N levels of priority for data packets;

Figure 4a and 4b illustrates, in block diagram form, an access device arrangement in multiplexed operation with the transmission pathway being a transmit end of a communication link;

Figure 5 illustrates, in block diagram form, an access device arrangement in multiplexed operation with the transmission pathway being a unidirectional ring; and,

Figure 6 is a table of error conditions for an arrangement as shown in Figure 2.

Consider Figure 1. The mechanism for contention resolution is based upon a contention loop<sup>1</sup> passing through all the access devices. The loop carries  $N$  distinguishable tokens where  $N$  is the number of priority levels required. There is only one set of  $N$  tokens in the loop at any time and each of the tokens has a different significance. One or more tokens may be held temporarily by a device. The relationship between this action, the state of the device and the required priority of access will be described in terms of two priority levels of access.

A state diagram for contention resolution at a device is given in Figure 2 where there are two levels of priority. If we assume that the data input is broken into conveniently sized packets, the packets need not all be the same size but do need to have a maximum size in order to avoid one device holding the data bus unduly long and hence denying access from other devices. Possession of the right combination of priority tokens by a device conveys the authority to transmit one packet of data on the common data bus. A device may not hold a token if it does not already have data ready to transmit.

The quiescent state for a device contending port is  $S_0$ . In this state a device simply passes tokens received on to the next device in the contention resolution loop 1. When a complete packet of data has<sup>2</sup> been received, the device state changes to  $S_1$ . If the device or packet

has the higher priority ( $P_1$ ) then it will wait for and hold the higher priority token  $T_1$ , it can then transmit the packet and release the token  $T_1$ . In some system configurations where the data packet on the bus is preceded by a busy/free indication, the token can be passed on whilst the packet is being transmitted; in this case the device has to wait for the current packet to end before transmitting the waiting packet (i.e. instead of the token meaning 'go', it means 'you're next').

If the device or packet has the lower priority ( $P_2$ ), it will first seize and hold  $T_2$ , moving to state  $S_2$  but will not transmit on the bus until it also holds  $T_1$  ( $S_3$ ). It may not seize  $T_1$  and  $T_2$  at the same time. This procedure ensures that all waiting packets in the contention resolution bus having the higher priority  $P_1$  will have had a prior opportunity to transmit on the bus. In order to ensure this, a device with  $P_1$  access (only requiring  $T_1$ ) will also hold  $T_2$  and release the two tokens together, otherwise the tokens may become detached and permit  $P_2$  access before all the devices have had an opportunity for  $P_1$  access.

It will be appreciated that there are within the ring several devices with  $P_1$  and  $P_2$  priority demanding access to the transmission path at the same time.

A device requiring  $P_1$  access ignores  $T_2$  but grabs and holds  $T_1$ . If  $T_2$  is available after it has got  $T_1$  but before it has finished transmitting then the device holds  $T_2$  as well. When the device is finished it releases  $T_1$  then  $T_2$ .



A device requiring  $P_2$  access ignores  $T_1$  but grabs and holds  $T_2$ . Only when it holds  $T_2$  can it grab and hold  $T_1$  and only then can it access the data bus. When finished it releases  $T_2$  then  $T_1$ .

It will be seen that a low priority device cannot use the data bus until any other device in the loop with high priority has had a chance to use it.

A practical embodiment of the invention could be a single dedicated wire loop with asynchronous logic between the ports in contention of the device. A single pulse circulates in the loop, the rising edge represents  $T_1$  and the falling edge  $T_2$ .

A device requiring  $P_1$  access, on detecting a low/high transition ( $T_1$ ) will hold the output low (i.e. 'holds' the token) and uses the bus. If it detects a high/low transition before completion, it leaves the output low (i.e. now 'holding'  $T_1$  and  $T_2$ ). If it does not detect a high/low transition before completion, it transmits low/high ( $T_1$ )-pause-high/low ( $T_2$ ).

A device requiring  $P_2$  access, on detecting a high/low ( $T_2$ ) will hold the output high (i.e. 'holds'  $T_2$ ). On detecting a low-high ( $T_1$ ) it uses the bus. On completion it transmits high/low ( $T_2$ )-pause-low-high( $T_1$ ).

With such a dedicated signal wire, untimed or 'self-timed' operation is possible. This has the advantage that the propagation delay of tokens through the nodes is minimised because the logic works at its own best speed instead of at the speed of an external clock, where the clock interval is set by 'worst case' propagation delays.

In this case, it is necessary to guard against the possibility of cumulative and variable propagation delays resulting in the interval between the two edges of the signal, in either direction, reducing to zero. This is achieved by providing a delay circuit in each node which ensures a minimum interval between positive and negative edges and between negative and positive edges of the outgoing signal. The effect on the contention signal loop as a whole is to set the minimum interval between edges to that of the node with a delay circuit at the upper end of its tolerance range.

An alternative embodiment of the present invention is in a bit multiplexed system with other data on a common communication data bus. However, this requires the signals to be timed.

Multiplexing is most suited to the case where a number of nodes are contending for access to a common transmission medium or data bus which may be unidirectional ring or the transmit end of a communication path.

The contention signal is represented by a single bit occurring regularly on the common serial medium at a known location. The uninterrupted repetition of a single state is interpreted as the continued presence of that state.

In Figure 3 a state diagram is illustrated for an arrangement having  $N$  levels of priority access using  $N$  tokens. The operation of the Figure 3 arrangement is similar that shown in Figure 2. Devices having the highest priority grab the highest priority token  $T_1$  and hold the lower priority tokens  $T_2, T_3, \dots, T_N$  if they are available until its data has been transmitted. Devices having the second highest priority grab the  $T_2$  priority token and holds lower priority

tokens if they are available T3 ..... TN, the highest priority token T1 being passed on to the next device in the ring. The regime is similar for the remaining tokens.

The case of the transmit end of a communication path is shown in Figure 4a and 4b. Data is propagated unchanged across each node, although a node having established access may add to that data. The contention signal bit is dealt with by the contention resolution logic in the node as previously described. The contention signal and the data can be considered as quite separate communications which happen to be carried on the same bus. In order to avoid the continuous cycling of the same data, the transmit terminal equipment may separate the two communications, transmitting the data and looping back the contention signal to the first node. In some architectures where new data simply overwrites old then this special provision may not be necessary.

The case of a unidirectional ring is shown in Figure 5. In this case data is both received and transmitted at each node with the contention signal handled as before. Data may be deleted at the receiving node or simply left and overwritten at a transmitting node with established access, according to the ring protocols adopted.

For a unidirectional ring, the possibility also exists of multiplexing several communication paths, each with its own contention signal, on the same bearer. This type of ring is sometimes referred to as a 'slotted ring'.

Certain conditions, identified in Figure 6, are error conditions. Error (1) implies that there is more than one T1 in the contention resolution loop and the device should delete the one detected. Error

(2) implies that there is more than one T2 in the loop and the one detected should be deleted. Error (3) implies that the device itself has made an error since it cannot be in state S2 with P1 access.

Action by the devices on Errors 1 and 2 will ensure that double access will be eliminated although a soft error in the contention resolution loop may result in a message being damaged by dual access before correction. This combined probability will be very small and unlikely to cause problems.

A soft error in the contention resolution loop may result in one or more tokens being lost. To cover this case and provide for start-up, each device will, for each token, time the interval between successive arrivals. If the period exceeds the time required for each device in the loop to transmit one packet then the device will introduce a new token. Since all devices will be timing the interval it may be that multiple tokens be added; in this case the surplus tokens will be removed by the error conditions described above.

It will be appreciated that the communication path or bus may be a time slot in a time division multiplexed (TDM) system or a fixed wire cable. Furthermore it will be noted that the T1 token can be passed around the ring independently while T2 tokens must be transmitted in packets associated with T1 tokens.

It will be further appreciated that the data bus may be any transmission pathway.

CLAIMS

1. A data packet switching arrangement for switching data packets into a transmission pathway including means arranged to determine data packet priority and to attach a priority token thereto, there being a single high priority token attachable to a data packet to ensure that packet is next to be switched into the transmission pathway, and at least one lower priority token attachable to a respective data packet in order and, in operation, there being no tokens of higher priority attached to other packets, those respective data packets, are switched into the transmission pathway in said order, and, upon a data packet being switched into the transmission pathway, its priority token is released.
2. A switching arrangement as claimed in Claim 1 wherein there is a single low priority token.
3. A switching arrangement as claimed in Claim 1 or 2 wherein the transmission pathway comprises a timeslot in a time division multiplexed (T.D.M) communication system.
4. A switching arrangement as claimed in Claim 1 or 2 wherein the transmission pathway comprises a fixed cable.
5. A switching arrangement as claimed in claims 2, 3 or 4 wherein tokens are constituted by leading and trailing edges of a token signal.
6. A switching arrangement as claimed in any preceding claim wherein a maximum time slot for transmission of a data packet is provided.
7. A switching arrangement substantially as hereinbefore described with reference to the accompanying drawings.