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Communication Method, Base Station and Terminal Apparatus

ABSTRACT

A communication apparatus according to the present invention includes an RF signal processing means for processing a received RF signal, an RF demodulating means for demodulating an output signal of the RF signal processing means, a decoding means (21) for decoding an output signal from the RF demodulating means, an encoding means (42) for encoding a predetermined information signal, an RF modulating means for modulating an output signal from the encoding means, and a transmission signal processing means (50) for processing an output signal from the RF modulating means. The encoding means (42) includes a memory means (123, 124, 125) for storing a predetermined control data, a selecting means (121) for selecting the predetermined control data in accordance with an information of circuit quality obtained from the decoding means, and an adding means (109) for adding the transmission data with an output of the selecting means (121). An output power of the transmission signal processing means is controlled by the information of the circuit quality.

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Invention Title: Communication Method, Base Station and Terminal Apparatus

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

COMMUNICATION METHOD, BASE STATION AND TERMINAL APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a communication method suitable for application to a base station and a terminal apparatus of a radio telephone system, for example, and a base station and a terminal apparatus to which the communication method is applied.

Description of the Related Art:

In a mobile communication such as a radio telephone system or the like, a multiple access in which a plurality of mobile stations (terminal apparatus or subscribers) are permitted to access a single base station is employed. In this case of a radio telephone, a number of mobile stations commonly utilize a single base station. Therefore, various communication systems have been proposed for avoiding interference between respective mobile stations. For example, a frequency division multiple access (FDMA) system, a time division multiple access (TDMA) system, a code division multiple access (CDMA) system and so on are conventionally proposed as this kind of communication systems.

Of these systems, the CDMA system is a multiple access system in which a particular code is assigned to each of the mobile stations, a modulated wave of an identical carrier wave (carrier) is spread in spectrum with the code and then transmitted to the identical base station, and a base station

receives it with taking code synchronism based on each code to identify a desired mobile station.

Specifically, the base station occupies the whole frequency band owing to the spectrum, and transmits signals to a plurality of mobile stations using an identical frequency band at the same time. Each of the mobile stations inversely spreads a signal of a fixed spread band width transmitted from the base station to extract a corresponding signal. Further, the base station discriminates each of the mobile stations by different spread codes one another.

In the CDMA system, communication can be achieved at every direct calling so long as a code is shared. Further, the system is excellent in secrecy of telephone conversation. Therefore, the system is suitable for a radio transmission utilizing mobile stations such as a portable telephone apparatus and so on.

The assignee of the present application has proposed a communication system called a band division multiple access (BDMA) system (disclosed in Japanese patent application No. 132434/1996 and so on) as another communication system. While details of the BDMA system will be described in the detailed description of the preferred embodiment later on, the BDMA system is as follows in short. A plurality of transmission bands in each of which subcarrier signals of a predetermined number are disposed at a predetermined frequency interval are prepared. A signal in each of the transmission bands is divided by every predetermined time to form time slots. A burst signal

is transmitted in the form of a multicarrier signal modulated by dispersing the signal intermittently into the subcarrier signals of the above predetermined number at a period of the time slots of a predetermined number. This BDMA system has a very excellent transmission characteristic.

A system having a frequency allocation called one-cell repetition system has been proposed as a radio telephone system to which the above communication systems are applied. In this one-cell repetition system, a frequency band used in a cell formed of each of base stations is made common in all the cells. In this case, since a frequency used in each of the cells is the same, there can be achieved an effect in which a system arrangement used when the base stations are located to form cells is considerably simplified.

However, if the one-cell repetition system is employed, then the same frequency is used even in adjacent cells. Therefore, since there is high possibility that communication at one station interfere with cells adjacent to the station, the one-cell repetition system can be applied only to a communication system having excellent selectivity of a specific path such as the above CDMA system or the above BDMA system.

Moreover, even if the above CDMA system or the above BDMA system having excellent selectivity of a specific path is employed, it is frequently observed that communication in one station interferes with cells adjacent thereto depending upon the communication state.

SUMMARY OF THE INVENTION

In view of such aspects, it is an object of the present invention to provide a communication method and a communication apparatus which can suppress interference of communication of adjacent cells to minimum when a one-cell repetition system is applied.

In accordance with one aspect of the present invention, there is provided a communication method in a predetermined band width with a predetermined format for multiple access by each cell, said method comprising the steps of:

a detecting step of detecting an interference to a communication between a first apparatus and a second apparatus by communication of a third apparatus; and

a lowering step of lowering an information transmission rate of said communication between said first and second apparatus.

In accordance with another aspect of the present invention, there is provided a communication method in a predetermined band width with a predetermined format for multiple access by each cell, said method comprising the steps of:

a detecting step of detecting an interference to a communication between a third apparatus and an other apparatus by a communication between a first apparatus and a second apparatus;

an informing step of sending an information that said interference is detected in said detecting step or an information that existence of said interference is unknown to said first or second apparatus;

a lowering step of lowering an information transmission rate of said communication between said first and second apparatus.

In accordance with another aspect of the present invention, there is provided a communication method in a predetermined band width with a predetermined format for multiple access by each cell, said method comprising the steps of:

a detecting step of detecting a status that a first base station is communicating with a subscriber in a cell where said first base station is located and said subscriber located at an edge of said cell where said first base station is located is approaching to a cell where a second base station is located; and

a lowering step of lowering an information transmission rate of said communication between said first base station and said subscriber.

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In accordance with another aspect of the present invention, there is provided a communication apparatus communicating in a predetermined band width with a predetermined format for multiple access by each cell, said apparatus comprising:

a status detecting means for detecting a communication status for a predetermined station; and

a rate adjusting means for lowering an information transmission rate of said communication when an output signal from said status detecting means indicates that a level of a communication status is lower than a predetermined value.

In accordance with another aspect of the present invention, there is provided a communication apparatus communicating in a predetermined band width with a predetermined format for multiple access by each cell, said apparatus comprising:

a communicating means for communicating with a predetermined station;

an information receiving means for receiving a predetermined communication status information from a third station; and

a rate adjusting means for lowering an information transmission rate of said communication when an output signal from said information receiving means indicates that a communication status of said third station is a status having a level lower than a predetermined value or an unknown status.

In accordance with another aspect of the present invention, there is provided a communication apparatus communicating in a predetermined band width with a predetermined format for multiple access by each cell, said apparatus comprising:

a communicating means for communicating with a predetermined station;

an information receiving means for receiving an information from a third station; and

a rate adjusting means for lowering an information transmission rate of said communication when an output signal from said communicating means indicates that said communicating means is located at an edge of a cell where said predetermined station is located and when an output signal from said information receiving means indicates that said communicating means approaches to a cell where said third station is located.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram used to explain a slot arrangement of a transmission signal used in a communication apparatus according to an embodiment of the present invention;

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FIGS. 2A to 2G are diagrams each used to explain a transmission state in a frame according to the embodiment;

FIGS. 3A to 3B are diagrams each used to explain an example of a band slot arrangement according to the embodiment;

FIG. 4 is a block diagram showing an arrangement of a terminal apparatus according to an embodiment of the present invention;

FIG. 5 is a block diagram showing an arrangement of an encoder of the terminal apparatus according to the embodiment;

FIG. 6 is a block diagram showing an arrangement of a convolutional encoder of the terminal apparatus according to the embodiment;

FIGS. 7A and 7B are diagrams showing examples of waveforms of a windowing data according to the embodiment;

FIG. 8 is a phase characteristic graph showing an example of a transmission data according to the embodiment;

FIG. 9 is a block diagram showing an arrangement of a decoder of the terminal apparatus according to the embodiment;

FIG. 10 is a timing chart showing a processing timing according to the embodiment;

FIG. 11 is a block diagram showing an arrangement of a base station according to the embodiment;

FIG. 12 is a block diagram showing a modulation processing of the base station according to the embodiment;

FIG. 13 is a block diagram showing a demodulation processing of the base station according to the embodiment; and

FIG. 14 is a diagram used to explain a communication state according to the embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A communication method and a communication apparatus according to an embodiment of the present invention will hereinafter be described with reference to FIG. 1 to FIG. 16.

Initially, a communication system to which the present embodiment is applied will be described. The communication system of the present embodiment is arranged as a so-called multicarrier system in which a plurality of subcarriers are continuously disposed within a band allocated in advance, and the plurality of subcarriers within the single band are utilized on a single transmission path at the same time. Further, the plurality of subcarriers within the single band are collectively divided in the band to be modulated. Here, this system is called a band division multiple access (BDMA: Band Division Multiple Access).

The arrangement thereof will be described below.

FIG. 1 is a diagram showing a slot arrangement of transmission signals of the present embodiment in which a frequency is set in the ordinate thereof and a time is expressed on the abscissa thereof. In the present example, the frequency-axis and the time-axis are divided in a lattice fashion to provide an orthogonal base system. Specifically, the transmission band width of one transmission band (one band slot) is set to 150 KHz and the one transmission band of the 150 KHz includes therein 24 subcarriers. The twenty-four subcarriers are disposed

continuously with an equal interval of 6.25 KHz, and every carrier is assigned with a subcarrier number from 0 to 23. However, practically existing subcarriers are allocated to bands of subcarrier numbers of 1 to 22. Bands of both end portions of the one band slot, i.e., bands of subcarrier numbers of 0 and 23 are assigned with no subcarrier, i.e., they are made to serve as a guard band and their electric power is set to zero.

One time slot is regulated at an interval of 200 μsec. in terms of the time-axis. A burst signal is modulated and transmitted together with 22 subcarriers at every time slot. One frame is defined as an array of 25 time slots (i.e., 5 msec.). Each of the time slots within one frame is assigned with a time slot number from 0 to 24. A hatched area in FIG. 1 represents a section of one time slot in one band slot. In this case, a time slot assigned with a slot number of 24 is a period in which no data is transmitted.

Multiple access in which a plurality of mobile stations (terminal apparatus) carry out communication with a base station at the same period, is carried out by using the orthogonal base system which derives from dividing the frequency-axis and time-axis in a lattice fashion. Connection condition with respective mobile stations is arranged as shown in FIGS. 2A to 2G. FIGS. 2A to 2G are diagrams each showing an operation condition indicating that how six mobile stations are connected to the base station by using time slots U0, U1, U2, ···, U5 with one band slot (actually utilized band slot is changed owing to a frequency hopping which will be described

later). A time slot represented by R is a reception slot while a time slot represented by T is a transmission slot. As shown in FIG. 2A, a frame timing regulated in the base station is set to a period including 24 time slots (of the 25 time slots, the last slot, i.e, a slot of number 24 is not utilized). In this case, the transmission slot is transmitted using a band different from one of the reception slot.

The mobile station U0 shown in FIG. 2B uses time slots of time slot numbers, 0, 6, 12, 18 within one frame as a reception slot, while time slots of time slot numbers, 3, 9, 15, 21 as a transmission slot. A burst signal is received or transmitted in each time slot. The mobile station U1 shown in FIG. 2C uses time slots of time slot numbers, 1, 7, 13, 19 within one frame as a reception slot, while time slots of time slot numbers, 4, 10, 16, 22 as a transmission slot. The mobile station U2 shown in FIG. 2D uses time slots of time slot numbers, 2, 8, 14, 20 within one frame as a reception slot, while time slots of time slot numbers, 5, 11, 17, 23 as a transmission slot. The mobile station U3 shown in FIG. 2E uses time slots of time slot numbers, 3, 9, 15, 21 within one frame as a reception slot, while time slots of time slot numbers, 0, 6, 12, 28 as a transmission slot. The mobile station U4 shown in FIG. 2F uses time slots of time slot numbers, 4, 10, 16, 22 within one frame as a reception slot, while time slots of time slot numbers, 1, 7, 13, 22 as a transmission slot. Further, the mobile station U5 shown in FIG. 2G uses time slots of time slot numbers, 5, 11, 16, 22 within one frame as a reception slot,

while time slots of time slot numbers, 2, 8, 14, 20 as a transmission slot.

In this embodiment, as described later on, a transmission rate of communication between a base station and a mobile station (a terminal apparatus) can be changed. A processing for changing the transmission rate is to change the number of time slots used on one path, for example. Therefore, allocation of the time slots shown in FIGS. 2A to 2G is normal allocation used when the transmission rate is set high. If the transmission rate is set low, a time slot allocated to a mobile station U0 shown in FIG. 2B and a time slot allocated to a mobile station U1 shown in FIG. 2C are used by one mobile station to thereby secure two successive time slots as a transmission slot T and also two successive time slots as a reception slot R. Thus, a processing for doubling the number of time slots to be used when the same amount of information is to be transmitted. In accordance with this processing, the transmission rate is lowered to 1/2. Accordingly, if a path in which the transmission rate is set low is used, the number of mobile stations which can simultaneously access one base station is decreased.

Since the arrangement shown in FIG. 2A to 2G is employed, six time-division multiple access (TDMA) in which six mobile stations accesses one band slot is carried out. In view of each of the mobile stations, there is a spare period of two time slots (i.e., 400 μsec.) from completion of reception or transmission of one time slot period to start of next

transmission or reception. Each of the mobile stations carries out a timing processing and a processing called a frequency hopping by utilizing this spare period. Specifically, each of the mobile stations carries out a timing processing TA for agreeing a transmission timing with a timing of a signal transmitted from a base station during after 200 μsec. have passed before each transmission slot T, and carries out the frequency hopping for switching a band slot used for transmission and reception to another band slot after about 200 μsec. have passed since completion of each transmission slot T. Since the above timing is one used when the transmission rate is set high, if the transmission rate is set low and the number of the band slot to be used is changed, then it is necessary to set the timing for the frequency hopping again. The frequency hopping permits a plurality of band slots prepared for one base station to be used by each of the mobile stations equally.

Specifically, a plurality of band slots are allocated to a single base station. In a case of a cellular system in which one base station forms one cell, if a band of 1.2 MHz is allocated to one cell, eight band slots can be allocated to one cell. Similarly, if a band of 2.4 MHz is allocated to one cell, 16 band slots can be allocated to one cell; if a band of 4.8 MHz is allocated to one cell, 32 band slots can be allocated to one cell; and if a band of 9.6 MHz is allocated to one cell, 64 band slots can be allocated to one cell. Then, a frequency switching processing called the frequency hopping is carried out so that a plurality of band slots allocated to one cell are utilized

uniformly. In the present example, a plurality of band slots of which frequencies are continuous are allocated to one cell.

FIGS. 3A and 3B shows an example of a band-slot allocation in which eight band slots is allocated to one cell. In each of the prepared eight band slots as shown in FIG. 3A, twenty-two carries are set for data transmission.

The communication condition is settled as above so that a signal transmitted between each mobile station and the base station is maintained to have orthogonal property with respect to other signals. Therefore, the signal will not suffer from interference from other signals and only a corresponding signal can be extracted satisfactorily. Since a band slot utilized for transmission is changed at any time by the frequency hopping, the transmission bands prepared for each base station is effectively utilized, which leads to effective transmission. In this case, as described above, a frequency band to be allocated to one base station (cell) can be freely settled. Therefore, a system can be freely settled depending on a used situation.

In this embodiment, it is assumed that one-cell repetition system in employing the same frequency band in all the prepared cells is employed. Specifically, it is assumed that if the eight band slots are prepared as a band which can be used in this radio telephone system as shown in FIGS. 3A and 3B, then all the cells (i.e., all the base stations) carry out communication using the eight band slots.

Next, an arrangement of a terminal apparatus (mobile

station) which carries out communication with the base station in the above-described system will be described. In this case, a band of 2.0 GHz is utilized as a down-link from the base station to the terminal apparatus while a band of 2.2 GHz is utilized as an up-link from the terminal apparatus to the base station.

FIG. 4 is a diagram showing an arrangement of the terminal apparatus. A reception system thereof will be described first. An antenna 11 serving for transmitting and receiving a signal is connected to an antenna sharing device. The antenna sharing device 12 is connected at its received signal output side with a band-pass filter 13, a reception amplifier 14 and a mixer 15 in series. The band-pass filter 13 extracts a signal of the 2.0 GHz band. The mixer 15 mixes the output from the band-pass filter with a frequency signal of 1.9 GHz output from a frequency synthesizer 31 so that the received signal is converted into an intermediate frequency signal of a 100 MHz. The frequency synthesizer 31 is formed of a PLL (phase·locked·loop circuit), and it is a synthesizer for generating signals in a band of 1.9 GHz with an interval of 150 kHz (i.e., one band slot interval) based on a signal of 150 kHz which is generated by frequency-dividing a signal of 19.2 MHz output from a temperature compensation type crystal oscillator (TCXO) 32 by a 1/128 frequency divider 33. Other frequency synthesizers, which will be described later on, utilized in the terminal apparatus are also formed of a PLL circuit.

The intermediate frequency signal output from the

mixer 15 is supplied through a band-pass filter 16 and a variable gain amplifier 17 to two mixers 18I, 18Q useful for demodulation. A frequency signal of 100 MHz output from a frequency synthesizer 34 is supplied to a phase shifter 35 in which the signal is made into two system signals of which phases are shifted from each other by 90 degrees. One of the two-system frequency signals is supplied to the mixer 18I while the other of the same is supplied to the mixer 18Q so that they are mixed with the intermediate frequency signal respectively, whereby an I component and a Q component contained in the received data are extracted. The frequency synthesizer 34 is a synthesizer for generating a signal of 100 MHz band based on the signal of 150 kHz generated by frequency-dividing of the 1/128 frequency-divider 33.

Then, the extracted I-component is supplied through a low-pass filter 19I to an analog-to-digital converter 20I in which the component is converted into digital I data. The extracted Q-component is supplied through a low-pass filter 19Q to an analog-to-digital converter 20Q in which the component is converted into digital Q data. In this case, the respective analog-to-digital converters 20I, 20Q use a clock of 200 kHz as a clock for conversion which is generated by dividing a clock of 19.2 MHz output from the TCXO 32 by a 1/96 frequency divider 36.

Then, the digital I data and digital Q data output from the analog-to-digital converters 20I, 20Q are supplied to a demodulating decoder 21 in which demodulated reception data is obtained at a terminal 22. The demodulating decoder 21 is

supplied with the clock of 19.2 MHz output from the TCXO 32 as a clock as it is, and also supplied with a clock of 5 kHz generated by frequency-dividing the clock of 200 kHz output from the 1/96 frequency divider 36 by a 1/40 frequency-divider 37. The clock of 5 kHz is utilized for generating slot timing date. Specifically, in the present example, one time slot is set to 200 μsec. as described above. However, a signal of which frequency is 5 kHz has one period of 200 μsec. Thus, slot timing data is generated in synchronism with the signal of 5 kHz.

Next, the transmission system of the terminal apparatus will be described. Transmission data obtained at a terminal 41 is supplied to a modulating encoder 42 in which processing for encoding and modulation is carried out for transmission so as to generate digital I data and digital Q data for transmission. In this case, the modulating encoder 42 is supplied with the clock of 19.2 MHz as a clock which is output from the TCXO 32 as it is, and also supplied with the signal of 5 kHz generated by division with the 1/40 frequency-divider 37 as data for generating a slot timing. The digital I data and the digital Q data output from the modulating encoder 42 are supplied to digital-to-analog converters 43I and 43Q in which the data are converted into an analog I signal and an analog Q signal. The converted I signal and Q signal are supplied through low-pass filters 44I and 44Q to mixers 45I and 45Q. Further, a frequency signal of 300 MHz output from a frequency synthesizer 38 is converted by a phase shifter 39 into two

system signals of which phases are shifted from each other by 90 degrees. One of the two system frequency signals is supplied to the mixer 45I while the other of the same is supplied to the mixer 45Q, whereby the frequency signals are mixed with the I signal and the Q signal, respectively, so as to form signals falling in a 300 MHz band. Both of the signals are supplied to an adder 46 in which carried out is an orthogonal modulation to unify them into a single system signal. The frequency synthesizer 38 is a synthesizer for generating a signal of 300 MHz band based on the signal of 150 kHz generated by a frequency-division with the 1/128 frequency-divider 33.

Then, the signal modulated into the signal of 300 MHz band output from the adder 46 is supplied through a transmission amplifier 47 and a band-pass filter 48 to a mixer 49, in which the signal is added with a frequency signal of 1.9 GHz output from the frequency synthesizer 31 so as to convert the signal into a signal of a transmission frequency of 2.2 GHz band. The transmission signal frequency-converted into the transmission frequency is supplied through a transmission amplifier (variable gain amplifier) 50 and a band-pass filter 51 to the antenna sharing device 12 so that the signal is transmitted from the antenna 11 connected to the antenna sharing device 12 in a wireless fashion. A gain of the transmission amplifier 50 is controlled to thereby adjust a transmission output. The control in transmission output is carried out based on output control data received from the base station side, for example.

Further, the signal of 19.2 MHz output from the TCXO

32 is supplied to a 1/2400 frequency-divider 40 to convert be converted into a signal of 8 kHz, and the signal of 8 kHz is supplied to a circuit of a speech processing system (not shown). That is, in the terminal apparatus of the present example, a speech signal transmitted between it and the base station is sampled at a rate of 8 kHz (or oversampling at a rate of an integral multiple of the frequency). Thus, the 1/2400 frequency divider 40 produces a clock necessary for speech data processing circuits such as an analog-to-digital converter and a digital-to-analog converter of a speech signal or a digital signal processor (DSP) for processing for compression and expansion on speech data and so on.

Next, the encoder in the transmission system of the terminal apparatus of the arrangement and its peripheral arrangement will be described in detail with reference to FIG. 5. A convolution encoder 101 subjects a transmission data to convolution encoding. The convolution encoding is carried out with a constrained length of k = 7 and a coding rate of R = 1/3, for example. FIG. 6 is a diagram showing an arrangement of the convolution encoder with a constrained length of k = 7 and a coding rate of R = 1/3. Input data is supplied to six delay circuits 101a, 101b, ···, 101f which are connected in series so that data of continuous 7 bits are made coincident in their timing. Ex-OR gate 101g, 101h, 101i take an exclusive-OR of a predetermined data of the seven bits and outputs of the respective Ex-OR gates 101g, 101h, 101i are converted into parallel data by a serial-to-parallel converting circuit 101j,

whereby convolution-encoded data is obtained.

FIG. 5 is again described. An output of the convolution encoder 101 is supplied to a four-frame interleave buffer 102 in which data interleave is carried out over four frames (20 msec.). An output of the interleave buffer 102 is supplied to a DQPSK encoder 110 in which a DQPSK modulation is carried out. That is, a DQPSK symbol generating circuit 111 generates a corresponding symbol based on supplied data, and then the symbol is supplied to a multiplier 112 at one input terminal thereof. A delay circuit 113 delays a multiplied output of the multiplier 112 by one symbol amount and returns it to the other input terminal thereof, whereby the DQPSK modulation is carried out. The DQPSK modulated data is supplied to a multiplier 103 so that random phase shift data output from a random phase shift data generating circuit 104 is multiplied with the modulated data, whereby phase of the data is apparently changed at random.

An output of the multiplier 103 is supplied to an inverse fast Fourier transformation (IFFT) circuit 105 in which a conversion processing to a time axis is carried out on the data of the frequency axis by calculation of the inverse fast Fourier transformation, whereby data on the real time axis of the multicarrier signal of 22 subcarriers with an interval of 6.25 kHz is produced. The IFFT circuit 105 for carrying out the inverse fast Fourier transformation enables an arrangement for generating subcarriers of a second powered number relatively easily. The IFFT circuit 105 employed in the present example is

capable of generating 2^5 subcarriers, i.e., 32 subcarriers and outputs data modulated into continuous 22 subcarriers of the generated subcarriers. The modulation rate of transmission data dealt by the FFT circuit 105 of the present example is set to 200 kHz. A signal of a modulation rate of 200 kHz is converted into thirty-two multicarriers to produce multicarrier signals with an interval of 6.25 kHz, which numeral derives from calculation of 200 kHz ÷ 32 = 6.25 kHz.

The multicarrier data transformed into data of the real time by the inverse fast Fourier transformation is supplied to a multiplier 107 in which the data is multiplied with a time waveform output from a windowing data generating circuit 106. The time waveform is a waveform having one waveform length T_u, or about 200 μsec. (that is, one time slot period) as shown in FIG. 7A, for example, on the transmission side. However, the waveform is arranged to have its both end portions T_{TR} (about 15 μsec.) changing gently in its waveform level. Hence, the neighboring time waveforms are arranged to overlap partly on each other as shown at FIG. 7B when the time waveform is utilized for multiplication.

FIG. 5 is again described. The signal multiplied with the time waveform by the multiplier 107 is supplied through a burst buffer 108 to an adder 109. The adder 109 adds control data output from a control data selector 121 to the signal at a predetermined position. The control data utilized for addition is control data indicating control of transmission output. Based on a result of determination over the condition of the

received signal at a terminal 122, the selector 121 sets the control data.

In this case, the selector 121 is connected with three control data memories 123, 124, 125 (actually, these memories may be provided by dividing an area of one memory into three portions). Control data for decreasing a transmission output (-1 data) is stored in the memory 123, control data for keeping the transmission output in an unchanged state (±0 data) is stored in the memory 124, and control data for increasing the transmission output (+1 data) is stored in the memory 125, respectively. The control data stored in this case is data equivalent to data when the corresponding control data is subjected to the modulation processing for transmission in the encoder up to the multiplier 107.

More concretely, the transmission data is a phase-modulated data changing on a plane formed by the I-axis and the Q-axis orthogonal to each other, i.e., the data changing along a circle on a plane shown in FIG. 8. Data (I, Q) at a position of (0, 0) is set to ±0 data, that at a position of (1, 0) behind from the position by 90 degrees is set to -1 data and that at a position of (0, 1) ahead of the position of ±0 data by 90 degrees is set to +1 data. Control data for the transmission output corresponding to a position of (1, 1) is undefined so that when the reception side discriminates the data of the position, the data is regarded as ± 0 data to keep the transmission output unchanged. The signal phase shown in FIG. 8 is a phase before being modulated into multicarrier signals.

Actually, the data of the signal phase is modulated into multicarrier signal and data generated by multiplied with a time waveform are stored in respective memories 123, 124, 125.

Transmission data added with the control data by the adder 109 is supplied to a digital-to-analog converter 43 (which corresponds to the digital-to-analog converters 43I, 43Q shown in FIG. 4) in which the transmission data is converted into an analog signal using a clock of 200 kHz for conversion.

Next, the decoder and the peripheral arrangement thereof of the reception system of the terminal apparatus of the present example will be described in detail with reference to FIG. 9. Digital data resulting from conversion by an analog-to-digital converter 20 (corresponding to the analog-to-digital converters 20I, 20Q in FIG. 4) using a clock of 200 kHz, is supplied through a burst buffer 131 to a multiplier 132, in which the digital data is multiplied with a time waveform output from an inverse windowing data generating circuit 133. The time waveform utilized for multiplication upon reception is a time waveform with a shape shown in FIG. 7A. This time waveform is arranged to have a length, T_M, i.e., 160 μsec. which is shorter than the length of the same upon transmission.

The reception data multiplied with the time waveform is supplied to a FFT circuit 134 in which conversion between a frequency axis and a timebase is carried out by the fast Fourier transformation processing, whereby the transmitted data modulated into 22 subcarriers with an interval of 6.25 kHz and arranged on the time base are separated into information

component which each carrier has. The conversion processing in this case is carried out by a circuit capable of processing subcarriers of 2^5, i.e., thirty-two subcarriers, similarly to the case in which conversion processing is carried out by the IFFT circuit in the transmission system. Data modulated into continuous twenty-two subcarriers of them are converted and output therefrom. The modulation rate of transmission data dealt by the FFT circuit 134 of the present example is set to 200 kHz. Since the circuit is capable of processing thirty-two multicarriers, conversion processing can be carried out on multicarriers with an interval of 6.25 kHz, which numeral derives from calculation of 200 kHz ÷ 32 = 6.25 kHz.

The reception data which has been subjected to the fast Fourier transformation in the FFT circuit 134 is supplied to a multiplier 135, in which the reception data is multiplied with inverse random phase shift data (this data is data changing in synchronism with random phase shift data on the transmission side) output from an inverse random phase shift data generating circuit 136, whereby the data is restored to have its original phase.

The data restored to have its original phase is supplied to a differential demodulation circuit 137 in which the data is subjected to differential demodulation. The differentially demodulated data is supplied to a four-frame de-interleave buffer 138 in which data interleaved over four frames upon transmission is restored to have its original data order. The deinterleaved data is supplied to a Viterbi decoder 139 in

which the data is Viterbi-decoded. The Viterbi-decoded data is supplied as decoded reception data to a reception data processing circuit (not shown) placed in the later stage.

FIG. 10 shows timings of processings described so far. Initially, data of one time slot is received at timing R11 in the reception system, and simultaneously with the reception, the received data is converted into digital data by the analog-to-digital converter 20 and then stored in the burst buffer 131. The stored reception data is subjected to demodulation processings such as multiplication with the time waveform, the fast Fourier transform, multiplication with the inverse random phase shift data, differential demodulation, Viterbi demodulation and so on at the next timing R12. Thereafter, decoding is carried out by data processing at the next timing R13.

Then, from timing R21 which is six time slots after timing R11, to timing R23, a processing the same as that of timing R11 to R13 is carried out. Thereafter, the same processing is repeated.

In the transmission system, transmission is carried out at a timing shifted by three time slots with respect to the timing of reception. That is, the transmission data is encoded at predetermined timing T11, the encoded data is subjected to a modulation processing by which the data is converted into transmission data of one burst amount at the next timing T12, and the data is once stored in the burst buffer 108 of the transmission system. Then, at timing T13 behind three time

slots from the reception timing R11, the transmission data stored in the burst buffer 108 is converted by the digital-to-analog converter 43 and then subjected to transmission processing and transmitted from the antenna 11. Then, from timing T21, which is six time slots after timing Y11, to timing T23 a processing the same as that of timing T11 to T13 is carried out. Thereafter, the same processing is repeated.

In this way, reception processing and transmission processing are carried out intermittently in a time sharing manner. In the present example, control data (control bit) of the transmission output to be added to transmission data is, i.e., the control data of the transmission output upon transmission as described with reference to FIG. 5 is, added by the adder 109 at the last timing when the encode processing is completed for transmission. Therefore, the state of the reception data can be swiftly reflected upon the control data to be transmitted. That is, for example, reception state of the burst signal received at timing R11 is detected at a midst of demodulation at timing R12, and the control state of the transmission output to be notified to the opponent of communication (base station) is determined (i.e., FIG. 10 shows a processing at a timing indicating control bit calculation). When the control bit is calculated, the result of calculation is sent from the terminal 122 to the selector 121, in which the calculation result is added with control data corresponding to transmission data stored in the burst buffer 108, and a burst signal to be transmitted at timing T13 is added with control

data of transmission output based on the last received data indicative of the state.

The opponent carrying out communication (base station) determines the control data transmitted at timing T13 so that the opponent controls the transmission output into the corresponding state when the burst signal is transmitted from the base station at the next timing R21. Consequently, the burst signal to be transmitted next is controlled in its transmission output on the basis of the reception state of the burst signal which has been transmitted in the preceding cycle. Thus, the transmission output is positively controlled at every one cycle when the burst signal is transmitted, and hence it is possible to substantially uniform transmission outputs of transmission signals transmitted through a plurality of paths between the terminal apparatus and one base station at the same time.

If it is not carried out the processing that, as in the present example, the control data of the transmission output is prepared in the memory in advance to carry out adding processing, then the following consequence will happen in the example of FIG. 10, for example. That is, a result received at timing R11 is determined in the process of demodulation at timing R12, thereafter the control data is encoded at timing T21 and demodulated at timing T22, and the control data based on the reception result at timing R11 is transmitted in response to the burst signal transmitted at timing T23. Thus, it is impossible to control the transmission output at every cycle. While

description has been made on a case in which the terminal apparatus side generates data useful for controlling the transmission output from the base station, it is needless to say that the base station side may also generate data useful for controlling the transmission output from the terminal apparatus.

In the terminal apparatus according to this embodiment, the low-speed transmission rate can be set other than the transmission rate obtained upon the operation with the clocks of the above respective frequencies. If the transmission rate is set to the low-speed transmission rate, a modulation clock frequency, a demodulation clock frequency and so on are changed in accordance with the setting. The transmission rate is set based on a command from a control unit, not shown, of the terminal apparatus. This control unit sets either of a norma (high speed) transmission rate and the low-speed transmission rate based on a set data of the transmission rate transmitted from the base station.

An arrangement of the base station will be described below with reference to FIG. 11. The arrangement of the base station for carrying out transmission and reception is fundamentally the same as the arrangement of the terminal apparatus side. But the base station is different from the terminal apparatus in an arrangement of multiple access which enables a plurality of terminal apparatus to access at a time.

Initially, an arrangement of the reception system shown in FIG. 11 will be described. An antenna 211 serving for transmission and reception is connected to an antenna sharing

device 212. The antenna sharing device 212 is connected at its reception signal output side with a band-pass filter 213, a reception amplifier 214 and a mixer 215 in series. The band-pass filter 213 extracts 2.2 GHz band. The mixer 215 mixes an extracted signal with a frequency signal of 1.9 GHz output from a frequency synthesizer 231 so that a reception signal is converted into an intermediate signal of 300 MHz band. The frequency synthesizer 231 is formed of a PLL circuit (phase-locked loop circuit). The frequency synthesizer is a synthesizer for generating signals of 1.9 GHz with an interval of 150 kHz (i.e., one band slot interval) on the basis of a signal of 150 kHz generated by frequency-dividing a signal of 19.2 MHz output from a temperature-compensated crystal oscillator (TCXO) 232 by a 1/128 frequency divider 233. Other synthesizers, which will be described later on, utilized in the base station are similarly formed of the PLL circuit.

The intermediate frequency signal output from the mixer 215 is supplied through a band-pass filter 216 and a reception amplifier 217 to two mixers 218I, 218Q useful for demodulation. A frequency signal of 300 MHz output from a frequency synthesizer 234 is converted into signals of two systems of which phases are shifted from each other by 90 degrees by a phase shifter 235. One of the two system frequency signals is supplied to the mixer 218I while the other of the same is supplied to the mixer 218Q so that they are mixed with the intermediate frequency signals, respectively. Thus, an I-component and a Q-component contained in the received data are

extracted. The frequency synthesizer 234 is a synthesizer for generating a signal of 300 MHz band on the basis of a signal of 150 kHz generated by the frequency division with the 1/128 frequency divider 233.

The extracted I-component is supplied through a low-pass filter 219I to an analog-to-digital converter 220I in which the component is converted into digital I data. The extracted Q-component is supplied through a low-pass filter 219Q to an analog-to-digital converter 220Q in which the component is converted into digital Q data. Each of the analog-to-digital converters 220I, 220Q utilizes a signal of 6.4 MHz generated by frequency-dividing a signal of 19.2 MHz output from the TCXO 232 by a 1/3 frequency divider 236 as a clock for conversion.

Then, the digital I data and the digital Q data output from the analog-to-digital converters 220I, 220Q are supplied to a demodulating unit 221 from which demodulated data is supplied to a demultiplexer 222, in which the data supplied thereto is classified into data from respective terminal apparatus and the classified data are supplied separately to decoders 223a, 223b, ···, 223n of which number corresponds to a number of terminal apparatus permitted to access at a time (six terminals per one band slot). The demodulating unit 221, the demultiplexer 222 and the decoders 223a, 223b, ···, 223n are supplied with the signal of 19.2 MHz output from the TCXO 32 as a clock as it is, and also supplied with a signal of 5 kHz generated by frequency-dividing a signal of 6,4 MHz output from the 1/3 frequency divider 236 by a frequency divider 237 as slot

timing data.

Next, an arrangement of a transmission system of the base station will be described. A multiplexer 242 synthesizes transmission data which are separately encoded by encoders 241a, 241b, ···, 241n prepared for respective opponents (terminal apparatus) capable of communicating at a time. An output of the multiplexer 242 is supplied to a modulation unit 243 in which modulation processing for transmission is carried out, whereby digital I data and digital Q data for transmission are generated. The respective encoders 241a to 241n, the multiplexer 242 and the modulation unit 243 are directly supplied with the signal of 19.2 MHz output from the TCXO 32 as a clock as it is, and also supplied with the signal of 5 kHz output from the 1/1280 frequency divider 237 as a clock.

The digital I data and the digital Q data output from the modulation unit 243 are supplied to digital-to-analog converters 244I and 244Q in which the digital data are converted into an analog I signal and an analog Q signal. The converted I signal and Q signal are supplied through low-pass filters 245I and 245Q to mixers 246I and 246Q. Further, a frequency signal of 100 MHz output from a frequency synthesizer 238 is converted by a phase shifter 239 into two system signals of which phases are shifted from each other by 90 degrees. One of the two system frequency signals is supplied to the mixer 246I while the other of the same is supplied to the mixer 246Q, whereby the frequency signals are mixed with the I signal and the Q signal, respectively, so as to form signals falling in a 300 MHz band.

Both of the signals are supplied to an adder 247 in which carried out is an orthogonal modulation to unify them into a single system signal. The frequency synthesizer 238 is a synthesizer for generating a signal of 100 MHz band based on the signal of 150 kHz generated by a frequency-division with a 1/128 frequency-divider 233.

Then, the signal modulated into the signal of 100 MHz band output from the adder 247 is supplied through a transmission amplifier 248 and a band-pass filter 249 to a mixer 250, in which the signal is added with a frequency signal of 1.9 GHz band output from the frequency synthesizer 231 so as to convert the signal into a signal of a transmission frequency of 2.0 GHz band. The transmission signal frequency-converted into the transmission frequency is supplied through a transmission amplifier 251 and a band-pass filter 252 to the antenna sharing device 212 so that the signal is transmitted from the antenna 211 connected to the antenna sharing device 212 in a wireless fashion.

Further, the signal of 19.2 MHz output from the TCXO 232 is supplied to a 1/2400 frequency-divider 240 to convert the signal into a signal of 8 kHz, and the signal of 8 kHz is supplied to a circuit of a speech processing system (not shown). That is, the base station of the present example is arranged to sample a speech signal, which is transmitted between the terminal apparatus and a base station, at a rate of 8 kHz (or oversampling at a rate of an integral multiple of the rate), and thus the 1/2400 frequency divider 240 produces a clock necessary

for speech data processing circuits such as an analog-to-digital converter and a digital-to-analog converter of a speech signal or a digital signal processor (DSP) for processing for compression and expansion on speech data and so on.

Next, an arrangement of the base station for encoding and modulating transmission data will be described in detail with reference to FIG. 12. In this case, it is supposed that N (N is an arbitrary number) terminal apparatus (users) carry out multiple access at a time. Thus, convolution encoders 311a, 311b, ···, 311n subjects transmission signals U0, U1, ···, UN to respective users of the terminal apparatus to convolution encoding, respectively. The convolution encoding is carried out with a constraint length k = 7 and a coding rate R = 1/3, for example.

Then, data convolution-encoded by respective systems are supplied to four-frame interleave buffers 312a, 312b, ···, 312n, respectively, in each of which interleave is carried out on data over four frames (20 msec.). Outputs of respective interleave buffers 312a, 312b, ···, 312n are supplied to DQPSK encoders 320a, 320b, ···, 320n, respectively, in each of which DQPSK modulation is carried out. Specifically, DQPSK symbol generating circuits 321a, 321b, ···, 321n generates corresponding symbols based on the supplied data. The symbols are supplied to one input of multipliers 322a, 322b, ···, 322n, and multiplied outputs of the multipliers 322a, 322b, ···, 322n are supplied to respective delay circuits 323a, 323b, ···, 323n in each of which the symbol is delayed by one symbol amount and

fed back to the other input. Thus, DQPSK modulation is carried out. Then, the data subjected to the DQPSK modulation are supplied to the multipliers 313a, 313b, ···, 313n, respectively, in which random phase shift data separately output from random phase shift data generating circuit 314a, 314b, ···, 314n are multiplied with modulation data. Thus, Respective data are changed in phase at random apparently.

Outputs of the respective multipliers 313a, 313b, ···, 313n are supplied to other multipliers 315a, 315b, ···, 315n in each of which the output are multiplied with control data output from transmission power control circuits 316a, 316b, ···, 316n provided at every system. Thus, the transmission output is adjusted. This adjustment of transmission output is carried out base on output control data contained in the burst signal transmitted from a terminal apparatus connected to each system. The control data has been described in detail with reference to FIG. 10. That is, if control data of (0, 0) and (1, 1) of (I, Q) data are discriminated from reception data, then the transmission output is maintained as it is, if control data of (0, 1) is discriminated from the reception data, then the transmission output is increased, and if control data of (1, 0) is discriminated from the reception data, then the transmission output is lowered.

The control data of (1, 1) is data which is not actually present on the transmission side. However, when the data of (1, 1) is determined on the reception side, the output is prevented from being changed. Owing to the setting, if the

control data of (1, 0) (i.e., data making the output to be lowered) is deviated in phase by 90 degrees due to any cause, and erroneously determined as data of (1, 1) or (0, 0) on the reception side, then it is possible to avoid at least an erroneous processing in the inverse direction which increases the output. Similarly, if the control data of (0, 1) (i.e., data making the output to be increased) is deviated in phase by 90 degrees due to any cause, and erroneously determined as data of (1, 1) or (0, 0) on the reception side, then it is possible to avoid at least an erroneous processing of the output.

The arrangement shown in FIG. 12 will be described again. The transmission data output from the respective multipliers 315a, 315b, ···, 315n are supplied to a multiplexer 242 and then synthesized thereby. When the transmission data are synthesized by the multiplexer 242 according to this embodiment, a frequency at which the transmission data are synthesized can be switched by a unit of 150 kHz. By the switching control, the frequency of the burst signal supplied to each terminal apparatus is switched. Specifically, in this embodiment, as described with reference to FIGS. 2A to 2G and so on, an operation of switching a frequency by a band slot unit which is called a frequency hopping is carried out, and the frequency switching operation is realized by switching processings of the multiplexer 242 upon the synthesizing operation.

The data synthesized by the multiplexer 242 is supplied to an IFFT circuit 332 which carries out the inverse

fast Fourier transform for the data, and then obtains a so-called multi-carrier data modulated so as to have twenty two subcarriers having frequencies at every 6.25 kHz per one band slot and converted into the real time. Then, the data converted into the real time signal by the inverse fast Fourier transform is supplied to a multiplier 333 which multiplies it with a time waveform output from a windowing data generating circuit 334. As shown in FIG. 7A, for example, the time wave form is a waveform whose length T_U of one waveform is about 200 μ second (i.e., one time slot period). However, at each of its both end portions T_{TR} thereof (about 15 μ second), a level of the waveform is smoothly changed. When the waveform is multiplied with the time wave form as shown in FIG. 7B, adjacent time waveforms are partially overlapped with each other.

Then, the signal multiplied with the time waveform by the multiplier 333 is supplied through a burst buffer 335 to a digital/analog converter 244 (corresponding to the converters 244I, 244Q shown in FIG. 11) which converts it into an analog I signal and an analog Q signal. Then, the analog signals are processed for transmission in the arrangement shown in FIG. 11.

In the base station according to this embodiment, since the band slot switching processing called the frequency hopping is carried out by the multiplexer 242 in the middle of the modulation processing as described above, it is possible to simplify the arrangement of the transmission system. Specifically, when the base station simultaneously handles a plurality of paths of signals as described in this embodiment,

it was necessary to convert a frequency of a signal of each of paths into that of a corresponding band slot (channel) to then synthesize the signals, and hence, in the transmission system, a set of the circuits up to the mixer 250 shown in FIG. 11 is required as much as the paths. On the other hand, in the base station of this embodiment, only one system of the circuits is sufficient in the circuits succeeding the multiplexer 242, and hence the arrangement of the base station can be simplified to that extent.

An arrangement for demodulating received data in the base station to decode it will be described in detail with reference to FIG. 13. A digital I data and a digital Q data converted by an analog/digital converter 220 (corresponding to the analog/digital converters 220I and 220Q in FIG. 11) are supplied through a burst buffer 341 to a multiplier 342. The multiplier multiplies them with a time waveform output from an inverse windowing data generating circuit 343. The time waveform is a time waveform having a shape shown in FIGS. 7A and 7B and also a time waveform having a length T_M of 160 μsec which is shorter than that used upon transmission.

The received data multiplied with the time waveform is supplied to a FFT circuit 344 and subjected to fast Fourier transform thereby to carry out a processing converting a frequency axis into a time axis. Thus, each of the data transmitted after modulation in the form of 22 subcarriers at an interval of 6.25 kHz per one band slot is obtained from the real time signal. Then, the data subjected to the fast Fourier

transform is supplied to a demultiplexer 222 and divided into data which is as much as the terminal apparatus permitted in multiple access to the base station simultaneously. When the data is divided by the demultiplexer 222 according to this embodiment, the frequency used for the above division is switched by a unit of 150 kHz and this switching operation is controlled, thereby frequencies of the burst signals transmitted from the respective terminal apparatus being switched. Specifically, in this embodiment, as described with reference to FIG. 1 and so on, the operation of switching the frequency of a band slot unit which is called the frequency hopping is carried out periodically, and the frequency switching operation carried out on the reception side is realized by time-dividing processings of the demultiplexer 222 upon reception of the received data.

The respective received data divided by the demultiplexer 222 are independently supplied to multiplexers 351a, 351b, ···, 351n provided so as to be as much as the terminal apparatus of the number N permitted in simultaneous multiple access to the base station. The multipliers 351a, 351b, ···, 351n respectively multiply the divided data with inverse random phase shift data (data changed in synchronization with the random phase shift data on the transmission side) output from the inverse random phase shift data generating circuits 352a, 352b, ···, 352n and returns the received divided data to the data having the original phases in the respective systems.

The respective data from the inverse random phase shift data generating circuits are supplied to delay detection circuits 353a, 353b, ···, 353n and delay-detected (differentially demodulated) thereby. The delay detection circuits supplies the delay detected data to four-frame interleave buffers 354a, 354b, ···, 354n which restores the data of four frames interleaved upon transmission to the data of the original data arrangement. The four-frame interleave buffers supply the de-interleaved data to Viterbi decoders 355a, 355b, ···, 355n for subjecting them to Viterbi decoding. The decoders supply the data subjected to the Viterbi decoding as the received data to received-data processing circuits (not shown) at the succeeding stages.

According to the base station of this embodiment, since the data dividing processing including the band slot switching processing called the frequency hopping is carried out by the demultiplexer 222 provided in the middle of the demodulation processing, similarly to the transmission system, it is possible to simplify the arrangement of the reception system. Specifically, when the base station simultaneously handles the signals of plural paths as described in this embodiment, it is necessary in the prior art to convert the frequencies of the signals of the band slots (channels) corresponding to the respective the signals of paths into the intermediate frequency signals and then to carry out the processings up to the fast Fourier transform to supply them to the respective multipliers 351a to 351n, and hence in the

reception system, sets, which are as much as the number of the paths, of the circuits from the mixer 215 to the demodulating unit 221 shown in FIG. 11 are required. On the other hand, since the base station according to this embodiment requires only one system of the circuits in the transmission system preceding to the demultiplexer 222, it is possible to simplify the arrangement of the base station to that extent.

In this base station, similarly to the terminal apparatus, the low-speed transmission rate can be set other than the transmission rate obtained upon the operation with the clocks of the above respective frequencies. If the transmission rate is set to the low-speed transmission rate, a modulation clock frequency, a demodulation clock frequency and so on are changed in accordance with the setting. The transmission rate is set based on a command from a control unit, not shown, of the terminal apparatus. This control unit sets either of a norma (high speed) transmission rate and the low-speed transmission rate based on a set data of the transmission rate transmitted from the base station.

A processing for setting the transmission rate according to this embodiment will be described with reference to FIG. 14 by way of example. For example, it is assumed that a certain terminal apparatus (mobile station) MS is kept in a state that it can communicate with a base station A forming an area (cell) A_0. It is assumed that the communication between the base station A and the terminal apparatus MS is started from call-out from the terminal apparatus MS or call-in to the

terminal apparatus MS. At this time, initially, the transmission rate is set low under the control of the base station A. The reason for setting the transmission rate to the low-speed one upon the initial access is that interference given to another station is unknown upon start of communication.

In a state that the low-speed transmission rate is set, a base station B in an adjacent area B_0 measures an interference power given to the adjacent base station B because of the communication between the base station A and the terminal apparatus MS. If it is determined that the interference is a large one having a predetermined level or larger based on the measurement, then the base station B informs the base station A of this determination through communication employing a ground communication path C between the base station B and the base station A. If no data indicating that the communication interferes largely with other base station adjacent to the area A_0 is not transmitted from all of the base stations adjacent to the area A_0, then it is determined that the communication condition is satisfactory. The transmission rate of the communication between the base station A and the terminal apparatus MS is changed to the high transmission rate (i.e., the normal transmission rate).

The base station of each cell always measures the interference power given by communication in other cell at any time as well as the start of the communication. If detecting the interference power of a predetermined lever or larger, the base station informs the base station carrying out the

communication serving as a source of interference of detection of the large interference power by using the ground communication path C. The base station received such information controls the transmission rate of the communication serving as the interference source to be lowered.

In particular, according to this embodiment, since the same frequency band is used in each of the areas (cells), as shown in FIG. 14, if the terminal apparatus MS is located in the vicinity of the boundary portion between the adjacent areas, then the interference power given to other station is large. If it is determined the communication is carried out in the vicinity of the boundary portion between the adjacent areas in consideration of the intensity of the interference power, then the processing for lowering the transmission rate is carried out. When the communication is carried out in the vicinity of the boundary portion between the adjacent areas as described above, if the terminal apparatus MS is moved to anther position and consequently a hand-off processing for switching a base station communicating with the terminal apparatus MS from the base station A to the base station B is carried out, the hand-off processing is carried out in a state that the communication with low transmission rate is carried out, which can reduce the possibility of failure of the hand-off processing.

Since, when the communication interferes with the adjacent cell largely, the transmission rate is lowered to carry out the communication, as the transmission rate is lowered, the amount of the data to be transmitted is lowered and hence the

interference given to the adjacent cell is lowered. Therefore, it is possible to effectively reduce the interference given to the adjacent cell when the one-cell repetition system is employed in a cell arrangement.

While in this embodiment the base station in the adjacent measures the interference power to measure the amount of the interference and determines whether or not the transmission rate is to be changed, the present invention is not limited thereto. The terminal apparatus MS may measure a power of a signal transmitted from the adjacent base station B and then determine the interference power thereof to transmit the measurement result to the base station A communicating therewith as the control data to reduce the transmission rate under the control of the base station A. In this arrangement, it is possible to change the transmission rate without the data of the interference power transmitted from the base station in the adjacent cell.

While the transmission rate is changed at two steps in this embodiment, the present invention is not limited thereto and the transmission rate may be changed at more steps. Moreover, while in this embodiment the transmission rate is changed by changing the number of the time slots to be used, the present invention is not limited thereto and other processing may be employed to change the transmission rate.

While in this embodiment the BDMA system is employed as the communication system, the present invention is not limited thereto and can be applied to any communication system

as long as the one-cell repetition system can be applied to the communication system. FOr example, when the one-cell repetition system is applied to a cellar system of the code-division multiple access (CDMA) system, if the interference power is at a predetermined lever or higher, then the transmission rate may be lowered upon the commencement of the access.

Moreover, values of the frequencies, time, coding rates and so on are described in this embodiment by way of example, and hence the present invention is not limited to the above embodiment. It is needless to say that the present invention can be applied to the modulation processing other than the DQPSK modulation in view of the modulation system.

According to the present invention, when there is possibility that the interference given to the another cell is large, it is possible to carry out the communication with the interference being suppressed to minimum. Therefore, it is possible to constantly carry out the communication employing the one-cell repetition system satisfactorily.

In this case, the following communication system is employed; a plurality of transmission bands in each of which subcarrier signals of a predetermined number are disposed at a predetermined frequency interval are prepared, a signal in each of the transmission bands is divided by every predetermined time to form time slots, and a burst signal is transmitted in the form of a multicarrier signal modulated by dispersing the signal intermittently into the subcarrier signals of the above predetermined number at a period of the time slots of a

predetermined number. Therefore, it is possible to satisfactorily carry out the communication employing the one-cell repetition system to which the above communication system is applied, without the interfering the communication of another cell.

Since the code-division multiple access system is employed as the communication system used between the base station and the terminal apparatus, it is possible to satisfactorily carry out the communication employing the one-cell repetition system to which the above communication system is applied, without the interfering the communication of another cell.

Having described preferred embodiments of the present invention with reference to the accompanying drawings, it is to be understood that the present invention is not limited to the above-mentioned embodiments and that various changes and modifications can be effected therein by one skilled in the art without departing from the spirit or scope of the present invention as defined in the appended claims.

The claims defining the invention are as follows:

1. A communication method in a predetermined band width with a predetermined format for multiple access by each cell, said method comprising the steps of:

a detecting step of detecting an interference to a communication between a first apparatus and a second apparatus by communication of a third apparatus; and

a lowering step of lowering an information transmission rate of said communication between said first and second apparatus.

2. A communication method in a predetermined band width with a predetermined format for multiple access by each cell, said method comprising the steps of:

a detecting step of detecting an interference to a communication between a third apparatus and an other apparatus by a communication between a first apparatus and a second apparatus;

an informing step of sending an information that said interference is detected in said detecting step or an information that existence of said interference is unknown to said first or second apparatus;

a lowering step of lowering an information transmission rate of said communication between said first and second apparatus.

3. A communication method in a predetermined band width with a predetermined format for multiple access by each cell, said method comprising the steps of:

a detecting step of detecting a status that a first base station is communicating with a subscriber in a cell where said first base station is located and said subscriber located at an edge of said cell where said first base station is located is approaching to a cell where a second base station is located; and

a lowering step of lowering an information transmission rate of said communication between said first base station and said subscriber.

4. A communication method as claimed in claim 2, wherein said third apparatus is a base station of a cell other than a cell said third apparatus belongs to, and

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processing of said informing step is carried out through a radio communication among plural base stations.

5. A communication method as claimed in claim 1, wherein a common frequency band for communication is employed in a cell said first apparatus belongs to and a cell said third apparatus belongs to.

6. A communication method as claimed in claim 2, wherein a common frequency band for communication is employed in a cell said first apparatus belongs to and a cell said third apparatus belongs to.

7. A communication method as claimed in claim 3, wherein a common frequency band for communication is employed in a cell said first base station belongs to and a cell said second base station belongs to.

8. A communication method as claimed in claim 2, wherein said predetermined format employs a multicarrier signal formed by a unit which includes subcarriers of a predetermined number and time slots of a predetermined number.

9. A communication method as claimed in claim 6, wherein said predetermined format employs a multicarrier signal formed by a unit which includes subcarriers of a predetermined number and time slots of a predetermined number.

10. A communication method as claimed in claim 2, wherein said predetermined format is a code division multiple access.

11. A communication method as claimed in clam 6, wherein said predetermined format is a code division multiple access.

12. A communication method as claimed in claim 1, wherein processing of said lowering step is carried out by lowering the information transmission rate in a communication path between said first and second apparatus without varying a capacity of said path.

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13. A communication method as claimed in claim 2, wherein processing of said lowering step is carried out by lowering the information transmission rate in a communication path between said first and second apparatus without varying a capacity of said path.

14. A communication method as claimed in claim 3, wherein processing of said lowering step is carried out by lowering the information transmission rate in a communication path between said first and second apparatus without varying a capacity of said path.

15. A communication method as claimed in claim 1, wherein processing of said lowering step is carried out by lowering the information transmission rate per unit of communication path between said first and second apparatus with increasing a capacity of said path.

16. A communication method as claimed in claim 2, wherein processing of said lowering step is carried out by lowering the information transmission rate per unit of communication path between said first and second apparatus with increasing a capacity of said path.

17. A communication method as claimed in claim 2, wherein processing of said lowering step is carried out by lowering the information transmission rate per unit of communication path between said first and second apparatus with increasing a capacity of said path.

18. A communication apparatus communicating in a predetermined band width with a predetermined format for multiple access by each cell, said apparatus comprising:

a status detecting means for detecting a communication status for a predetermined station; and

a rate adjusting means for lowering an information transmission rate of said communication when an output signal from said status detecting means indicates that a level of a communication status is lower than a predetermined value.

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19. A communication apparatus communicating in a predetermined band width with a predetermined format for multiple access by each cell, said apparatus comprising:

a communicating means for communicating with a predetermined station;

an information receiving means for receiving a predetermined communication status information from a third station; and

a rate adjusting means for lowering an information transmission rate of said communication when an output signal from said information receiving means indicates that a communication status of said third station is a status having a level lower than a predetermined value or an unknown status.

20. A communication apparatus communicating in a predetermined band width with a predetermined format for multiple access by each cell, said apparatus comprising:

a communicating means for communicating with a predetermined station;

an information receiving means for receiving an information from a third station; and

a rate adjusting means for lowering an information transmission rate of said communication when an output signal from said communicating means indicates that said communicating means is located at an edge of a cell where said predetermined station is located and when an output signal from said information receiving means indicates that said communicating means approaches to a cell where said third station is located.

21. A communication apparatus as claimed in claim 19, wherein said third station is a base station of a cell other than a cell said third station belongs to, and said communication status information is transmitted by wire communication.

22. A communication apparatus as claimed in claim 19, wherein a common frequency band for communication is employed in a cell said predetermined station belongs to and a cell said third station belongs to.

23. A communication apparatus as claimed in claim 20, wherein a common frequency band for communication is employed in a cell said predetermined station belongs to and a cell said third station belongs to.

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24. A communication apparatus as claimed in claim 18, wherein said predetermined format employs a multicarrier signal formed by a unit which includes subcarriers of a predetermined number and time slots of a predetermined number.

25. A communication apparatus as claimed in claim 19, wherein said predetermined format employs a multicarrier signal formed by a unit which includes subcarriers of a predetermined number and time slots of a predetermined number

26. A communication apparatus as claimed in claim 20, wherein said predetermined format employs a multicarrier signal formed by a unit which includes subcarriers of a predetermined number and time slots of a predetermined number.

27. A communication method as claimed in claim 18, wherein said predetermined format is a code division multiple access.

28. A communication method as claimed in claim 19, wherein said predetermined format is a code division multiple access.

29. A communication method as claimed in claim 20, wherein said predetermined format is a code division multiple access.

30. A communication apparatus as claimed in claim 18, wherein processing of said lowering step is carried out by lowering the information transmission rate in a communication path between said first and second apparatus without varying a capacity of said path.

31. A communication apparatus as claimed in claim 19, wherein processing of said lowering step is carried out by lowering the information transmission rate in a communication path between said first and second apparatus without varying a capacity of said path.

32. A communication apparatus as claimed in claim 20, wherein processing of said lowering step is carried out by lowering the information transmission rate in a communication path between said first and second apparatus without varying a capacity of said path.

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33. A communication apparatus as claimed in claim 18, wherein processing of said lowering step is carried out by lowering the information transmission rate per unit of communication path between said first and second apparatus with increasing a capacity of said path.

34. A communication apparatus as claimed in claim 19, wherein processing of said lowering step is carried out by lowering the information transmission rate per unit of communication path between said first and second apparatus with increasing a capacity of said path.

35. A communication apparatus as claimed in claim 20, wherein processing of said lowering step is carried out by lowering the information transmission rate per unit of communication path between said first and second apparatus with increasing a capacity of said path.

36. A communication method, substantially as herein described in relation to any one embodiment with reference to the drawings.

37. A communication apparatus, substantially as herein described in relation to any one embodiment with reference to the drawings.

DATED this Eighteenth Day of August, 2000

Sony Corporation

Patent Attorneys for the Applicant

SPRUSON & FERGUSON

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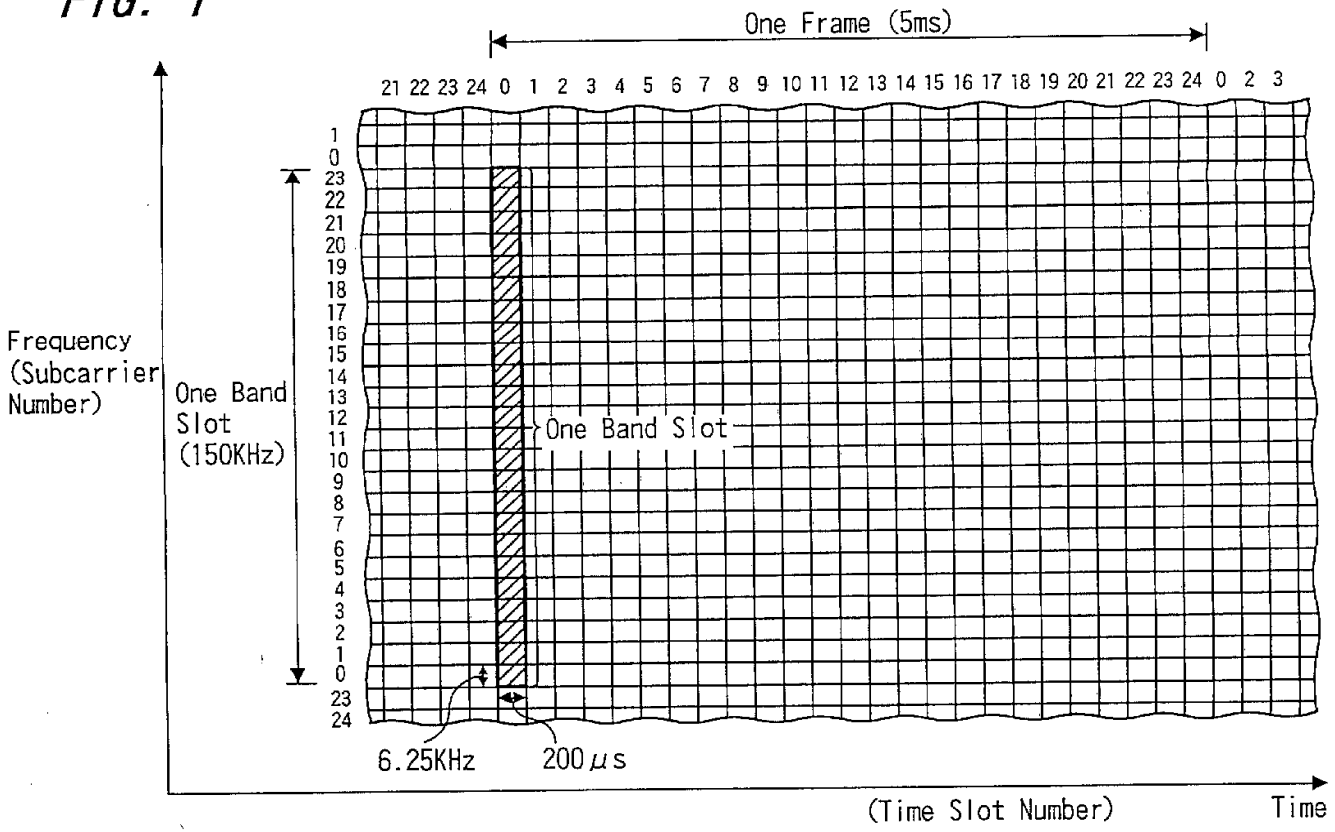
FIG. 1



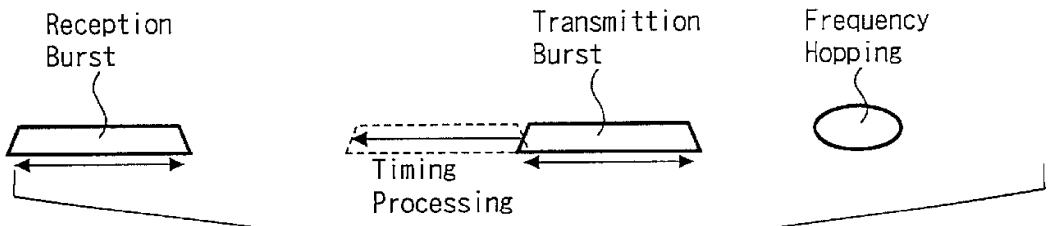


FIG. 2G U5 Timing

FIG. 2F U4 Timing

FIG. 2E U3 Timing

FIG. 2D U2 Timing

FIG. 2C U1 Timing

FIG. 2B U0 Timing

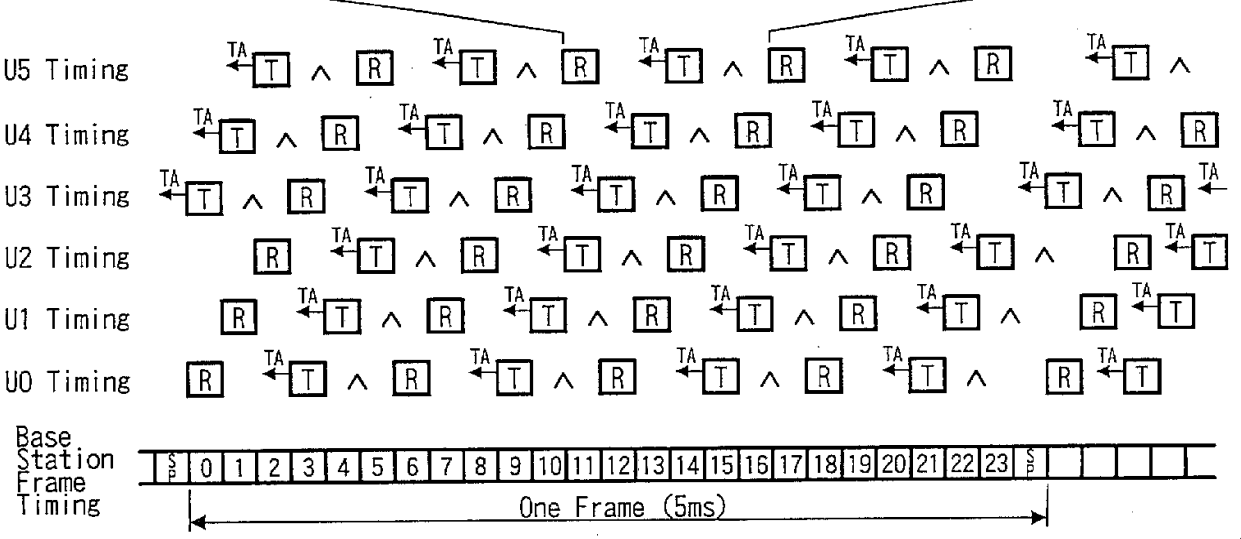


FIG. 2A

FIG. 3A

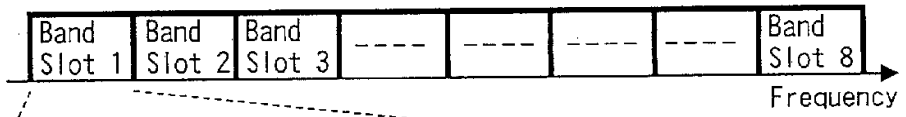

Band Slot 1
Band Slot 2
Band Slot 3
Band Slot 8
Frequency

FIG. 3B


Frequency

FIG. 4

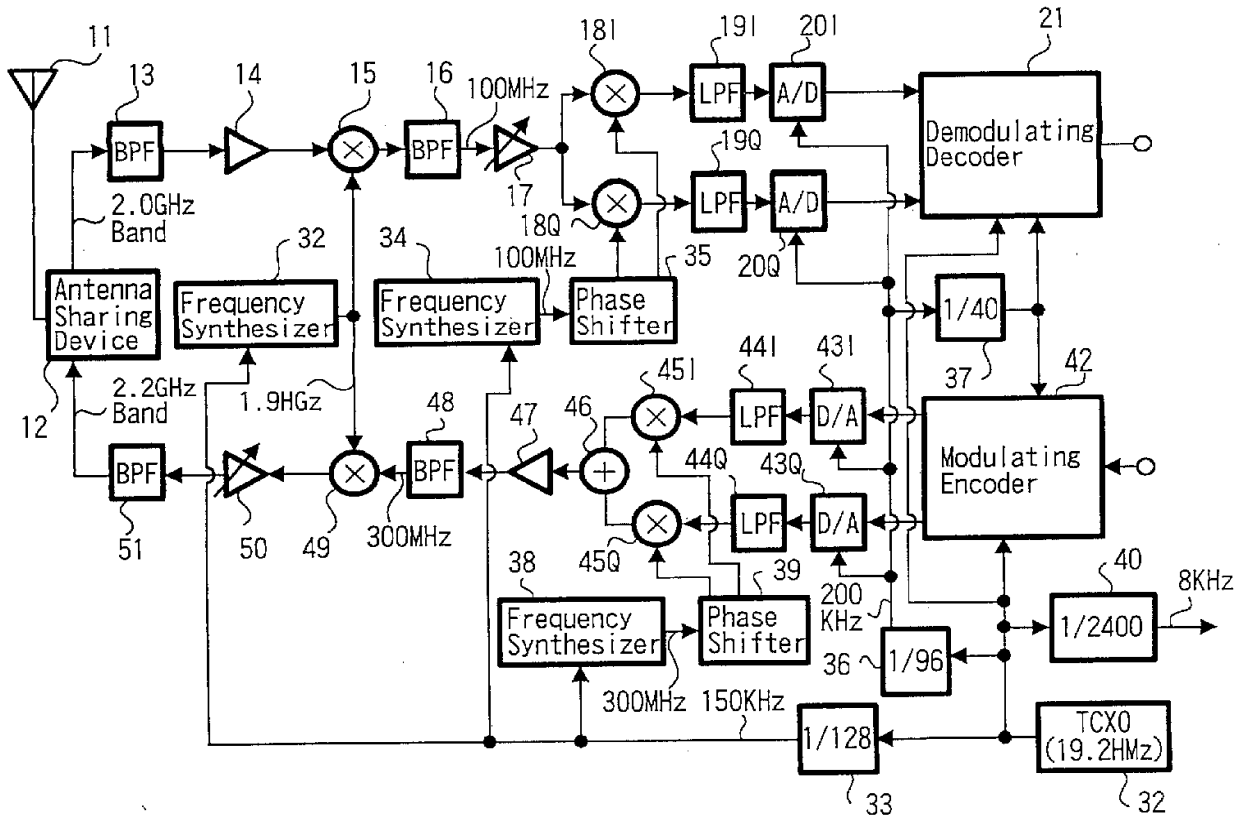
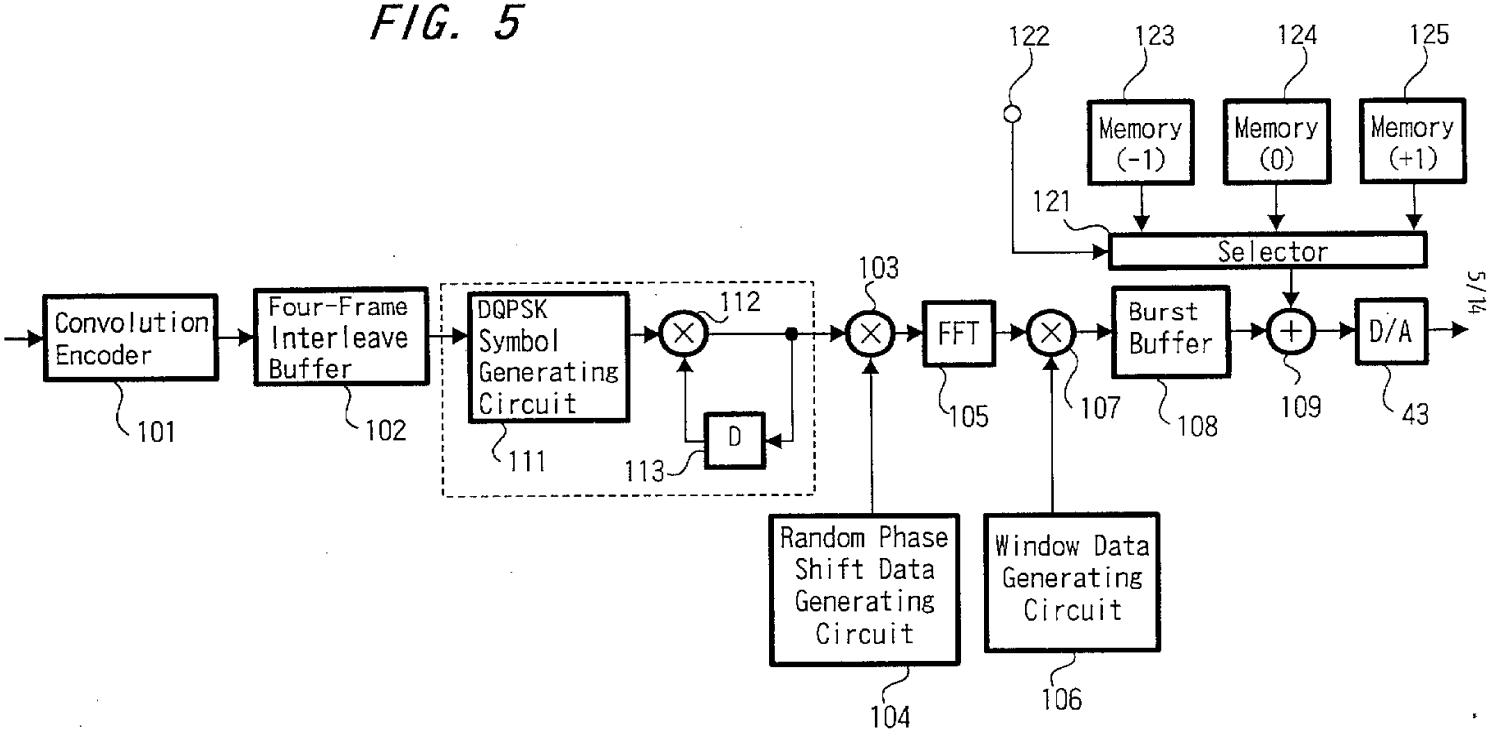

11
13
BPF
14
15
16
BPF
100MHz
17
18I
18Q
19I
LPF
20I
A/D
19Q
LPF
A/D
20Q
21
Demodulating Decoder
2.0GHz Band
Antenna Sharing Device
12
32
Frequency Synthesizer
34
Frequency Synthesizer
100MHz
Phase Shifter
35
1/40
37
42
Modulating Encoder
2.2GHz Band
1.9HGz
BPF
51
50
49
48
BPF
300MHz
47
46
45I
44I
LPF
43I
D/A
44Q
43Q
LPF
D/A
45Q
38
Frequency Synthesizer
39
Phase Shifter
200 KHz
36
1/96
40
1/2400
8KHz
300MHz
150KHz
1/128
33
TCXO (19.2HMz)
32

FIG. 5


Convolution Encoder
101
Four-Frame Interleave Buffer
102
DQPSK Symbol Generating Circuit
111
112
D
113
103
FFT
105
107
Random Phase Shift Data Generating Circuit
104
Window Data Generating Circuit
106
122
123
124
125
Memory (-1)
Memory (0)
Memory (+1)
121
Selector
Burst Buffer
108
109
D/A
43

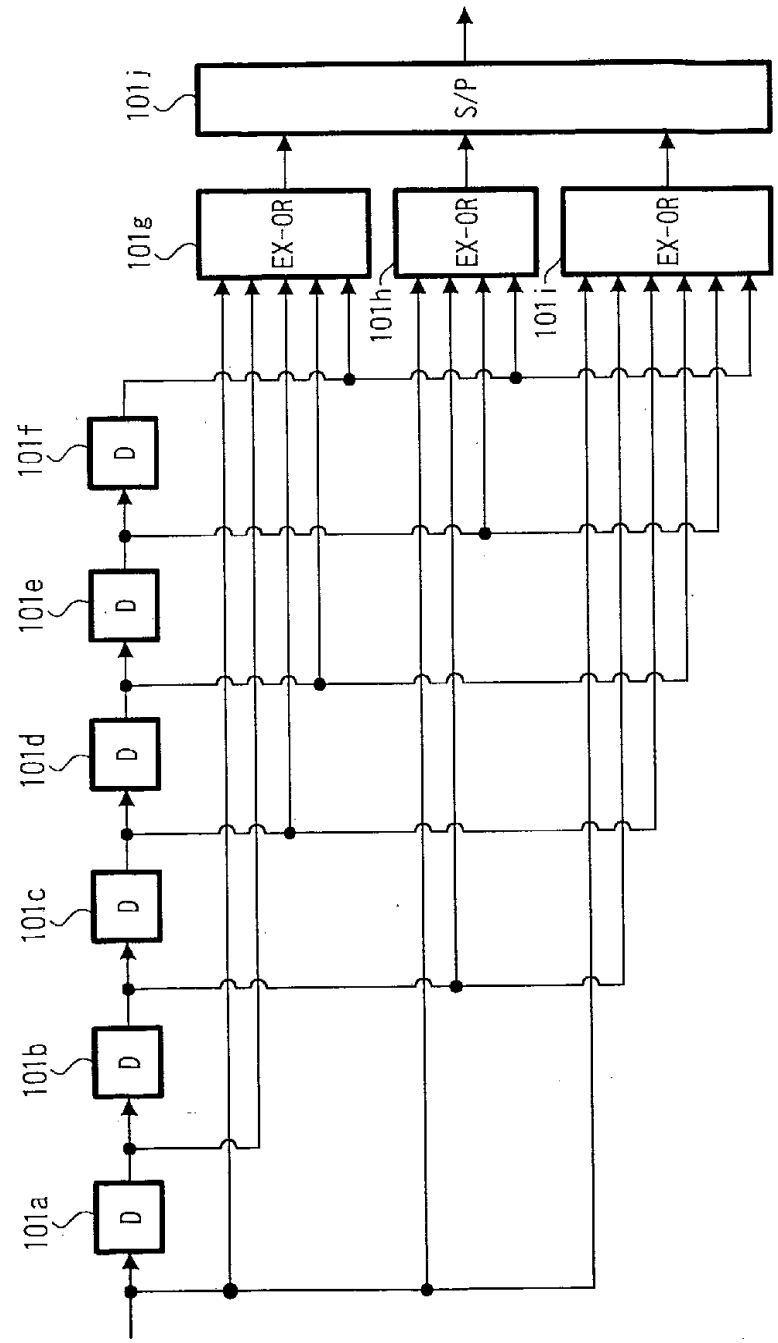

101j
S/P
101g
EX-OR
EX-OR
EX-OR
101h
101i
101f
101e
101d
101c
101b
101a
D
D
D
D
D
D

FIG. 6

FIG. 7A

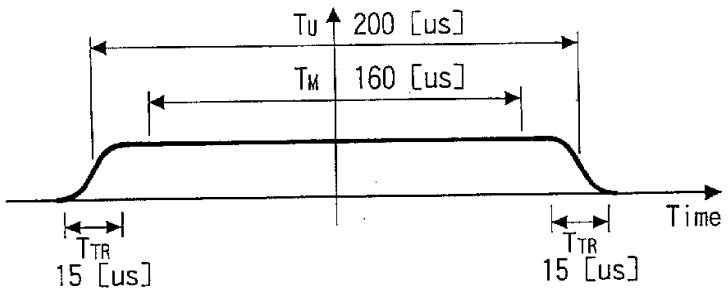


FIG. 7B



FIG. 8

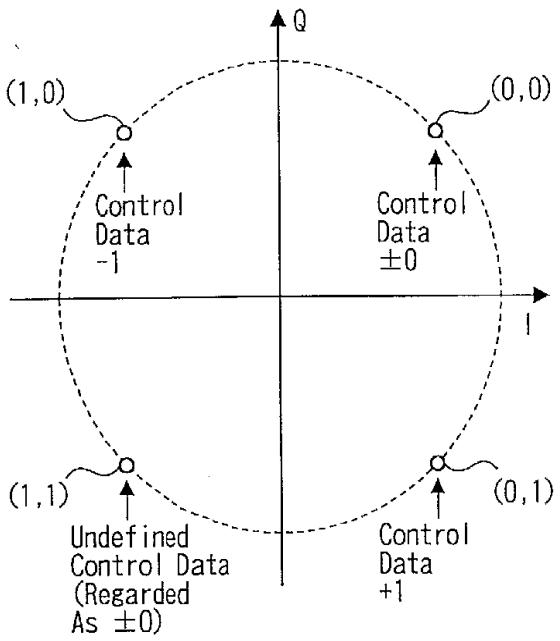

Q
(1,0)
(0,0)
Control Data -1
Control Data ±0
I
(1,1)
(0,1)
Undefined Control Data (Regarded As ±0)
Control Data +1

FIG. 9

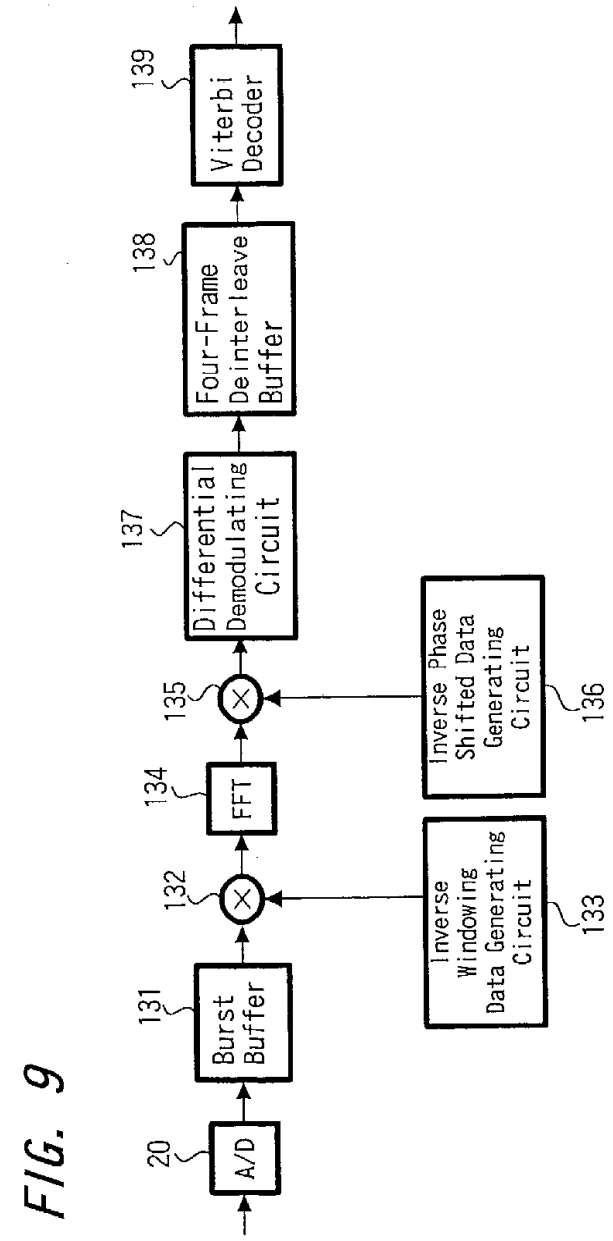

20
A/D
131
Burst Buffer
132
134
FFT
135
137
Differential Demodulating Circuit
138
Four-Frame Deinterleave Buffer
139
Viterbi Decoder
Inverse Windowing Data Generating Circuit
133
Inverse Phase Shifted Data Generating Circuit
136

FIG. 10

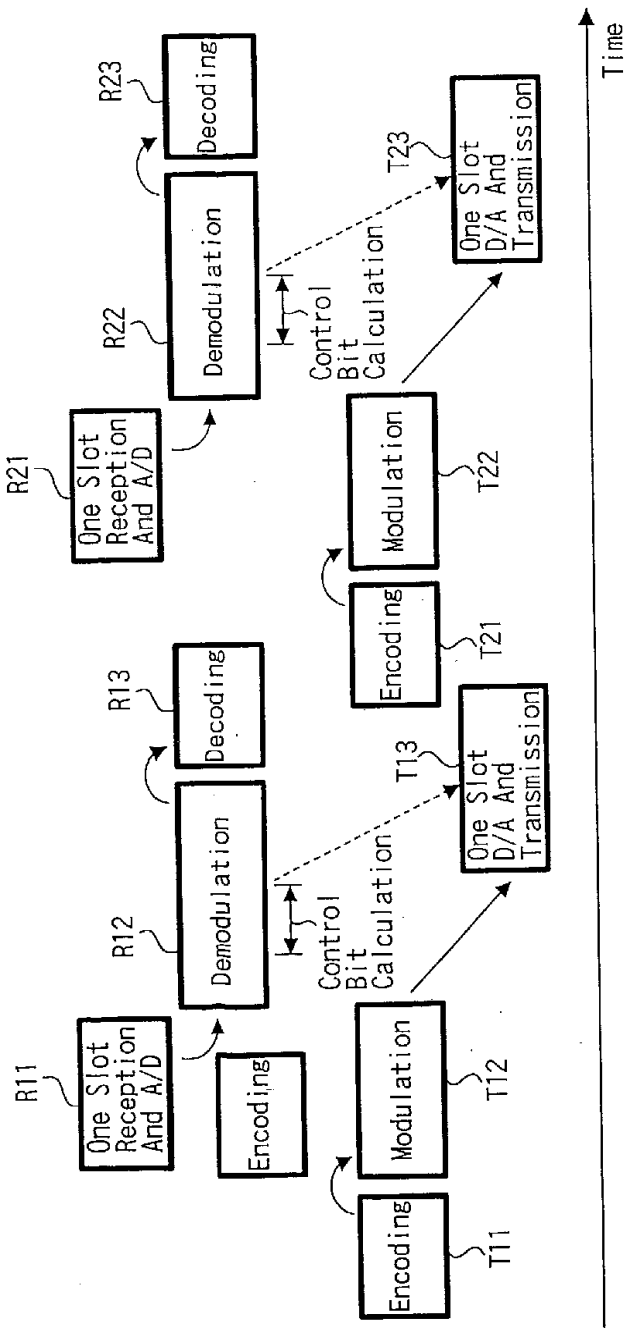

R11
One Slot Reception And A/D
R12
Demodulation
R13
Decoding
Encoding
T11
Encoding
Modulation
T12
Control Bit Calculation
T13
One Slot D/A And Transmission
R21
One Slot Reception And A/D
R22
Demodulation
R23
Decoding
Encoding
T21
Modulation
T22
Control Bit Calculation
T23
One Slot D/A And Transmission
Time

FIG. 11

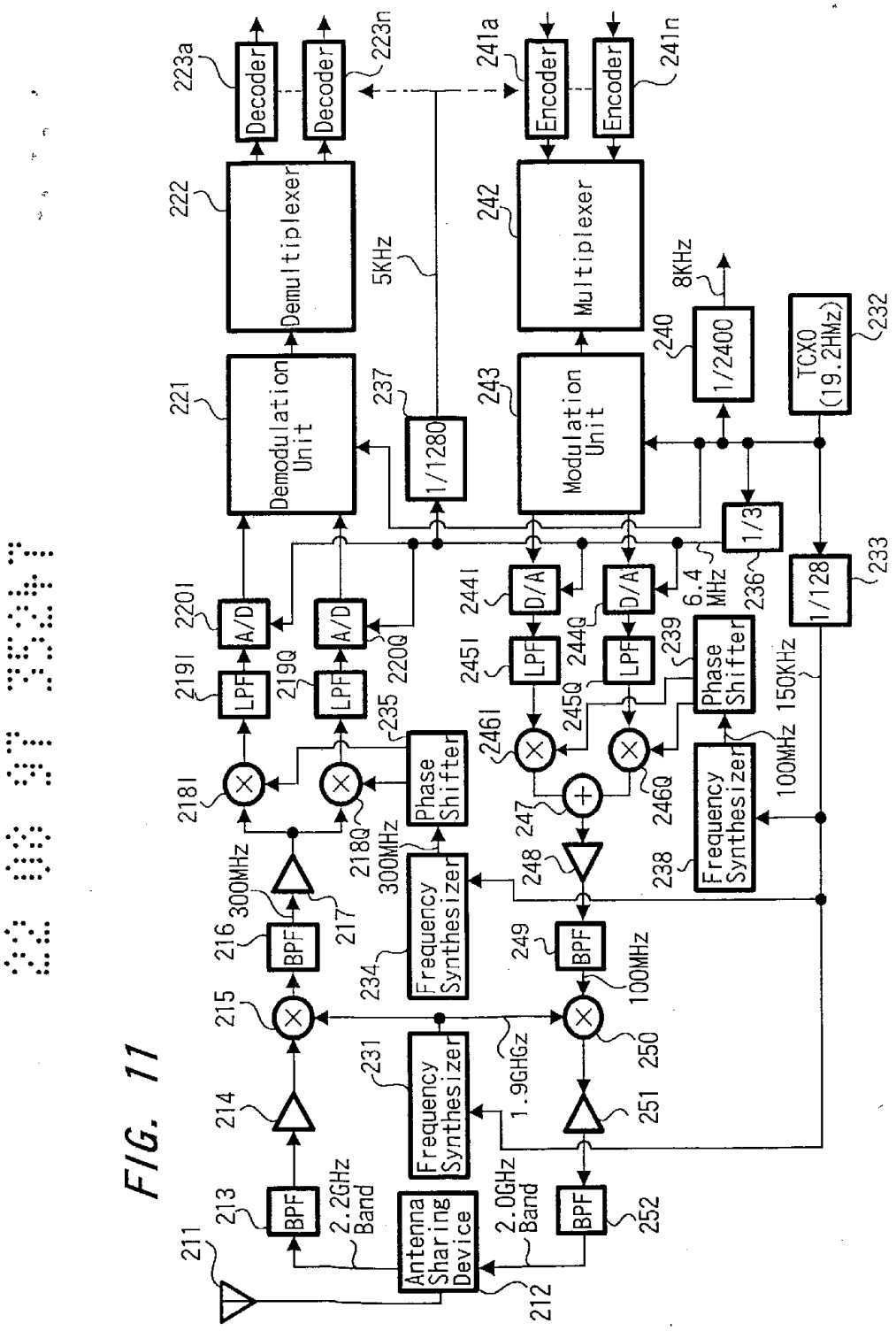

Decoder
Decoder
223a
223n
Demultiplexer
222
Demodulation Unit
221
5KHz
1/1280
237
Encoder
Encoder
241a
241n
Multiplexer
242
Modulation Unit
243
8KHz
1/2400
240
TCXO (19.2HMz)
232
1/3
236
6.4 MHz
1/128
233
A/D
A/D
2201
2200
LPF
LPF
2191
2190
D/A
D/A
2441
2440
LPF
LPF
2451
2450
Phase Shifter
239
Phase Shifter
235
150KHz
2181
2180
2461
2460
247
300MHz
Frequency Synthesizer
234
300MHz
248
Frequency Synthesizer
238
100MHz
216
BPF
217
249
BPF
215
100MHz
214
Frequency Synthesizer
231
1.9GHGz
250
251
211
213
BPF
2.2GHz Band
Antenna Sharing Device
212
2.0GHz Band
BPF
252

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FIG. 12

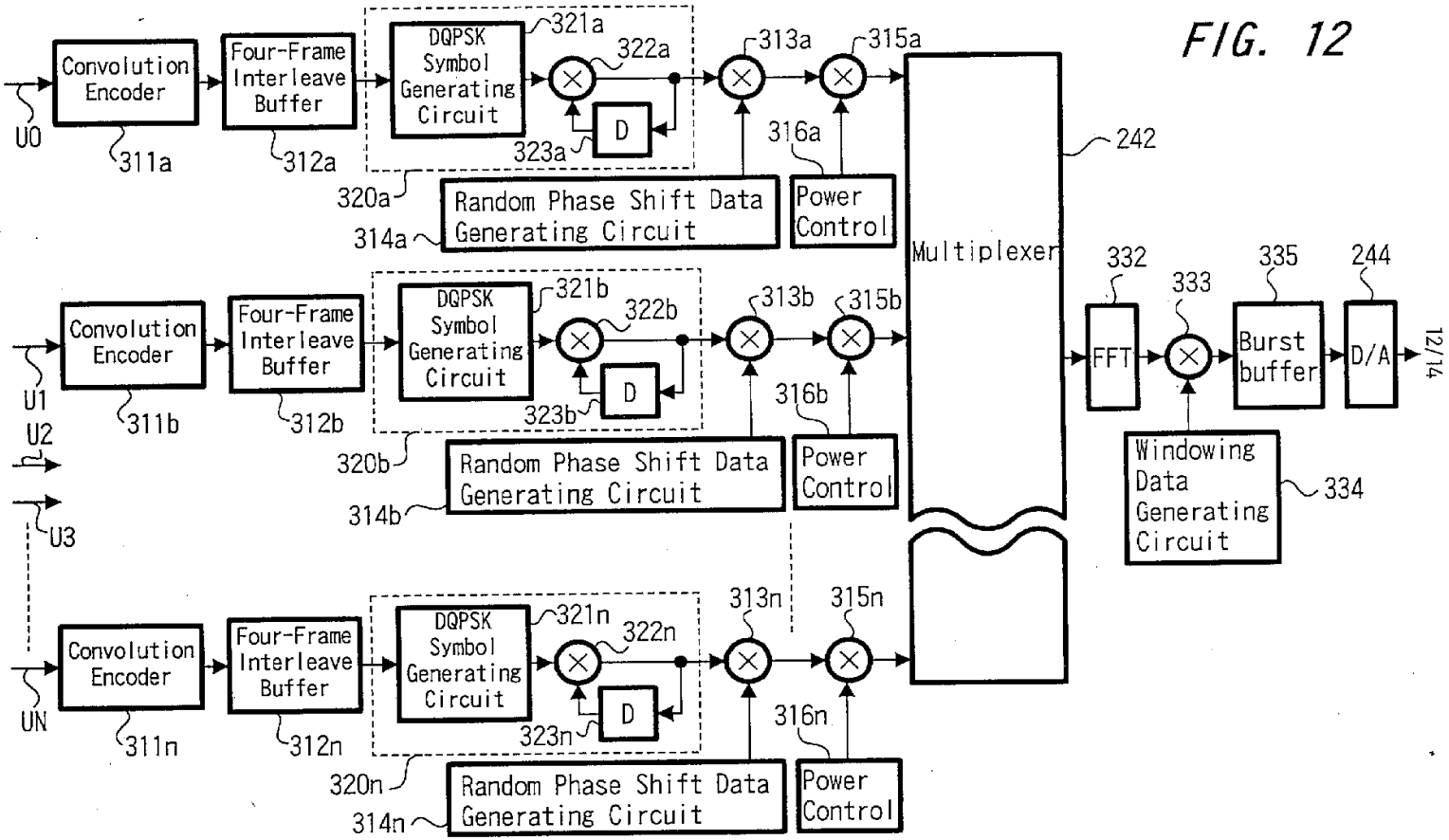

FIG. 13

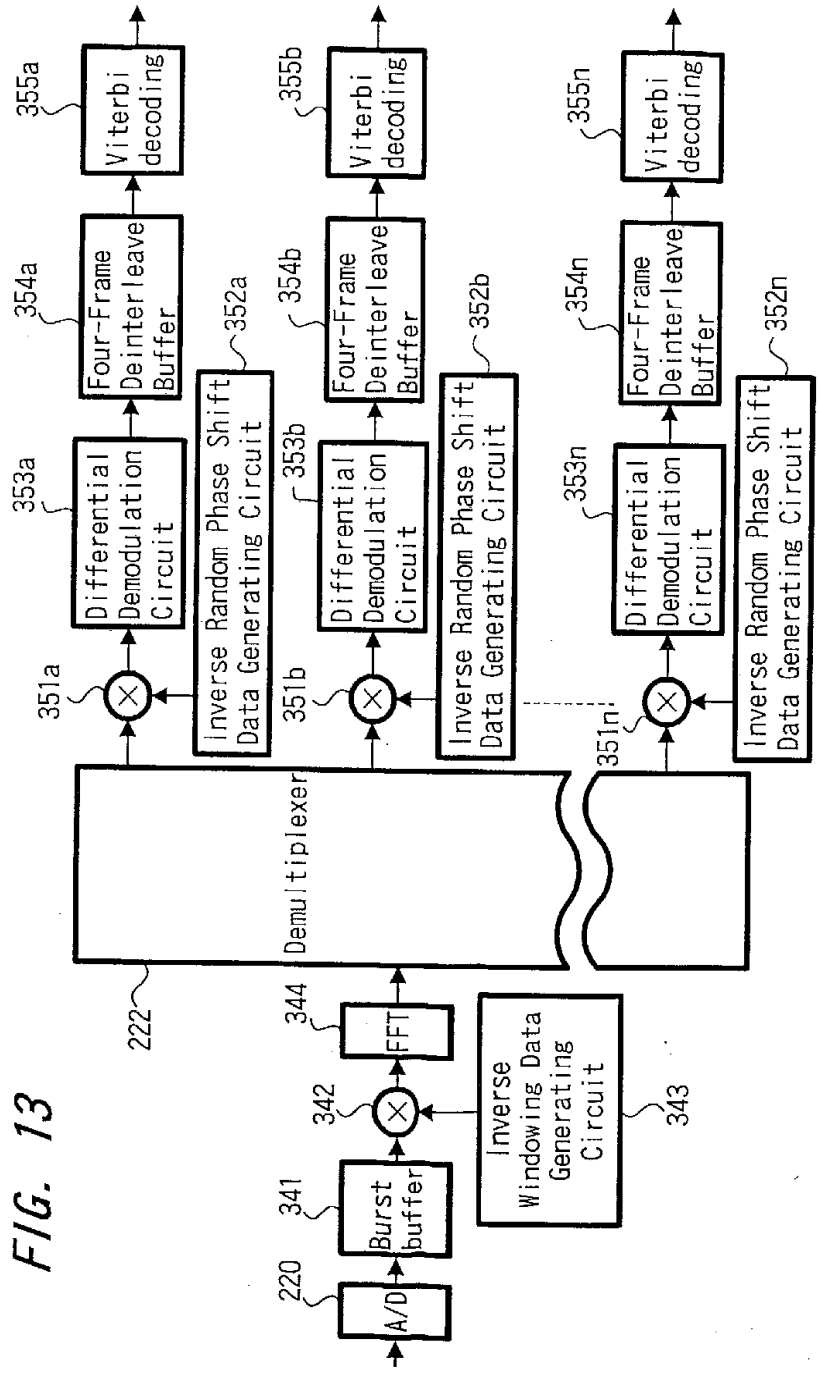
220
A/D
341
Burst buffer
342
344
FFT
Inverse Windowing Data Generating Circuit
343
222
Demultiplexer
351a
351b
351n
Inverse Random Phase Shift Data Generating Circuit
352a
352b
352n
353a
353b
353n
Differential Demodulation Circuit
354a
354b
354n
Four-Frame Deinterleave Buffer
355a
355b
355n
Viterbi decoding

FIG. 14

